FINAL LOG FILE

Name: Shailesh Samudrala *(percentage effort - 50%)*
Partner 1: Vijay Gandrapu *(percentage effort - 50%)*

Wednesday, Sept 8 - 4 hours

- Brainstormed on selection of possible topics for the project.

Friday, Sept 10 - 5 hours

- Researched various topics of interest

Saturday, Sept 11 - 2 hours

- Decided to proceed with project on "*A Study of Scalar Compilation Techniques for Different Architectures*"

Monday, Sept 13 - 2 hours

- Discussed the division of work

Wednesday, Sept 15- 3 hours

- Researched Loop Unrolling

Friday, Sept 17 – 3 hours

- Researched Software Pipelining

Monday, Sept 20 – 2 hours

- Researched MIPS R2000 Architecture

Thursday, Sept 23 – 4 hours

- Researched Cray-1S Architecture

Friday, September 24 -3 hours

- Installed SimpleScalar on Ubuntu. Resolved all problem with installation, and browsed through User manuals.

Sunday, Sept 26 - Monday, Sept 27 – 5 hours

- Preparation of Proposal

Tuesday, Sept 28

- Milestone 1: Submission of Proposal: *A Study of Scalar Compilation Techniques for Different Architectures*

Thursday, Sept 30 – 1 hour

- Met with faculty for clarifications regarding proposal
- Project "A *Study of Scalar Compilation Techniques for Different Architectures*" dropped due to complexity involved in development of algorithm.

Friday, Oct 1 – 4 hours

- Researched other topics of interest

Saturday, Oct 2 – 6 hours

- Decided to proceed with project on "*Simulation and Optimization of VLIW Architecture*"
- Discussed the division of work

Sunday, Oct 3 – 3 hours

- Researched VLIW Architecture

Monday, Oct 4 – 1 hour

- Researched Possible Test Benches

Tuesday, Oct 5 - Thursday, Oct 7

- Preparation for Midterm

Sunday, Oct 10 - Monday, Oct 11 – 2 hours

- Preparation of proposal

Tuesday, Oct 12 – 1 hour

- Milestone 2: Submission of Proposal: *Simulation and Optimization of VLIW Architecture*

Thursday, Oct 14

- Project "*Simulation and Optimization of VLIW Architecture*" dropped due to lack of research value and complexity in developing a simulator.

Friday, Oct 15 – 10 hours

- Researched other topics of interest

Saturday, Oct 16 – 2 hours

- Decided to proceed with project on "*Dead Block Elimination in Caches using Software Techniques*"
- Discussed the division of work

Sunday, Oct 17

- Preparation for Midterm

Monday, Oct 18 – 4 hours

- Researched Dead Blocks in Caches.

Tuesday, Oct 19 - Wednesday, Oct 20

- Preparation for midterm

Thursday, Oct 21 – Friday, Oct 22 -10 hours

- Researched mechanisms to implement an annotator.

Saturday, Oct 23

- Sent mail to faculty seeking clarifications about the annotator

Monday, Oct 24 – Thursday, Oct 28

- Further researched on mechanisms to implement annotator, but without success.
- Sent a mail to the authors of the reference papers, requesting information regarding the annotator, but didn't get any helpful response.

Thursday, Oct 28

- Received reply from faculty
- Project "Dead *Block Elimination in Caches using Software Techniques*" dropped due to complexities in programming.

Friday, Oct 29 – 4 hours

- Researched other topics of interest
- Decided to proceed with project on "*Memory Latency using Cache-based Enhancements*"
- Discussed the division of work

Saturday, Oct 30 – 2 hours

- Researched Memory Latencies

Sunday, Oct 31 - Monday, Nov 1

- Preparation of Proposal

Tuesday, Nov 2

- Milestone 3: Submission of Proposal: *Memory Latency using Cache-based Enhancements.*
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Thursday Nov 4

- Worked on modifications to the proposal: *Memory Latency using Cache-based Enhancements.*

Friday Nov 5

- Discussed the Division of work

Saturday, Nov 6 - Tuesday, Nov 9

- Researched Trace Cache

Wednesday, Nov 10 - Thursday, Nov 11

- Researched Cache Characteristics for sim-outorder simulator

Friday, Nov 12

- Downloaded the Binaries for the SPEC2000Benchmarks
- Ran the following benchmarks on Instruction and Data L1 and Unified L2 Cache, without the introduction of victim cache
  - bzip2
  - gcc
  - vpr

Saturday, Nov 13

- Modified main.h to include trace cache

Wednesday, Nov 17

- Tested the simulator with the modified code

Monday, Nov 15 - Tuesday, Nov 16

- Proposal approved by Professor
- Modified sim-outorder.c to include trace cache

Wednesday, Nov 17

- Tested the simulator with the modified code

Thursday Nov 18 - Friday Nov 19

- Revised the Modifications to sim-outorder.c

Saturday Nov 20

- Tested the simulator with the modified code

Sunday Nov 21 - Monday Nov 22

- Revised the Modifications to sim-outorder.c

Tuesday Nov 23

- Tested the simulator with the modified code

Wednesday Nov 24

- Revised the Modifications to sim-outorder.c

Thursday Nov 25

- Tested the simulator with the modified code

Friday Nov 26

- Ran the following benchmarks on Instruction and Data L1 and Unified L2 Cache, with the trace cache enabled
  - bzip2
  - gcc
  - vpr

Sunday Nov 28

- Compared the data and generate the results

Monday Nov 29

- Prepared the final report

Tuesday Nov 30

- Submission of final report