

Week 2 Task – BabySoC Fundamentals & Functional Modelling

Objective

To build a solid understanding of SoC fundamentals and practice functional modelling of the BabySoC using simulation tools (Icarus Verilog & GTKWave).

Part 1 – Theory (Conceptual Understanding)

- Go through the **Fundamentals of SoC Design** notes:
Theory Reference:- <https://github.com/hemanthkumardm/SFAL-VSD-SoC-Journey/tree/main/11.%20Fundamentals%20of%20SoC%20Design>
- Focus on:
 - What is a System-on-Chip (SoC)?
 - Components of a typical SoC (CPU, memory, peripherals, interconnect).
 - Why BabySoC is a simplified model for learning SoC concepts.
 - The role of functional modelling before RTL and physical design stages.

Deliverable:

A 1–2 page write-up on GitHub summarizing your understanding of SoC design fundamentals and how BabySoC fits into this learning journey.
