Week 2 Task – BabySoC Fundamentals & Functional Modelling

Objective

To build a solid understanding of SoC fundamentals and practice functional modelling of the BabySoC using simulation tools (Icarus Verilog & GTKWave).

Part 2 – Labs (Hands-on Functional Modelling)

- Follow the **VSDBabySoC Project labs**:
  Lab Reference:- https://github.com/hemanthkumardm/SFAL-VSD-SoC-Journey/tree/main/12.%20VSDBabySoC%20Project
- Install and use:
  - **Icarus Verilog (iverilog)** for compiling Verilog code.
  - **GTKWave** for viewing simulation waveforms.
- Steps:

1. Clone the BabySoC project repo.
2. Compile the BabySoC Verilog modules using iverilog.
3. Simulate and generate .vcd waveform files.
4. Open .vcd files in GTKWave and analyze:
   - Reset operation
   - Clocking
   - Dataflow between modules
5. Document your observations with screenshots of waveforms.

Deliverable:

- Simulation logs
- GTKWave screenshots highlighting correct BabySoC behavior
- Short explanation (per screenshot) of what the waveform represents

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✅ By the end of Week 2, you should be able to explain the **theory behind SoC design** and demonstrate **BabySoC functional modelling with simulation waveforms**.