Experiment 6

Aim: To design a binary adder and subtractor using full adder circuit.

Tools Used: Circuit Verse.

Theory: In Digital Circuits, A Binary Adder-Subtractor is one which is capable of both addition and subtraction of binary numbers in one circuit itself. The operation being performed depends upon the binary value the control signal holds. It is one of the components of the ALU (Arithmetic Logic Unit). This Circuit Requires prerequisite knowledge of Exor Gate, Binary Addition and Subtraction, Full Adder. Here we will consider, two 4-bit binary numbers A and B as inputs to the Digital Circuit for the operation with digits

A0 A1 A2 A3 for A

B0 B1 B2 B3 for B

The circuit consists of 4 full adders since we are performing operation on 4-bit numbers. There is a control line M or we can say a mode bit M is used that which is used to hold a binary value of either 0 or 1 which determines that the operation being carried out is addition or subtraction. The addition and subtraction operations can be combined into one common circuit by including an XOR gate with each full - adder.

CASE 1: M=0

When M is 0 then C_{in} will be 0 and 0 XOR B_0 gives B_0, then S_0 will be sum of A_0 and B_0. Hence M=0 will perform addition.

CASE 2: M=1

When M is 1 then C_{in} will be 1 and 1 XOR B_0 gives B_0', then S_0 will be $A_0+B_0'+1= A_0-B_0+1$. Hence M=1 will perform subtraction.

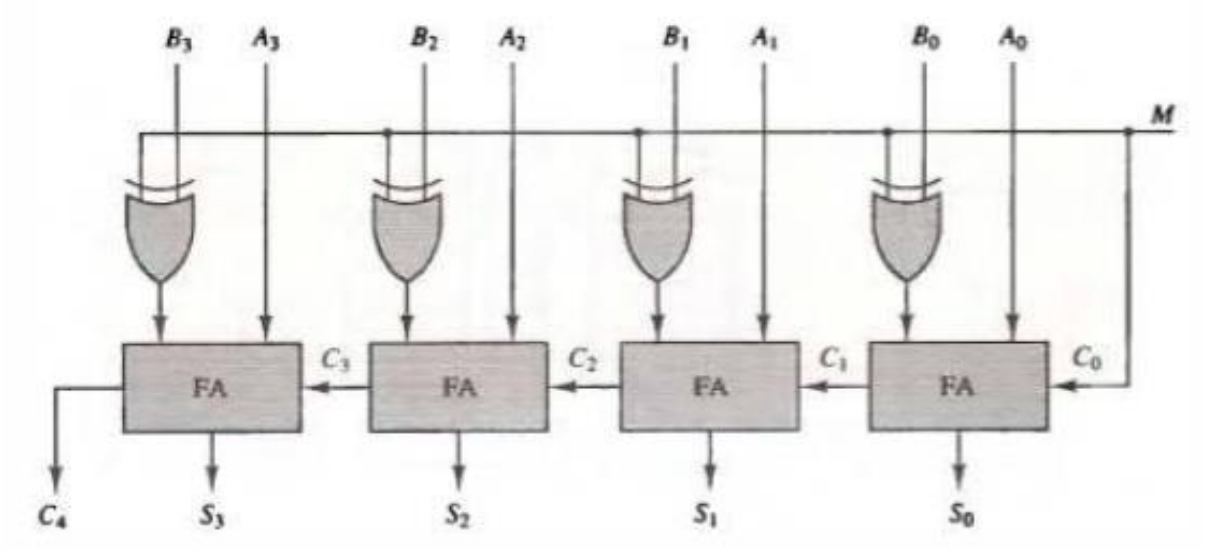


Fig 1: Blueprint of Binary Adder and Subtractor

As shown in the above figure, the first full adder has control line directly as its input (input carry C0), The input A0 (The least significant bit of A) is directly input in the full adder. The

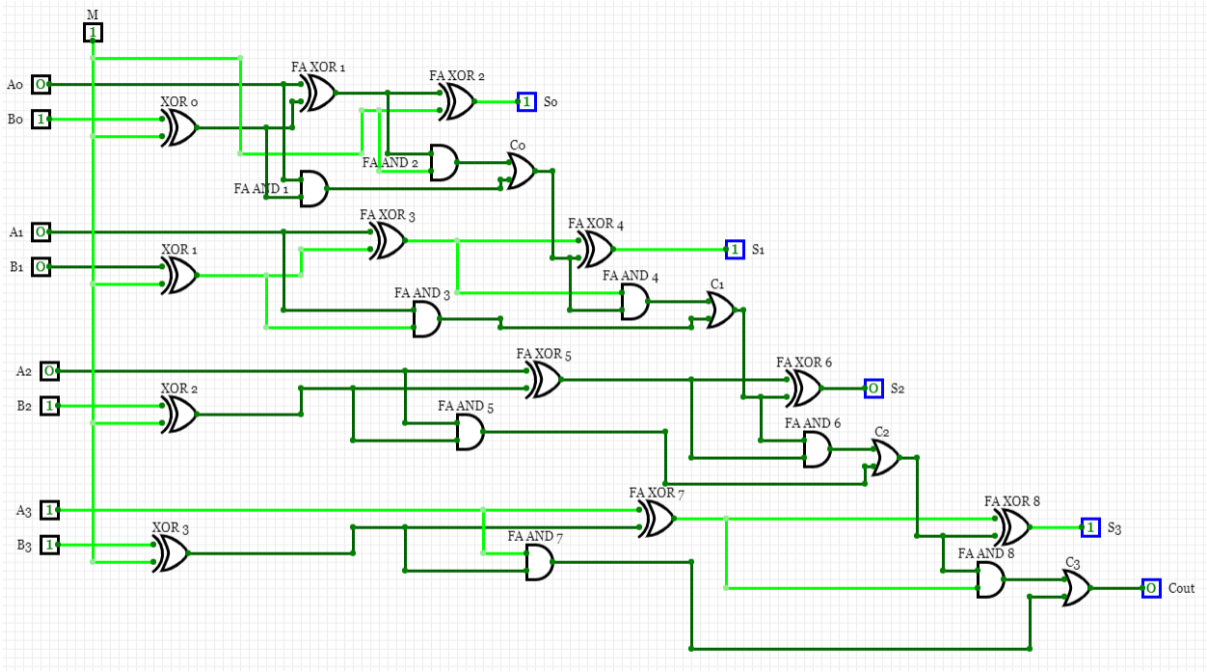
third input is the exor of B0 and M. The two outputs produced are Sum/Difference (S0) and Carry (C1).

If the value of M (Control line) is 1, the output of B0(EX-OR) M=B0′ (Complement B0). Thus, the operation would be A+(B0′). Now 2's complement subtraction for two numbers A and B is given by A+B'. This suggests that when M=1, the operation being performed on the four - bit numbers is subtraction. Similarly, if the value of M=0, B0 (Ex-OR) M=B0. The operation is A+B which is simple binary addition. This suggests that When M=0, the operation being performed on the four - bit numbers is addition.

Then C0 is serially passed to the second full adder as one of it's outputs. The sum/difference S0 is recorded as the least significant bit of the sum/difference. A1, A2, A3 are direct inputs to the second, third and fourth full adders. Then, the third input is the B1, B2, B3 (Ex-OR)ed with M to the second, third and fourth full adder respectively. The carry C1, C2 are serially passed to the successive full adder as one of the inputs. C3 becomes the total carry to the sum/difference. S1, S2, S3 are recorded to form the result with S0. For an n-bit binary adder-subtractor, we use n number of full adders.

Observations:

Circuit Representation of Binary Adder and Subtractor:



Result: The designing of the binary adder subtractor has been done successfully.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
(A) CONCEPT	2		
(B) IMPLEMENTATION	2		
(C) PERFORMANCE	2		
TOTAL	6		