Lab File

Basic Electronics Engineering

(ES201)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

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AMITY UNIVERSITY UTTAR PRADESH

NOIDA -201301

Exp No	Assignment Category	Code	Name of Experiment	Date of Allotment	Date of Evaluation	Max Marks	Marks Obtained	Faculty Sign
1	Mandatory Experiment		To study and plot the characteristics of a junction diode in forward and reverse biased condition and calculate its dynamic resistance in each condition.	28-07-2020	13-10-2020			
2			To study the I-V characteristics of Zener Diode-Voltage Regulator.	4-08-2020	13-10-2020			
3			To Study Half Wave Rectifier.	11-08-2020	13-10-2020			
4			To Study Full Wave Rectifier	18-08-2020	13-10-2020			
5			To study the input and output characteristics of a transistor in its common Emitter configurations (CE).	25-08-2020	13-10-2020			
6			To study the input and output characteristics of a transistor in its Common Base configurations (CB).	1-09-2020	13-10-2020			
7			To study the gain and plot the frequency response of a single stage transistor amplifier (BJT CE Amplifier).	8-09-2020	13-10-2020			
8			To study the op amp as an inverting and non- inverting amplifier.	15-09-2020	13-10-2020			

9			To verify the truth tables of NOT, OR, AND, NOR, NAND, XOR, XNOR gates.	22-09-2020	13-10-2020			
10			To study and plot the characteristics of a JFET in its various configurations.	6-10-2020	13-10-2020			
	Viva	Viva						

Experiment 1

Aim: To study and plot the characteristics of a junction diode in forward and reverse biased condition and calculate its dynamic resistance in each condition.

Tools Used: Virtual Labs.

Theory:

Structure of P-N junction diode: The diode is a device formed from a junction of n-type and p-type semiconductor material. The lead connected to the p-type material is called the anode and the lead connected to the n-type material is the cathode. In general, the cathode of a diode is marked by a solid line on the diode.

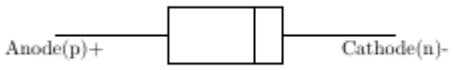


Fig 1: Structure of p-n Junction Diode

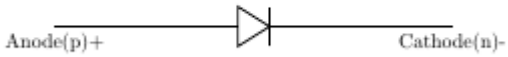


Fig 2: Symbol of p-n Junction Diode

Function of a P-N junction diode in Forward Bias: The positive terminal of battery is connected to the P side(anode) and the negative terminal of battery is connected to the N side(cathode) of a diode, the holes in the p-type region and the electrons in the n-type region are pushed toward the junction and start to neutralize the depletion zone, reducing its width. The positive potential applied to the p-type material repels the holes, while the negative potential applied to the n-type material repels the electrons. The change in potential between the p side and the n side decreases or switches sign. With increasing forward-bias voltage, the depletion zone eventually becomes thin enough that the zone's electric field cannot counteract charge carrier motion across the p–n junction, which as a consequence reduces electrical resistance. The electrons that cross the p–n junction into the p-type material (or holes that cross into the n-type material) will diffuse into the nearby neutral region. The amount of minority diffusion in the near-neutral zones determines the amount of current that may flow through the diode.

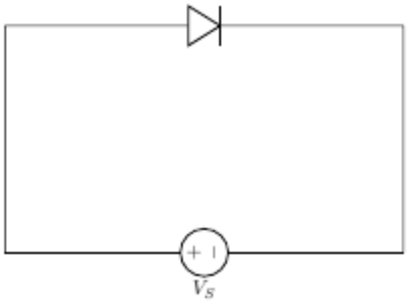


Fig 3: Representation of p-n Junction Diode in Forward Biasing Condition

Function of a P-N junction diode in Reverse Bias: The positive terminal of battery is connected to the N side(cathode) and the negative terminal of battery is connected to the P side(anode) of a diode. Therefore, very little current will flow until the diode breaks down. The positive terminal of battery is connected to the N side(cathode) and the negative terminal of battery is connected to the P side(anode) of a diode, the 'holes' in the p-type material are pulled away from the junction, leaving behind charged ions and causing the width of the depletion region to increase. Likewise, because the n-type region is connected to the positive terminal, the electrons will also be pulled away from the junction, with similar effect. This increases the voltage barrier causing a high resistance to the flow of charge carriers, thus allowing minimal electric current to cross the p–n junction. The increase in resistance of the p–n junction results in the junction behaving as an insulator.

The strength of the depletion zone electric field increases as the reverse-bias voltage increases. Once the electric field intensity increases beyond a critical level, the p–n junction depletion zone breaks down and current begins to flow, usually by either the Zener or the avalanche breakdown processes. Both of these breakdown processes are non-destructive and are reversible, as long as the amount of current flowing does not reach levels that cause the semiconductor material to overheat and cause thermal damage.

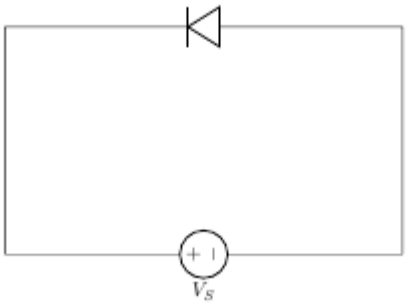


Fig 3: Representation of p-n Junction Diode in Reverse Biasing Condition

Forward and Reverse Biased Characteristics of a Silicon diode:

(a) Forward Biasing: In forward biasing, the positive terminal of battery is connected to the P side and the negative terminal of battery is connected to the N side of the diode. Diode will conduct in forward biasing because the forward biasing will decrease the depletion region width and overcome the barrier potential. In order to conduct, the

forward biasing voltage should be greater than the barrier potential. During forward biasing the diode acts like a closed switch with a potential drop of nearly 0.6 V across it for a silicon diode. The forward and reverse bias characteristics of a silicon diode. From the graph, you may notice that the diode starts conducting when the forward bias voltage exceeds around 0.6 volts (for Si diode). This voltage is called cut-in voltage.

(b) Reverse Biasing: In reverse biasing, the positive terminal of battery is connected to the N side and the negative terminal of battery is connected to the P side of a diode. In reverse biasing, the diode does not conduct electricity, since reverse biasing leads to an increase in the depletion region width; hence current carrier charges find it more difficult to overcome the barrier potential. The diode will act like an open switch and there is no current flow.

Forward and Reverse Biased Characteristics of a Germanium diode:

(a) Forward Biasing: In forward biasing, the positive terminal of battery is connected to the P side and the negative terminal of battery is connected to the N side of the diode. Diode will conduct in forward biasing because the forward biasing will decrease the depletion region width and overcome the barrier potential. In order to conduct, the forward biasing voltage should be greater than the barrier potential. During forward biasing the diode acts like a closed switch with a potential drop of nearly 0.3 V across it for a germanium diode. The forward and reverse bias characteristics of a germanium diode. From the graph, you may notice that the diode starts conducting when the forward bias voltage exceeds around 0.3 volts (for Ge diode). This voltage is called cut-in voltage.

(b) Reverse Biasing: In reverse biasing, the positive terminal of battery is connected to the N side and the negative terminal of battery is connected to the P side of a diode. In reverse biasing, the diode does not conduct electricity, since reverse biasing leads to an increase in the depletion region width; hence current carrier charges find it more difficult to overcome the barrier potential. The diode will act like an open switch and there is no current flow.

Diode Equation: In the forward-biased and reversed-biased regions, the current (If), and the voltage (Vf), of a semiconductor diode are related by the diode equation:

$$I_f = I_s \times \left(e^{V_f/\eta \times V_t} - 1\right)$$

where,

I_s is reverse saturation current or leakage current,

I_f is current through the diode(forward current),

V_f is potential difference across the diode terminals(forward voltage)

V_T is thermal voltage, given by

$$V_t = (K \times T)/q$$

and

K is Boltzmann's constant = 1.38x10−23 J /°Kelvin,

q is the electronic charge = 1.6x10−19 joules/volt (Coulombs),

T is the absolute temperature in °Kelvin (°K = 273 + temperature in °C),

At room temperature (25 °C), the thermal voltage is about 25.7 mV,

η is an empirical constant between 0.5 and 2

The empirical constant, η, is a number that can vary according to the voltage and current levels. It depends on electron drift, diffusion, and carrier recombination in the depletion region. Among the quantities affecting the value of η are the diode manufacture, levels of doping and purity of materials.

If η=1, the value of (K×T)/q is 26 mV at 25°C.

When η=2, the value of (KxT)/q becomes 52 mV. For germanium diodes, η is usually considered to be close to 1. For silicon diodes, η is in the range of 1.3 to 1.6.

Diode Resistance: Resistance is the opposition offered to the flow of current through the device. Hence, diode resistance can be defined as the effective opposition offered by the diode to the flow of current through it. Ideally speaking, a diode is expected to offer zero resistance when forward biased and infinite resistance when reverse biased. However, no device can ever be ideal. Thus, practically speaking, every diode is seen to offer a small resistance when forward biased, and a considerable resistance when reverse biased. One can characterise the given diode regarding its forward and reverse resistances.

(a) Forward Resistance: Even after forward biasing, the diode will not conduct until it reaches a minimum threshold voltage level. After the applied voltage exceeds this threshold level, the diode starts to conduct. We refer the resistance, offered by the diode under this condition as the forward resistance of the diode. That is, the forward resistance is nothing but the resistance offered by the diode when the diode is working in its forward biased condition. Forward resistance is classified into two types viz., static or dynamic depending on whether the current flowing through the device is D.C. (Direct Current) or A.C. (Alternating Current), respectively.

(1) Static or DC Resistance: It is the resistance offered by the diode to the flow of DC through it when we apply a DC voltage to it. Mathematically the static resistance is expressed as the ratio of DC voltage applied across the diode terminals to the DC flowing through it i.e.
$R_{dc}=V_{dc}/I_{dc}$

(2) Dynamic or AC Resistance: It is the resistance offered by the diode to the flow of AC through it when we connect it in a circuit which has an AC voltage source as an active circuit element. Mathematically the dynamic resistance is given as the ratio of change in voltage applied across the diode to the resulting change in the current flowing through it. This is shown by the slope-indicating red solid lines in Figure 1 and is expressed as:
$R_{ac}=\Delta V_{dc}/\Delta I_{dc}$ (Point to point)

(b) Reverse Resistance: When we connect the diode in reverse biased condition, there will be a small current flowing through it which is called the reverse leakage current. We can attribute the cause behind this to the fact that when the diode functions in its reverse mode, it will not be completely free of charge carriers. That is, even in this state, one

can experience the flow of minority carriers through the device. Due to this current flow, the diode exhibits reverse resistance characteristic which is shown by the purple dotted line in Figure 1. The mathematical expression for the same is similar to that for the forward resistance and is given by

$R_r=V_r/I_r$

Where, V_r and I_r are the reverse voltage and the reverse current respectively.

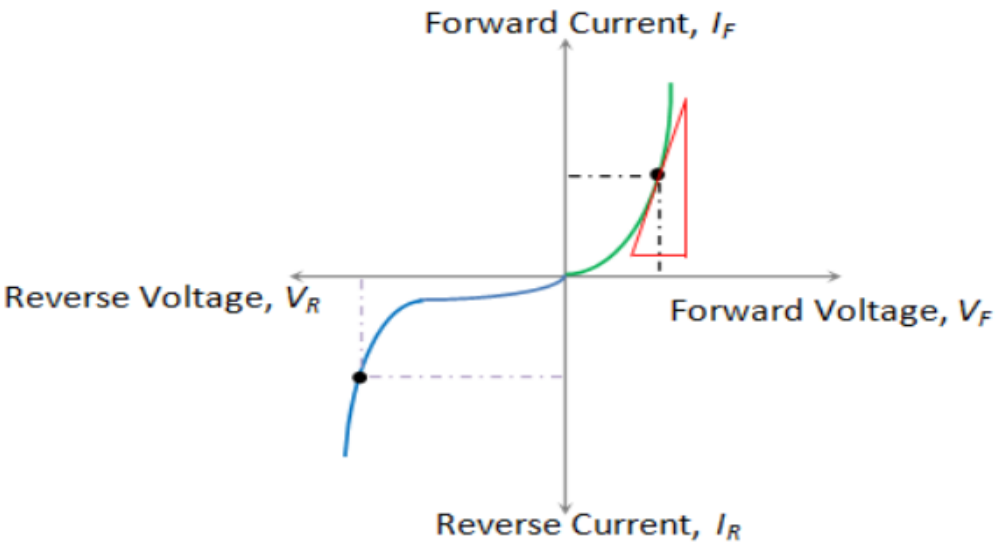
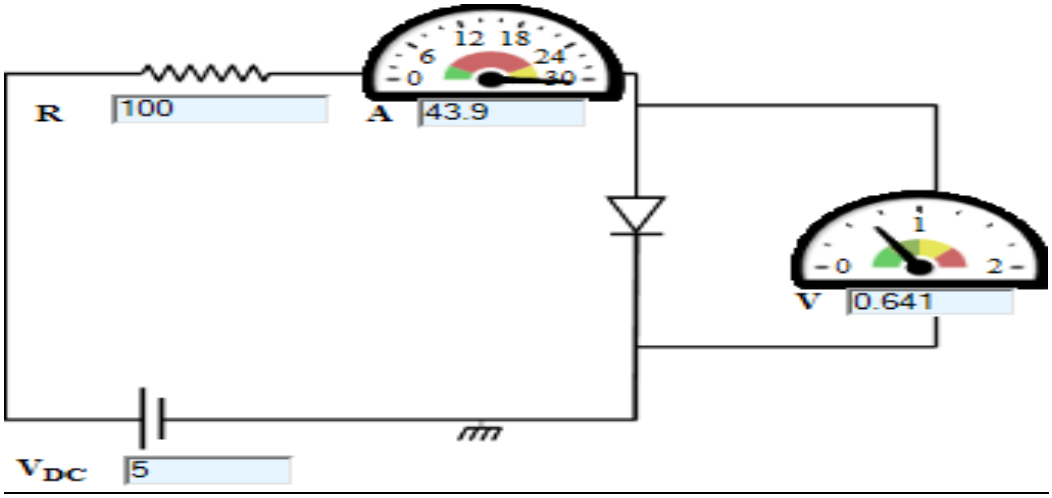


Fig 5: Diode Resistance Shown as a Part of a Resistance.

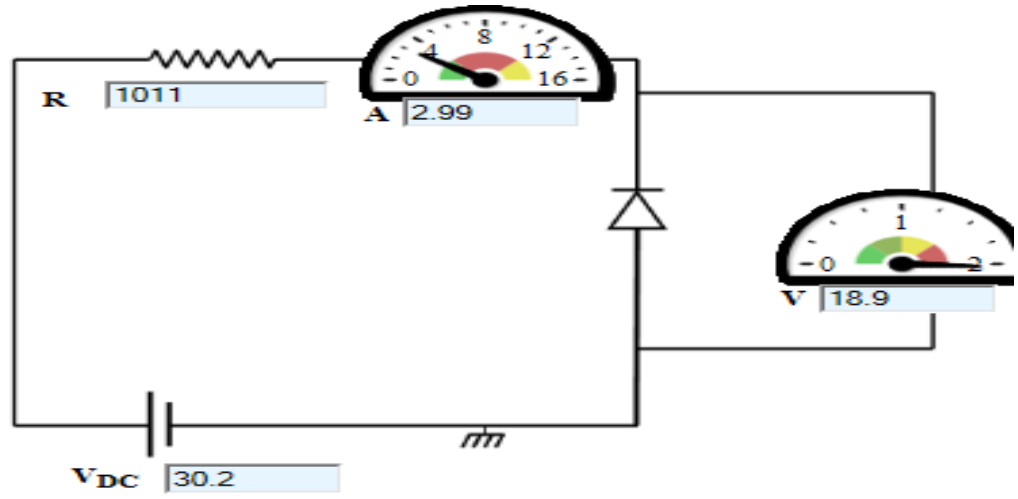
Circuit Diagram:

(A) Silicon Diode:

(1) Forward Biasing:

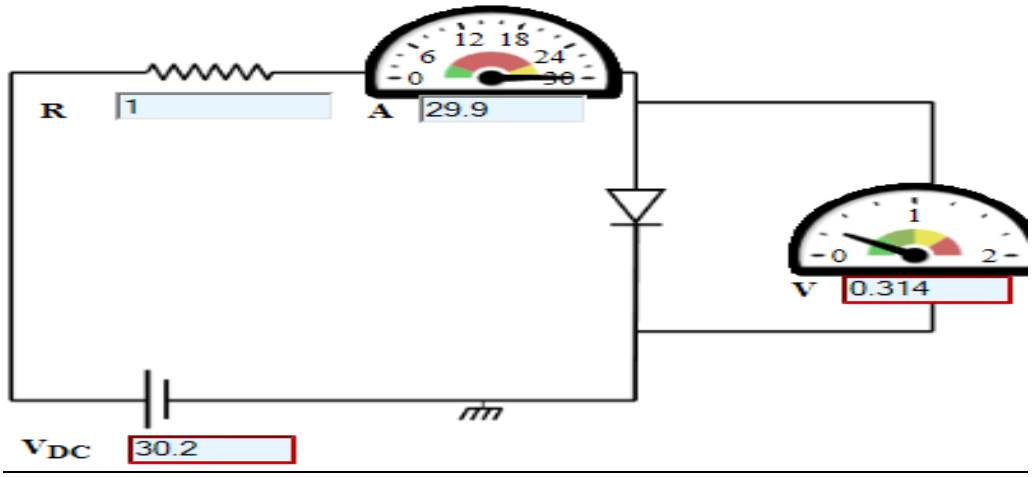


(2) Reverse Biasing:

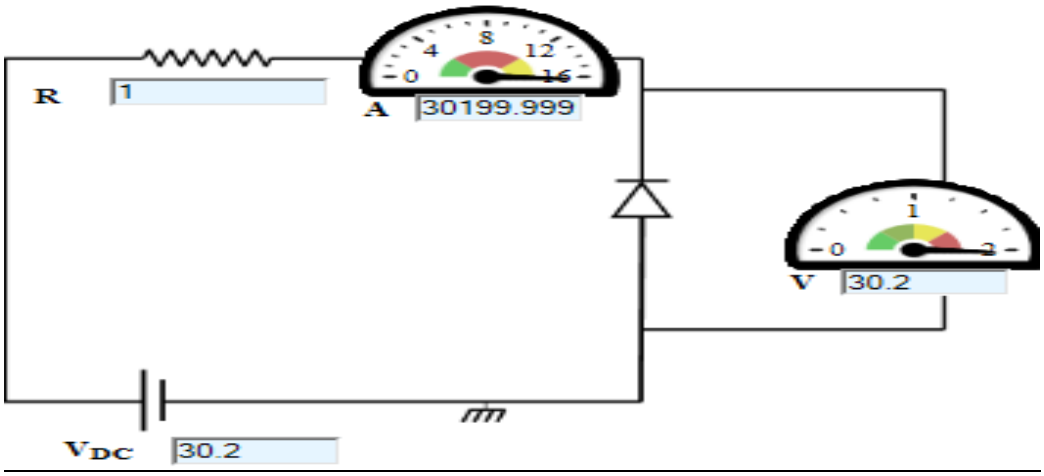


(B) Germanium Diode:

(1) Forward Biasing:

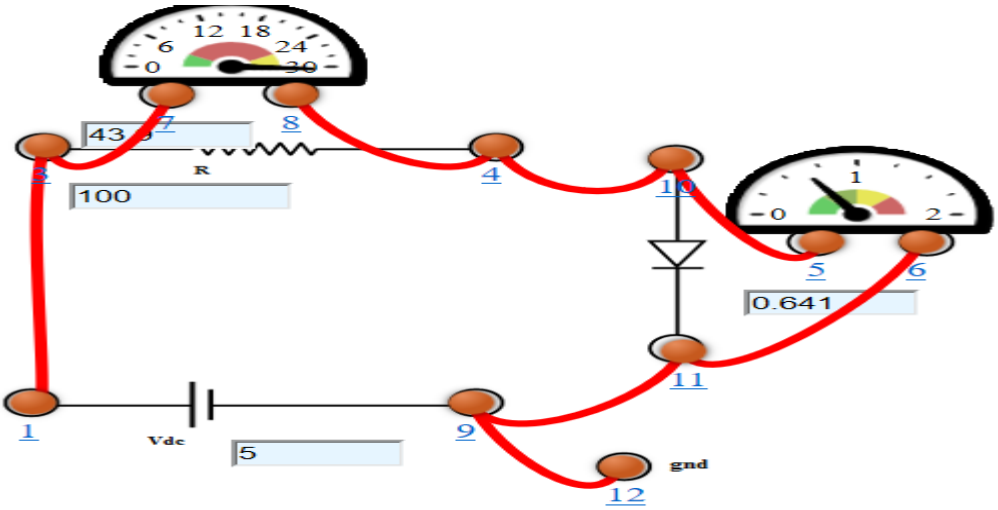


(2) Reverse Biasing:

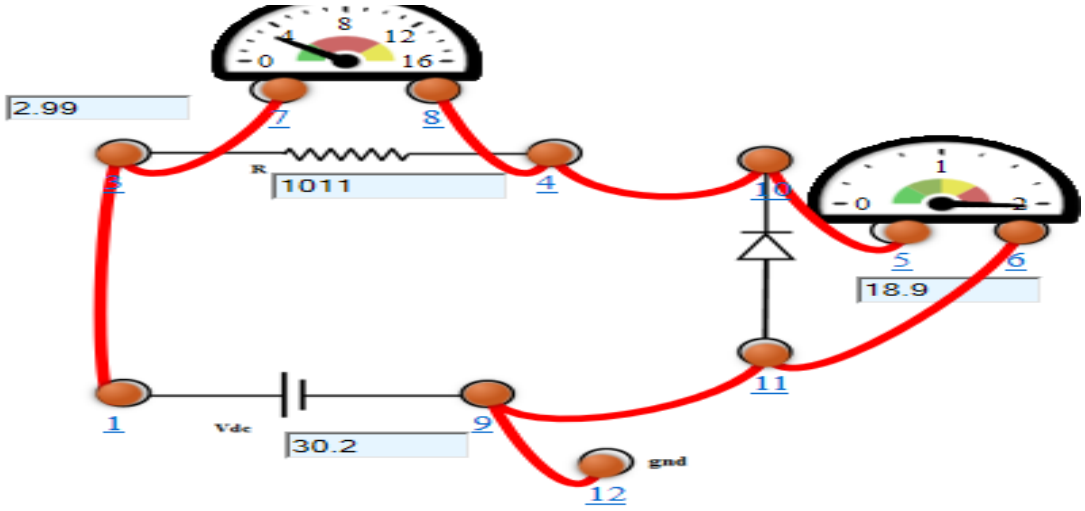


Wiring Diagram:

(A) Forward Biasing:



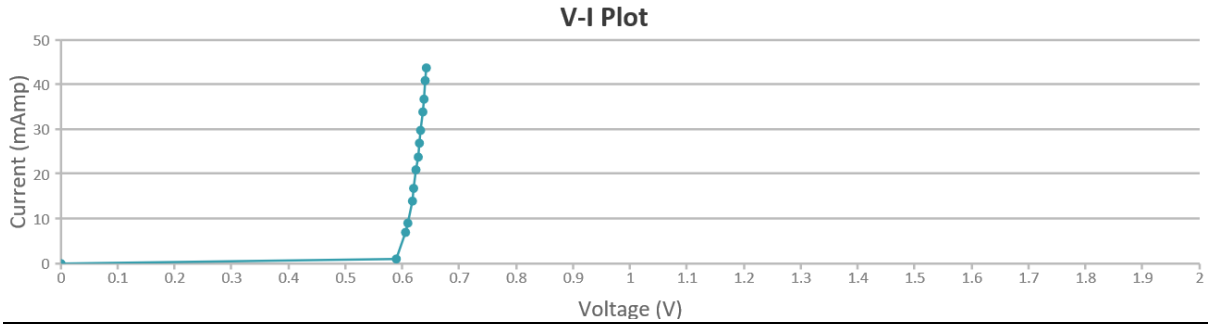
(B) Reverse Biasing:



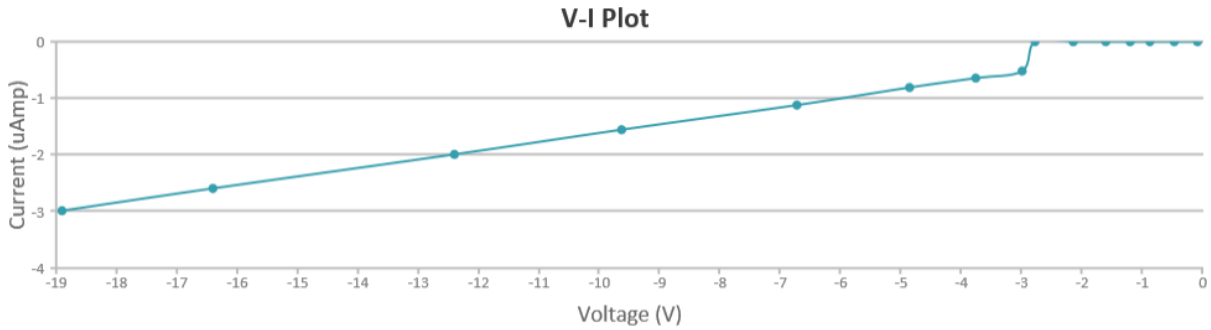
Graph:

(A) Silicon Diode:

(1) Forward Biasing:

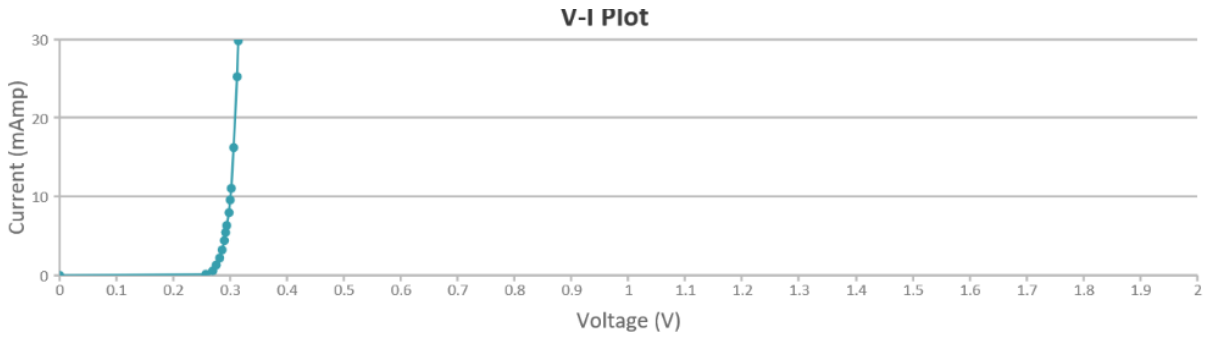


(2) Reverse Biasing:

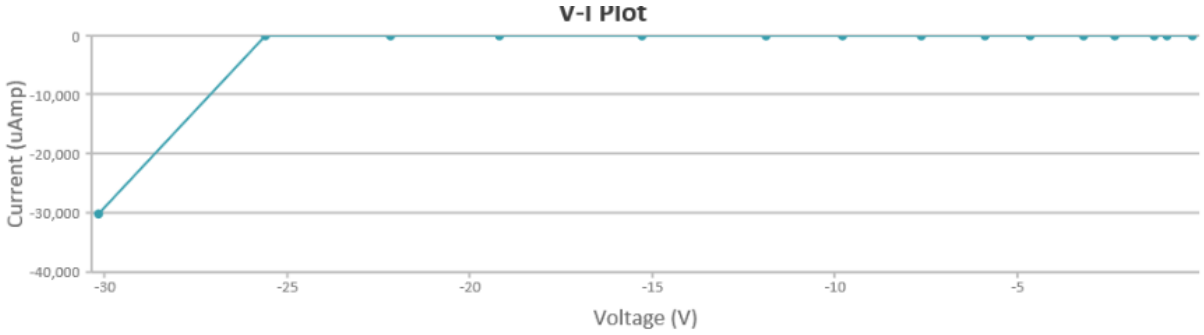


(B) Germanium Diode:

(1) Forward Biasing:



(2) Reverse Biasing:



Observations:

(A) Silicon Diode:

(1) Forward Biasing:

Serial No.	Forward Voltage(Volt)	Forward Current(mAmp)
1	0	0
2	0.589	0.997
3	0.605	6.98
4	0.609	8.97
5	0.617	14.0
6	0.620	16.9
7	0.624	20.9
8	0.627	23.9
9	0.630	26.9
10	0.632	29.9
11	0.635	33.9
12	0.637	36.9
13	0.639	40.9
14	0.641	43.9

(2) Reverse Biasing:

Serial No.	Reverse Voltage(Volt)	Reverse Current(µAmp)
1	0.0993	0
2	0.482	0
3	0.881	0
4	1.20	0
5	1.61	0
6	2.15	0
7	2.78	0
8	2.99	0.509
9	3.76	0.633
10	4.86	0.811
11	6.73	1.11
12	9.64	1.56
13	12.4	1.99
14	16.4	2.60
15	18.9	2.99

(B) Germanium Diode:

(1) Forward Biasing:

Serial No.	Forward Voltage(Volt)	Forward Current(mAmp)
1	0	0
2	0.257	0.100
3	0.268	0.600
4	0.276	1.30
5	0.281	2.20
6	0.286	3.25
7	0.290	4.50
8	0.292	5.40
9	0.294	6.30
10	0.297	8.05
11	0.299	9.65
12	0.301	11.1
13	0.306	16.3
14	0.312	25.3
15	0.314	29.9

(2) Reverse Biasing:

Serial No.	Reverse Voltage(Volt)	Reverse Current(µAmp)
1	0.200	0
2	0.900	0
3	1.25	0
4	2.35	0
5	3.20	0
6	4.65	0
7	5.90	0
8	7.65	0
9	9.80	0
10	11.9	0
11	15.3	0
12	19.2	0
13	22.2	0
14	25.6	0
15	30.2	30199.999999999996

Calculations: Dynamic Resistance for Silicon Diode

(A) Forward Biasing:

From the graph,

V1= 2.77 Volts

V2= 3.07 Volts

I1= 0.570 Amp

I2= 0.573 Amp

Dynamic Resistance, $R_{ac} = \Delta V_{dc}/\Delta I_{dc} = (V2-V1)/(I2-I1)$

= (3.07-2.77)/(0.573-0.570)

= 0.3/0.003=100Ω

(B) Reverse Biasing:

From the graph,

V1= 6.48 Volts

V2= 8.36 Volts

I1= 1.07 µAmp

I2= 1.41 µAmp

Dynamic Resistance, $R_{ac} = \Delta V_{dc}/\Delta I_{dc} = (V2-V1)/(I2-I1)$

= (8.36-6.48)/(1.41-1.07)

= $(1.88 \times 10^6)/0.34=5.529 \times 10^6\Omega$

Result: From the graph we get:

(A) Silicon Diode:

Forward Cut-in Voltage = 0.589 Volts ≈ 0.6 Volts

Knee Voltage = 0.589 Volts ≈ 0.6 Volts

Reverse Saturation Current= -3µAmpere

(B) Germanium Diode:

Forward Cut-in Voltage = 0.257 Volts ≈ 0.3 Volts

Knee Voltage = 0.257 Volts ≈ 0.3 Volts

Reverse Saturation Current= -30,000 µAmpere

Conclusion: The V-I characteristics of forward biasing and reverse biasing current has been obtained and studied successfully.

Experiment 2

Aim: To study the I-V characteristics of Zener Diode-Voltage Regulator.

Tools Used: Virtual Labs.

Theory:

Zener Diode: A Zener Diode is a special kind of diode which permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above the breakdown voltage or 'zener' voltage. Zener diodes are designed so that their breakdown voltage is much lower - for example just 2.4 Volts.

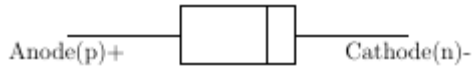


Fig 1: Structure of Zener Diode

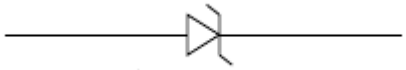


Fig 2: Symbolic Representation of Zener Diode

Function of Zener Diode:

- Zener diodes are a special kind of diode which permits current to flow in the forward direction.
- Zener diodes will also allow current to flow in the reverse direction when the voltage is above a certain value. This breakdown voltage is known as the Zener voltage. In a standard diode, the Zener voltage is high, and the diode is permanently damaged if a reverse current above that value is allowed to pass through it.
- In the reverse bias direction, there is practically no reverse current flow until the breakdown voltage is reached. When this occurs there is a sharp increase in reverse current. Varying amount of reverse current can pass through the diode without damaging it. The breakdown voltage or zener voltage (VZ) across the diode remains relatively constant.

Zener Diode As A Voltage Regulator: A voltage regulator is an electronic circuit that provides a stable DC voltage independent of the load current, temperature and AC line voltage variations. A Zener diode of break down voltage VZ is reverse connected to an input voltage source VI across a load resistance RL and a series resistor RS. The voltage across the zener will remain steady at its break down voltage VZ for all the values of zener current IZ as long as the current remains in the break down region. Hence a regulated DC output voltage V0=VZ is obtained across RL, whenever the input voltage remains within a minimum and maximum voltage. Basically there are two type of regulations such as:

- Line Regulation: In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value.

- Load Regulation: In this type of regulation, input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value.

(A) Line Regulation:

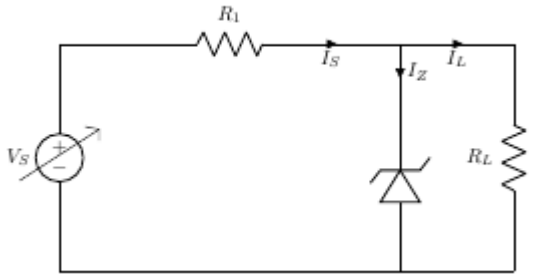


Fig 3: Circuit Diagram of Line Regulation of Zener Diode

In Line Regulation, Load resistance is constant and input voltage varies. VI must be sufficiently large to turn the Zener Diode ON.

$$V_L = V_z = \frac{V_{Imin} \times R_L}{(R_s + R_L)}$$

So, the minimum turn-on voltage V_{Imin} is:

$$V_{imin} = \frac{V_z \times (R_s + R_L)}{R_L}$$

The maximum value of V_I is limited by the maximum zener current I_{Zmax}

$$I_R = I_{Zmax} + I_L$$

I_L is fixed at:

$$\frac{V_s}{R_s} \qquad since, V_L = V_Z$$

So, maximum V_I is

$$V_{Imax} = V_{Rmax} + V_Z$$

$$or$$

$$V_{Imax} = I_{Rmax} \times R + V_Z$$

For $V_I < V_z$,

$$V_O = V_I$$

For $V_I > V_Z$,

$$V_O = V_I - I_s \times R_s$$

(B) <u>Load Regulation:</u>

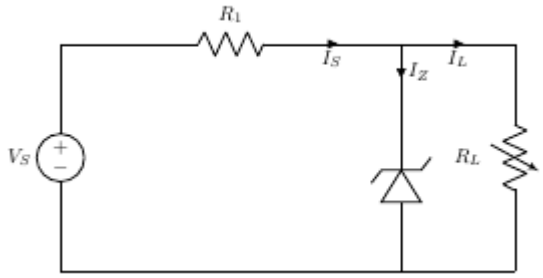


Fig 4: Circuit Diagram of Load Regulation of Zener Diode

In Load Regulation, input voltage is constant and Load resistance varies. Too small a Load Resistance R_L, will result in V_{Th}<V_Z and Zener Diode will be OFF.

$$V_L = V_z = \frac{V_{Imin} \times R_L}{(R_S + R_L)}$$

So, the minimum load resistance R_L

$$R_{Lmin} = \frac{V_Z \times R_S}{V_I - V_Z}$$

Any load resistance greater than R_{Lmin} will make Zener Diode ON

$$I_S = I_Z + I_L$$

R_{Lmin} will establish maximum I_L as

$$I_{Lmax} = \frac{V_L}{R_{Lmin}} = \frac{V_Z}{R_{Lmin}} \qquad \text{since, } \mathrm{V_L} = \mathrm{V_Z}$$

V_S is the voltage drop across R_S

$$V_S = V_{Imin} - V_Z$$

$$I_S = \frac{V_{Imin} - V_Z}{R_S}$$

For $R_L < R_{Lmin}$,

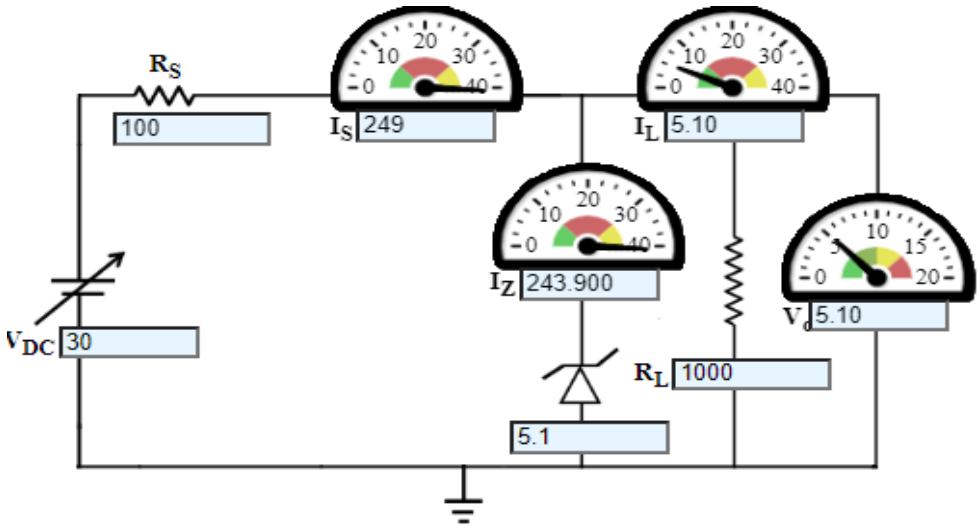
$$V_O = V_I$$

For $R_L > R_{Lmin}$,

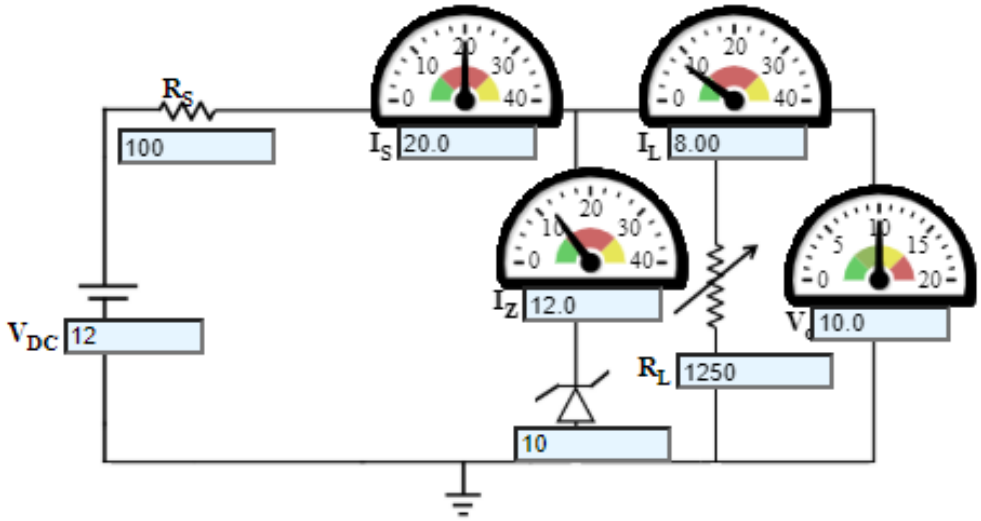
$$V_O = V_I - I_s \times R_s$$

Circuit Diagram:

(A) Line Regulation:

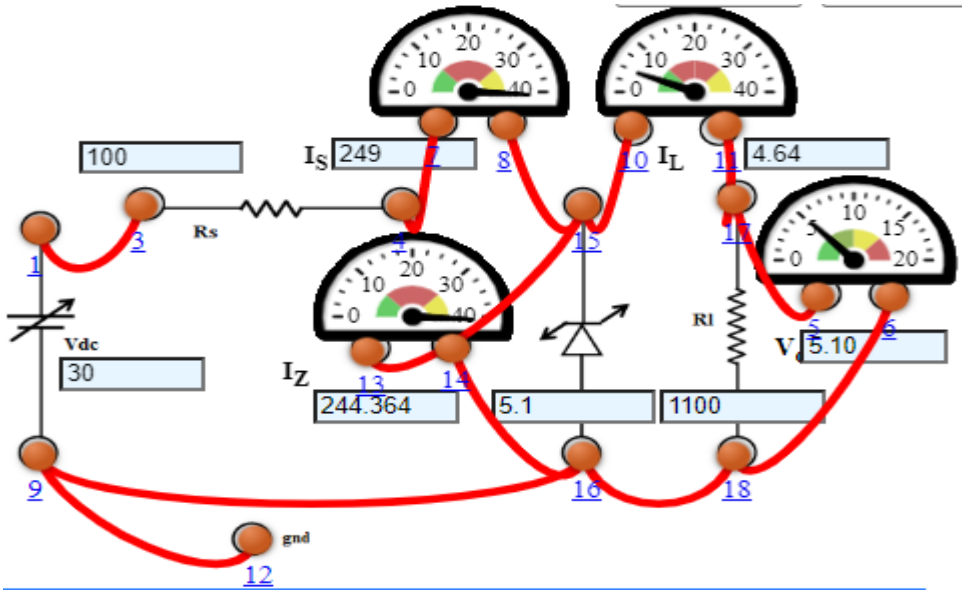


(B) Load Regulation:

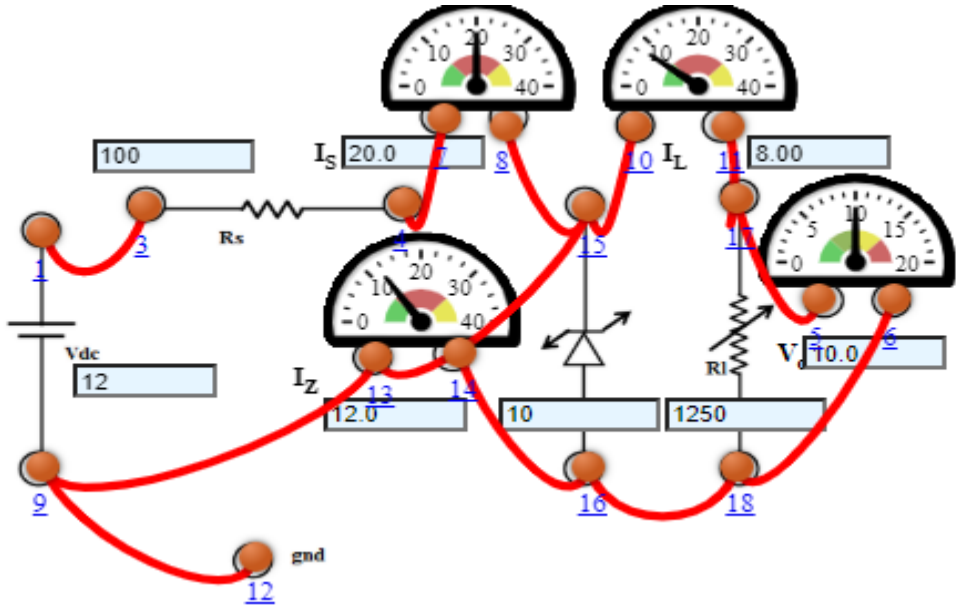


Wiring Diagram:

(A) Line Regulation:

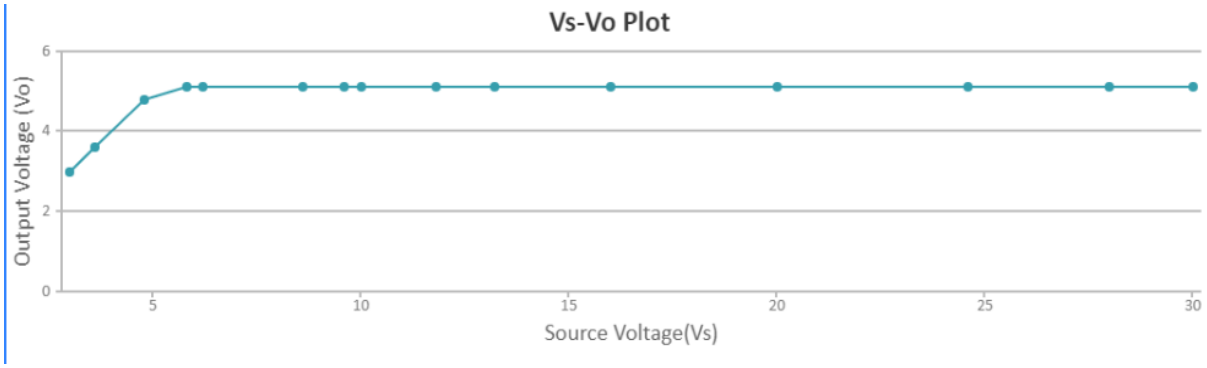


(B) Load Regulation:

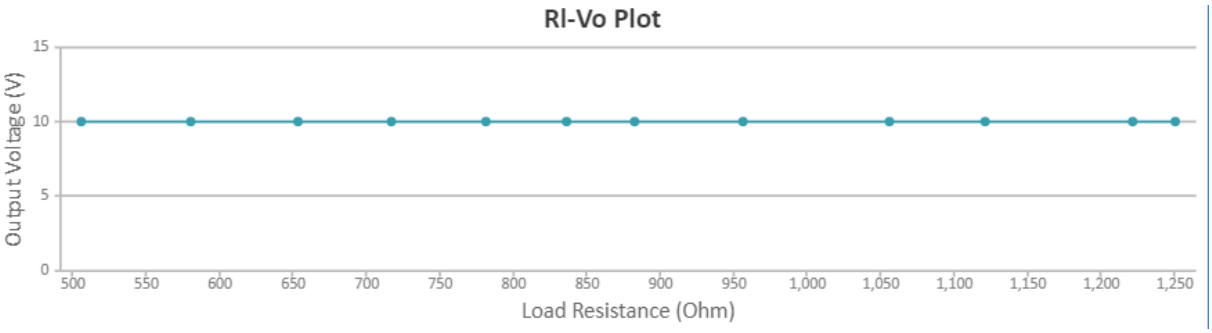


Graph:

(A) Line Regulation:



(B) Load Regulation:



Observations:

(A) Line Regulation:

DC Voltage (V_{DC}) = 12 V

Zener Voltage (V_Z) = 10 V

Series Resistance (R_S) = 0.1 KΩ

S. No.	Load Resistance (R_L) Ω	Load Current (I_L) m Amp	Zener Current (I_Z) m Amp	Regulated Output Voltage (V_O) V	% Voltage Regulation
1	506	19.8	0.237	10.0	16.5
2	580	17.2	2.76	10.0	14.7
3	653	15.3	4.69	10.0	13.3
4	717	13.9	6.05	10.0	12.2
5	781	12.8	7.20	10.0	11.4
6	836	12.0	8.04	10.0	10.7
7	882	11.3	8.66	10.0	10.2
8	956	10.5	9.54	10.0	9.47
9	1056	9.47	10.5	10.0	8.65

10	1121	8.92	11.1	10.0	8.19
11	1221	8.19	11.8	10.0	7.57
12	1250	8.00	12.0	10.0	7.41

(B) Load Regulation:

Zener Voltage (V_Z) = 5.1 V

Series Resistance (R_S) = 0.1 KΩ

Load Resistance (R_L) = 1 KΩ

S. No.	Unregulated Supply Voltage (V_S) V	Load Current (I_L) m Amp	Zener Current (I_Z) m Amp	Regulated Output Voltage (V_O) V	% Voltage Regulation
1	3	5.10	0	3	100
2	3.6	5.10	0	3.6	100
3	4.8	5.10	0	4.8	100
4	5.8	5.10	1.900	5.10	100
5	6.2	5.10	5.900	5.10	83.3
6	8.6	5.10	29.900	5.10	62.5
7	9.6	5.10	39.900	5.10	55.6
8	10	5.10	43.900	5.10	50.0
9	11.8	5.10	61.900	5.10	45.5
10	13.2	5.10	75.900	5.10	38.5
11	16	5.10	103.900	5.10	31.3
12	20	5.10	143.900	5.10	25.0
13	24.6	5.10	189.900	5.10	20.8
14	28	5.10	223.900	5.10	17.9
15	30	5.10	243.900	5.10	16.7

Result: The V-I characteristics of Zener diode as a voltage regulator has been studied and the graph has been plotted successfully.

Experiment 3

Aim: To Study Half Wave Rectifier.

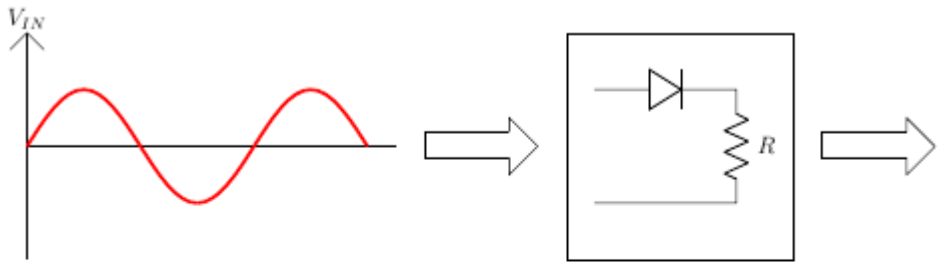
Tools Used: Virtual Labs.

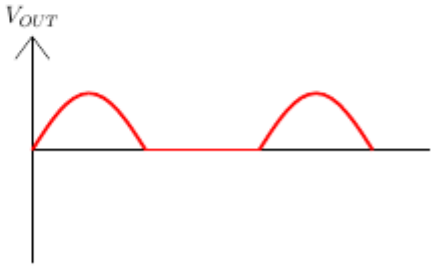
Theory:

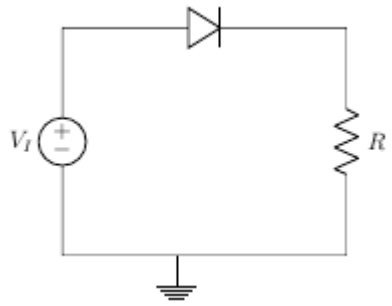
Rectification: A rectifier is a device that converts alternating current (AC) to direct current (DC), a process known as rectification. On the positive cycle the diode is forward biased and on the negative cycle the diode is reverse biased. By using a diode, one can convert an AC source into a pulsating DC source. In summary we have 'rectified' the AC signal. Rectifiers are essentially of two types:

- Half Wave Rectifier
- Full Wave Rectifier

Half Wave Rectifier: The simplest kind of rectifier circuit is the half-wave rectifier. The half-wave rectifier is a circuit that allows only part of an input signal to pass. The circuit is simply the combination of a single diode in series with a resistor, where the resistor is acting as a load.







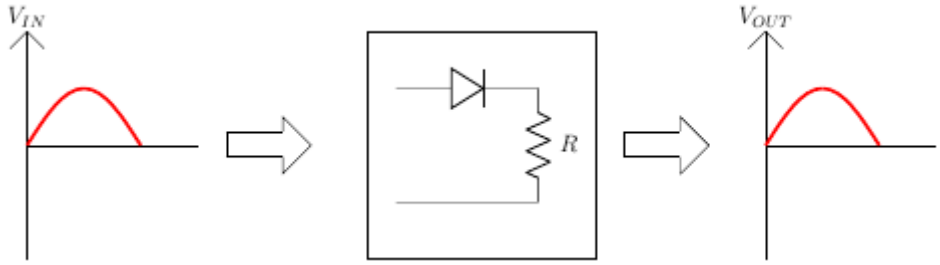
Half Wave Rectifier Waveforms: The output DC voltage of a half wave rectifier can be calculated with the following two ideal equations.

$$V_{peak} = V_{rms} \times \sqrt{2}$$

$$V_{dc} = \frac{V_{peak}}{\pi}$$

Half Wave Rectification for Positive Half Cycle: Diode is forward biased, acts as a short circuit, passes the waveform through.

For positive half cycle:



$$V_I - V_b - I \times r_b - I \times R = 0$$

where,

V_I is the input voltage,

V_b is barrier potential,

r_d is diode resistance,

I is total current,

R is resistance

$$I = \frac{V_I - V_b}{r_b + R}$$

$$V_O = I \times R$$

$$V_O = \frac{V_I - V_b}{r_b + R} \times R$$

For $r_d << R$,

$$V_O = V_I - V_b$$

V_b is 0.3 for Germanium,

V_b is 0.7 for Silicon

For $V_I < V_b$,

The diode will remain OFF. The Output voltage will be,

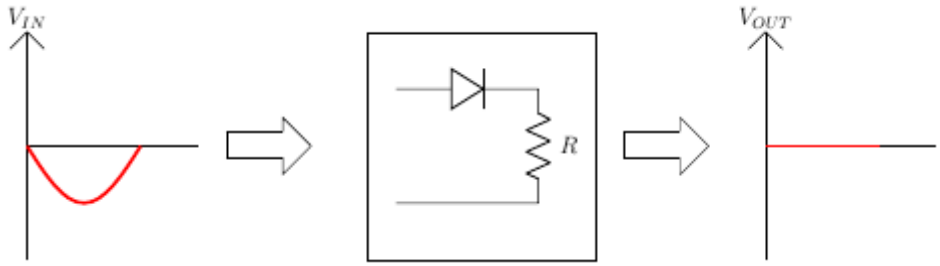
$$V_O = 0$$

For $V_I > V_b$,

The diode will be ON. The Output voltage will be,

$$V_O = V_I - V_b$$

Half Wave Rectification for Negative Half Cycle:



Diode is reverse biased, acts as a open circuit, does not pass the waveform through.

For negative half cycle:

$$V_O = 0 \text{ since, } I = 0$$

Half Wave Rectification for an Ideal Diode:

For Ideal Diode,

$$V_b = 0$$

For positive half cycle,

$$V_O = V_I$$

For negative half cycle,

$$V_O = 0$$

Average Output Voltage:

$$V_O = V_m \sin \omega t \ \ for\ 0 \leq \omega t \leq \pi$$

$$V_O = 0\ for\ \pi \leq \omega t \leq 2\pi$$

$$V_{av} = \frac{V_m}{\pi} = 0.318V_m$$

RMS Load Voltage:

$$V_{rms} = I_{rms} \times R = \frac{V_m}{2}$$

Average Load Current:

$$V_{av} = \frac{I_{av}}{R} = \frac{I_m}{\pi \times R} = \frac{V_m}{\pi}$$

RMS load current:

$$I_{rms} = \frac{I_m}{2}$$

Form Factor: It is defined as the ratio of rms load voltage and average load voltage.

$$F.F. = \frac{V_{rms}}{V_{av}}$$

$$F.F. = \frac{\frac{V_m}{2}}{\frac{V_m}{\pi}} = \frac{\pi}{2} = 1.57$$

$F.F. \geq 1$

$V_{rms} \geq V_{av}$

Ripple Factor:

$$\gamma = \sqrt{F.F.^2 - 1} \times 100\%$$

$$\gamma = \sqrt{1.57^2 - 1} \times 100\% = 1.21\%$$

Efficiency: It is defined as ratio of dc power available at the load to the input ac power.

$$\eta\% = \frac{P_{load}}{P_{in}} \times 100\%$$

$$\eta\% = \frac{I_{dc}^2 \times R}{I_{rms}^2 \times R} \times 100\%$$

$$\eta\% = \frac{\frac{I_m^2}{\pi^2}}{\frac{I_m^2}{4}} \times 100\% = \frac{4}{\pi^2} \times 100\% = 40.56\%$$

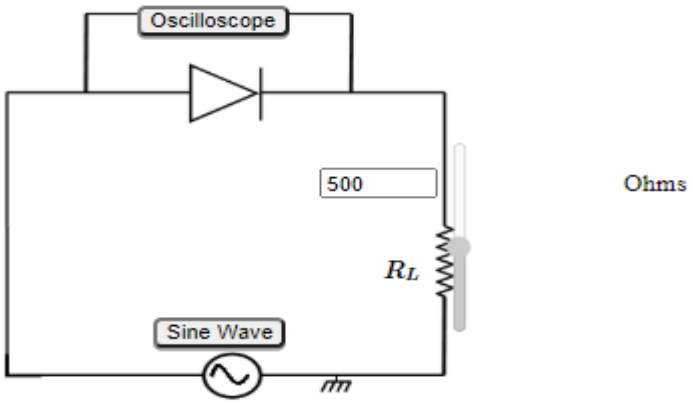
Peak Inverse Voltage: For rectifier applications, peak inverse voltage (PIV) or peak reverse voltage (PRV) is the maximum value of reverse voltage which occurs at the peak of the input cycle when the diode is reverse-biased. The portion of the sinusoidal waveform which repeats or duplicates itself is known as the cycle. The part of the cycle above the horizontal axis is called the positive half-cycle, the part of the cycle below the horizontal axis is called the negative half cycle. With reference to the amplitude of the cycle, the peak inverse voltage is specified as the maximum negative value of the sine-wave within a cycle's negative half cycle.

$$PIV = V$$

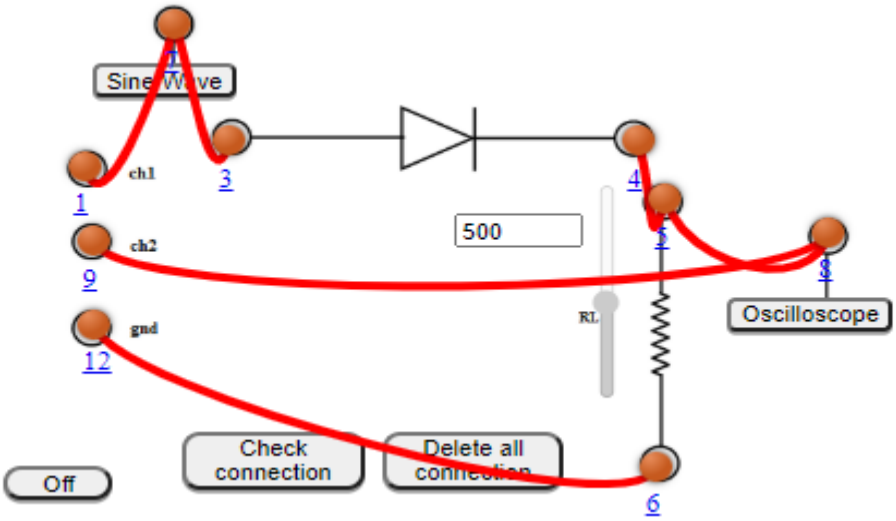
$$-V_m + V = 0 \Longrightarrow V = V_m$$

$$PIV \geq V_m$$

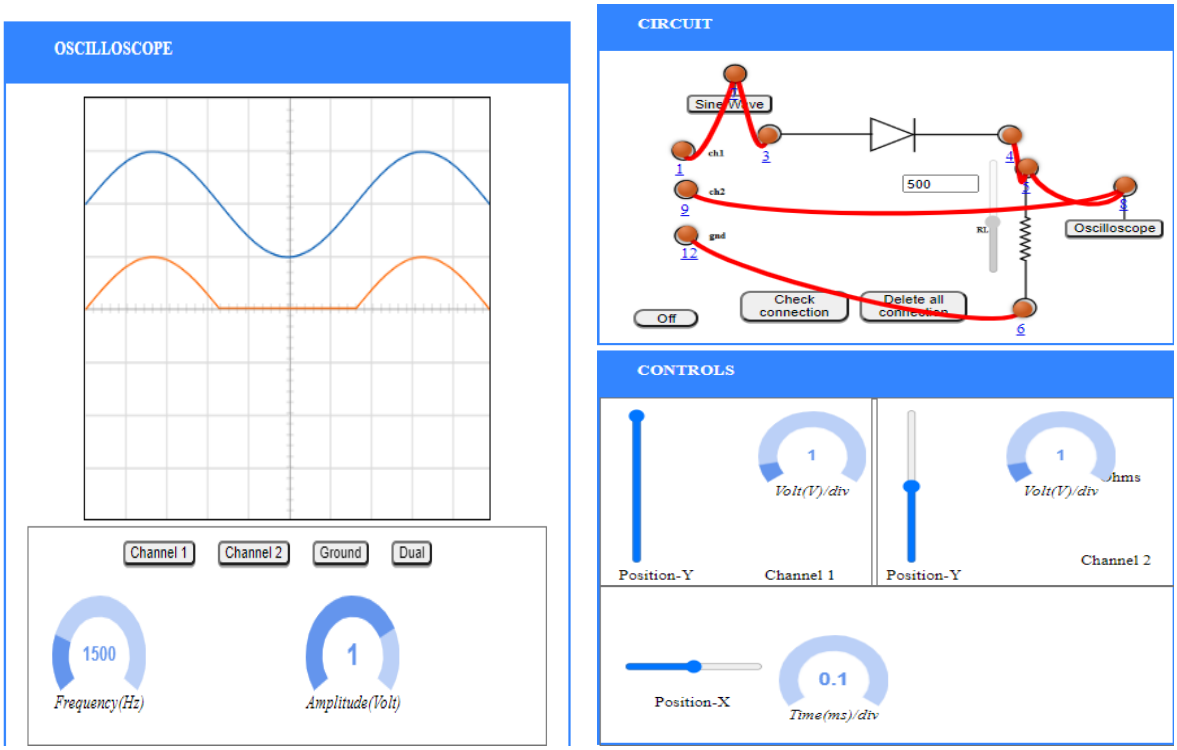
Circuit Diagram:



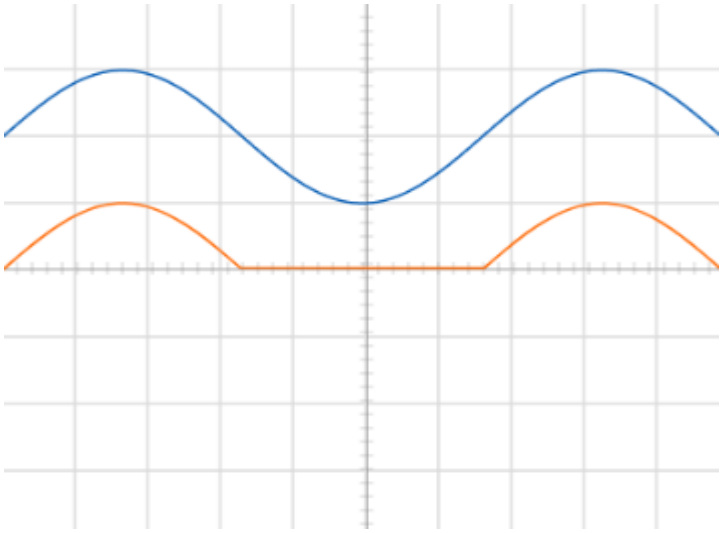
Wiring Diagram:



Experimental Setup:



Graph:



Observations and Calculations:

A.C. Frequency = 1500 Hz

Amplitude, Amp= 1Volts

$V_m = Amp \times \frac{volt}{div} = 1 \times 1 = 1Volts$

$V_{rms} = \frac{V_m}{2} = \frac{1}{2} = 0.5Volts$

$V_{dc} = \frac{V_m}{\pi} = \frac{1}{\pi}$ = 0.31847Volts

Ripple actor , $\gamma_{exp} = \sqrt{\left(\frac{V_{rms}}{Vdc}\right)^2 - 1}$ = $\sqrt{1.57000659}$ = 1.252996672≈ 1.25

Standard Value of Ripple Factor, γ_{std} = 1.21

%Error = $\frac{\gamma_{exp} - \gamma_{std}}{\gamma_{std}} \times 100 = 3.30\%$

Result: The ripple factor of Half Wave Rectifier is = 1.25 volts.

Standard Value of ripple factor is = 1.21

Percentage error = 3.30%

Conclusion: The properties of half wave rectifier has been studied successfully and the ripple factor has been calculated successfully.

Experiment 4

Aim: To Study Full Wave Rectifier

Tools Used: Virtual Labs.

Theory:

Full Wave Rectifier: A full-wave rectifier is exactly the same as the half-wave but allows unidirectional current through the load during the entire sinusoidal cycle (as opposed to only half the cycle in the half-wave). A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output.
For a full wave rectifier,
Average Output Voltage:

$$V_O = V_m \sin \omega t \ \ for\ 0 \leq \omega t \leq \pi$$

$$V_{av} = \frac{2V_m}{\pi} = 0.636V_m$$

RMS Load Voltage:

$$V_{rms} = I_{rms} \times R = \frac{V_m}{\sqrt{2}}$$

Average Load Current:

$$V_{av} = \frac{I_{av}}{R} = \frac{2I_m}{\pi \times R} = \frac{2V_m}{\pi}$$

RMS load current:

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

Form Factor: It is defined as the ratio of rms load voltage and average load voltage.

$$F.F. = \frac{V_{rms}}{V_{av}}$$

$$F.F. = \frac{\frac{V_m}{\sqrt{2}}}{\frac{2V_m}{\pi}} = \frac{\pi}{2\sqrt{2}} = 1.11$$

$F.F. \geq 1$

$V_{rms} \geq V_{av}$

Ripple Factor:

$$\gamma = \sqrt{F.F.^2 - 1}\ \times 100\%$$

$$\gamma = \sqrt{1.11^2 - 1} \times 100\% = 48.1\%$$

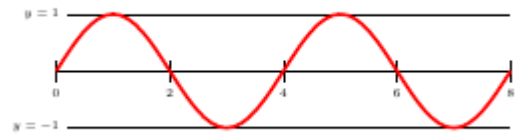
Efficiency: It is defined as ratio of dc power available at the load to the input ac power.

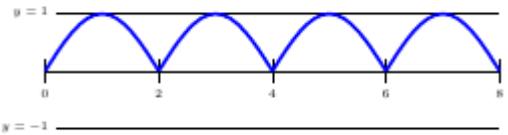
$$\eta\% = \frac{P_{load}}{P_{in}} \times 100\%$$

$$\eta\% = \frac{I_{dc}^2 \times R}{I_{rms}^2 \times R} \times 100\%$$

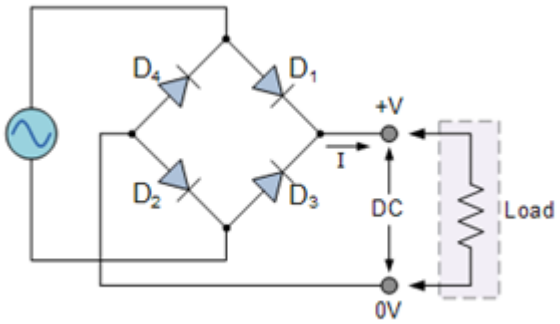
$$\eta\% = \frac{\frac{4I_m^2}{\pi^2}}{\frac{I_m^2}{2}} \times 100\% = \frac{8}{\pi^2} \times 100\% = 81.13\%$$

Full Wave Rectifier – Waveforms:

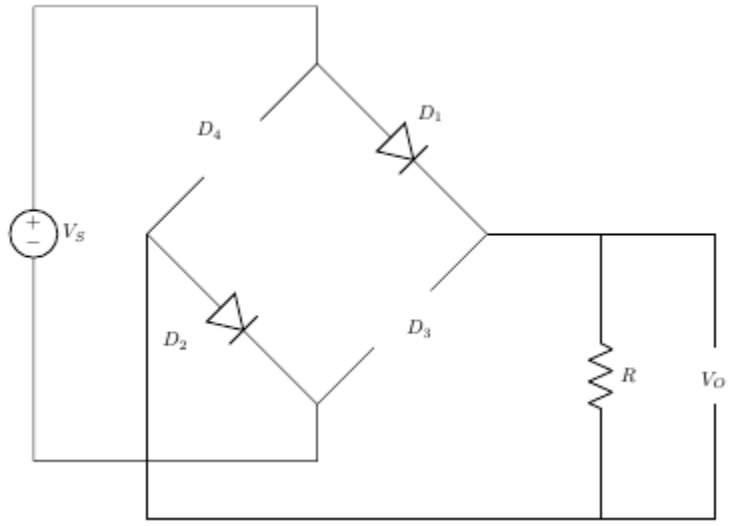




Full wave Bridge Rectifier: Bridge rectifier uses 4 rectifying diodes connected in a "bridged" configuration to produce the desired output but does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side.



For Positive Half Cycle:
During the positive half cycle of the supply diodes D1 and D2 conduct in series while diodes D3 and D4 are reverse biased (ideally they can be replaced with open circuits) and the current flows through the load as shown below.



$$V_o - V_I = 0$$
$$V_o = V_I$$
$$V_O = V_I - 2V_b$$
$$V_I - 2V_b - I \times r_d = 0$$

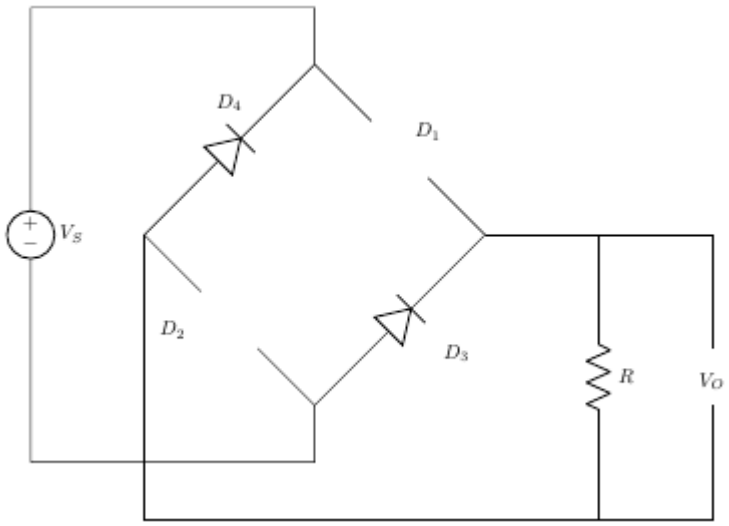
where,

V_I is the input voltage,

V_b is barrier potential,

r_d is diode resistance

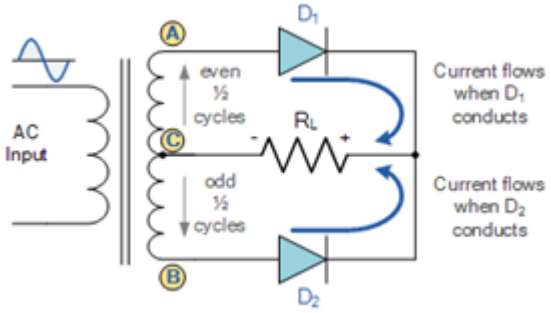
For Negative Half Cycle:



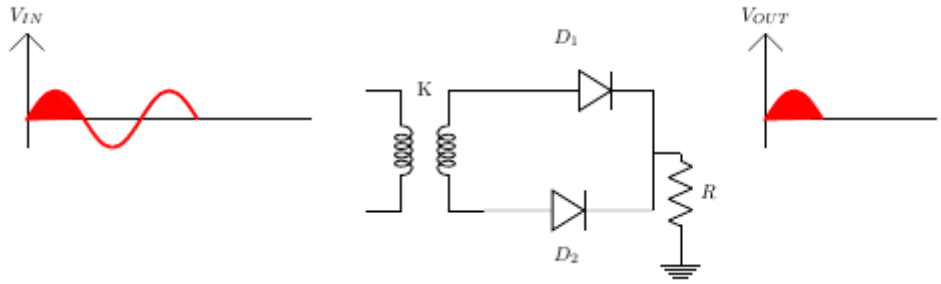
$$V_o - V_I = 0$$
$$V_o = V_I$$

Centre Tapped Full Wave Rectifier: A Full-Wave Rectifier can be constructed using Centre-Tapped transformer – which give us two shifted sinusoids so that exactly one of the waveforms is positive at one time and two diodes. As compared to the half wave rectifier we use two diodes instead of one; one of the two diodes remain in conduction in both of the half cycles. At any

point in time, only one of the diodes is forward biased. This allows for continuous conduction through load.



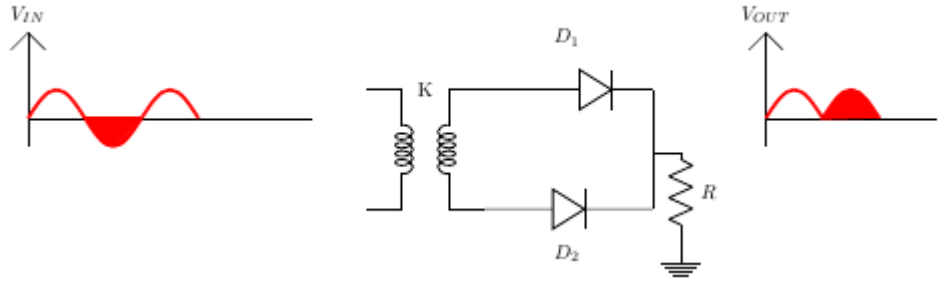
For Positive Half Cycle:



For Positive Cycle D1 is Forward Biased and D2 is Reverse Biased

$$V_o - V_I = 0$$
$$V_o = V_I$$

For Negative Half Cycle:



For Negative Cycle D1 is Reverse Biased and D2 is Forward Biased

$$V_o - V_I = 0$$
$$V_o = V_I$$

Peak Inverse Voltage: For rectifier applications, peak inverse voltage (PIV) or peak reverse voltage (PRV) is the maximum value of reverse voltage which occurs at the peak of the input cycle when the diode is reverse-biased. The portion of the sinusoidal waveform which repeats or duplicates itself is known as the cycle. The part of the cycle above the horizontal axis is called the positive half-cycle, the part of the cycle below the horizontal axis is called the negative half cycle. With reference to the amplitude of the cycle, the peak inverse voltage is specified as the maximum negative value of the sine - wave within a cycle's negative half cycle.
For Bridge Rectifier,
D1 and D2 is Forward Biased
D3 and D4 is Reverse Biased

$$V_o - V_m = 0$$
$$V_o = V_m$$

$$PIV = V$$

$$-V_0 + PIV = 0 \Longrightarrow PIV = V_m$$

$$PIV \geq V_m$$

For Center Tapped Rectifier,
D2 is Forward Biased,
PIV at D1,

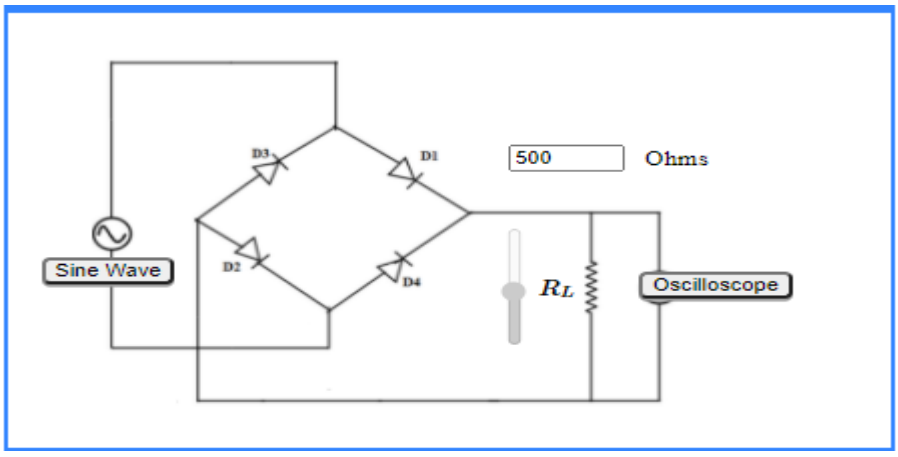
$$V_o - V_m = 0$$
$$V_o = V_m$$

$$PIV = V$$

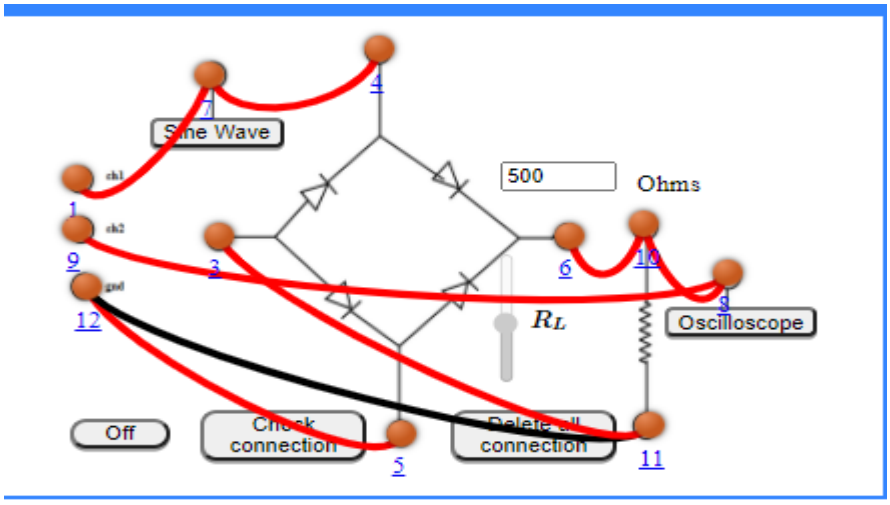
$$-V_0 + PIV - V_m = 0 \Longrightarrow PIV = 2V_m$$

$$PIV \geq 2V_m$$

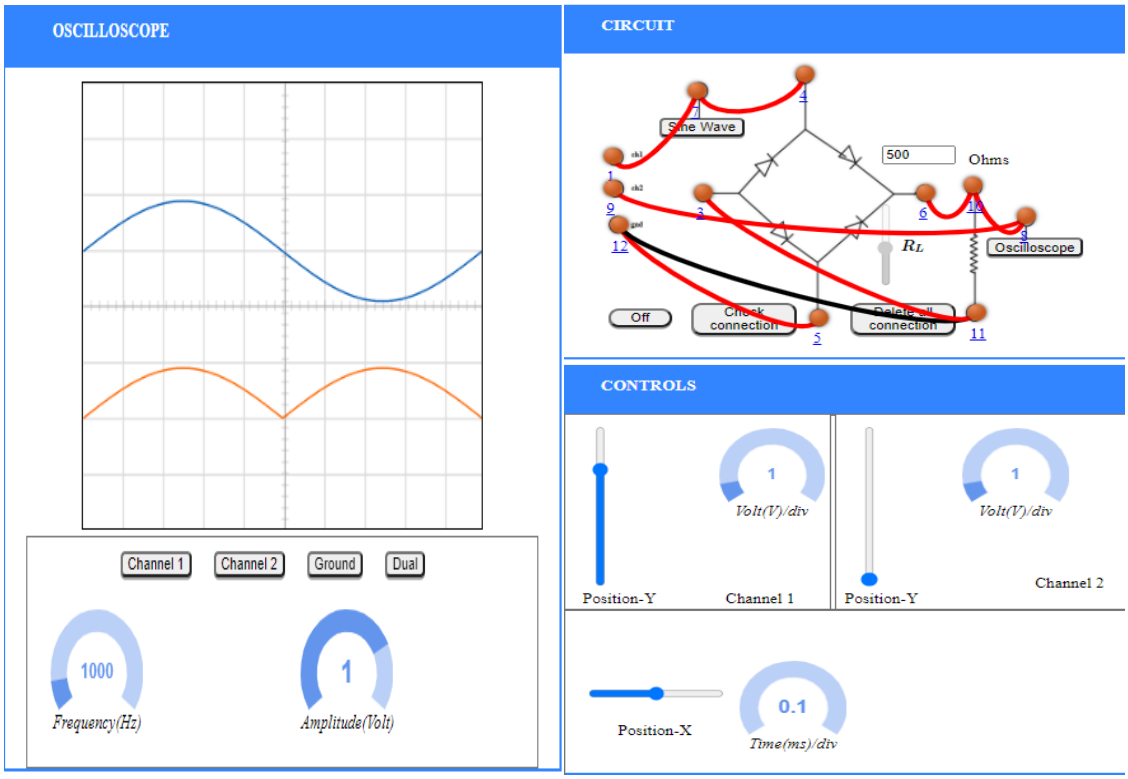
Circuit Diagram:



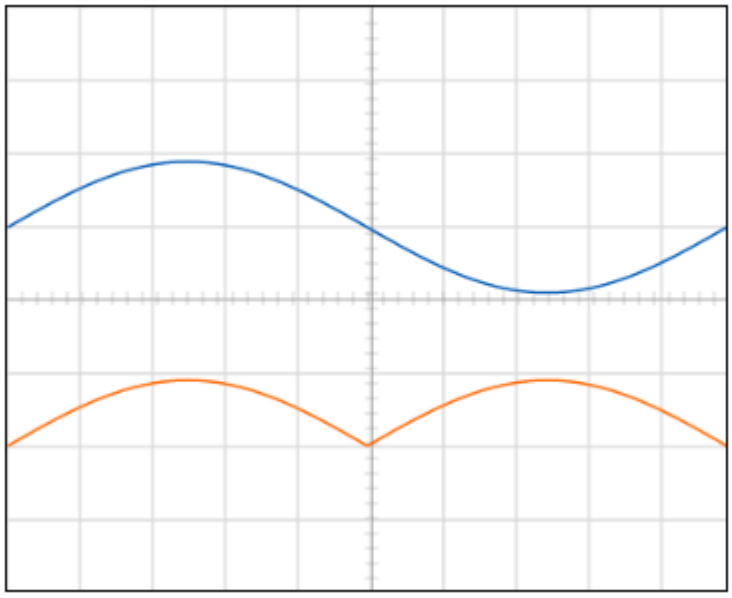
Wiring Diagram:



Experimental Setup:



Graph:



Observations and Calculations:

A.C. Frequency = 1000 Hz

Amplitude, Amp= 1Volts

$V_m = Amp \times \frac{volt}{div} = 1 \times 1 = 1Volts$

$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{1}{\sqrt{2}} = 0.707V$olts

$V_{dc} = \frac{2V_m}{\pi} = \frac{2}{\pi}$ = 0.6369Volts

Ripple actor , γ_{exp}= $\sqrt{\left(\frac{V_{rms}}{Vdc}\right)^2 - 1}$ = $\sqrt{1.11 - 1}$ = 0.33

Standard Value of Ripple Factor, γ_{std} = 0.481

%Error = $\frac{\gamma_{exp} - \gamma_{std}}{\gamma_{std}} \times 100 = 31.39\%$

Result: The ripple factor of Full Wave Rectifier is = 0.33

Standard Value of ripple factor is = 0.481

Percentage error = 31.39%

Conclusion: The properties of full wave rectifier has been studied successfully and the ripple factor has been calculated successfully.

Experiment 5

Aim: To study the input and output characteristics of a transistor in its common Emitter configurations (CE).

Tools Used: Virtual Labs.

Theory: A bipolar junction transistor, BJT, is a single piece of silicon with two back-to-back P-N junctions' can be made either as PNP or as NPN. They have three regions and three terminals, emitter, base, and collector represented by E, B, and C respectively. The direction of the arrow indicates the direction of the current in the emitter when the transistor is conducting normally.

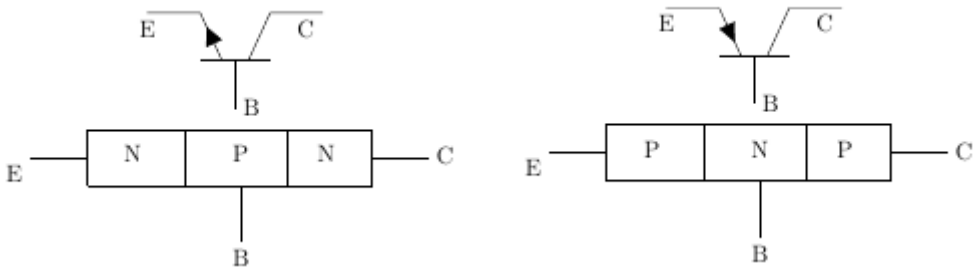


Fig 1: Representation of NPN and PNP transistor respectively

Emitter (E): It is the region to the left end which supply free charge carriers i.e., electrons in n-p-n or holes in p-n-p transistors. These majority carriers are injected to the middle region i.e. electrons in the p region of n-p-n or holes in the n region of p-n-p transistor. Emitter is a heavily doped region to supply a large number of majority carriers into the base.

Base (B): It is the middle region where either two p-type layers or two n-type layers are sandwiched. The majority carriers from the emitter region are injected into this region. This region is thin and very lightly doped.

Collector (C): It is the region to right end where charge carriers are collected. The area of this region is largest compared to emitter and base region. The doping level of this region is intermediate between heavily doped emitter region and lightly doped base region.

In CE configuration, the input current I_B and the output current I_C are related by the equation shown below.

$$I_E=I_C+I_B$$

Operation of Bipolar Junction Transistor:

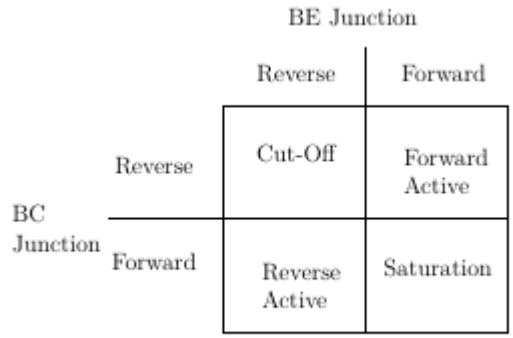


Fig 2:Four Operating Conditions

Cut-Off Region: In Cut-Off region both junctions are reverse biased, Base-emitter junction is reverse biased (V_{BE}<0)and also Collector-Base junction is reverse biased(V_{CB}>0).With reverse biasing, all currents are zero.There are some leakage currents associated with reverse biased junctions,but these currents are small and therefore can be neglected.

Application: Open switch

Forward Active Region: In Forward Active region Base-emitter junction is forward biased(V_{BE}>0) and Collector-Base junction is reverse biased(V_{CB}>0). In this case, the forward bias of the BE junction will cause the injection of both holes and electrons across the junction. The holes are of little consequence because the doping levels are adjusted to minimize the hole current. The electrons are the carriers of interest. The electrons are injected into the base region where they are called the minority carrier even though they greatly outnumber the holes.

Application: Amplifier in analog circuits

$$I_C=\alpha_F \times I_E+I_{CO}$$

where,

α_F is the forward current transfer ratio

ICO is Collector reverse saturation current

Saturation Region: In Saturation region both junctions are Forward biased,Base-emitter junction is forward biased(V_{BE}>0) and also Collector-Base junction is forward biased(V_{CB}<0). Maximum currents flows through the transistor with only a small voltage drop across the collector junction.The transistor also does not respond to any change in emitter current or base-emitter voltage.

Application: Closed switch

Reverse Active Region: In Reverse Active region Base-emitter junction is reverse biased(V_{BE}<0) and Collector-Base junction is forward biased(V_{CB}<0).The operation is just the same as the forward active region, except all voltage sources, and hence collector and emitter currents, are the reverse of the forward bias case. The current gain in this mode is smaller than that of forward active mode for which this mode in general unsuitable for amplification.

Application: In digital circuits and analog switching circuits.

$$I_E = -\alpha_R * I_C + I_{EO}$$

where,

α_R is the reverse current transfer ratio\newline I_{EO} is the Emitter reverse saturation current

This configuration is rarely used because most transistors are doped selectively to give forward current transfer ratios very near unity, which automatically causes the reverse current transfer ratio to be very low.

BJT -Common Emitter Circuit:

The DC behavior of the BJT can be described by the Ebers-Moll Model. The equations for the model are:

$$I_F = I_{ES} \times (\exp^{VBE/VT} - 1)$$

$$I_R = I_{CS} \times (\exp^{VCB/VT} - 1)$$

where,

I_{ES} is base-emitter saturation currents,

I_{CS} is base-collector saturation currents

$$V_T = (k \times T)/q$$

where,

k is the Boltzmann's constant (k = 1.381 e^{-23} V.C/ K),

T is the absolute temperature in degrees Kelvin, and

q is the charge of an electron (q = 1.602 e^{-19} C).

$$\beta_F = \alpha_F/(1 - \alpha_F)$$

$$\beta_R = \alpha_R/(1 - \alpha_R)$$

where,

β_F is large signal forward current gain of common-emitter configuration,

β_R is the large signal reverse current gain of the common-emitter configuration

$$\alpha_F = \beta_F/(1 + \beta_F)$$

$$\alpha_R = \beta_R/(1 + \beta_R)$$

where,

α_R is large signal reverse current gain of a common-base configuration,

α_F is large signal forward current gain of the common-base configuration.

$$I_C = \alpha_F \times I_F - I_R$$

$$I_E = -I_F + \alpha_R * I_R$$

$$I_B=(1-\alpha_F)\times I_F+(1-\alpha_R)\times I_R$$

The forward and reverse current gains are related by the expression

$$\alpha_R\times I_{CS}=\alpha_F\times I_{ES}=I_S$$

where,

IS is the BJT transport saturation current.

The parameters α_R and α_F are influenced by impurity concentrations and junction depths.

The saturation current, I_S , can be expressed as

$$I_S=J_S\times A$$

where,

A is the area of the emitter and

J_S is the transport saturation current density.

Input Characteristics: The most important characteristic of the BJT is the plot of the base current, I_B, versus the base-emitter voltage, $v_{BE}$for various values of the collector-emitter voltage, v_{CE}.

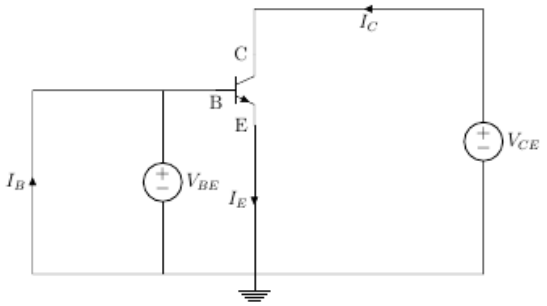


Fig 3: Input Characteristics Circuit

Output Characteristics: The most important characteristic of the BJT is the plot of the collector current, I_C, versus the collector-emitter voltage,v_{CE}, for various values of the base current, I_B,as shown on the circuit on the right.

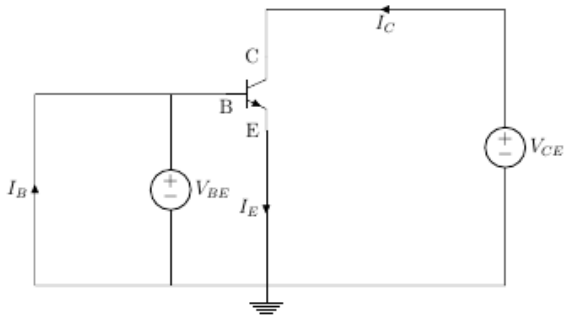
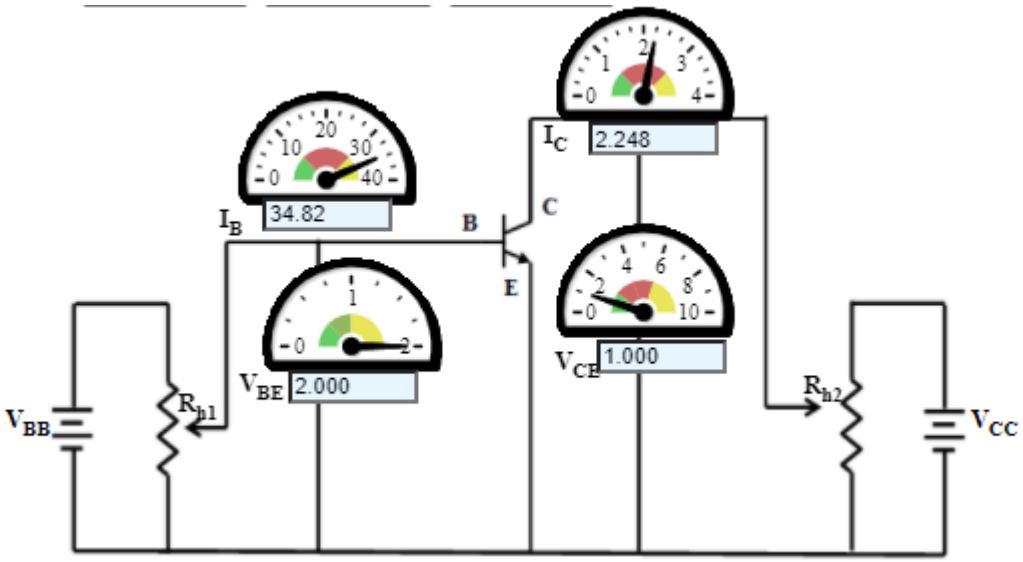


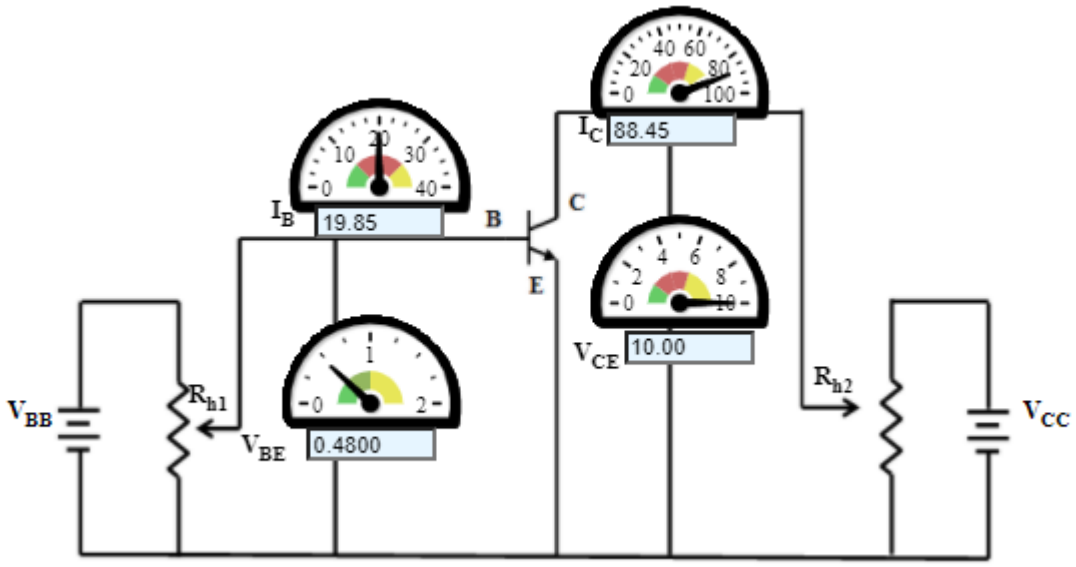
Fig 4: Output Characteristics Circuit

Circuit Diagram:

(A) Input Characteristics:

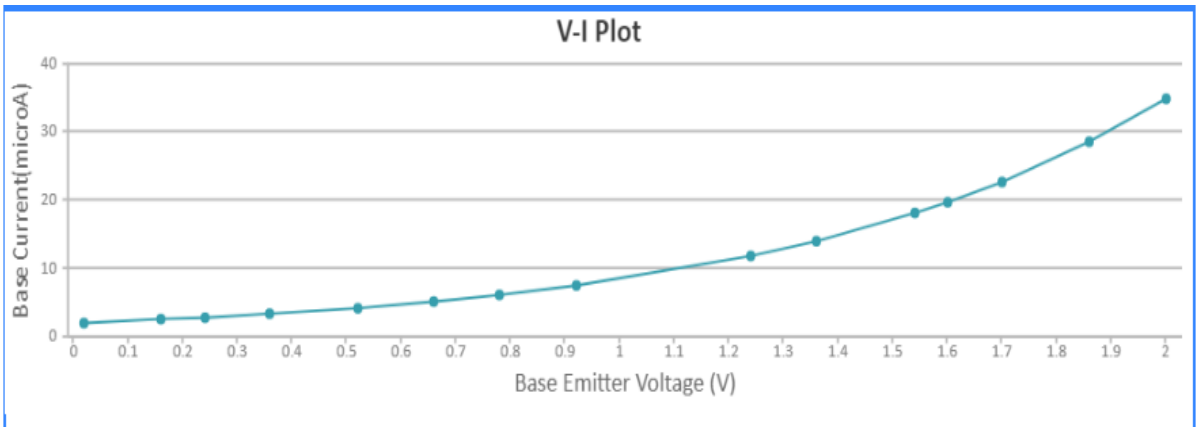


(B) Output Characteristics:



Graph:

(A) Input Characteristics:



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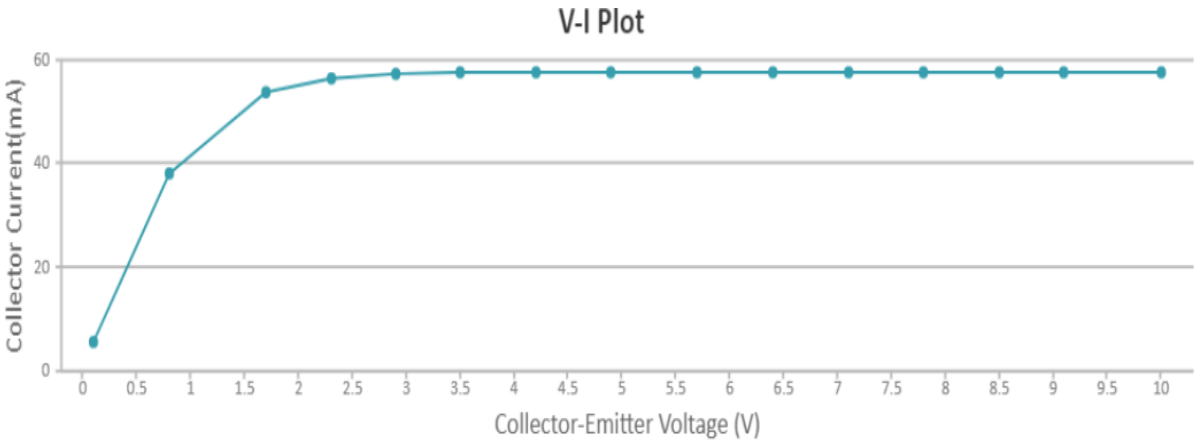


Observations:

(A) Input Characteristics:

Collector Emitter Voltage, V_{CE}=1.000 Volts

S.No.	Base Emitter Voltage (V)	Base Emitter Current (µA)
1	0.02000	2.058
2	0.1600	2.514
3	0.2400	2.818
4	0.3600	3.345
5	0.5200	4.204
6	0.6600	5.135
7	0.7800	6.095
8	0.9200	7.444
9	1.240	11.76
10	1.360	13.96
11	1.540	18.05
12	1.600	19.67
13	1.700	22.69
14	1.860	28.51
15	2.000	34.82

(B) Output Characteristics:

Base Current, I_B=14.92 µA

S.No.	Collector Emitter Voltage (V)	Collector Current (mA)
1	0.1000	5.743
2	0.8000	38.26
3	1.700	53.90
4	2.300	56.47
5	2.900	57.27

6	3.500	57.52
7	4.200	57.59
8	4.900	57.61
9	5.700	57.62
10	6.400	57.62
11	7.100	57.62
12	7.800	57.62
13	8.500	57.62
14	9.600	57.62
15	10.00	57.62

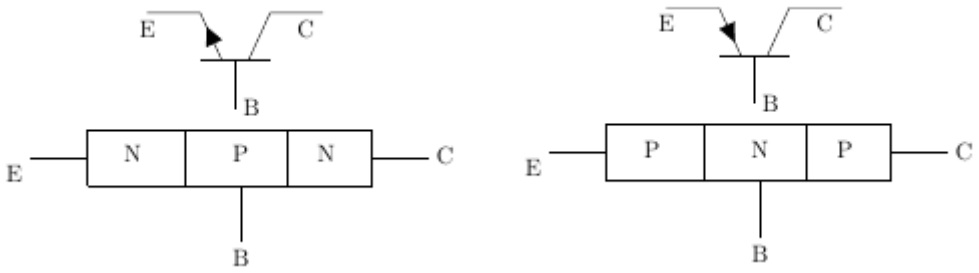
Result and Conclusion: The input and output characteristics of Common Emitter configuration of n-p-n transistor has obtained and plotted successfully.

Experiment 6

Aim: To study the input and output characteristics of a transistor in its Common Base configurations (CB).

Tools Used: Virtual Labs.

Theory: A bipolar junction transistor, BJT, is a single piece of silicon with two back-to-back P-N junctions' can be made either as PNP or as NPN. They have three regions and three terminals, emitter, base, and collector represented by E, B, and C respectively. The direction of the arrow indicates the direction of the current in the emitter when the transistor is conducting normally.



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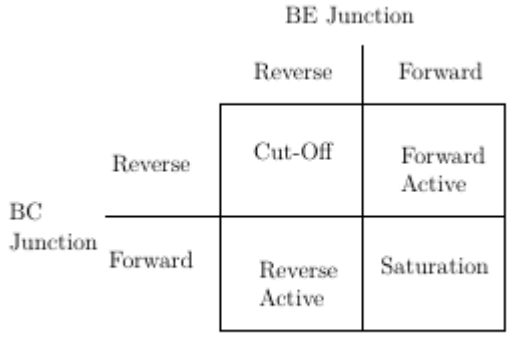

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Application:Amplifier in analog circuits

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Saturation Region: In Saturation region both junctions are Forward biased,Base-emitter junction is forward biased(V_{BE}>0) and also Collector-Base junction is forward biased(V_{CB}<0). Maximum currents flows through the transistor with only a small voltage drop across the collector junction.The transistor also does not respond to any change in emitter current or base-emitter voltage.

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$$\beta_R = \alpha_R/(1-\alpha_R)$$

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β_R is the large signal reverse current gain of the common-emitter configuration

$$\alpha_F = \beta_F/(1+\beta_F)$$

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where,

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α_F is large signal forward current gain of the common-base configuration.

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$$I_E = -I_F + \alpha_R * I_R$$

$$I_B = (1-\alpha_F) \times I_F + (1-\alpha_R) \times I_R$$

The forward and reverse current gains are related by the expression

$$\alpha_R \times I_{CS} = \alpha_F \times I_{ES} = I_S$$

where,

IS is the BJT transport saturation current.

The parameters α_R and α_F are influenced by impurity concentrations and junction depths.

The saturation current, I_S , can be expressed as

$$I_S = J_S \times A$$

where,

A is the area of the emitter and

J_S is the transport saturation current density.

Input Characteristics: The most important characteristic of the BJT is the plot of the base current, I_E, versus the base-emitter voltage, $v_{BE}$for various values of the collector-emitter voltage, v_{CB}.

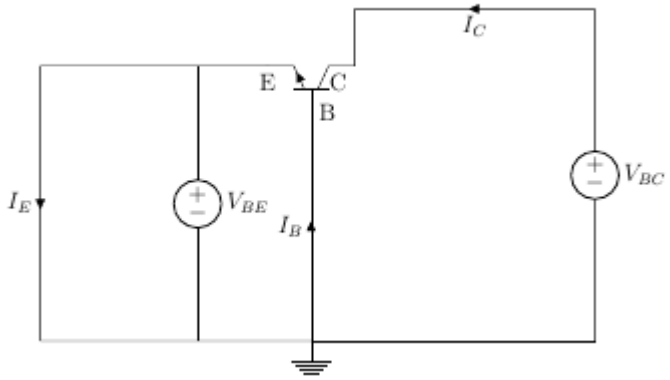


Fig 3: Input Characteristics Circuit

Output Characteristics: The most important characteristic of the BJT is the plot of the collector current, I_C, versus the collector-emitter voltage,v_{CB}, for various values of the base current, I_E,as shown on the circuit on the right.

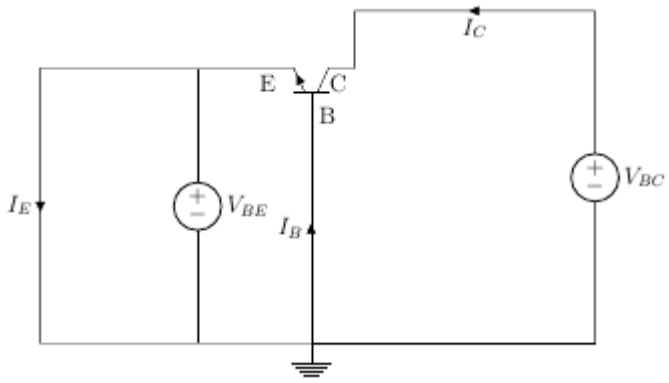
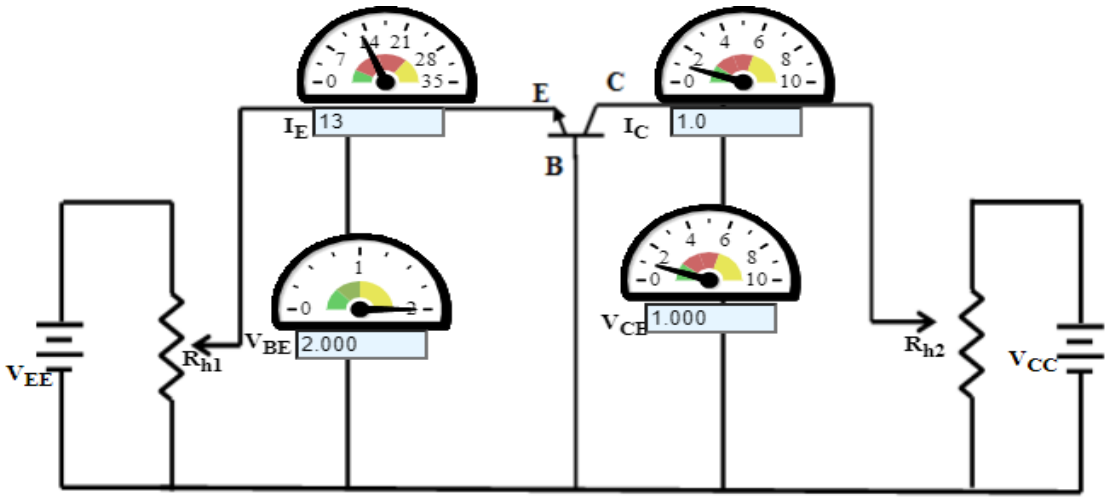


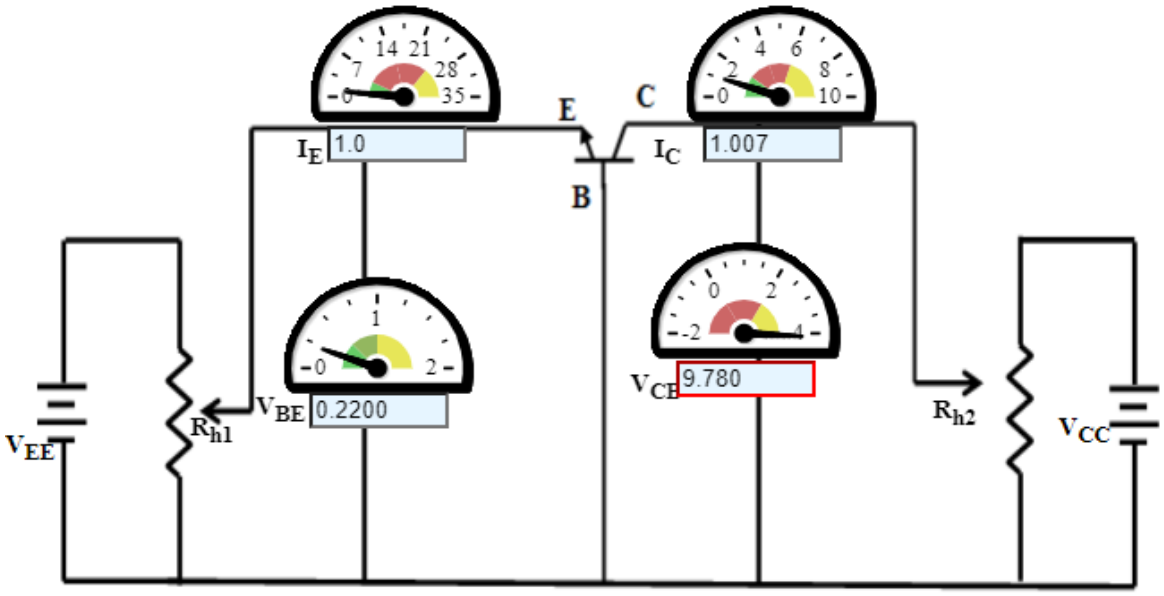
Fig 4: Output Characteristics Circuit

Circuit Diagram:

(C) Input Characteristics:

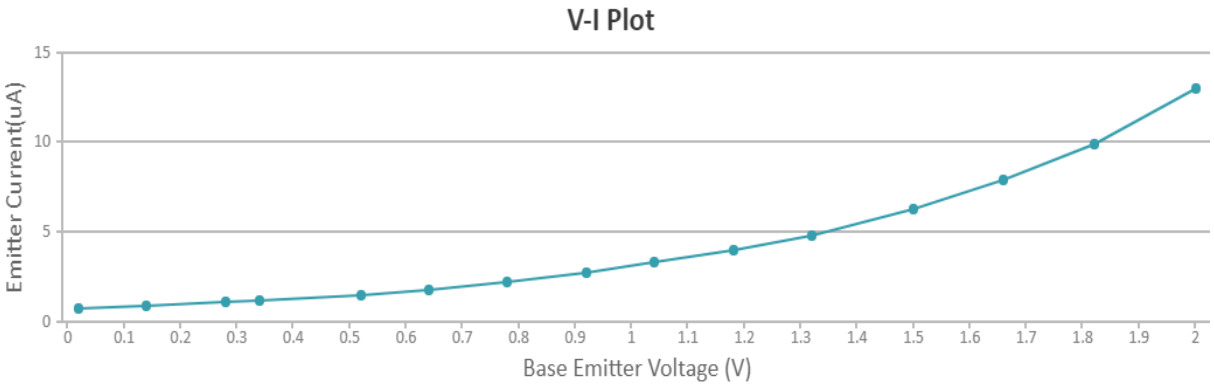


(D) Output Characteristics:

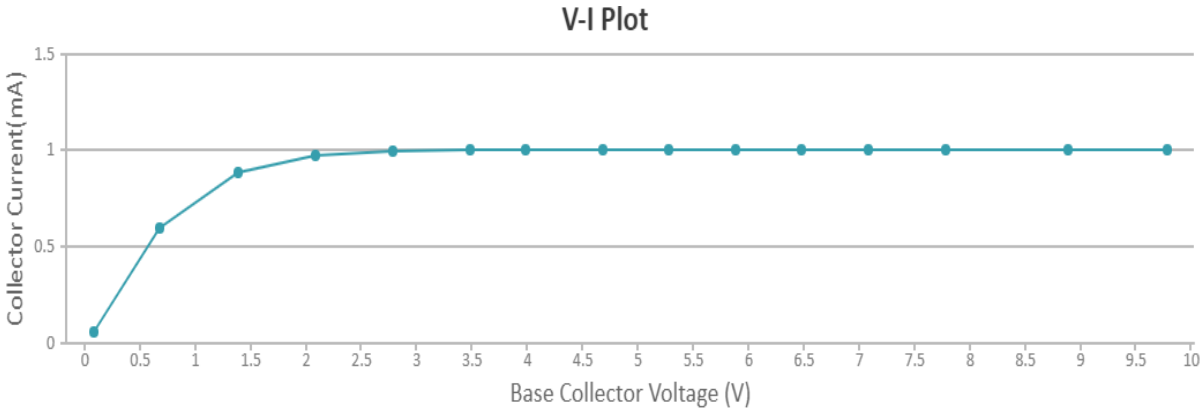


Graph:

(A) Input Characteristics:



(B) Output Characteristics:



Observations:

(A) Input Characteristics:

Base Collector Voltage, V_{CB}=1.000 Volts

S.No.	Base Emitter Voltage (V)	Emitter Current (mA)
1	0.02000	0.76
2	0.1400	0.90
3	0.2800	1.1
4	0.3400	1.2
5	0.5200	1.5
6	0.6400	1.8
7	0.7800	2.2
8	0.9200	2.7
9	1.040	3.3
10	1.180	4.0
11	1.320	4.8
12	1.500	6.3
13	1.660	7.9
14	1.820	9.9
15	2.000	1.3

(B) Output Characteristics:

Emitter Current, I_E=1.0 mA

S.No.	Base Collector Voltage (V)	Collector Current (mA)
1	0.08000	0.06043
2	0.6800	0.5959
3	1.380	0.8875
4	2.080	0.9764
5	2.780	0.9997
6	3.480	1.005
7	3.980	1.007
8	4.680	1.007
9	5.280	1.007
10	5.880	1.007
11	6.480	1.007
12	7.080	1.007
13	7.780	1.007
14	8.880	1.007
15	9.780	1.007

Result and Conclusion: The input and output characteristics of Common Base configuration of n-p-n transistor has obtained and plotted successfully.

Experiment 7

Aim: To study the gain and plot the frequency response of a single stage transistor amplifier (BJT CE Amplifier).

Tools Used: Virtual Labs.

Theory: The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification.

Resistors R_{B1} and R_{B2} form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter-base junction is operating in the proper region.

In order to operate transistor as an amplifier, biasing is done in such a way that the operating point is in the active region. For an amplifier, the Q-point is placed so that the load line is bisected. Therefore, in practical design V_{CE} is always set to $V_{CC}/2$. This will confirm that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. For the maximum input signal, output is produced without any distortion and clipping

The Bypass Capacitor: The emitter resistor R_E is required to obtain the DC quiescent point stability. However, the inclusion of R_E in the circuit causes a decrease in amplification at higher frequencies. In order to avoid such a condition, it is bypassed by a capacitor so that it acts as a short circuit for AC and contributes stability for DC quiescent condition. Hence capacitor is connected in parallel with emitter resistance.

$$X_{CE} \ll R_E$$

$$\frac{1}{2 \times \pi \times f \times C_E} \ll R_E$$

$$C_E \gg \frac{1}{2 \times \pi \times f \times R_E}$$

The Input/ Output Coupling (or Blocking) Capacitor: An amplifier amplifies the given AC signal. In order to have noiseless transmission of a signal (without DC), it is necessary to block DC i.e. the direct current should not enter the amplifier or load. This is usually accomplished by inserting a coupling capacitor between two stages.

$$X_{CC} \ll R_i \times h_{ie}$$

$$\frac{1}{2 \times \pi \times f \times C_C} \ll R_i \times h_{ie}$$

$$C_C \gg \frac{1}{2 \times \pi \times f \times (R_i + h_{ie})}$$

C_C - Output Coupling Capacitor

C_B - Input Coupling Capacitor

Frequency response of Common Emitter Amplifier: Emitter bypass capacitors are used to short circuit the emitter resistor and thus increases the gain at high frequency. The coupling and bypass capacitors cause the fall of the signal in the low frequency response of the amplifier because their impedance becomes large at low frequencies. The stray capacitances are effectively open circuits. In the mid frequency range large capacitors are effectively short circuits and the stray capacitors are open circuits, so that no capacitance appears in the mid frequency range. Hence the mid band frequency gain is maximum. At the high frequencies, the bypass and coupling capacitors are replaced by short circuits. The stray capacitors and the transistor determine the response.

The input resistance is medium and is essentially independent of the load resistance R_L. The output resistance is relatively high and is essentially independent of the source resistance.

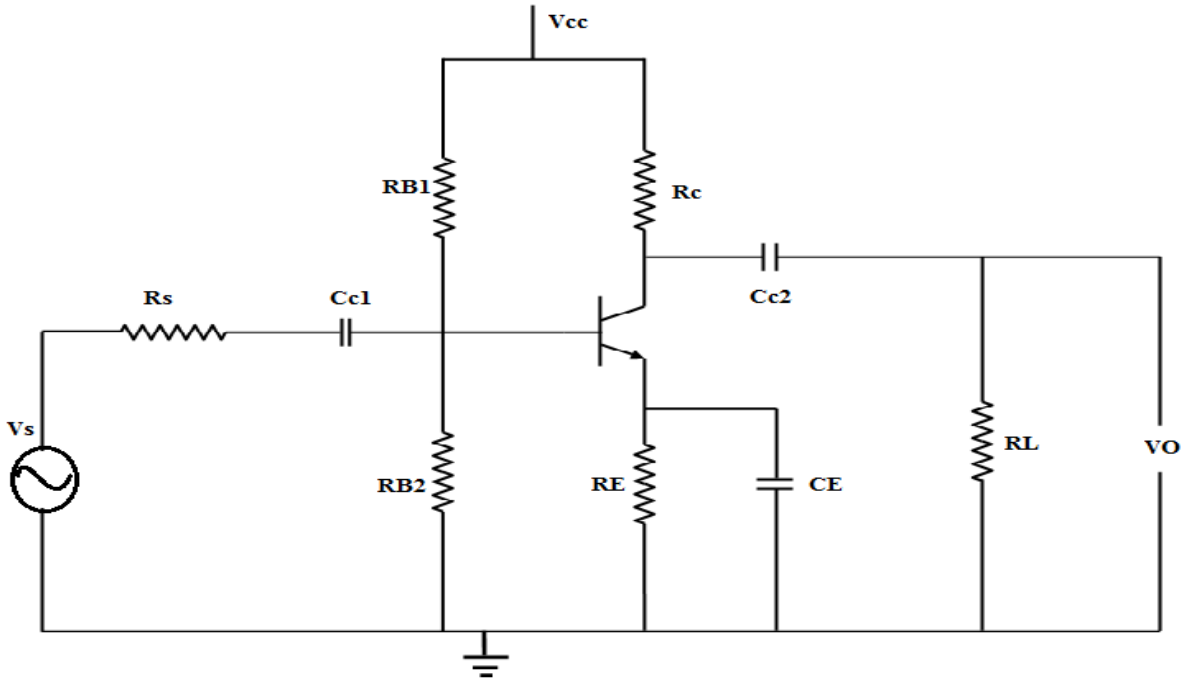


Figure 1

The coupling capacitor, C_{C1}, couples the source voltage V_S to the biasing network. Coupling capacitor C_{C2} connects the collector resistance R_C to the load R_L. The bypass capacitance C_E is used to increase the midband gain, since it effectively short circuits the emitter resistance R_E at midband frequencies. The resistance R_E is needed for bias stability. The external capacitors C_{C1}, C_{C2}, C_E will influence the low frequency response of the common emitter amplifier. The internal capacitances of the transistor will influence the high frequency cut-off.

$$A(s) = \frac{A_m \times S^2 \times (S + \omega_z)}{(S + \omega_{L1}) \times (S + \omega_{L2}) \times (S + \omega_{L3}) \times \left(1 + \frac{S}{\omega_H}\right)}$$

where,

A_m is the midband gain,

ω_H is the frequency of the dominant high frequency pole,

ω_{L1}, ω_{L2}, ω_{L3} are low frequency poles introduced by the coupling and bypass capacitors,

ω_Z is the zero introduced by the bypass capacitor.

The midband gain is obtained by short circuiting all the external capacitors and open circuiting the internal capacitors. Figure 2 shows the equivalent for calculating the midband gain.

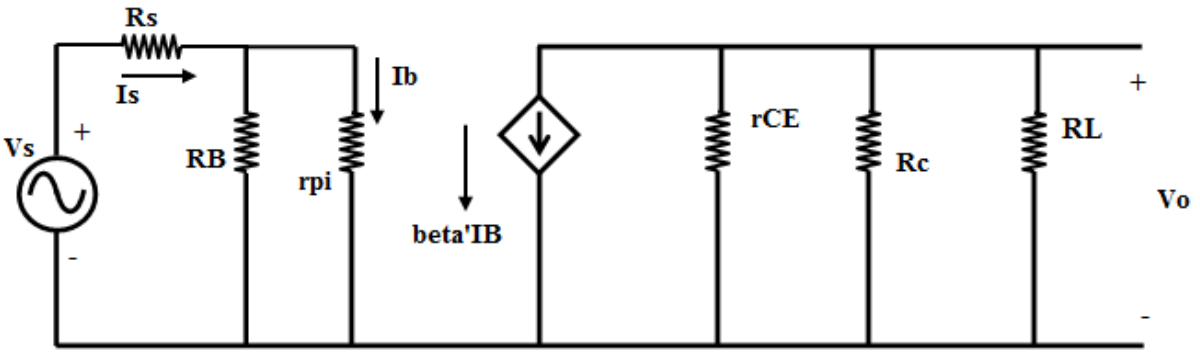


Figure 2

$$A_m = \frac{V_o}{V_s} = -\beta[r_{CE} \parallel R_C \parallel R_L]\left[\frac{R_B}{R_B + r_{pi}}\right]\left[\frac{1}{R_s + (R_B + r_{pi})}\right]$$

It can be shown that the low frequency poles, ω_{L1}, ω_{L2}, ω_{L3} can be obtained by the following equations:

$$\tau_1 = \frac{1}{\omega_{L1}} = C_{C1} \times R_{IN}$$

where,

$$R_{IN} = R_S + [R_B + r_{pi}]$$

$$\tau_2 = \frac{1}{\omega_{L2}} = C_{C2} \times [R_L + (R_L \parallel R_E)]$$

$$\tau_3 = \frac{1}{\omega_{L3}} = C_E \times R'_E$$

$$R'_E = R_E \parallel \left[\frac{r_{pi}}{\beta_F + 1} + \left(\frac{(R_B \parallel R_S)}{\beta_F + 1}\right)\right]$$

$$\omega_Z = \frac{1}{R_E \times C_E}$$

Normally, $\omega_Z < \omega_{L3}$ and the low frequency cut-off ω_L is larger than the largest pole frequency. The low frequency cut-off can be approximated as

$$\omega_L \cong \sqrt{(\omega_{L1})^2 + (\omega_{L2})^2 + (\omega_{L3})^2}$$

The high frequency equivalent circuit of the common-emitter amplifier is shown in Figure 3.

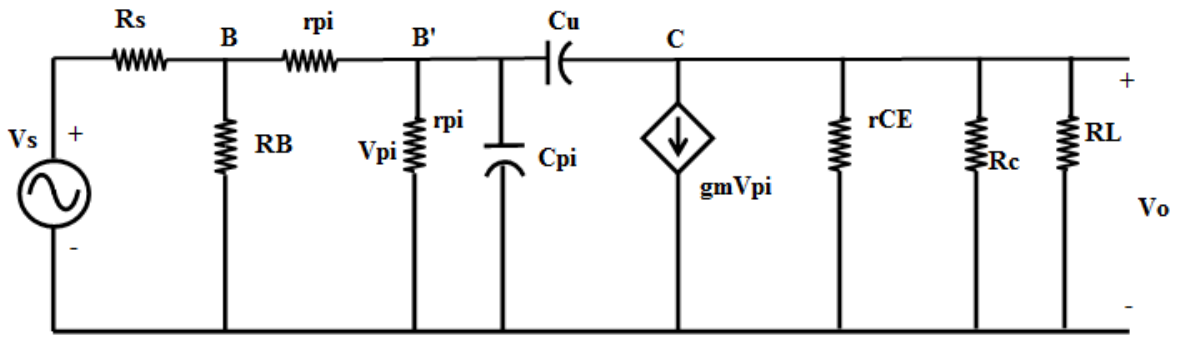


Figure 3

In Figure 3, C_μ is the collector-base capacitance, C_π is the emitter to base capacitance, r_x is the resistance of silicon material of the base region between the base terminal B and an internal or intrinsic base terminal B'. Using the Miller Theorem, it can be shown that the 3-dB frequency at high frequencies is approximately given as

$$\omega_H^{-1} = \left(r_{pi} \parallel [r_x + (R_B \parallel R_S)]\right) \times C_T$$

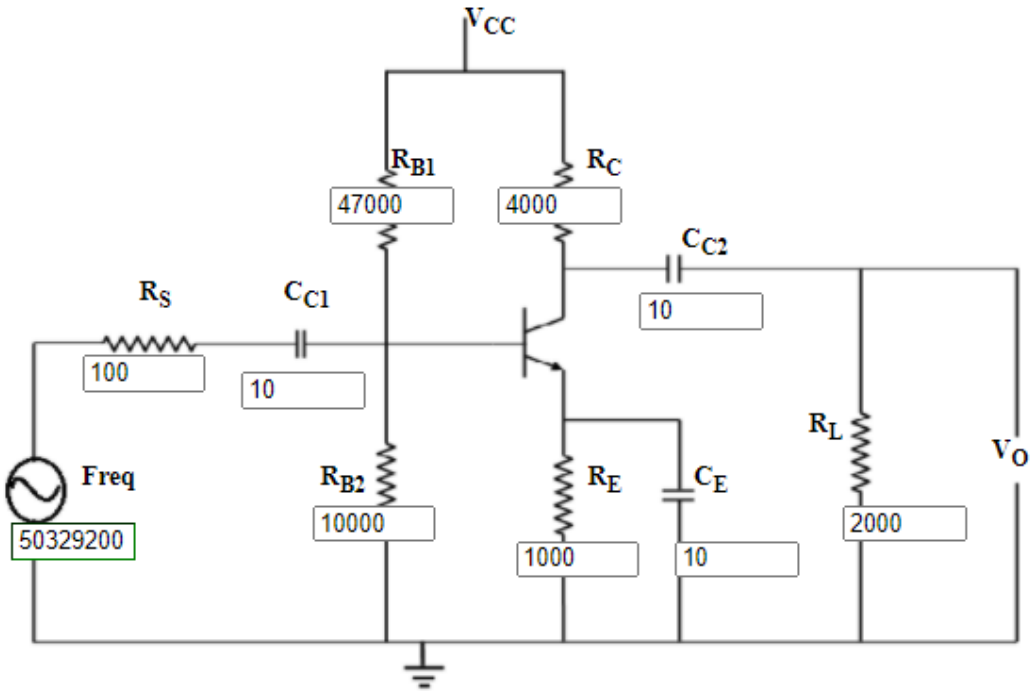
where,

$$C_T = C_\pi + C_\mu[1 + g_m(R_L \parallel R_C)]$$

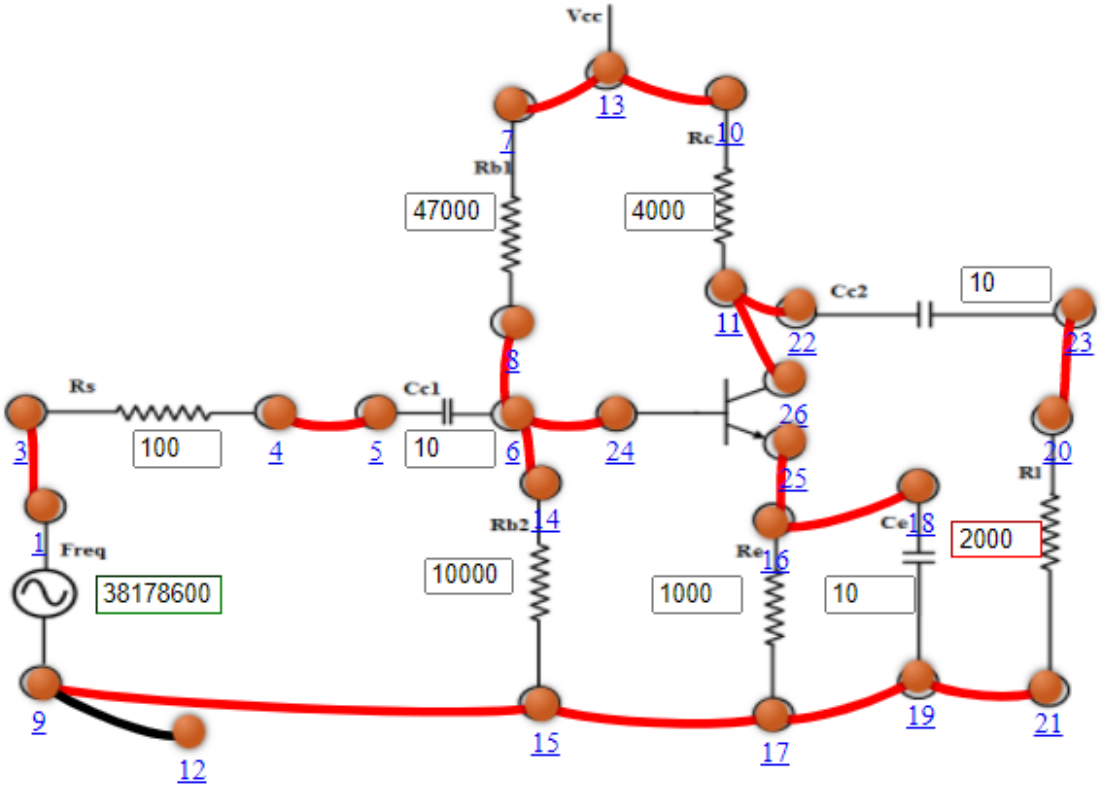
and

$$g_m = \frac{I_C}{V_T}$$

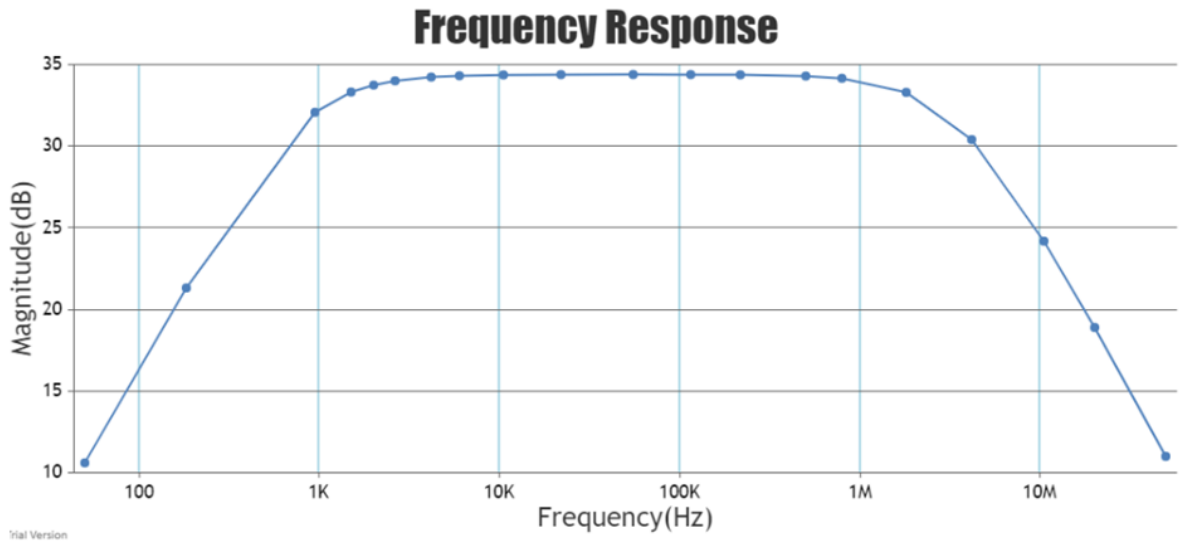
Circuit Diagram:



Wiring Diagram:



Graph:



Observations:

Midband gain = -52.4119

Low frequency cut-off = 5058.95432374 Hz

High frequency cut-off = 2.11455e+7 Hz

Serial No.	Frequency (Hz)	Magnitude (dB)
1	50	10.599
2	183	21.3138
3	959	32.0726
4	1520	33.3148
5	2004	33.7386
6	2641	34.0028
7	4186	34.2308
8	6051	34.3124
9	10515	34.3632
10	21970	34.382600000000004
11	55185	34.3864
12	115298	34.3834
13	219695	34.370599999999996
14	503292	34.295
15	797664	34.1576
16	1827340	33.294000000000004
17	4186200	30.401799999999998
18	10515300	24.18
19	20036400	18.89108
20	50329200	10.99534

Results and Conclusion: The gain and the frequency response of a single stage transistor amplifier (BJT CE Amplifier) has been studied and plotted successfully.

Experiment 8

Aim: To study the op amp as an inverting and non- inverting amplifier.

Tools Used: Virtual Labs.

Theory: Operational Amplifier commonly known as Op-Amp, is a linear electronic device having three terminals, two high impedance input and one output terminal. Op-Amp can perform multiple function when attached to different feedback combinations like resistive, capacitive or both. Generally, it is used as voltage amplifier and the output voltage of the Op-Amp is the difference between the voltages at its two input terminals.

Op-Amp shows some properties that make it an ideal amplifier, its open loop gain and input impedance is infinite (i.e., practically very high), Output impedance and offset voltage is zero (i.e., practically very low) and bandwidth is infinite (i.e., practically limited to frequency where its gain become unity).

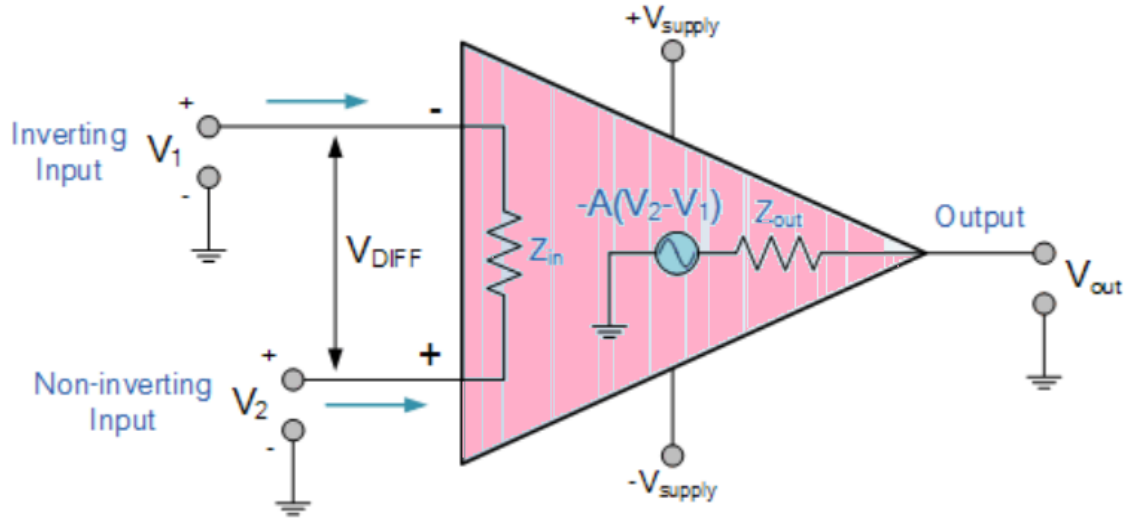


Fig. 1: Operational Amplifier

Inverting Op-Amp: The open loop gain (A_o) of the Om-Amp is very high which makes it very unstable, so to make it stable with a controllable gain, a feedback is applied through some external resistor (R_F) from its output to inverting input terminal(i.e., also known as negative feedback) resulting in reduced gain (closed loop gain, A_v). So, the voltage at inverting terminal is now the sum of the actual input and feedback voltages, and to separate both an input resistor (R_i) is introduced in the circuit. The non-inverting terminal of the Op-Amp is grounded, and the inverting terminal behaves like a virtual ground as the junction of the input and feedback signal are at the same potential.

Current can be given

$$I = \frac{V_{in} - V_{out}}{R_{in} + R_{out}}$$

or,

$$I = \frac{V_{in} - V_2}{R_{in}}$$

or,

$$I = \frac{V_2 - V_{out}}{R_F}$$

$$I = \frac{V_{in}}{R_{in}} - \frac{V_2}{R_{in}} = \frac{V_2}{R_F} - \frac{V_{out}}{R_F}$$

So,

$$\frac{V_{in}}{R_{in}} = V_2 \times \left(\frac{1}{R_{in}} + \frac{1}{R}\right) - \frac{V_{out}}{R_F}$$

and as, V_2=0

$$I = \frac{V_{in} - 0}{R_{in}} = \frac{0 - V_{out}}{R_F}$$

or,

$$\frac{R_F}{R_{in}} = -\frac{V_{out}}{V_{in}}$$

The close loop gain (A_{cl}) is given by :-

$$A_{cl} = \frac{V_{out}}{V_{in}} = -\frac{R_F}{R_{in}}$$

Output voltage (V_{out}) is given by :-

$$V_{out} = -\frac{R_F}{R_{in}} \times V_{in}$$

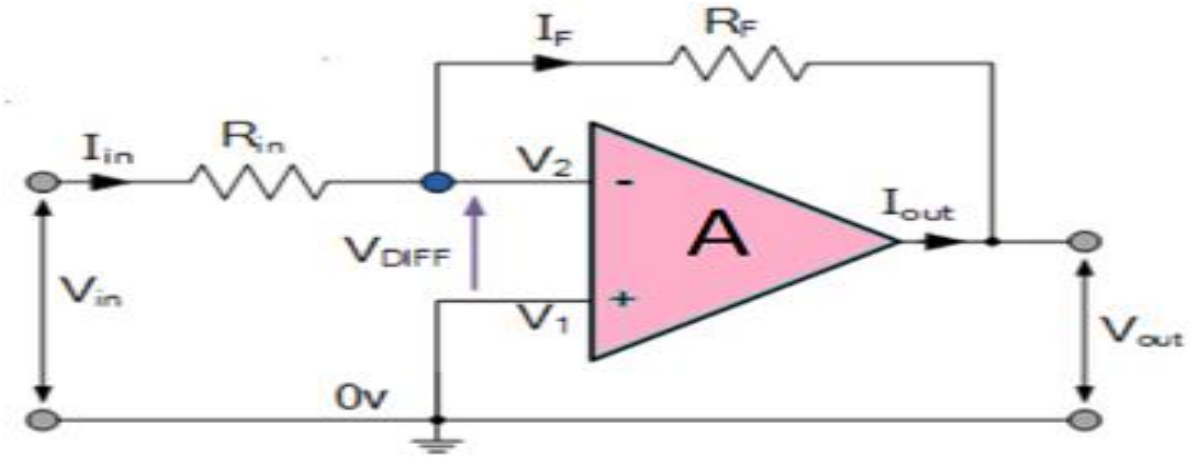


Fig. 2: Inverting Operational Amplifier

Non-Inverting Op-Amp: In this configuration of Op-Amp the input signal is directly fed to the non-inverting terminal resulting in a positive gain and output voltage in phase with input as compared to inverting Op-Amp where the gain is negative and output voltage is out of phase with input , and to stabilize the circuit a negative feedback is applied through a resistor(R_F) and the inverting terminal is grounded with an input resistor(R_2).This inverting Op-Amp like layout the at inverting terminal creates a virtual ground at the summing point make the R_F and R_2 a potential divider across inverting terminal, Hence determines the gain of the circuit.

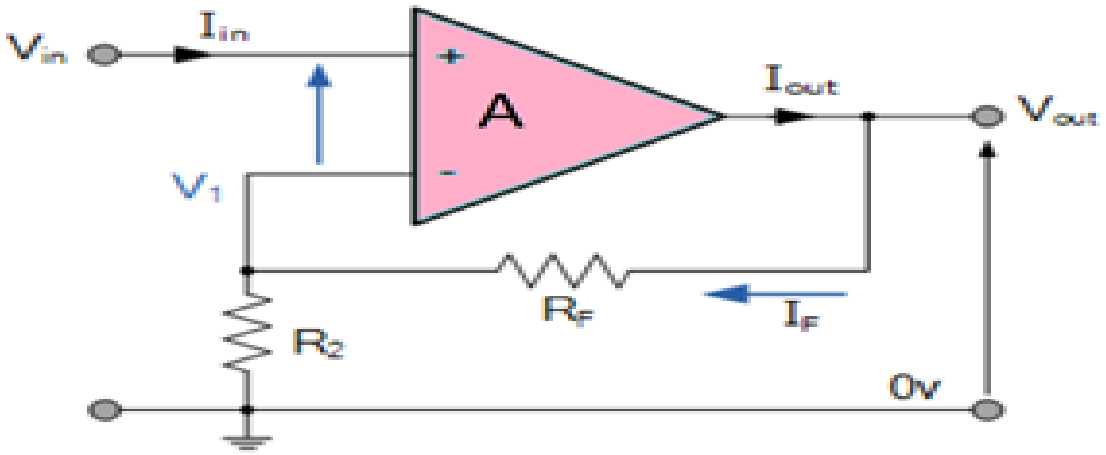


Fig. 3: Non-Inverting Operational Amplifier

Potential difference V_1 can be written as

$$V_1 = \frac{R_2}{(R_2 + R_F)} \times V_{out}$$

in ideal condition: $V_1=V_{in}$

So,

$$V_{in} = \frac{R_2}{(R_2 + R_F)} \times V_{out}$$

and as we know Gain $A_{cl} = \frac{V_{out}}{V_{in}}$

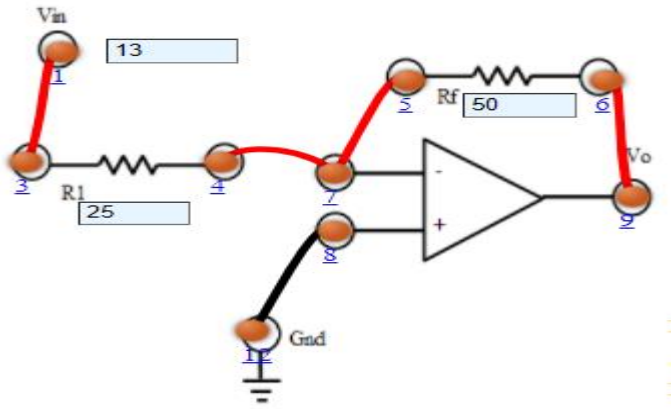
$$A_{cl} = \frac{(R_2 + R_F)}{R_2} = 1 + \frac{R_2}{R_F}$$

and Output Voltage (V_{out}) is given by:

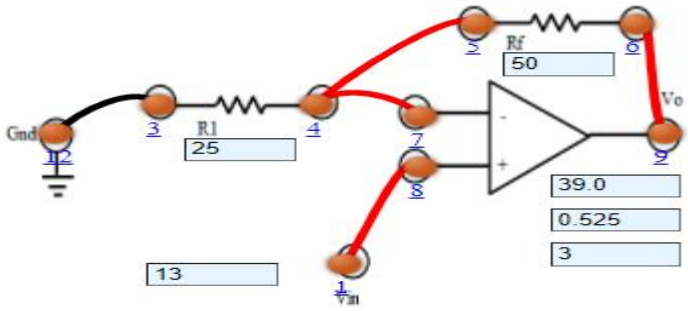
$$V_{out} = \left(1 + \frac{R_F}{R_2}\right) \times V_{in}$$

Wiring Diagram:

(A) Inverting Op-Amp:

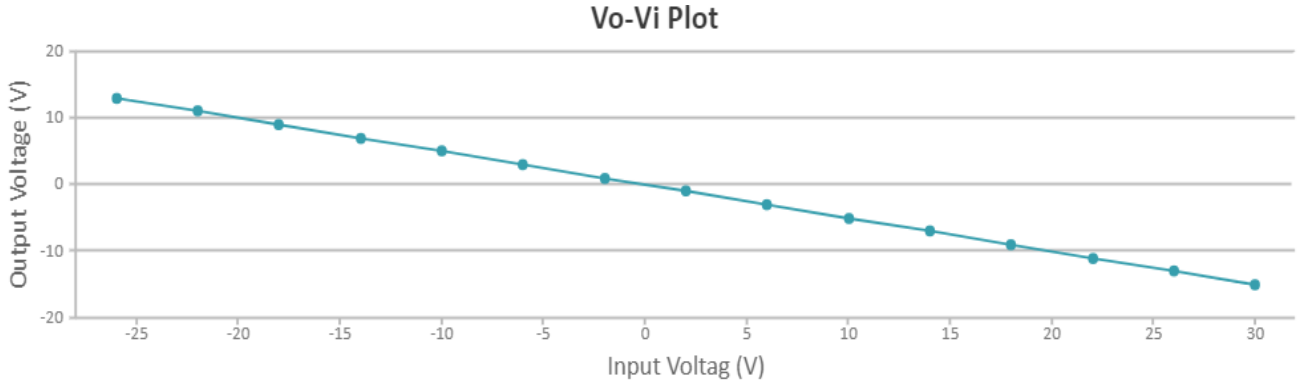


(B) Non-Inverting Op-Amp:

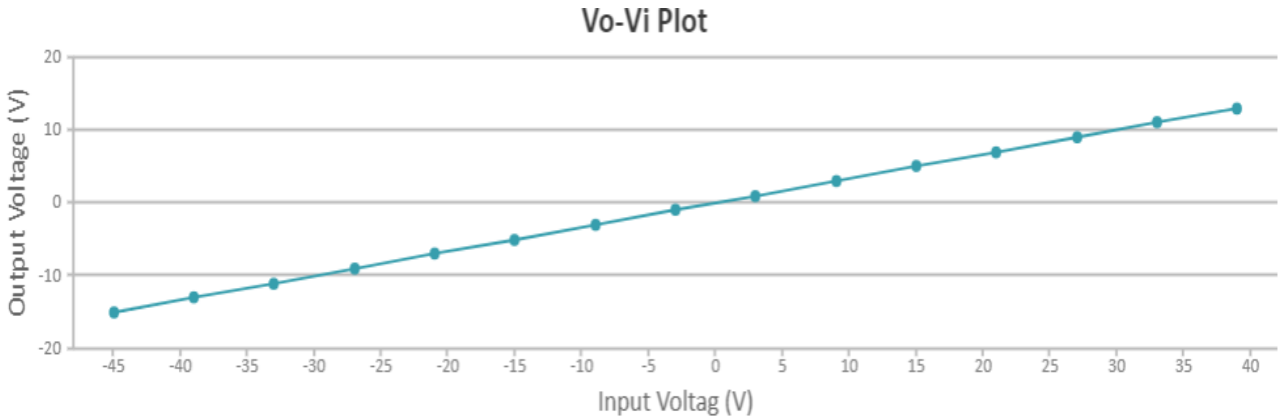


Graph:

(A) Inverting Op-Amp:



(B) Non-Inverting Op-Amp:



Observations:

(A) Inverting Op-Amp:

Resistance = 25Ω

Serial No.	Input Voltage (V)	Output Voltage (V)	Current (mA)
1	-15	30.0	-0.0176
2	-13	26.0	-0.0153
3	-11	22.0	-0.0129
4	-9	18.0	-0.0106
5	-7	14.0	-0.00824
6	-5	10.0	-0.00588
7	-3	6.0	-0.00353
8	-1	2.0	-0.00118
9	1	-2.0	0.00118
10	3	-6.0	0.00353
11	5	-10.0	0.00588
12	7	-14.0	0.00824
13	9	-18.0	0.0106
14	11	-22.0	0.0129
15	13	-26.0	0.0176

(B) Non-Inverting Op-Amp:

Resistance = 25Ω

Serial No	Input Voltage (V)	Output Voltage (V)	Current (mA)
1	-15	-45.0	NaN
2	-13	-39.0	NaN
3	-11	-3300	NaN
4	-9	-27.0	NaN
5	-7	-21.0	NaN
6	-5	-15.0	NaN
7	-3	-9.0	NaN
8	-1	-3.0	NaN
9	1	3.0	0.00510
10	3	9.0	0.0153

11	5	15.0	0.202
12	7	21.0	0.283
13	9	27.0	0.364
14	11	33.0	0.444
15	13	39.0	0.525

Results and Conclusion: The designing and testing of inverting and non-inverting operational amplifier and its graph between voltage and the current has been plotted successfully.

Experiment 9

Aim: To verify the truth tables of NOT, OR, AND, NOR, NAND, XOR, XNOR gates.

Tools Used: Virtual Labs.

Theory: Logic gates are the basic building blocks of any digital system. Logic gates are electronic circuits having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as

- AND gate
- OR gate
- NOT gate
- NAND gate
- NOR gate
- Ex-OR gate
- Ex-NOR gate

AND gate: The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high and low output (0) when all or any one input is low. A dot (.) is used to show the AND operation i.e. A.B or can be written as AB.

Y=A.B

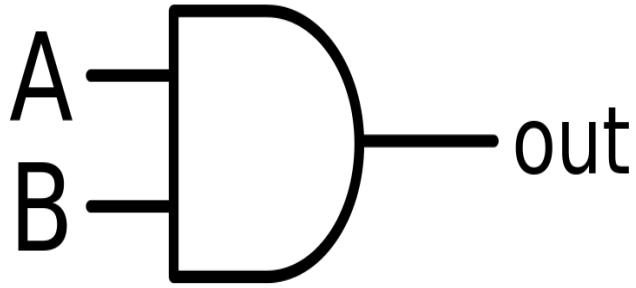


Fig 1: Symbol of AND Gate

A	B	Y(Output)
0	0	0
0	1	0
1	0	0
1	1	1

Table 1: Truth Table of AND Gate

A simple 2-input logic AND gate can be constructed using RTL (Resistor-Transistor-Logic) switches connected together as shown below with the inputs connected directly to the transistor bases. Both transistors must be saturated “ON” for an output at Q.

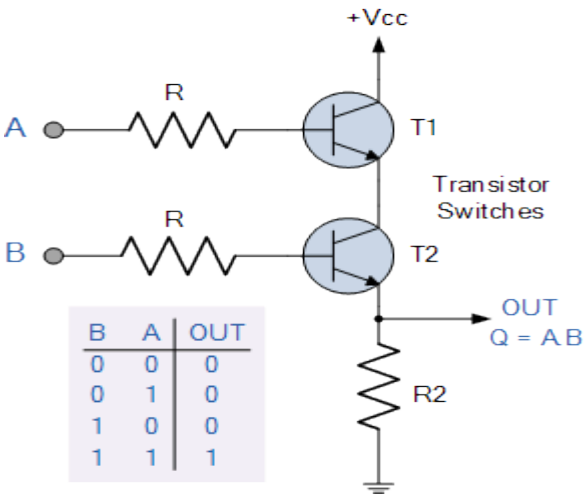


Fig 2: AND Gate Through RTL Logic

OR gate: The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high and gives lower output (0) when if all the inputs are low. A plus (+) is used to show the OR operation.

Y= A+B

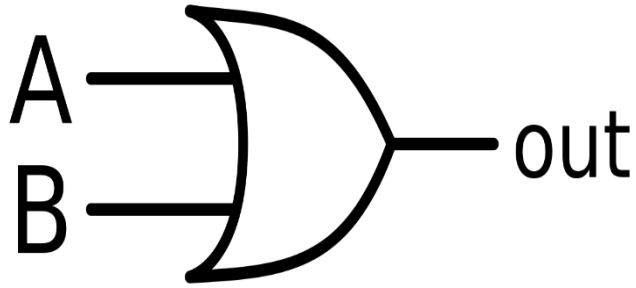


Fig 3: Symbol of OR Gate

A	B	Y(Output)
0	0	0
0	1	1
1	0	1
1	1	1

Table 2: Truth Table of OR Gate

OR gate can be realized by DRL (Diode-Resistance-Logic) or by TTL (Transistor-Transistor-Logic). Presently, we will learn how to implement the OR gate using DRL (Diode-Resistance-Logic). To realise OR gate, we will use a diode at every input of the OR gate. The anode part of diode is connected with input while the cathode part is joined together and a resistor, connected with the cathode is grounded. In this case, we have taken two inputs which can be seen in the circuit below.

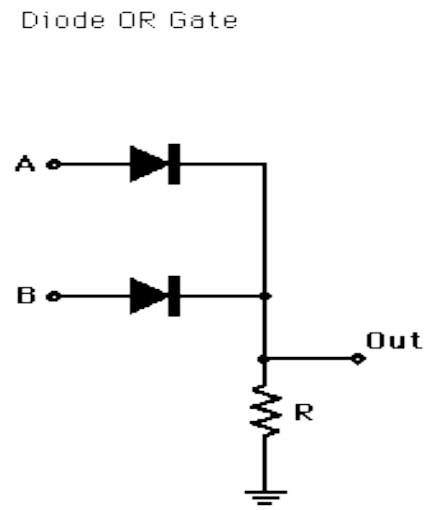


Fig 4: OR Gate Through DRL Logic

When both the inputs are at logic 0 or low state then the diodes D1 and D2 become reverse biased. Since the anode terminal of diode is at lower voltage level than the cathode terminal, so diode will act as open circuit so there is no voltage across resistor and hence output voltage is same as ground. When either of the diodes is at logic 1 or high state then the diode corresponding to that input is forward bias. Since this time anode is at high voltage than cathode therefore current will flow through forward biased diode and this current then appears on resistor causing high voltage at output terminal also. Hence at output we get high or logic 1 or +5V. So, if any or both inputs are high, the output will be high or "1".

NOT gate: The NOT gate is an electronic circuit that produces an inverted version of the input at its output i.e. it gives low output (0) when high input (1) is passed and it gives high output (1) when low input (0) is passed. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A' or A with a bar over the top, as shown at the outputs.

Y= A'

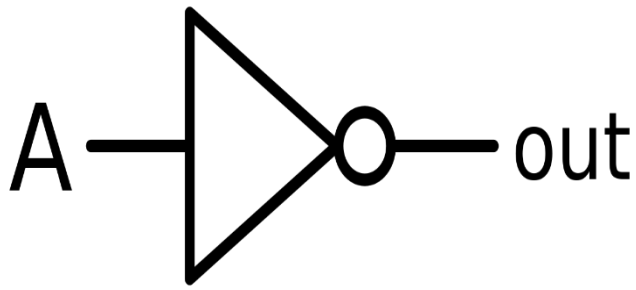


Fig 5: Symbol of NOT Gate

A	Y(Output)
0	1
1	0

Table3: Truth Table of NOT Gate

NOT gate can be realized through transistor.The input is connected through resistor R2 to the transistor's base. When no voltage is present on the input, the transistor turns off. When the transistor is off, no current flows through the collector-emitter path. Thus, current from the

supply voltage (Vcc) flows through resistor R1 to the output. In this way, the circuit's output is high when its input is low.
When voltage is present at the input, the transistor turns on, allowing current to flow through the collector-emitter circuit directly to ground. This ground path creates a shortcut that bypasses the output, which causes the output to go low. In this way, the output is high when the input is low and low when the input is high.

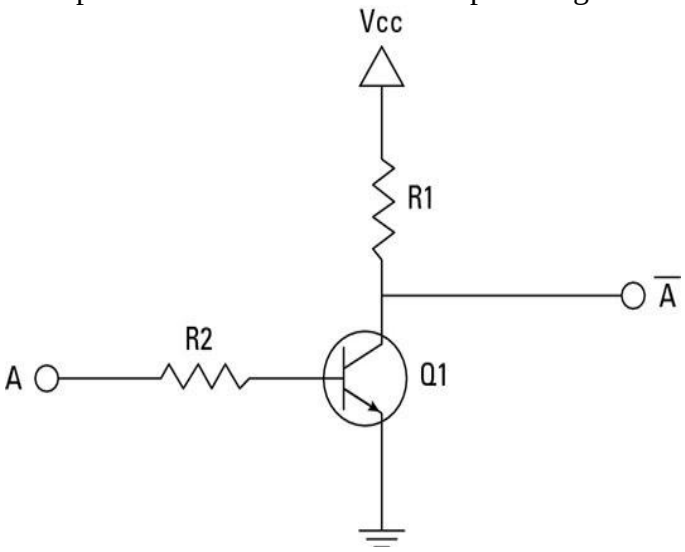


Fig 6: NOT Gate Through Transistor

NAND gate: This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

Y= (A.B)'

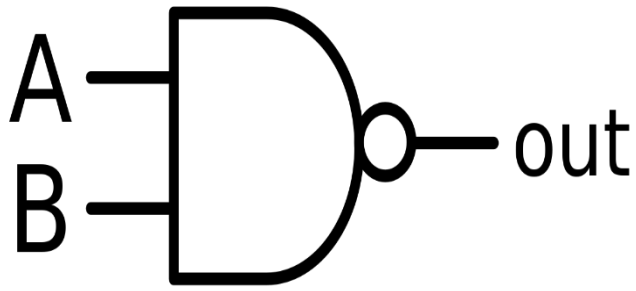


Fig 7: Symbol of NAND Gate

A	B	Y(Output)
0	0	1
0	1	1
1	0	1
1	1	0

Table 4: Truth Table of NAND Gate

A simple 2-input logic NAND gate can be constructed using RTL (Resistor-transistor-logic) switches connected together as shown below with the inputs connected directly to the transistor bases. Either transistor must be cut-off or “OFF” for an output at Q.

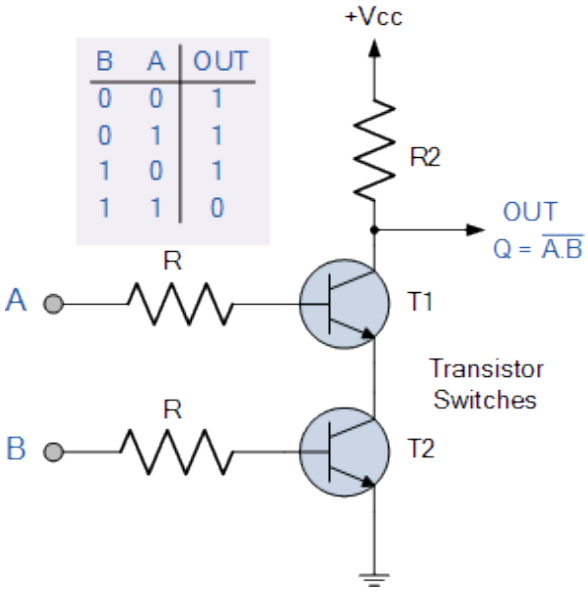


Fig 8: NAND Gate Trough RTL Logic

NOR gate: This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

Y= (A+B)’

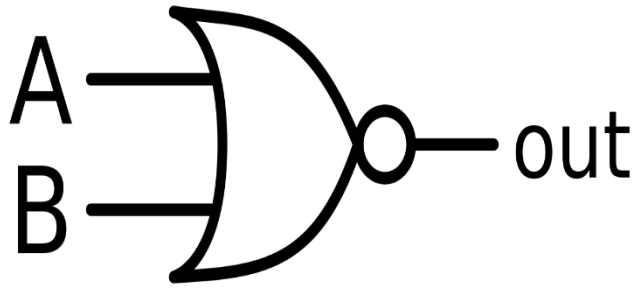


Fig 9: Symbol of NOR Gate

A	B	Y(Output)
0	0	1
0	1	1
1	0	1
1	1	1

Table 5: Truth Table of NOR Gate

A simple 2-input logic NOR gate can be constructed using RTL (Resistor-transistor-logic) switches connected together as shown below with the inputs connected directly to the transistor bases. Both transistors must be cut-off or “OFF” for an output at Q.

Note: NAND and NOR Gate are Universal Gates. Universal Gate is a gate which can implement any Boolean function without need to use any other gate type.

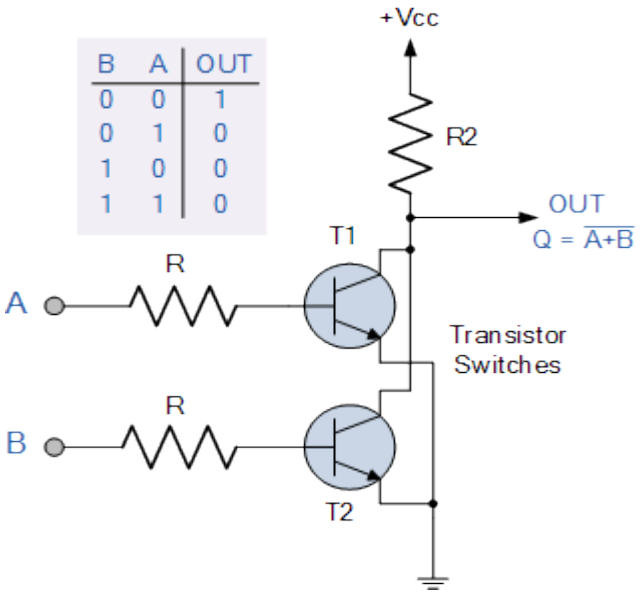


Fig 10: NOR Gate Through RTL Logic

Ex-OR gate: The 'Exclusive-OR' gate is a circuit which will give a high output if either, but not both of its two inputs are high. An encircled plus sign (⊕) is used to show the Ex-OR operation. Ex-OR gate is created from AND, NAND and OR gates. The output is high only when both the inputs are different.

Y= A⊕B

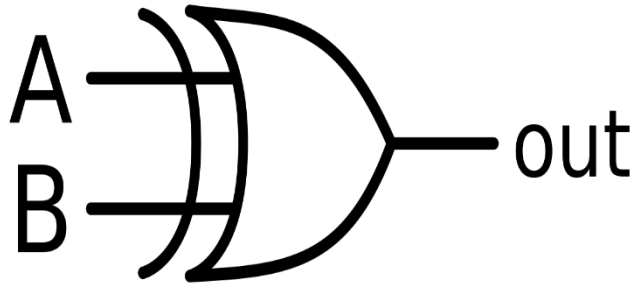


Fig 11: Symbol of Ex-OR Gate

A	B	Y(Output)
0	0	0
0	1	1
1	0	1
1	1	0

Table 6: Truth Table of XOR Gate

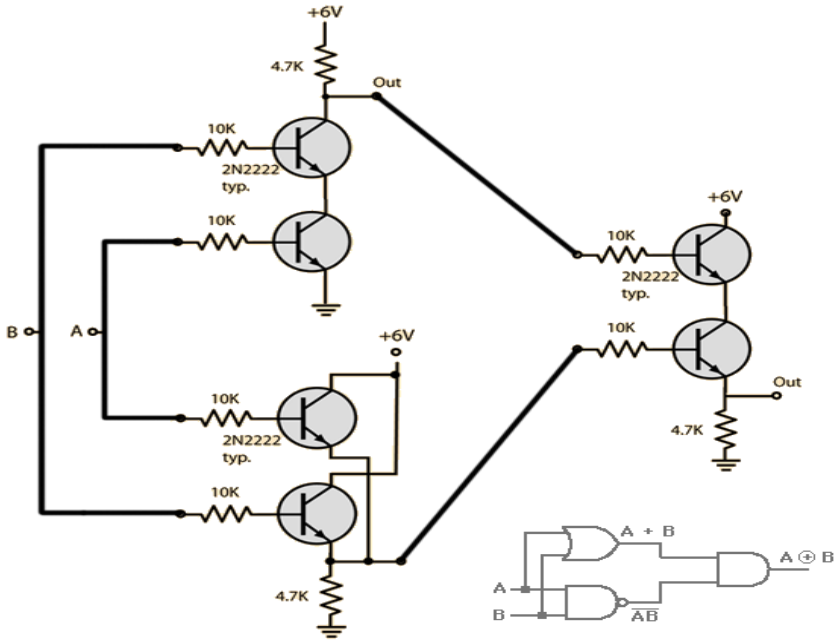


Fig 12: NOR Gate Using RTL

Ex-NOR gate: The 'Exclusive-NOR' gate circuit does the opposite to the EX-OR gate. It will give a low output if either, but not both of its two inputs are high. The symbol is an EX-OR gate with a small circle on the output. The small circle represents inversion. Ex-NOR gate is created from AND, NOT and OR gates. The output is high only when both the inputs are same.

Y= (A⊕B)'

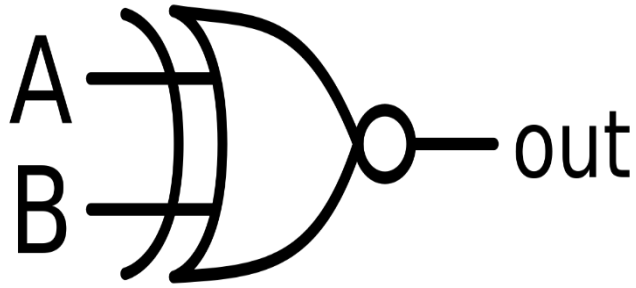


Fig 13: Symbol of Ex-NOR Gate

A	B	Y(Output)
0	0	1
0	1	0
1	0	0
1	1	1

Table 7: Truth Table of XNOR Gates

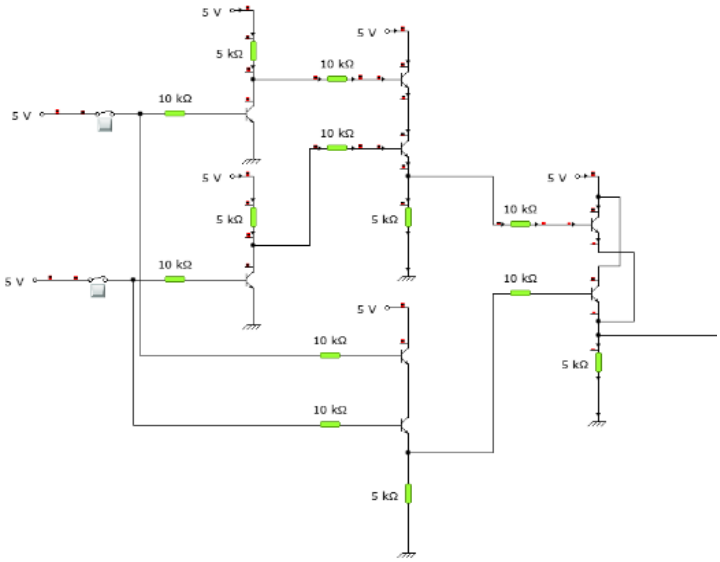
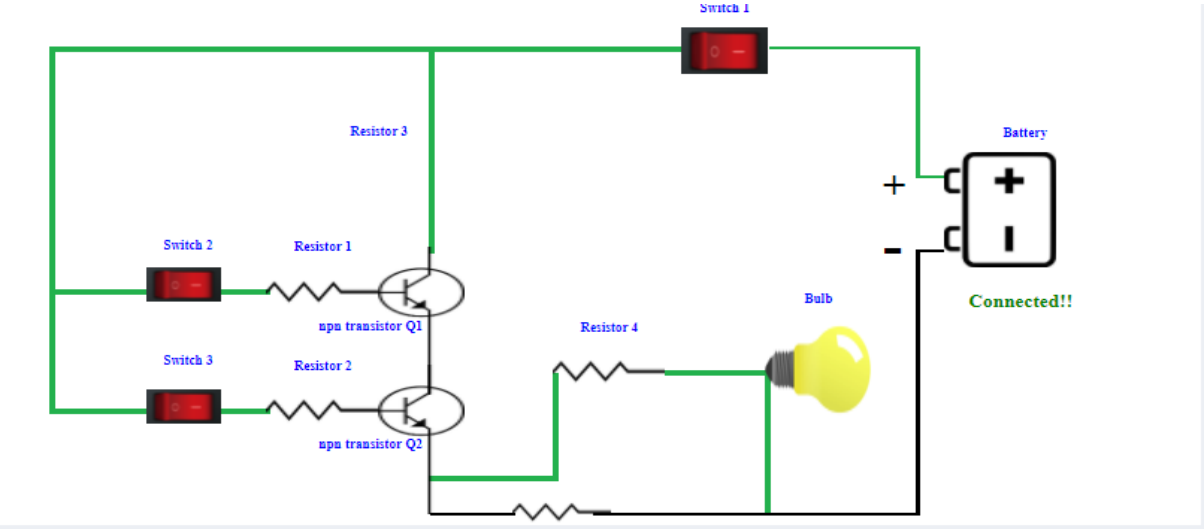


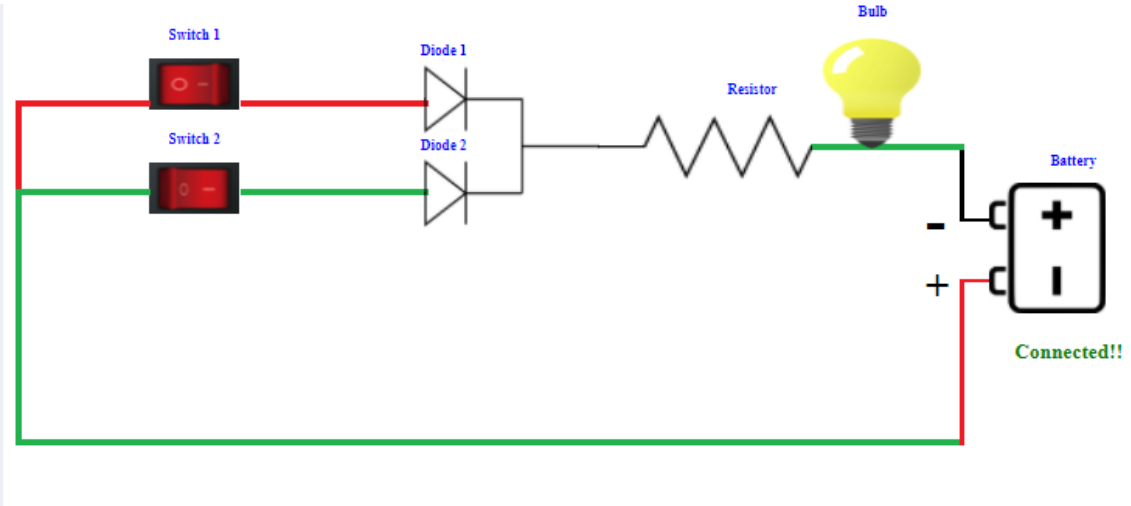
Fig 14: Ex-NOR Gate Through RTL Logic

Circuit Diagram:

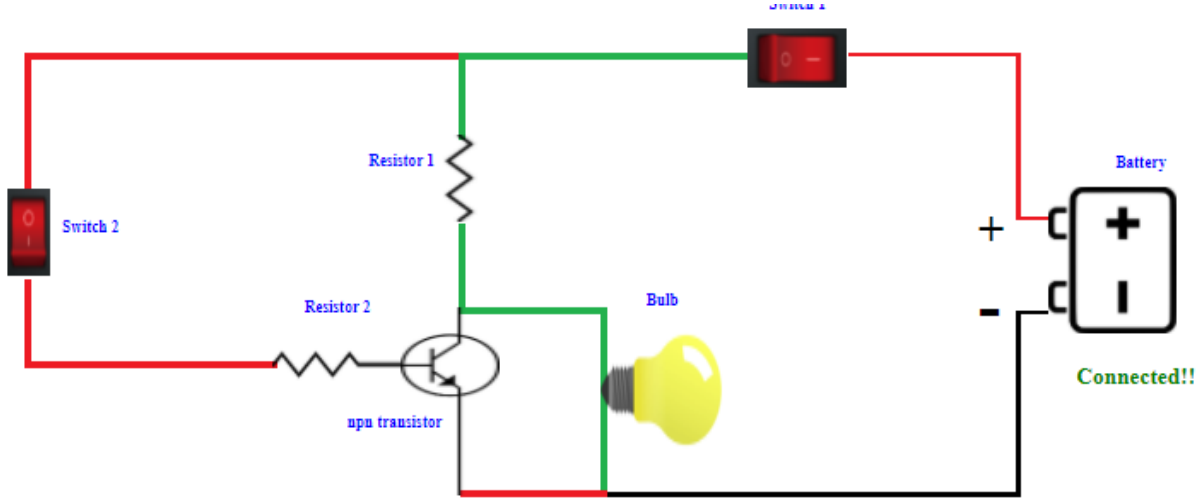
(A) AND Gate:



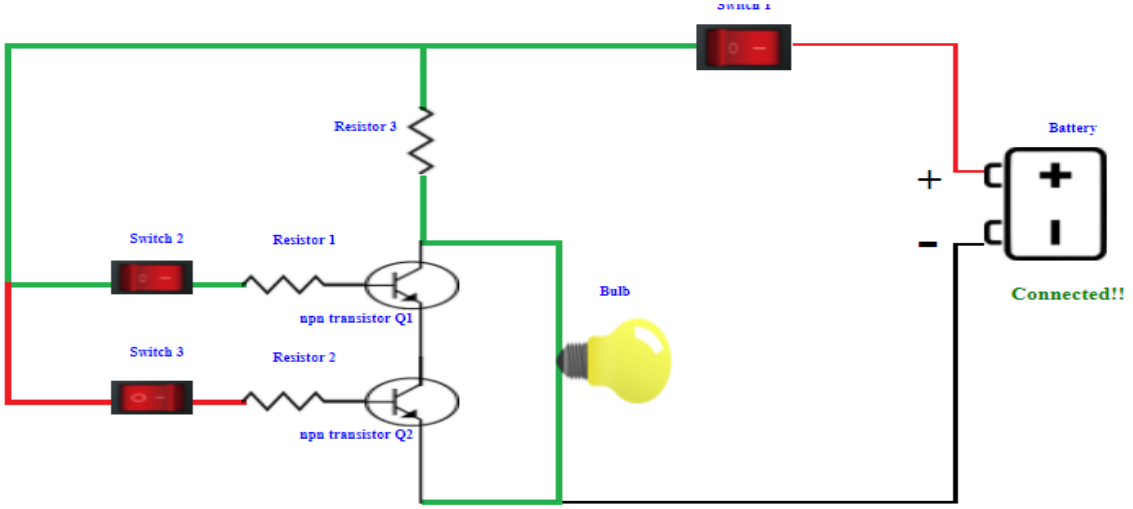
(B) OR Gate:



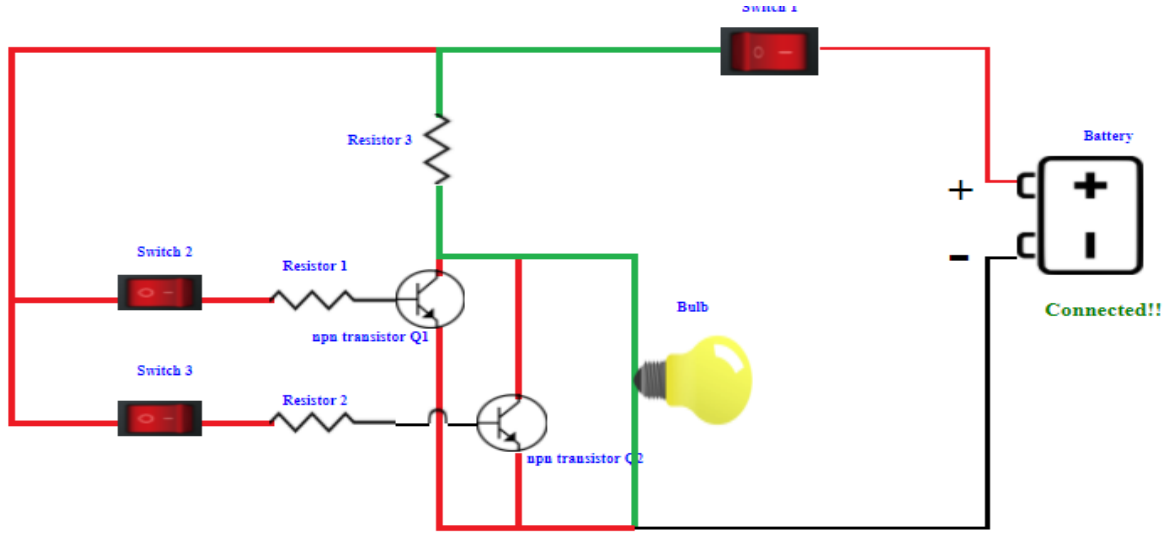
(C) NOT Gate:



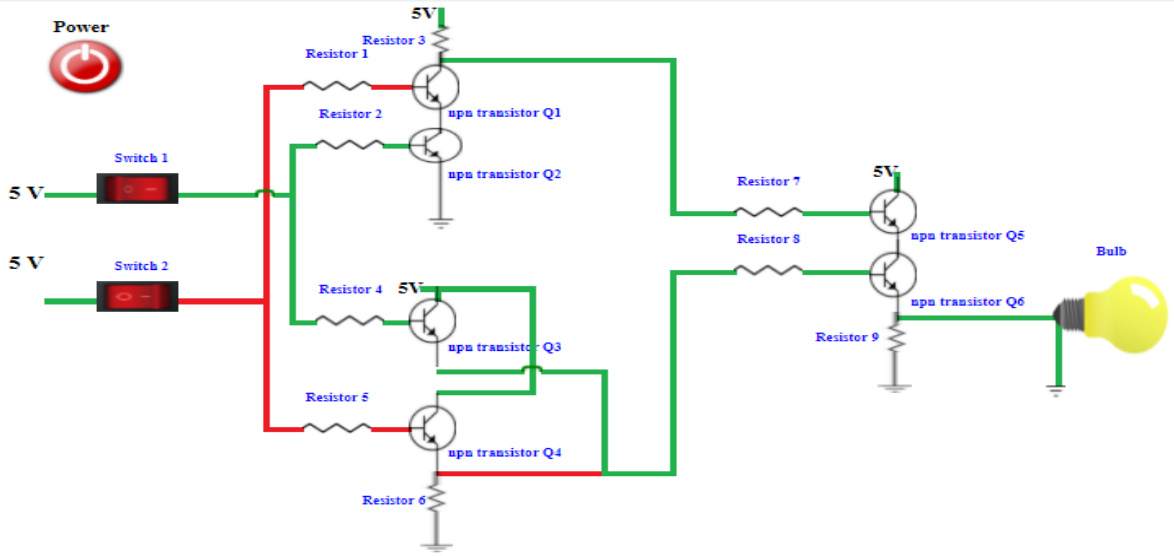
(D) NAND Gate:



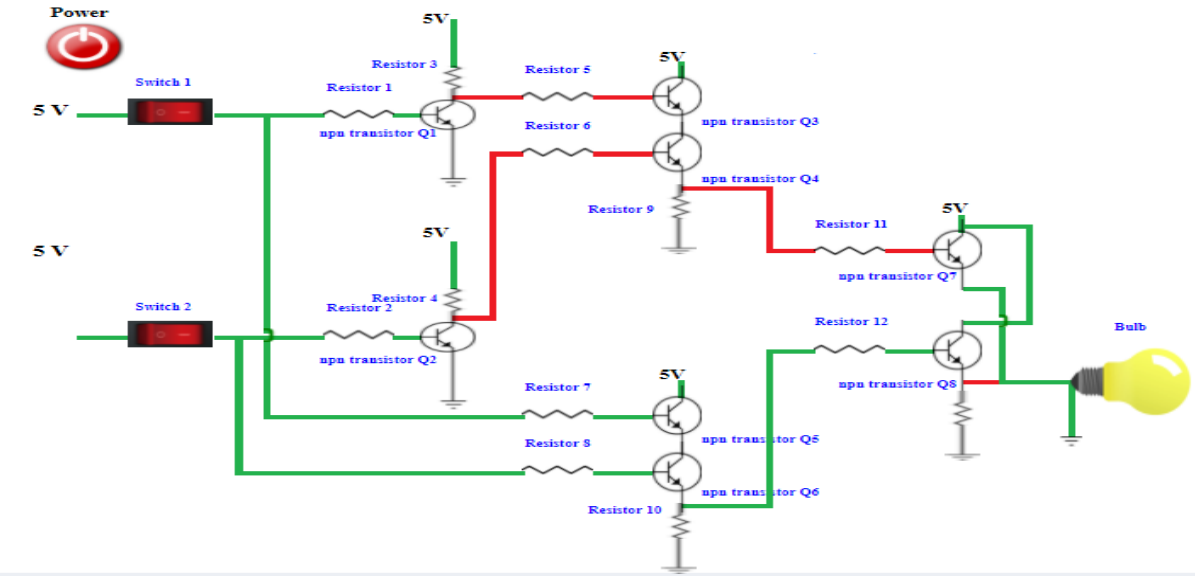
(E) NOR Gate:



(F) Ex-OR Gate:



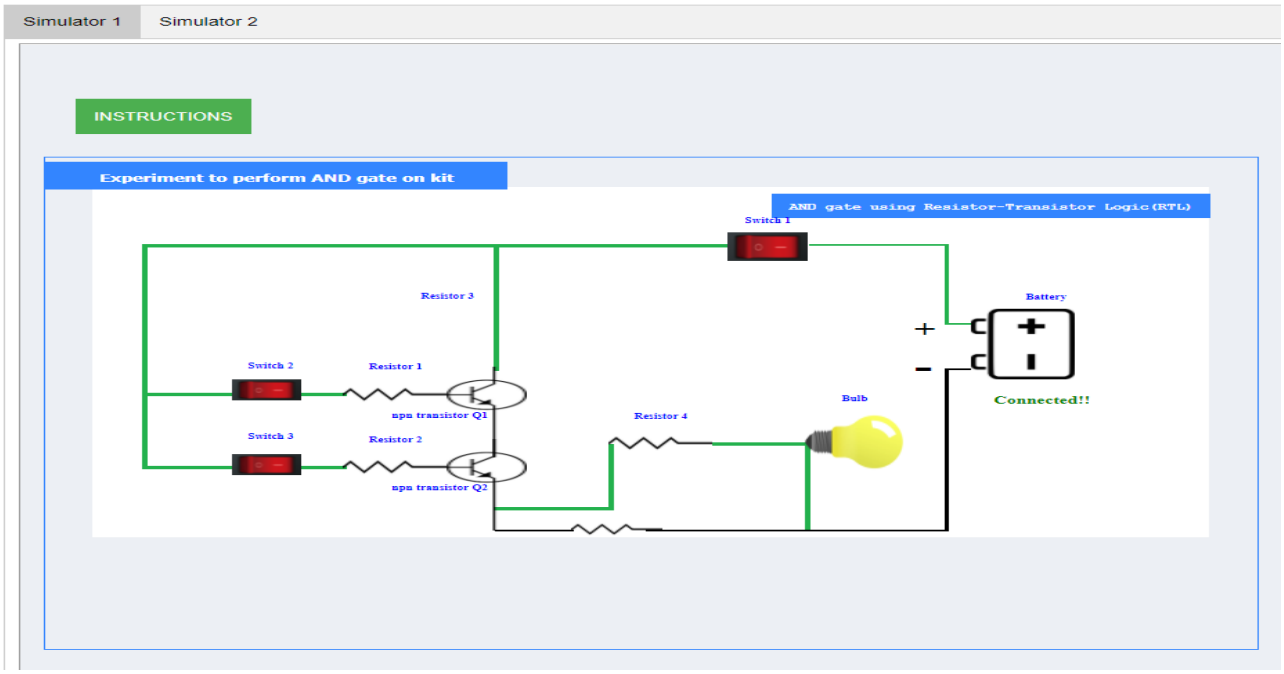
(G) Ex-NOR Gate:



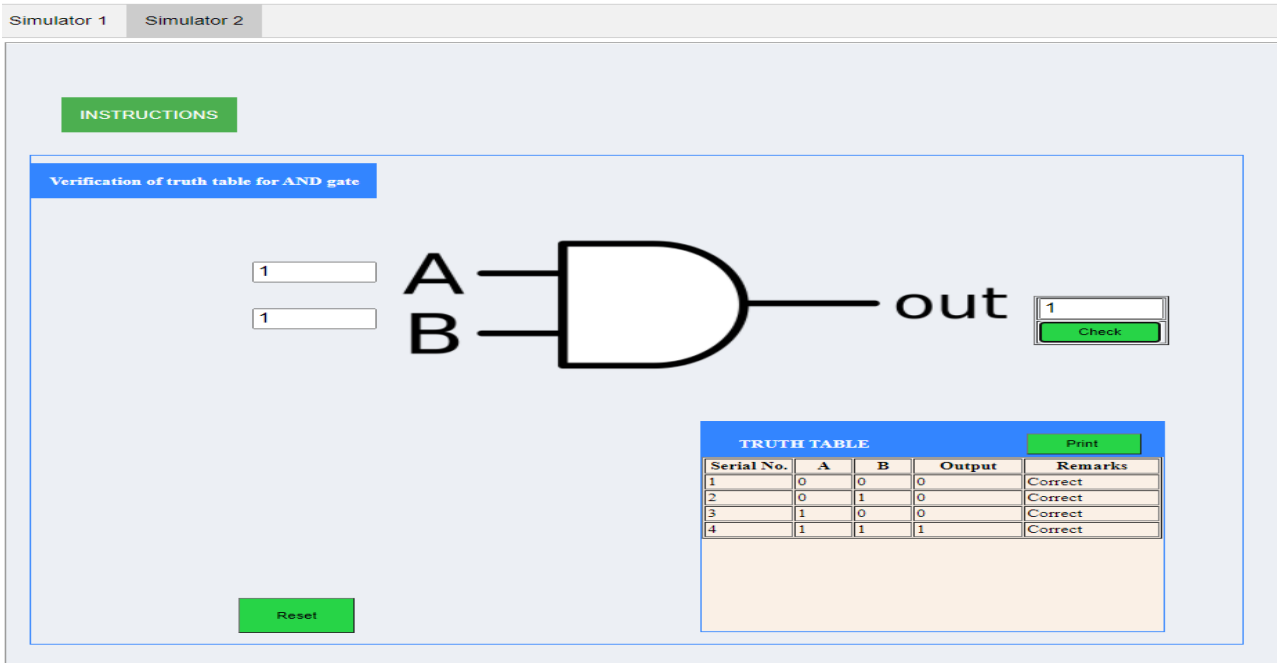
Observations:

(A) AND Gate:

(1) Simulator 1:

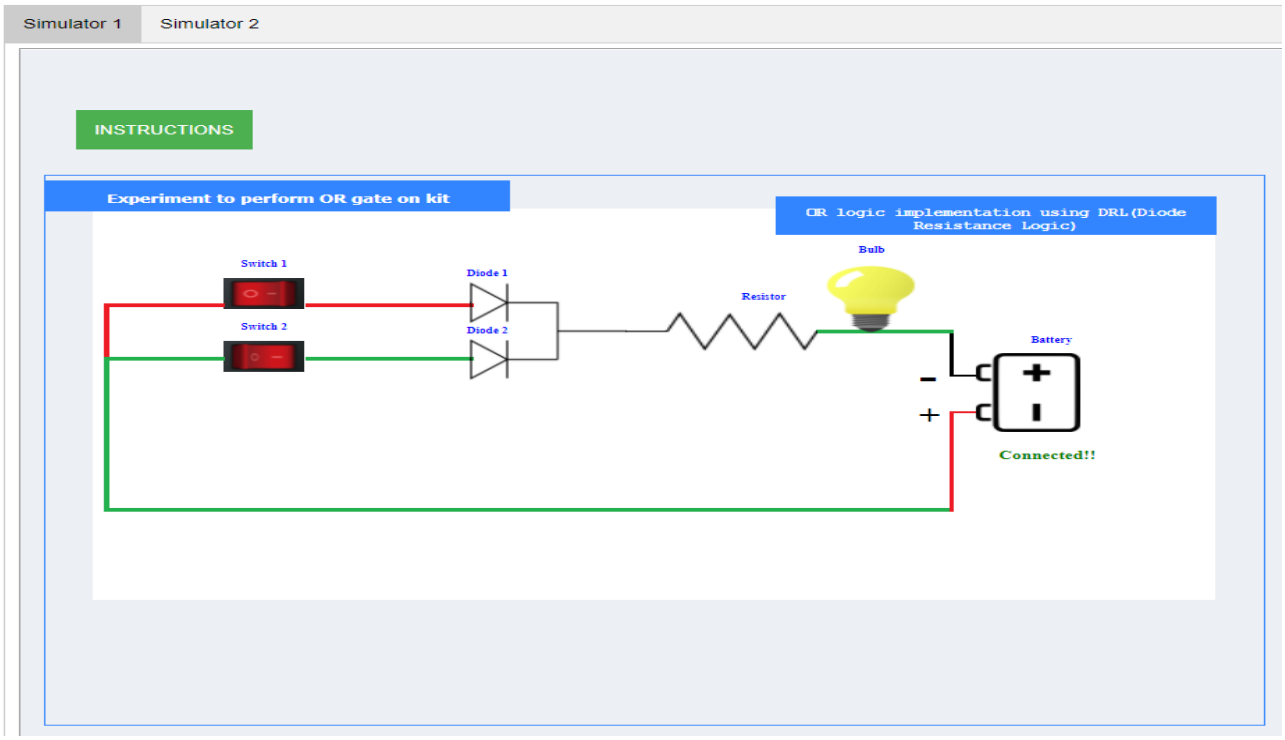


(2) Simulator 2:

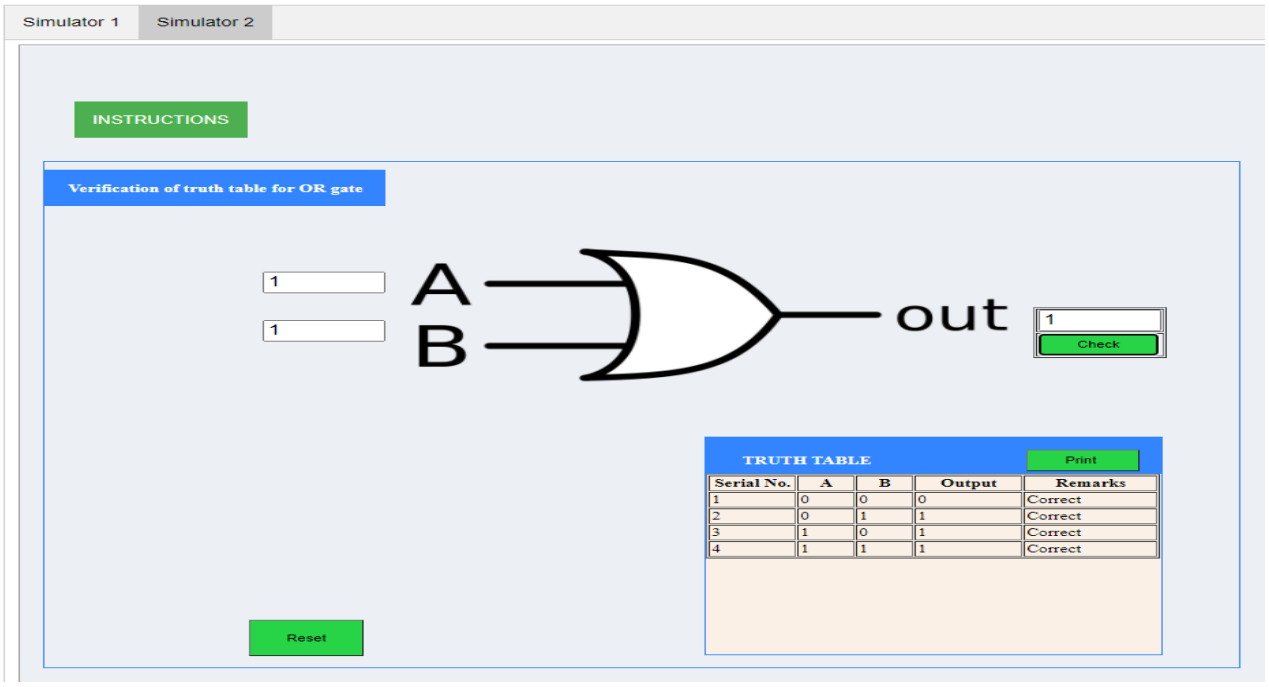


(B) OR Gate:

(1) Simulator 1:

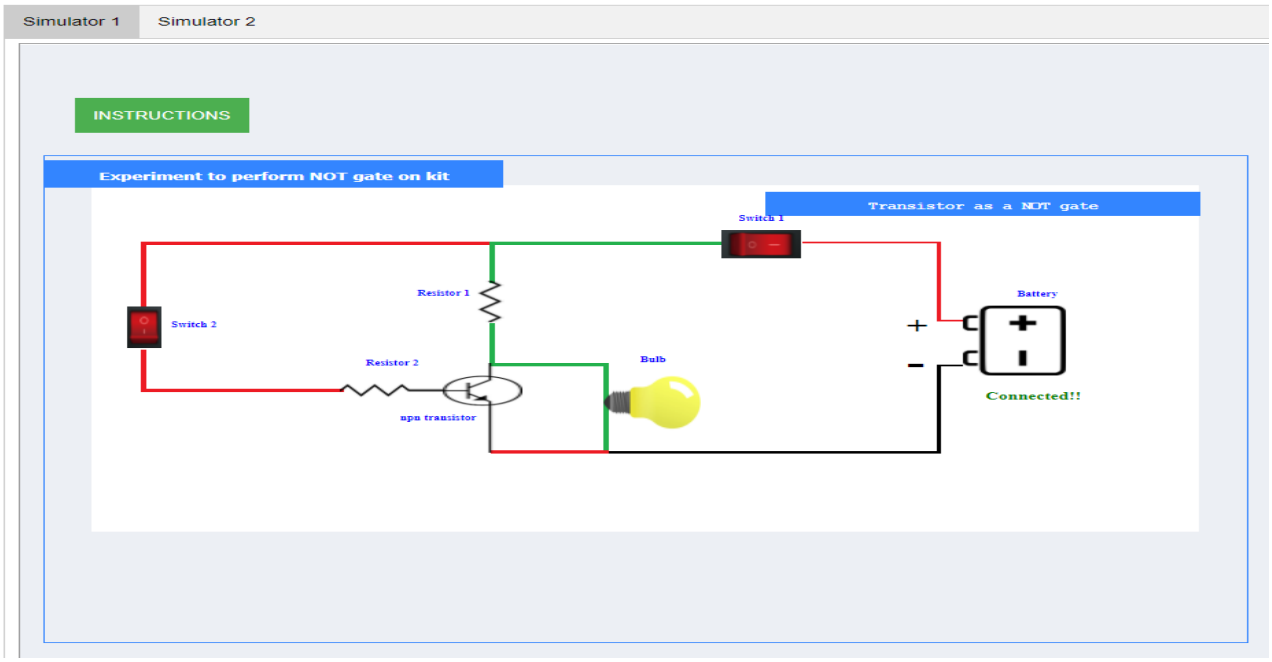


(2) Simulator 2:

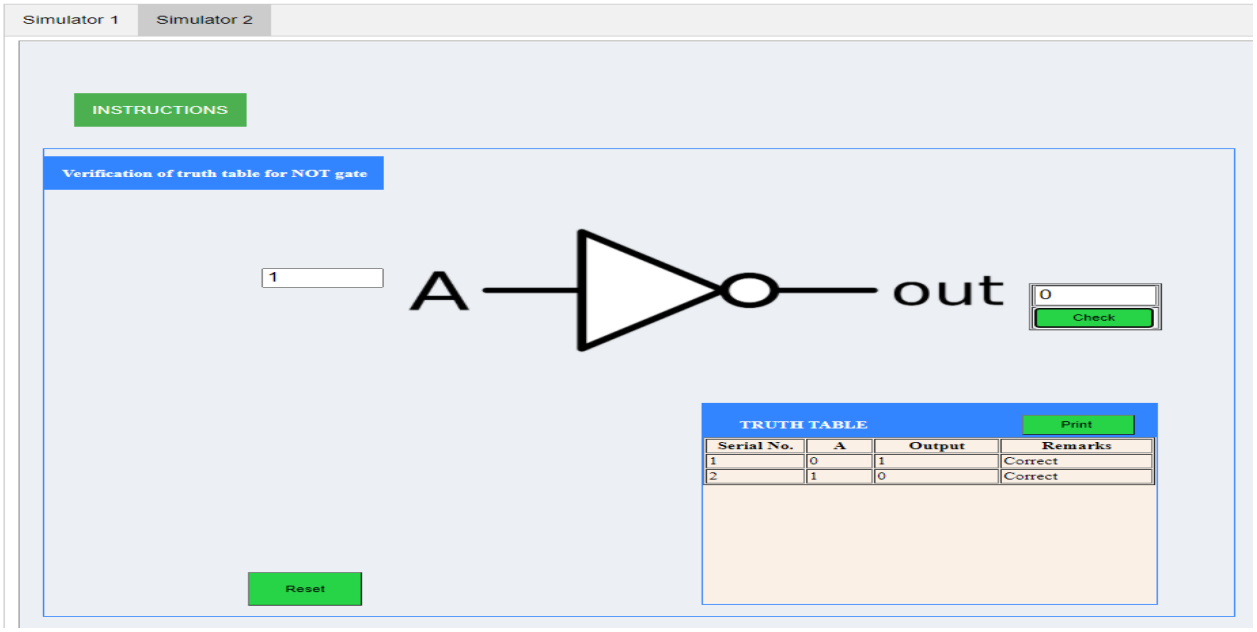


(C) NOT Gate:

(1) Simulator 1:

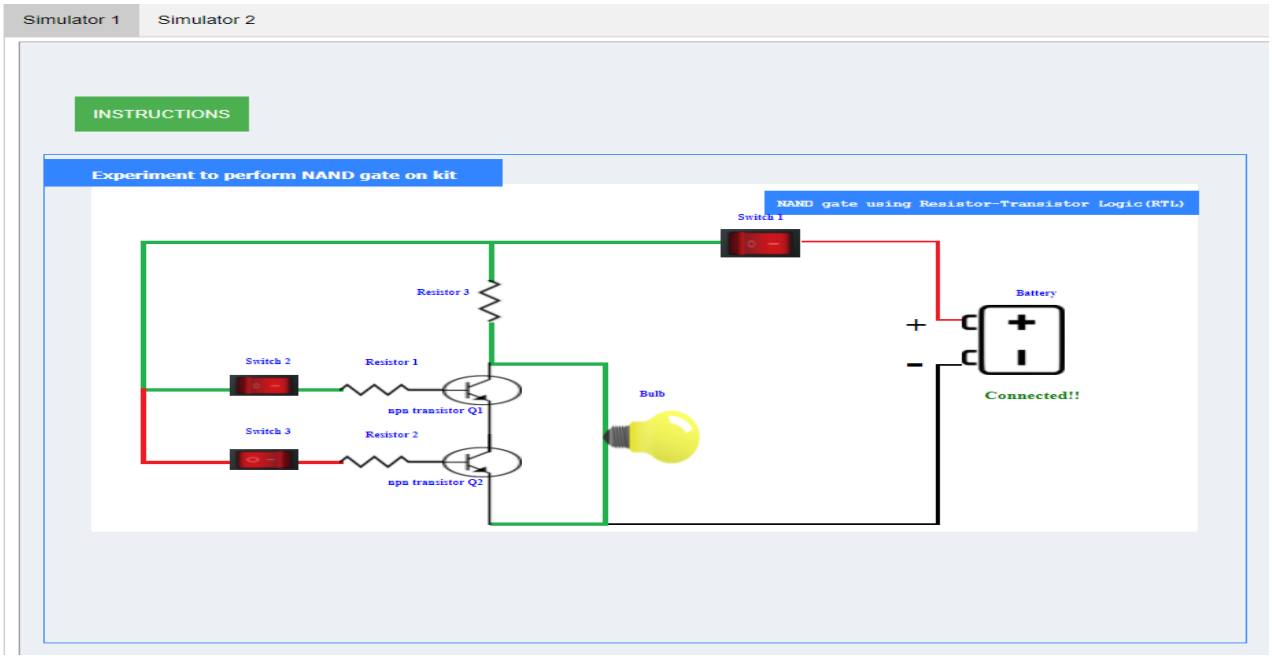


(2) Simulator 2:

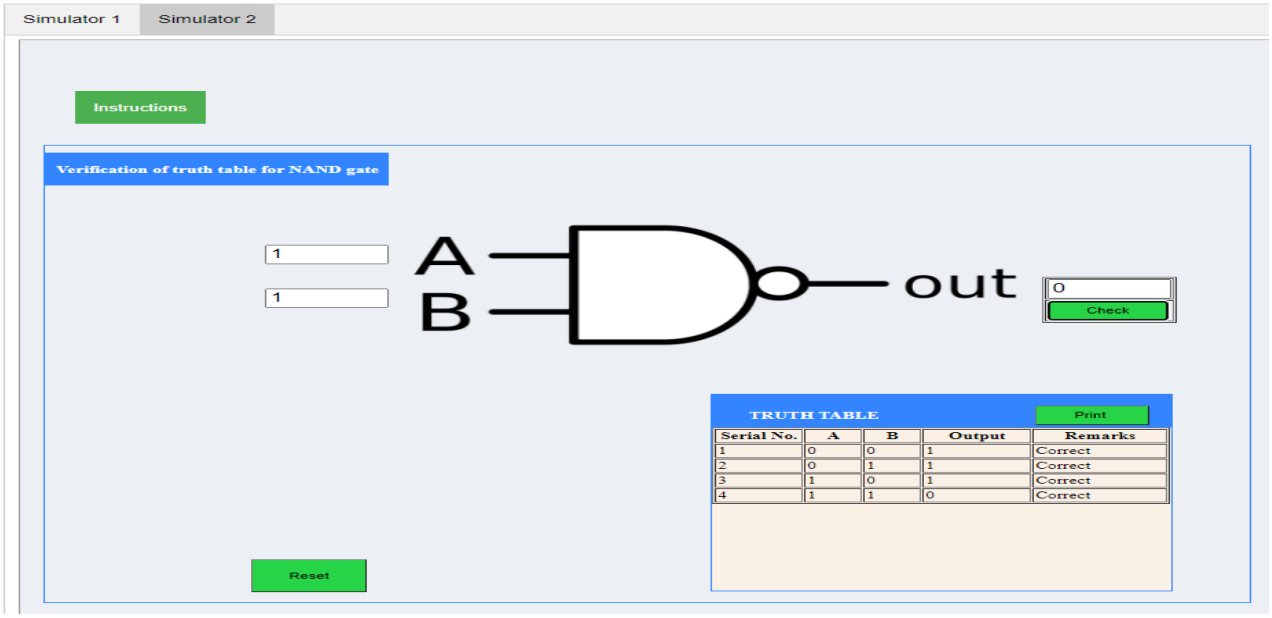


(D) NAND Gate:

(1) Simulator 1:

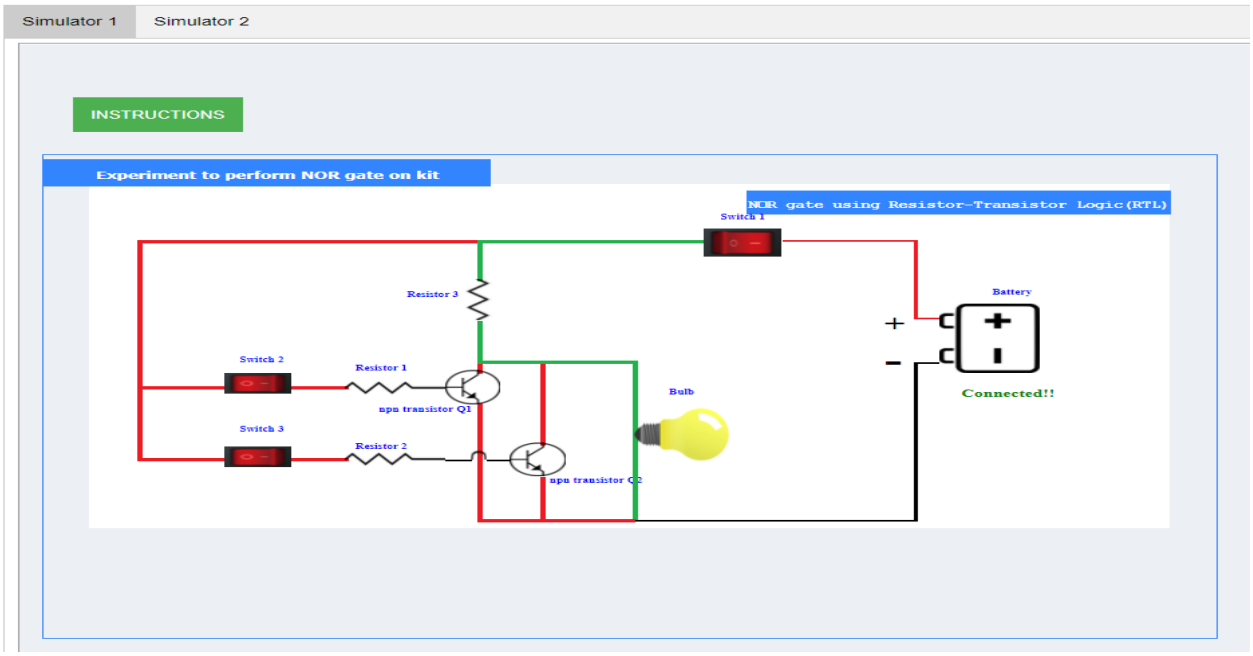


(2) Simulator 2:

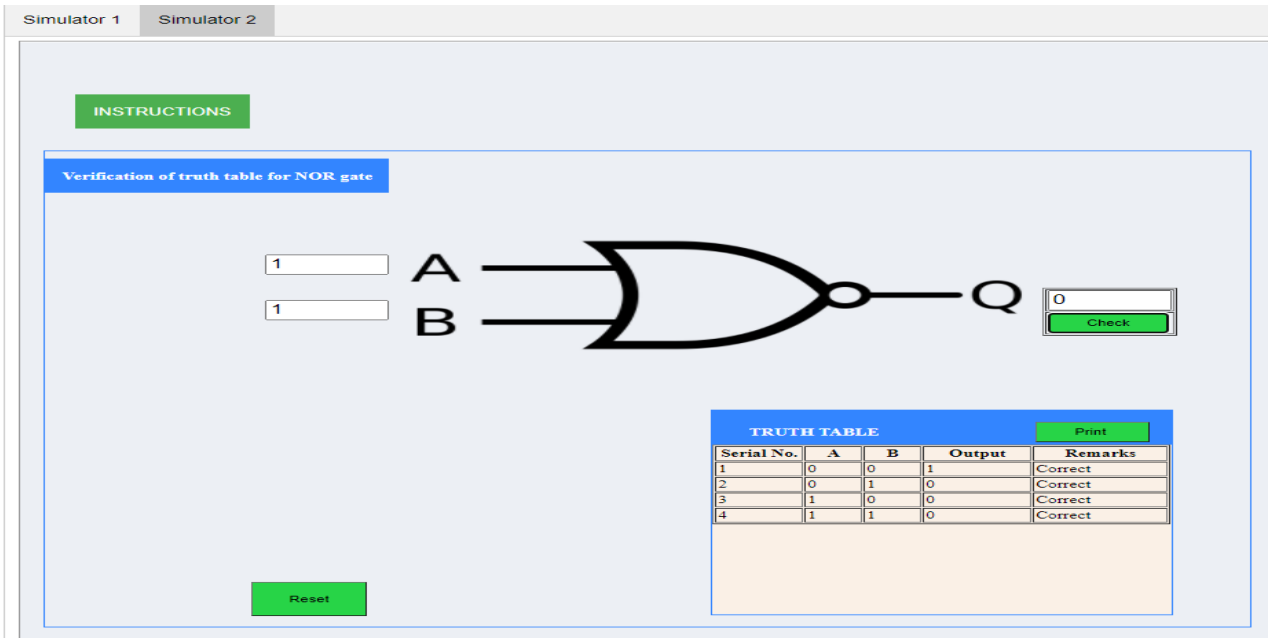


(E) NOR Gate:

(1) Simulator 1:

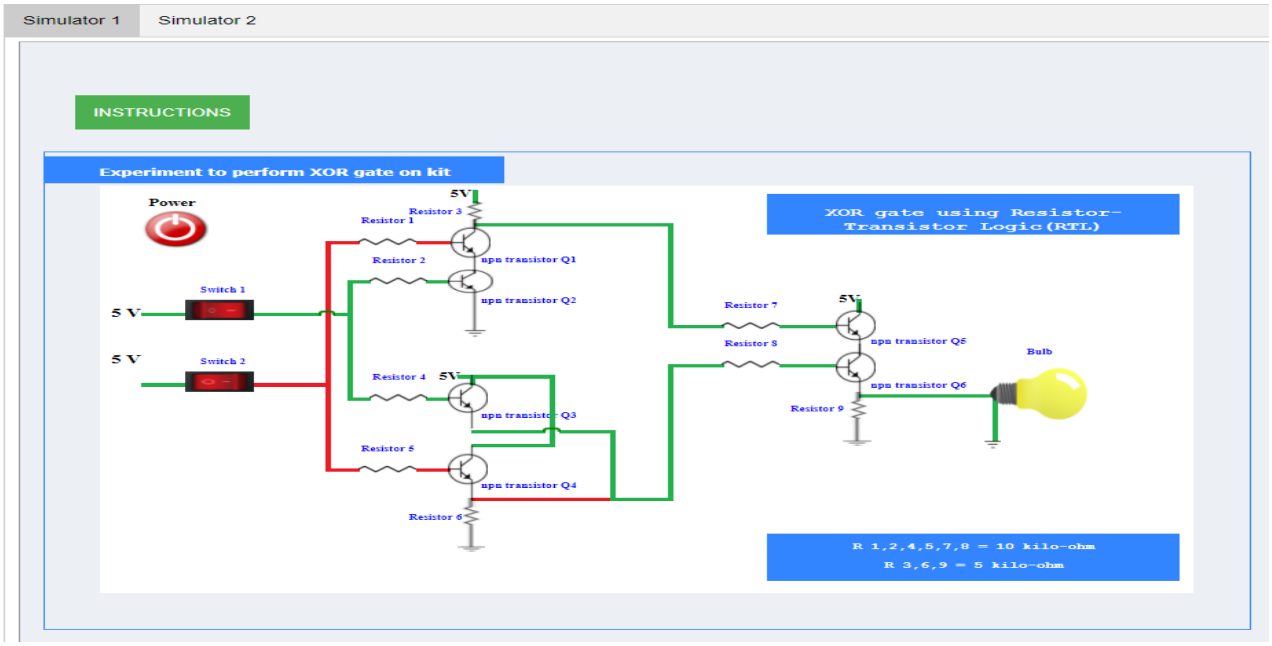


(2) Simulator 2:

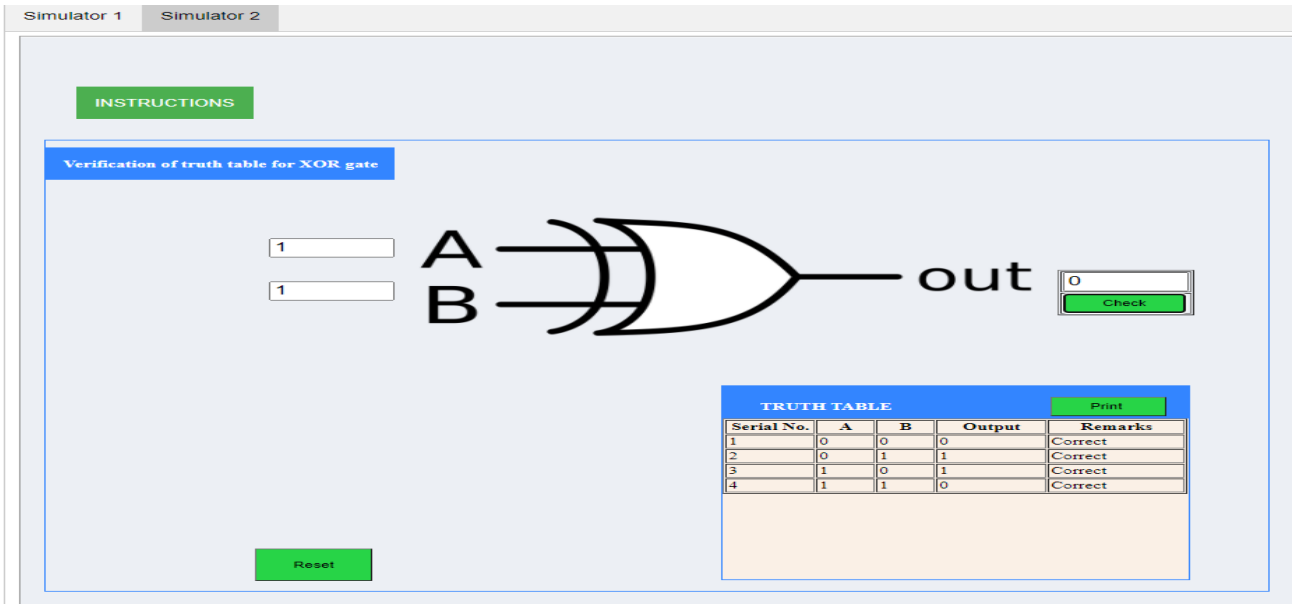


(F) Ex-OR Gate:

(1) Simulator 1:

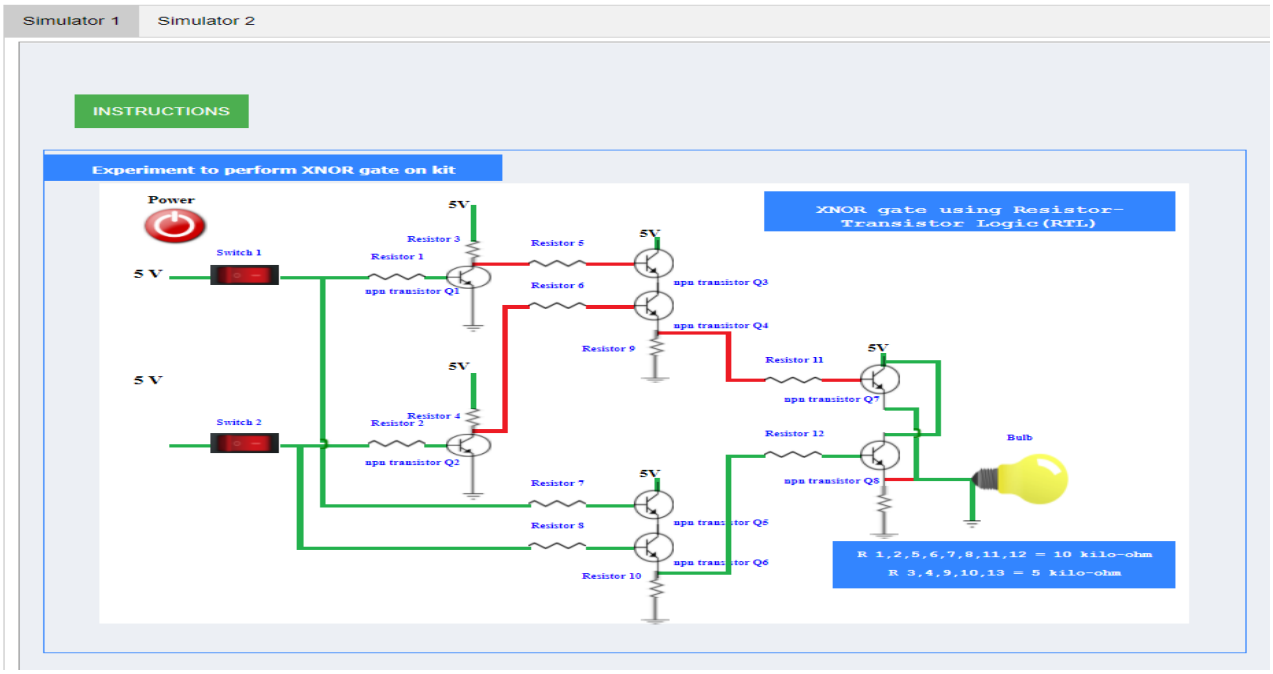


(2) Simulator 2:

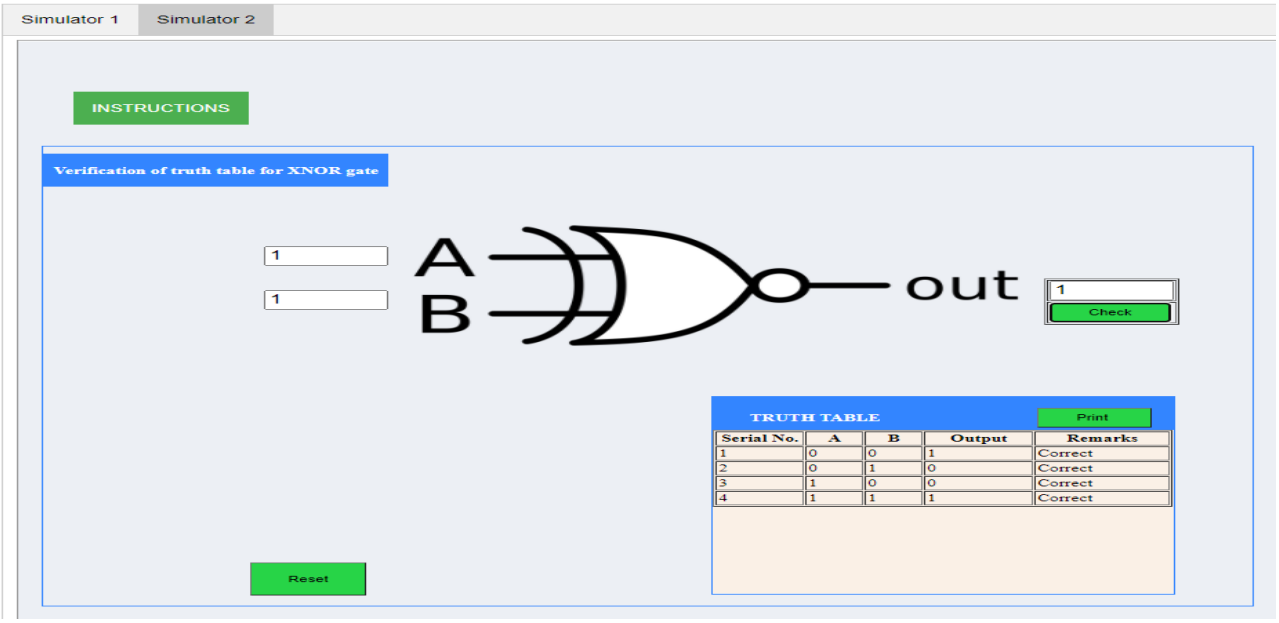


(G) Ex-NOR Gate:

(1) Simulator 1:



(2) Simulator 2:



Serial No.	A	B	Output	Remarks
1	0	0	1	Correct
2	0	1	0	Correct
3	1	0	0	Correct
4	1	1	1	Correct

Results and Conclusion: The verification of the truth tables of NOT, OR, AND, NOR, NAND, XOR, XNOR gates has been done successfully.

Experiment 10

Aim: To study and plot the characteristics of a JFET in its various configurations.

Tools Used: Experimental Kit, Multi-Meters, and Connecting Wires.

Theory: JFET was the earlier FET (Field emitter Transistor) avaliable. It a unipolar transistor since either the electrons or the holes (i.e. majority charge carriers) responsible for the current flow at a time unlike BJT which is bipolar transistor. It has three terminals i.e. Drain, Gate, and Source. It is a voltage -controlled device unlike BJT which is a current - controlled device since the flow of drain current is controlled by the volage between the gate and the source. The main difference between JFET and BJT is that in JEFT no gate current flows, the current through this device is controlled by the electric field, hence "Field effect transistor".

JFET is of two types:

- n-Channel JEFT
- p-Channel JEFT

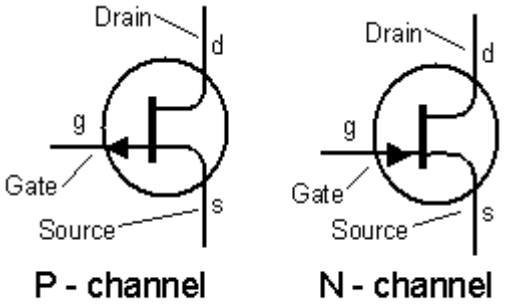


Fig 1: Representation of the p-Channel and n-Channel JFET.

n-Channel JFET: In n- Channel device, the n – Channel is sandwiched between two p-type regions that are connected together electrically to form the gate. The N-type channel is connected to the source and the drain terminal via heavily doped N+ type regions. The drain to the positive supply and the source to zero volts. N+ type silicon has a lower resistivity than N type. This gives it a lower resistance, increasing conduction and reducing the effect of placing standard N type silicon next to the aluminium connector, which because aluminium is a tri-valent material, having three valence electrons whilst silicon has four, would tend to create an unwanted junction, similar in effect to a PN junction at this point.

The P type gate is at 0V and is therefore negatively biased compared to the channel, which has a potential gradient on it as one end is connected to 0 volts, (the source) and the other to a positive voltage (the drain). Any point on the channel (apart from the extreme end near the source terminal) must therefore be more positive than the gate. Hence the two PN junctions formed between the N type channel and the P type areas of the gate and the substrate are both reverse biased, and so have a depletion layer that extends into the channel. The shape of the depletion layer is not symmetrical.

It is generally thicker towards the drain end of the channel, because the voltage on the drain is more positive than that on the source due to voltage gradient that exists along the channel. This

causes a larger potential across the junctions nearer the drain, and hence a thickening of the depletion layer. The effect becomes more marked when the voltage between drain and source is greater than about 1volt or so.

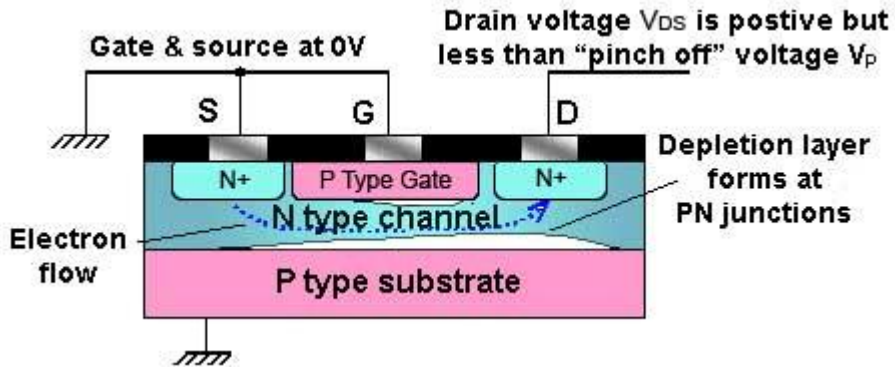


Fig 2: JFET Operation Below 'Pinch Off'

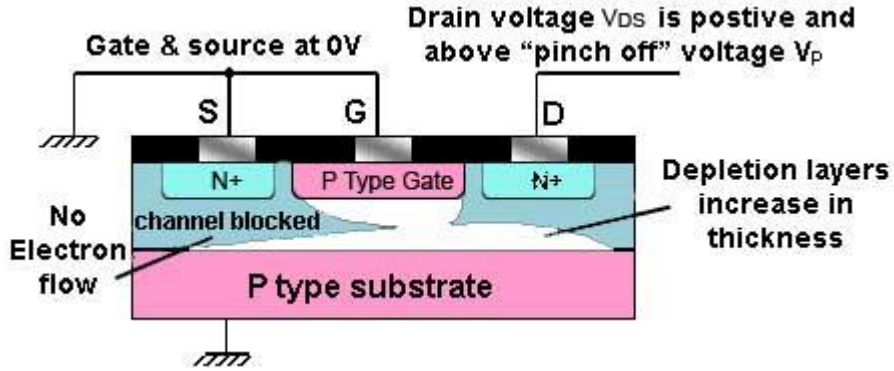


Fig 3: JFET Operation Above 'Pinch Off'

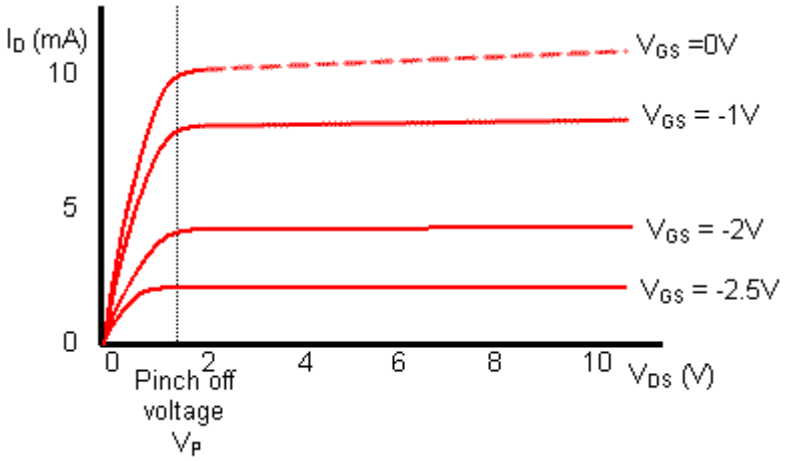


Fig 4: JFET Output/Drain Characteristics

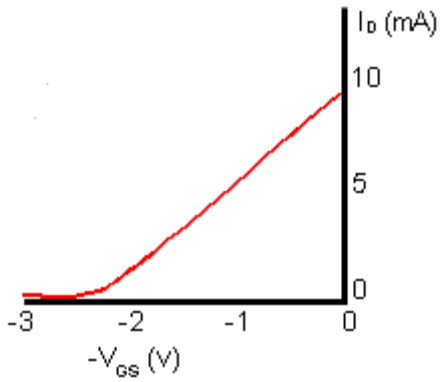


Fig 5: JFET Transfer Characteristics

When a voltage is applied between drain and source (VDS) current flows and the silicon channel acts rather like a conventional resistor. Now if VDS is increased (with VGS held at zero volts) towards what is called the pinch off value VP, the drain current ID also at first, increases. The transistor is working in the "q ohmic region".

However as drain source voltage VDS increases, the depletion layers at the gate junctions are also becoming thicker and so narrowing the N type channel available for conduction. There comes a point, known as "pinch off" where the conducting channel has become narrow enough to cancel out the effect of current increasing with the applied voltage VDS. Above this point there is little further increase in drain current and the transitor is said to operating in "saturation mode". With the JFET biased in this way, a small change in VGS can be used to control the current through the source-drain channel from its maximum(saturated) value to zero current.

This type of operation is shown in the fairly flat top to the output characteristics. Notice that each curve is drawn for a particular value of negative voltage between gate and source, and that when sufficient reverse bias is applied to the gate (e.g. more than -2.5V; the lowest value on the graph) the drain current ceases completely.

In the JFET output characteristics, because the curves are very nearly horizontal at voltages greater than the pinch off voltage.

The transfer characteristic for a JFET, which shows the change in drain current for a given change in gate source voltage. Because the JFET input (the gate) is voltage operated we cannot talk of current gain as we do with bipolar transistors. The drain current is controlled by gate-source voltage so the graph shows milliamperes per volt (mA/V). As I/V is CONDUCTANCE (the inverse of resistance V/I) we call the slope of this graph (the gain of the device) the FORWARD or MUTUAL TRANSCONDUCTANCE, which has the symbol gm. Thus the higher the value of gm the greater the amplification

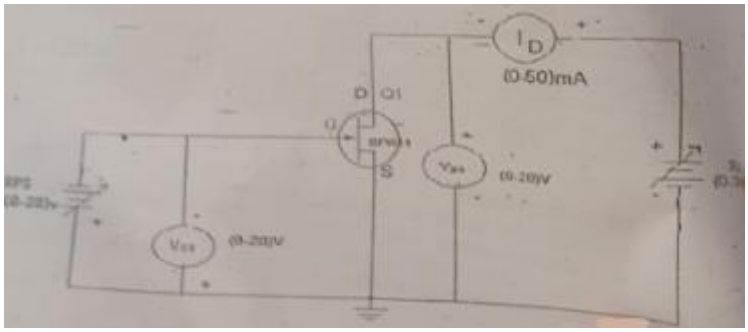
Notice that VGS is always shown as being negative; in reality it may be zero or slightly above zero, but the gate is always more negative than the N type channel between source and drain. Note also that the slope of the curve in the transfer characteristic is less steep than that of the transfer characteristic for a typical bipolar transistor'.This means that a JFET will have a lower gain than that of a bipolar transistor.

This disadvantage is offset by the advantage of having an extremely high input resistance. A typical input resistance for a JFET would be in the region of 1 x 1010 ohms (10,000 Megohms!) compared with 2 to 3 Kohms for a bipolar device.

This makes the JFET ideal for applications where the circuit or device driving the JFET amplifier cannot supply any appreciable current, an example being the Electret microphone, which uses a FET within the microphone to amplify the tiny voltage variations appearing across the vibrating diaphragm element.

Another feature of the JFET makes it better suited to very high frequency use than bipolar transistors. That is the absence of junctions in transistor. In a bipolar transistor two PN junctions forming tiny capacitances, exist between base and emitter, and base and collector, due to the PN junctions, These capacitances will limit high frequency performance, as they provide negative feedback paths at high frequencies. Because the JFET is in effect just a slab of silicon between source and drain the stray capacitances that exist in bipolar devices are absent, so high frequency performance is improved, making JFETs usable even at hundreds of MHz.

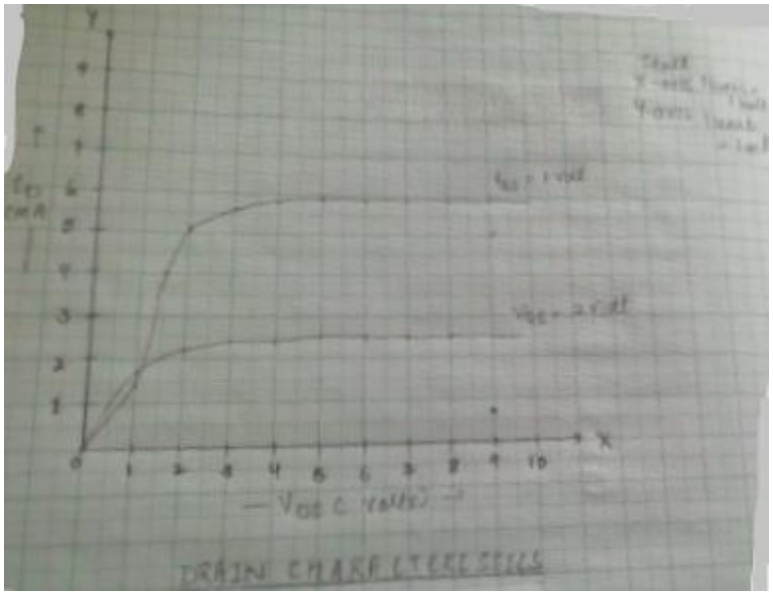
Circuit Diagram:



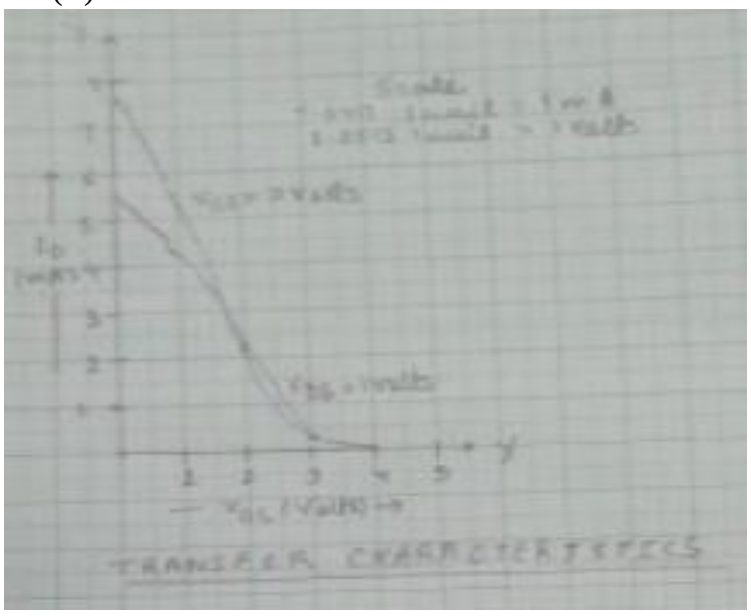
Experimental setup:

Graph:

(A) Drain Characteristics:



(B) Transfer Characteristics



Observations:

(A) Drain Characteristics

Sr. No.	VGS=1V		VGS=2V	
	VDS (V)	ID (mA)	VDS (V)	ID (mA)
1	0	0	0	0
2	1	1.4	1	1.7
3	2	5.1	2	2.2
4	3	5.6	3	2.4
5	4	5.8	4	2.4
6	5	5.9	5	2.5
7	6	5.9	6	2.5
8	7	5.9	7	2.5
9	8	5.8	8	2.5

(B) Transfer Characteristics

Sr. No.	VDS=1V		VDS=2V	
	VGS (V)	ID (mA)	VGS (V)	ID (mA)
1	0	0	0	0
2	0.1	5.4	0.1	7.6
3	0.2	5.3	0.2	7.4
4	0.3	5.2	0.3	7.2
5	0.4	5	0.4	6.9
6	0.5	4.9	0.5	6.7
7	0.6	4.8	0.6	6.4
8	0.7	4.7	0.7	6.2
9	0.8	4.6	0.8	5.9
10	0.9	4.3	0.9	5.5
11	1	4.2	1	5.3
12	2	2.3	2	2.2
13	3	0.3	3	0.3
14	4	0	4	0

Results and Conclusion: The characteristics of the JFET has been studied and plotted successfully.