

Experiment 2

Aim: To design the half adder using both the gates and verify its operation.

Tools Used: Virtual Labs and Circuit Verse.

Theory: Adders digital circuits that carry out addition of numbers. Adders are a key component of arithmetic logic unit. Adders can be constructed for most of the numerical representations like Binary Coded Decimal (BDC), are Excess – 3, Gray code, Binary etc. out of these, binary addition is the most frequently performed task by most common adders. Apart from addition, adders are also used in certain digital applications like table index calculation, address decoding etc. Binary addition is similar to that of decimal addition. Some basic binary additions are shown below.

$$\begin{array}{r} 0 \quad 0 \quad 1 \quad 1 \\ +0 \quad +1 \quad +0 \quad +1 \\ \hline 0 \quad 1 \quad 1 \text{ (carry) } 10 \end{array}$$

Fig 1: Schematic Representation of Half Adder

Half Adder Circuits: Half adder is a combinational circuit that performs simple addition of two binary numbers. The block diagram of a half adder is shown below.

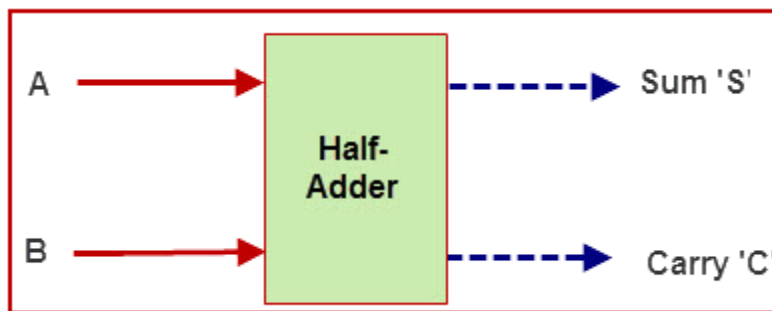
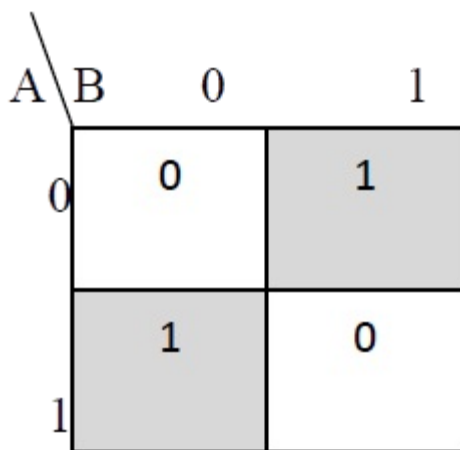


Fig 2: Block Diagram of Half Adder Circuit

If we assume A and B as the two bits whose addition is to be performed, then the sum output of the binary addition carried out above is similar to that of an Ex-OR operation while the carry output is similar to that of an AND operation. The same can be verified with help of Karnaugh Map.

A	B	Sum
0	0	0
0	1	1
1	0	1
1	1	0

Table1: Truth Table of Sum Output Line of the Half Adder Circuit



$$\text{Sum} = AB' + A'B$$

Fig 3: K-map Representation of the Sum Output Line of the Half Adder Circuit

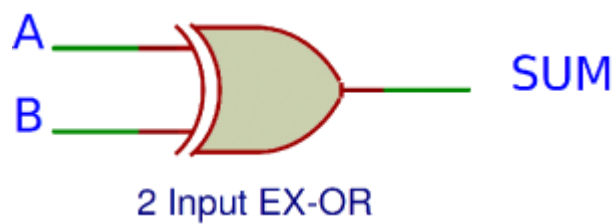


Fig 4: Logic Gate Representation of the Sum Output of the Half Adder Circuit

A	B	Carry
0	0	0
0	1	0
1	0	0
1	1	1

Table 2: Truth Table of Carry Output Line of the Half Adder Circuit

A \ B	0	1
0	0	0
1	0	1

Carry=A.B.

Fig 5: K-map Representation of the Carry Output Line of the Half Adder Circuit

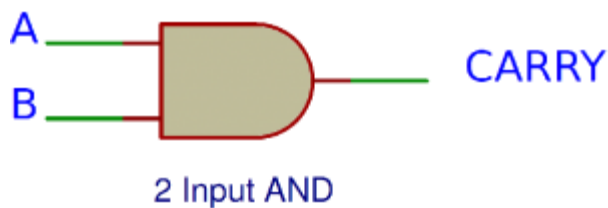


Fig 6: Logic Gate Representation of the Sum Output of the Half Adder Circuit

Half Adder Circuit Using AND and XOR Gates: If A and B are binary inputs to the half adder, then the logic function to calculate sum S is Ex – OR of A and B and logic function to calculate carry C is AND of A and B. Combining these two, the logical circuit to implement the combinational circuit of half adder.

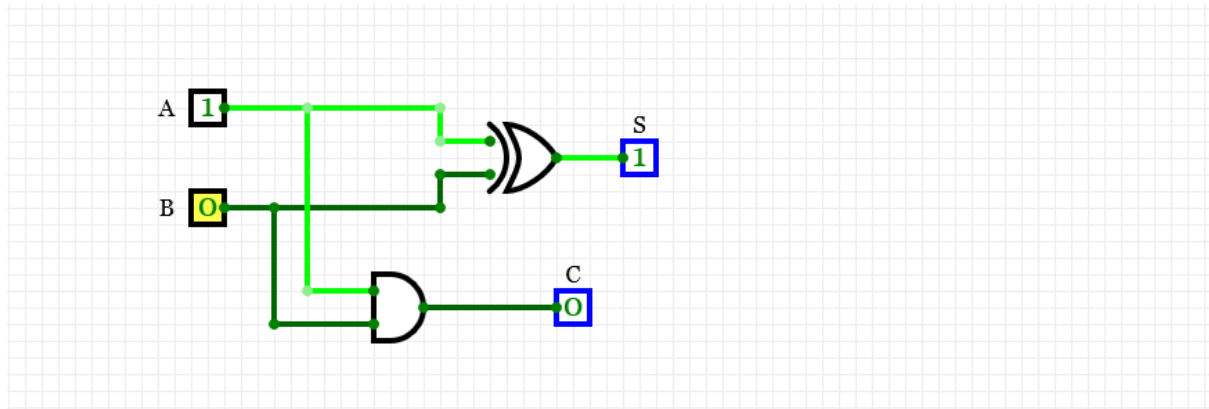
As we know that NAND and NOR are called universal gates as any logic system can be implemented using these two, the half adder circuit can also be implemented using them. We know that a half adder circuit has one Ex – OR gate and one AND gate. Here, we show the designing and implementation of Half Adder Circuit using NAND gate only.

Half Adder Circuit Using NAND Gate: Five to seven NAND gates are required in order to design a half adder. The circuit to realize half adder using NAND gates.

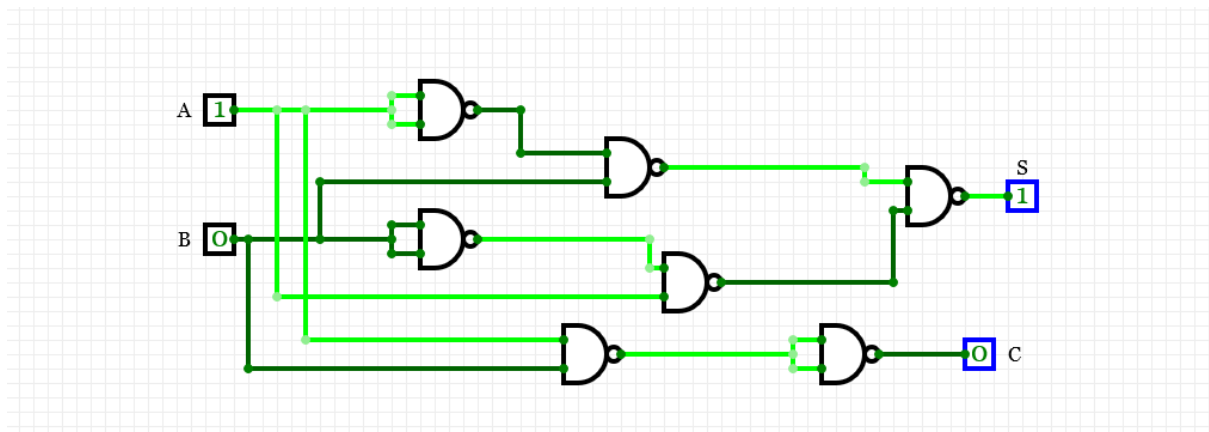
Observations:

Circuit representation of Half Adder Circuit using:

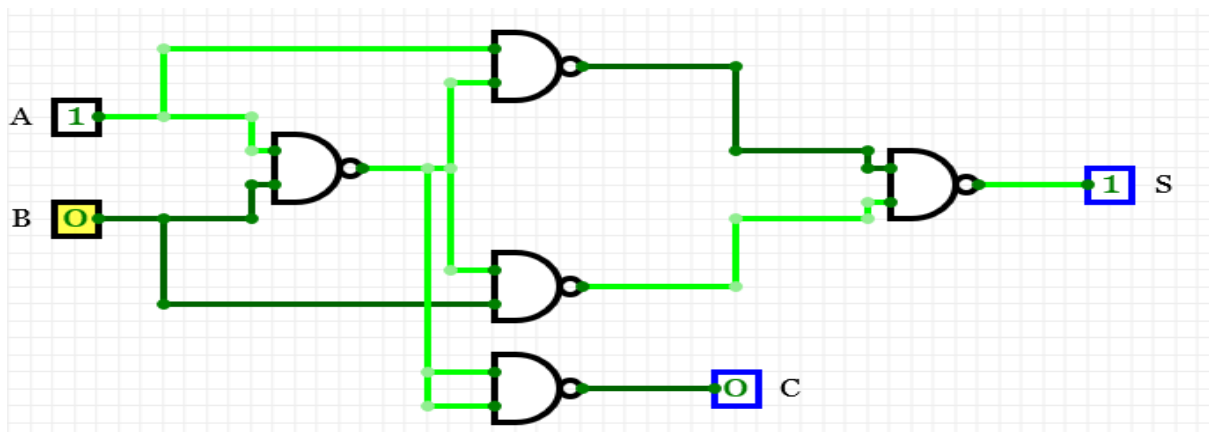
(A) XOR and AND Gates:



(B) NAND Gate:



OR



Result: The operation of Half Adder Circuit has been verified successfully.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
(A) CONCEPT	2		
(B) IMPLEMENTATION	2		
(C) PERFORMANCE	2		
TOTAL	6		