Experiment 9

Aim: To design and simulate a 4-bit bus using multiplexers.

Theory: A typical computer has many registers and we need to transfer the information between these registers. A way to transfer the information is using the common bus system.
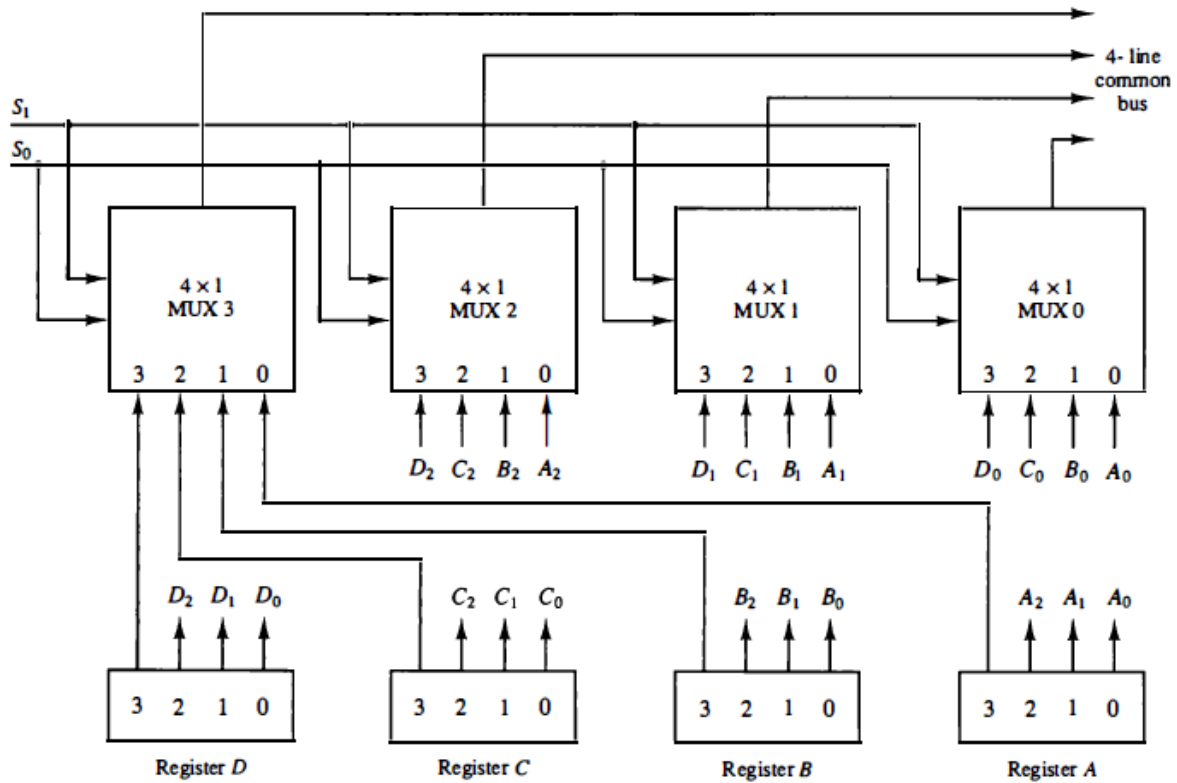

Fig 1: Bus Line with Multiplexers

The construction of this bus system for 4 registers is shown above. The bus consists of 4×1 multiplexers with 4 inputs and 1 output and 4 registers with bits numbered 0 to 3. There are 2 select inputs S0 and S1 which are connected to the select inputs of the multiplexers which will decide which register data must be transferred on common bus. The output 1 of register A is connected to input 0 of MUX 1 and similarly other connections are made as shown in the diagram. The data transferred to the bus depends upon the select lines. A table for the various combinations of select lines is shown below.

Select Lines Combination		Register Selected
S0	S1	
0	0	A
0	1	B
1	0	C
1	1	D

*Table 1: Truth Table of Selection of Registers by Select Lines in Bus Line with Multiplexers*

As we can see that when S1S0=00, register A is selected because on 00 the 0 data inputs of all the multiplexers are applied to the common bus. Since the 0 data inputs of all the multiplexers receive the inputs from the register A, thus register A gets selected. Similarly, for other combinations of S1S0 other register are selected.

Note:

- No. of multiplexers needed = No. of bits in each register
- Common bus system can be designed for a bus transfer of n registers using n MUX of n X 1 size.
- In general, a bus system will multiplex k registers of n bits each to produce an n-line common bus. The number of multiplexers needed to construct the bus is equal to n, no of bits in each register. The size of each multiplexer must be k × 1 since it multiplexer k data lines.

Observations:

Circuit Representation of 4-Bit Bus System Using Multiplexers:
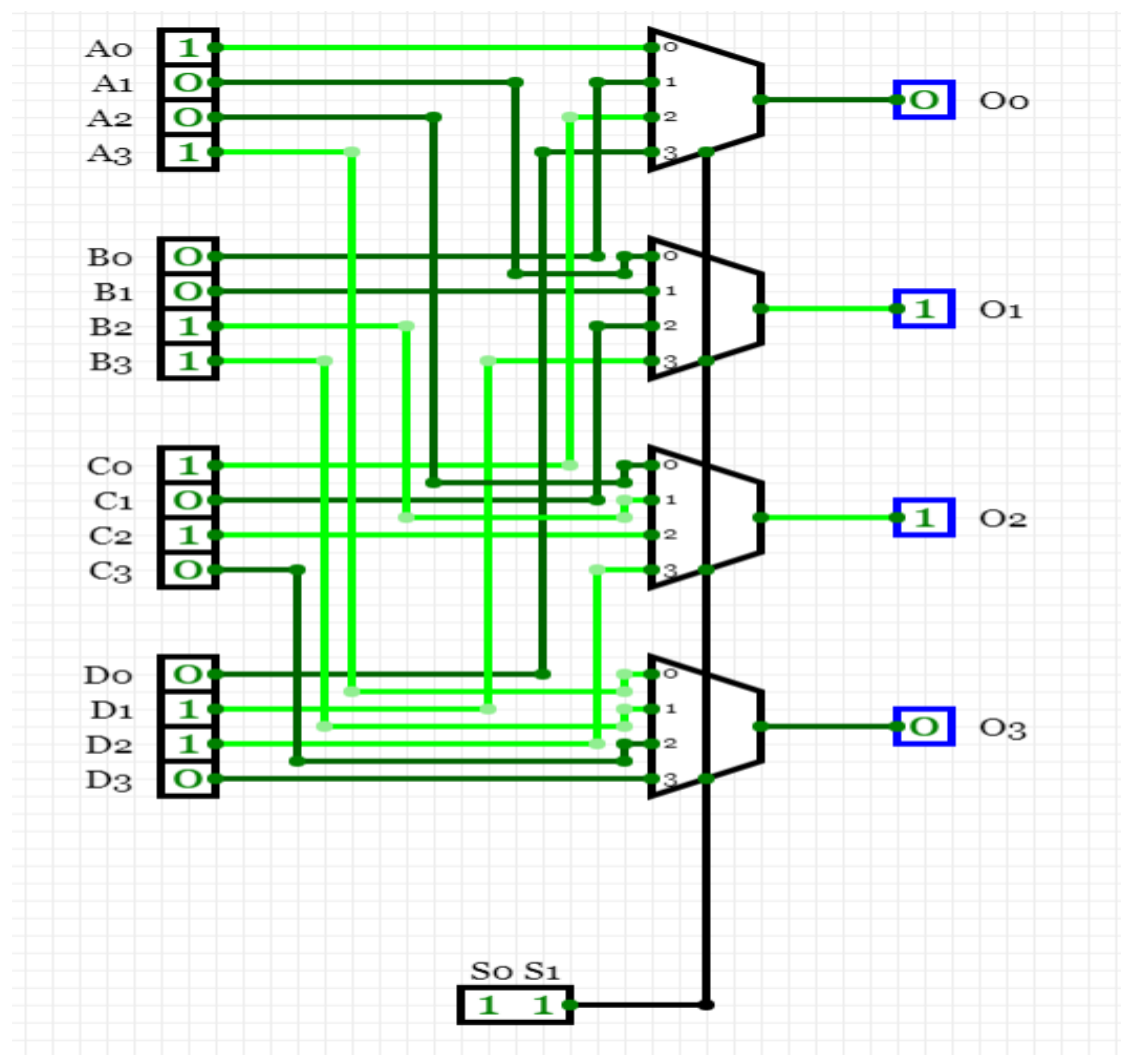
Result: The designing of a 4-bit bus system with multiplexers has been done successfully.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
(A) CONCEPT	2		
(B) IMPLEMENTATION	2		
(C) PERFORMANCE	2		
TOTAL	6		