

Experiment 3

Aim: To design full adder by using XOR and NAND gates and verify its truth table.

Tools Used: Virtual Labs and Circuit Verse.

Theory: Adders digital circuits that carry out addition of numbers. Adders are a key component of arithmetic logic unit. Adders can be constructed for most of the numerical representations like Binary Coded Decimal (BDC), are Excess – 3, Gray code, Binary etc. out of these, binary addition is the most frequently performed task by most common adders. Apart from addition, adders are also used in certain digital applications like table index calculation, address decoding etc. Binary addition is similar to that of decimal addition. Some basic binary additions are shown below.

0	0	1	1
<u>+0</u>	<u>+1</u>	<u>+0</u>	<u>+1</u>
0	1	1	(carry) 10

Fig 1: Schematic Representation of Half Adder

Full adder Circuits: Full adder is a digital circuit used to calculate the sum of three binary bits which is the main difference between full adder and half adder. Full adders are complex and difficult to implement when compared to half adders. Two of the three bits are same as before which are A, the augend bit and B, the addend bit. The additional third bit is carry bit from the previous stage and is called 'Carry' – in generally represented by CIN. It calculates the sum of three bits along with the carry. The output carry is called Carry – out and is represented by COUT. The block diagram of a full adder with A, B and CIN as inputs and S, COUT as outputs is shown below.

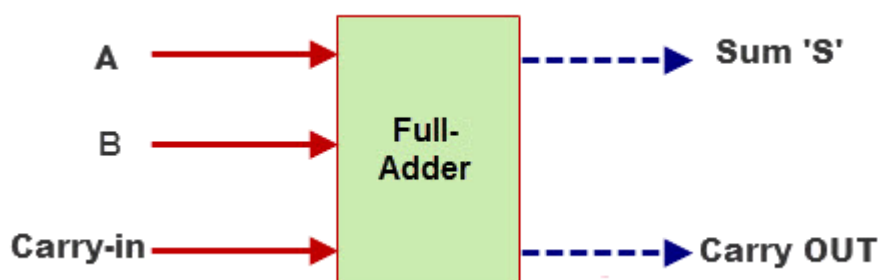


Fig 2: Block Diagram of Full Adder Circuit

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth Table of Full Adder Circuit

Based on the truth table, the Boolean functions for Sum (S) and Carry – out (COUT) can be derived using K – Map.

A	BC _{IN}	00	01	11	10
0		0	1	0	1
1		1	0	1	0

The simplified equation for sum is $S = A'B'C_{IN} + A'BC_{IN}' + ABC_{IN} + AB'C_{IN}$

Fig 2: K-map Representation of the Sum Output Line of the Full Adder Circuit

A	BC _{IN}	00	01	11	10
0		0	0	1	0
1		0	1	1	1

The simplified equation for COUT is $COUT = AB + AC_{IN} + BC_{IN}$

Fig 3: K-map Representation of the Carry Output Line of the Full Adder Circuit

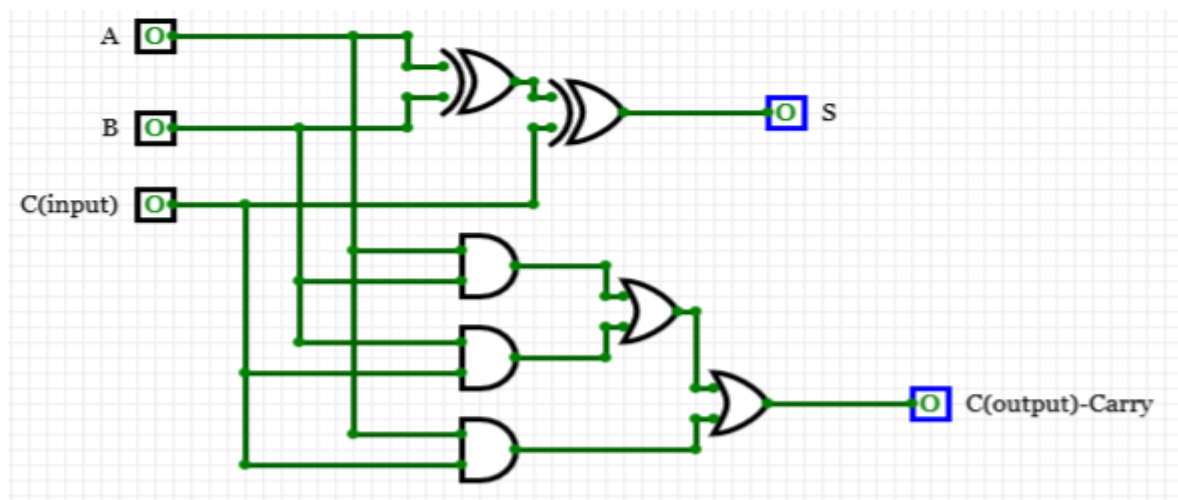
Full Adder Circuit Using XOR and AND Gate: In order to implement a combinational circuit for full adder, it is clear from the equations derived above, that we need four 3-input AND gates and one 4-input OR gates for Sum and three 2-input AND gates and one 3-input OR gate for Carry – out.

Full Adder Circuit Using NAND Gate: As mentioned earlier, a NAND gate is one of the universal gates and can be used to implement any logic design.

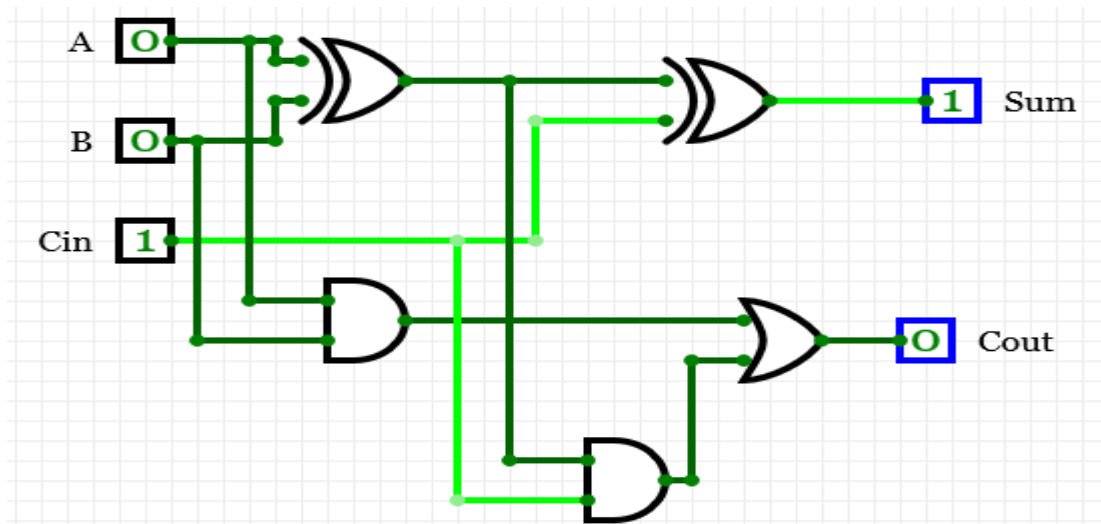
Circuit Representation:

Circuit representation of full adder circuit using:

(A) XOR and AND Gates:

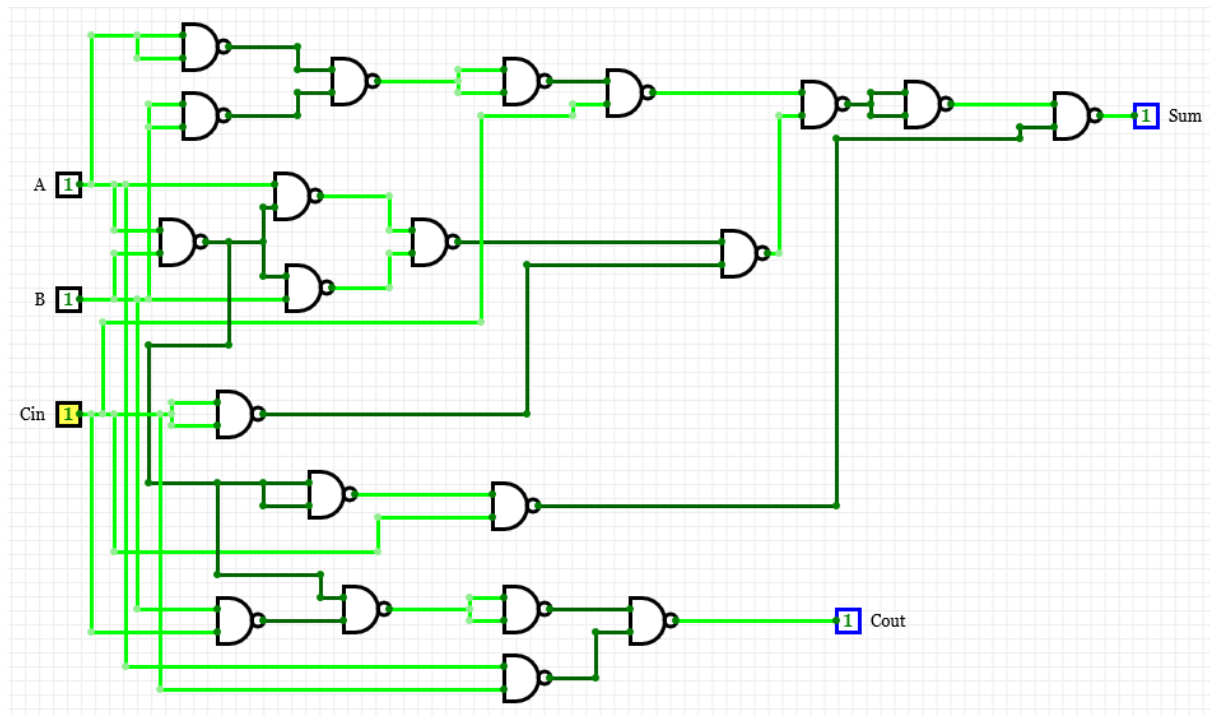


OR



(By Using Half Adder Circuit)

(B) NAND Gate:



Result: The operation of Full Adder Circuit has been verified successfully.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
(A) CONCEPT	2		
(B) IMPLEMENTATION	2		
(C) PERFORMANCE	2		
TOTAL	6		