Experiment 8

Aim: To design 4-bit bus using three-state buffer gate and decoder.

Tools Used: Circuit Verse

Theory: Usually any logic circuit has 2 states, i.e., in binary form (0 and 1). The buffer exhibits three states. It has 3 pins which include:
Input – accepts 1 or 0 (0 – disable and 1 – enable)
Output – if 3-state control is 0 then output follows input(according to the input 0 and 1.
Definition: A three state bus buffer is an integrated circuit that connects multiple data sources to a single bus. The open drivers can be selected to be either a logical high, a logical low, or high impedance which allows other buffers to drive the bus.
Now, let's see the more detailed analysis of a 3-state bus buffer in points:

1. As in a conventional gate, 1 and 0 are two states.
2. Third state is a high impedance state.
3. The third state behaves like an open circuit.
4. If the output is not connected, then there is no logical significance.
5. It may perform any type of conventional logic operations such as AND, OR, NAND, etc.

Difference Between Normal Buffer and Three-State Buffer: It contains both normal input and control input. Here, the output state is determined by the control input.

- When the control input is 1, the output is enabled and the gate will behave like conventional buffer.
- When the control input is 0, the output is disabled and the gate will be in high impedance state.

How to Form a Bus Line using Three-State Buffer:

1. To form a single bus line, all the outputs of the 4 buffers are connected together.
2. The control input will now decide which of the 4 normal inputs will communicate with the bus line.
3. The decoder is used to ensure that only one control input is active at a time.

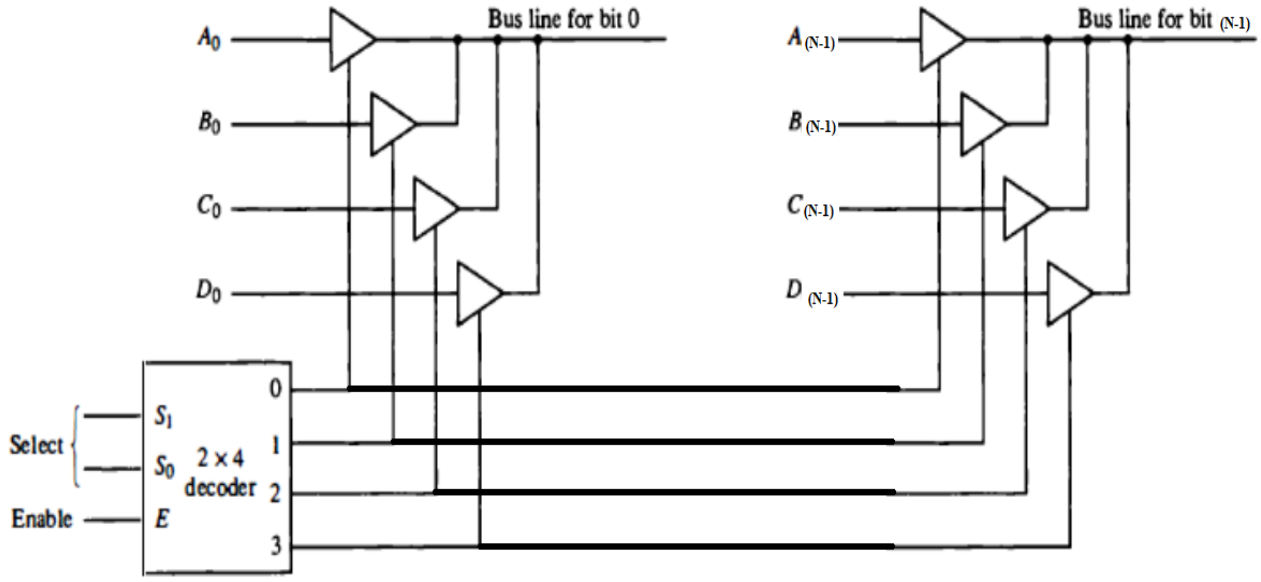
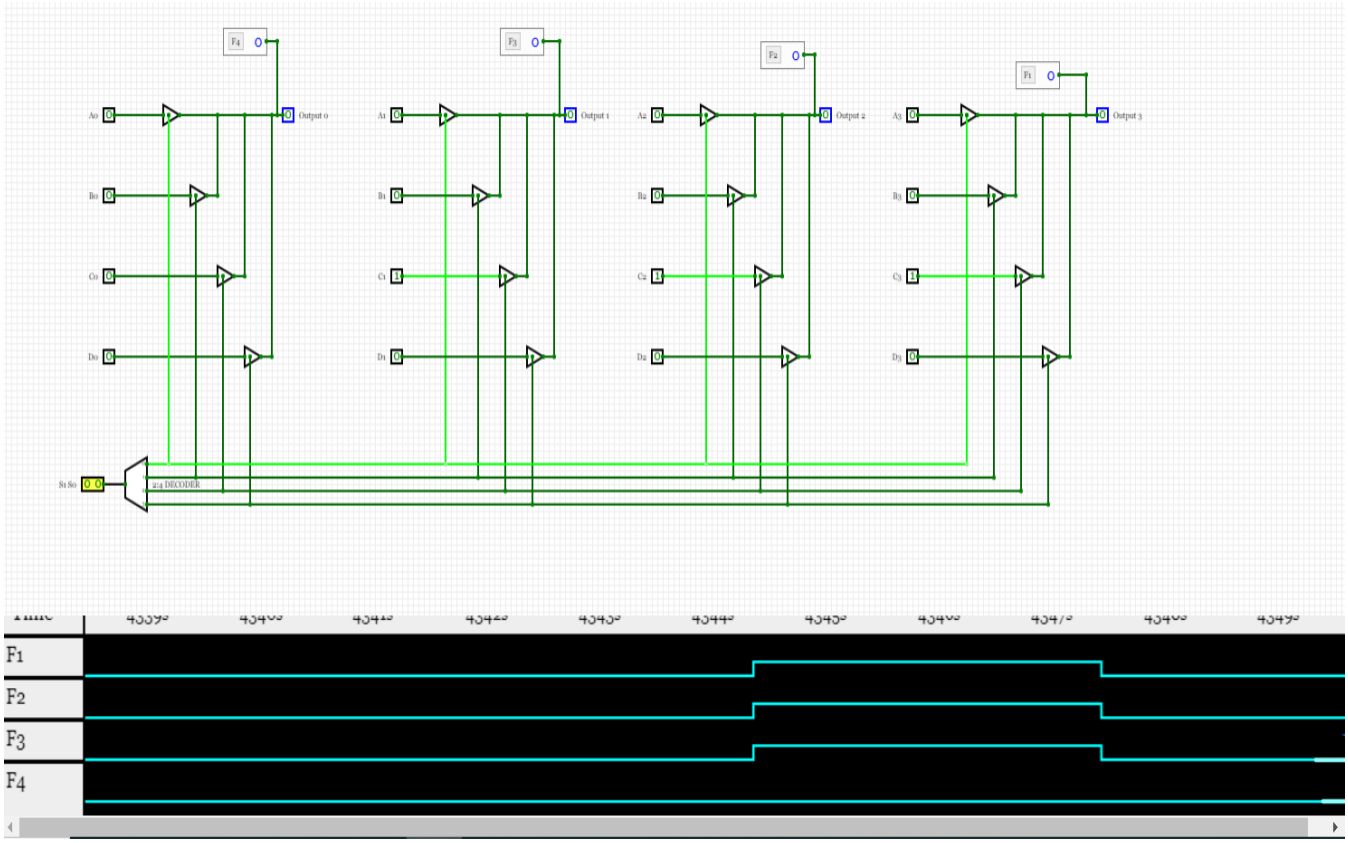


Fig 1: Bus Line with Three State Buffers and Decoder

Observations:

Circuit Representation of 4-Bit Bus System Using Three State Buffer Gate and Decoder:



Result: The designing of three-state buffer gate has been done successfully.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
(A) CONCEPT	2		
(B) IMPLEMENTATION	2		
(C) PERFORMANCE	2		
TOTAL	6		