Experiment 10

Aim: To design and simulate 4-to2-Priority Encoder using logic gates.

Tools Used: Circuit Verse.

Theory: An encoder has 2^n inputs, and n output lines. Only one input can be at logic 1 at any given time (active input). All other inputs must be 0's. It accepts an active level on one of its inputs representing a digit, such as a decimal or octal digit, and converts it to a coded output, such as BCD or binary. The major problem with the encoder is that it can generate the wrong output code when there is more than one input present at logic level "1". To prevent this one can use priority encoder. A priority encoder is a device which has same functioning as encoders but it will produce the output corresponds to the currently active input which has the highest priority. So, when an input with a higher priority is present, all other inputs with a lower priority will be ignored.

It consists of:

- 4 input channels having sixteen input combinations.
- Three output variables A1, A0, and V.
- A valid indicator, V, is included to indicate whether or not the output is valid.
- Output is invalid when no inputs are active i.e. V = 0. Output is valid when at least one input is active V = 1.

In last row we have 1111 input combinations, whose output is 11. This is because E3 is the highest priority input, and it is equal to 1. Though the other inputs with smaller subscripts, namely, E2, E1, and E0 are also having values of one in some combinations, but they do not have the priority.

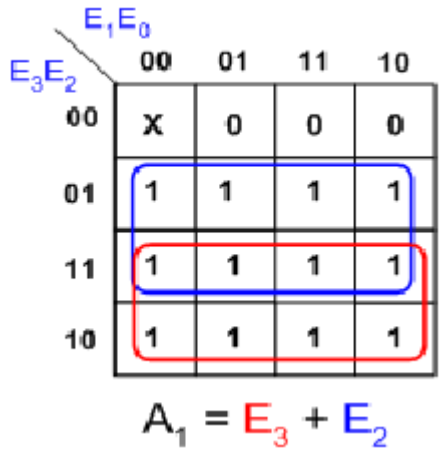


Fig 1: K-map Representation of the A_1 Output Line of the Priority Encoder

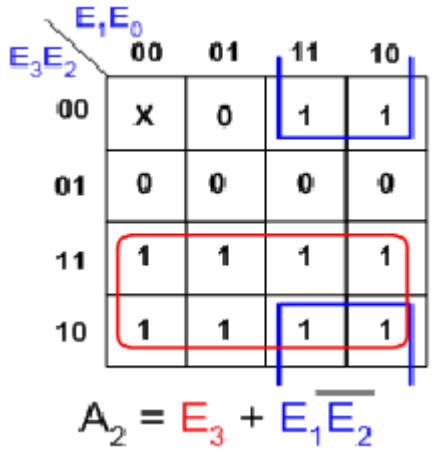


Fig 2: K-map Representation of the A_0 Output Line of the Priority Encoder

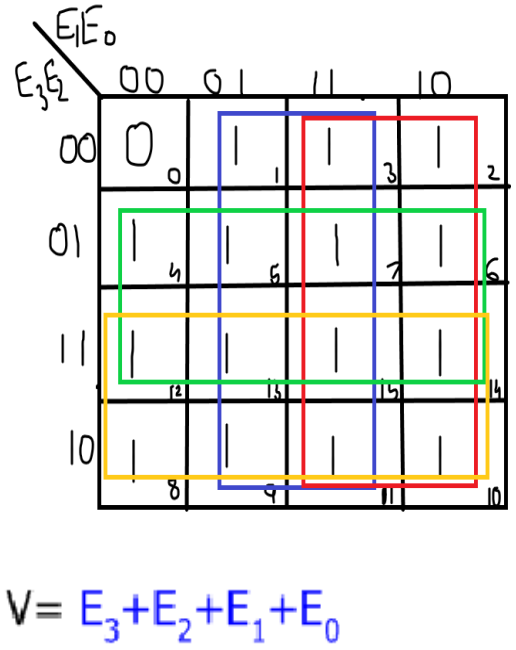


Fig 3: K-map Representation of the V Output Line of the Priority Encoder

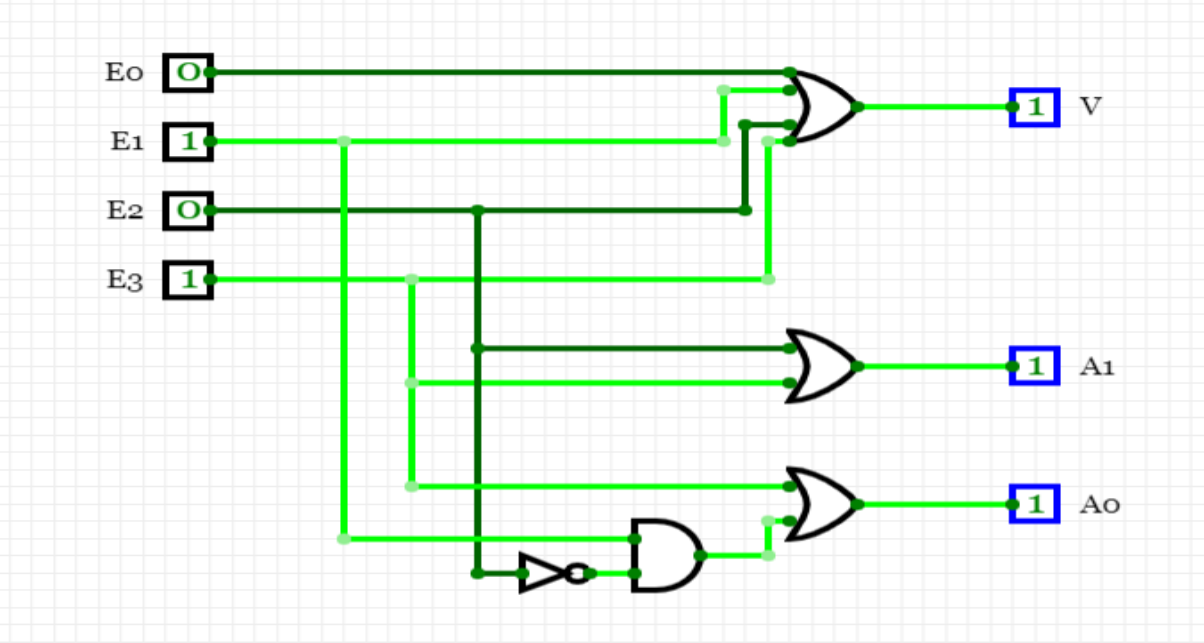
E3	E2	E1	E0	A1	A0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1

1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

Table 1: Truth Table of Priority Encoder

Circuit Representation:

Circuit representation of the Priority Encoder circuit using Logic Gates is:



Result: The designing of the 4-to-2 Priority Encoder has been done successfully.

CRITERIA	TOTAL MARKS	MARKS OBTAINED	COMMENTS
(A) CONCEPT	2		
(B) IMPLEMENTATION	2		
(C) PERFORMANCE	2		
TOTAL	6		