# Experiment 7

**Aim:** To design and simulate 4-bit BCD adder.

**Tools Used:** Circuit Verse.

**Theory:** BCD is Binary Coded Decimal number, where each digit of a decimal number is respected by its equivalent binary number. That means, LSB of a decimal number is represented by its equivalent binary number and similarly other higher significant bits of decimal number are also represented by their equivalent binary numbers.

Suppose, we have 4 bit numbers i.e. A and B which can vary from 0 (0000) to 9 (1001 in binary). For example:

Example 1:

```
Input :
A = 0111   B = 1000
Output :
Y = 1 0101

Explanation: We are adding A(=7) and B(=8).
The value of binary sum will be 1111(=15).
But, the BCD sum will be 1 0101,
where 1 is 0001 in binary and 5 is 0101 in binary.
```

Example 2:

```
Input :
A = 0101   B = 1001
Output :
Y = 1 0100

Explanation: We are adding A(=5) and B(=9).
The value of binary sum will be 1110(=14).
But, the BCD sum will be 1 0100,
where 1 is 0001 in binary and 4 is 0100 in binary.
```

If the decimal numbers are less than or equal to 9, then the value of BCD sum and the binary sum will be same otherwise they will be same otherwise they will be diff by 6 (0110 in binary).

| **Decimal** | **Binary Sum** | | | | | **BCD Sum** | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | C’ | S3’ | S2’ | S1’ | S0’ | C | S3 | S2 | S1 | S0 |
| **0** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **1** | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| **2** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| **3** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **4** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| **5** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| **6** | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| **7** | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| **8** | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| **9** | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| **10** | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| **11** | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| **12** | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| **13** | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| **14** | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| **15** | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| **16** | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| **17** | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| **18** | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| **19** | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

*Table 1: Truth Table of Binary to BCD Adder.*

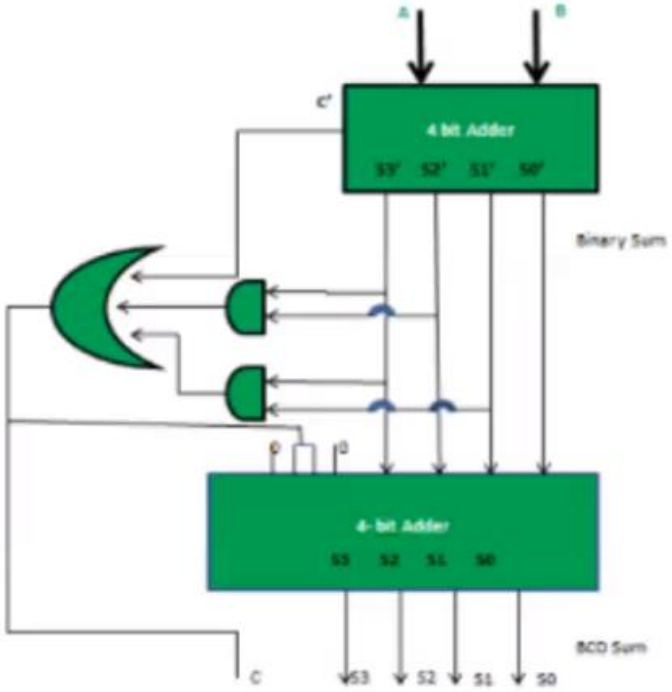
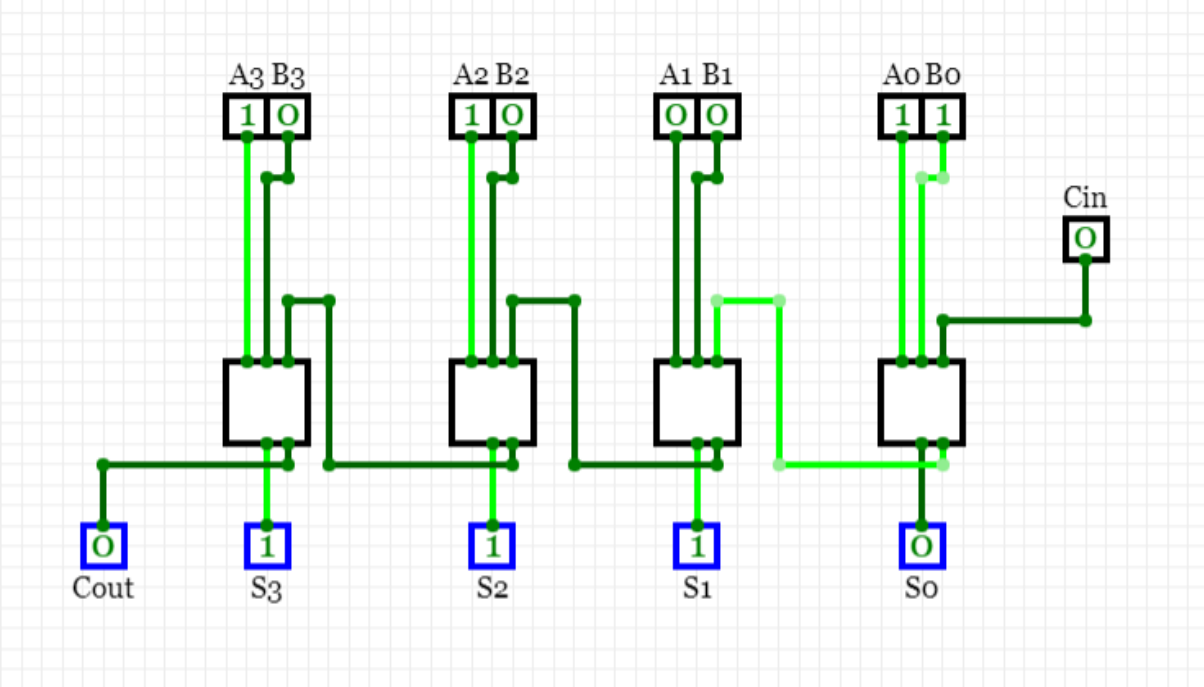


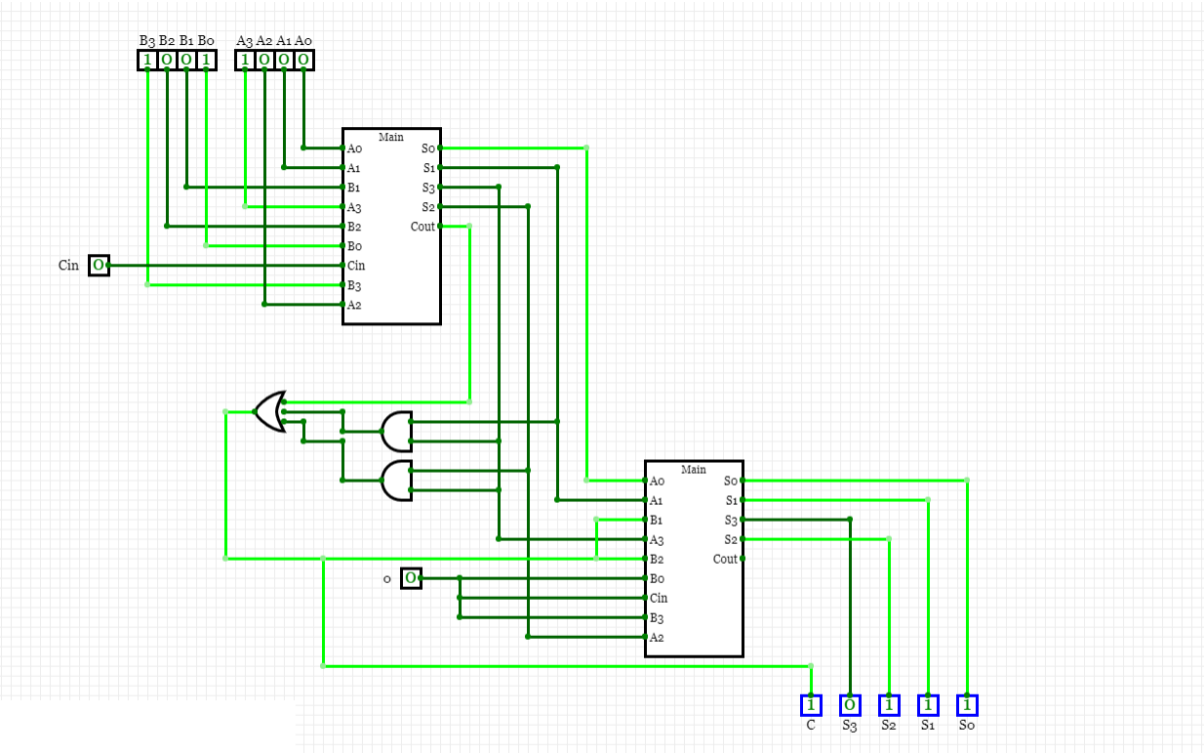

*Fig 1: Blueprint of 3 Bit Binary to BCD Adder.*

## Observations:

Circuit Representation of Full Adder Circuit:




Circuit Representation of Binary to BCD:




**Result:** The designing and simulation of binary to BCD adder has been done successfully.

| CRITERIA | TOTAL MARKS | MARKS OBTAINED | COMMENTS |
|---|---|---|---|
| (A) CONCEPT | 2 | | |
| (B) IMPLEMENTATION | 2 | | |
| (C) PERFORMANCE | 2 | | |
| TOTAL | 6 | | |