Shaizeen Aga

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Research Interests

My interests lie in three vital axes of computing: security, performance and energy efficiency, and ease of programmability. I am interested in designing architectural support to provide security guarantees efficiently. I am also keen to explore near-data computing techniques to tackle the data deluge we face and in designing runtime and hardware support to ease programmability.

Education

- **Ph.D.** Computer Science and Engineering, **University of Michigan, Ann Arbor.** Sep 2012 – Present
  Advisor: Prof. Satish Narayanasamy
- **MS**, Computer Science and Engineering, **University of Michigan, Ann Arbor.** Sep 2011 - May 2013
- **B Tech**, Information Technology, **College of Engineering**, **Pune, India.** Aug 2005 - May 2009
  - **Class rank 2nd** in Information Technology Department

Awards and Achievements

- **1st place** at **University of Michigan CSE Graduate Students Honors Competition 2016;** a yearly competition, which recognizes research of broad interest and exceptional quality done by graduate students.
- **Best demo** at Center for Future Architectures Research (CFAR) Annual Research Workshop 2016 which showcased nearly 50 projects in computer architecture related topics from several leading institutions.
- **Parallel Computing Award** at **Imagine Cup 2009;** a worldwide student technical competition organized by Microsoft.
- Recipient of **K.C. Mahindra Scholarship** for graduate studies; awarded to select few students across India.
- Recipient of **BP Corporation Scholarship** for graduate studies; awarded to select few students across India.
- **Microsoft Student Partner** at College of Engineering, Pune, India.
- Recipient of **Dhirubhai Ambani Scholarship** for undergraduate studies; awarded to select few students across India.
- **Winner** of **elocution competitions** at school and national level.
- **Class rank 1st** throughout schooling.

Academic and Professional Experience

- **Graduate Student Research Assistant,** *University of Michigan, Ann Arbor.* January 2012 - Present

Efficient secure hardware [1, 6]: In this work, I implemented a low-overhead hardware design that provides strong defenses against memory bus side-channels using compute capable 3D memories wherein we harness logic layer close to memory to implement cryptographic primitives. This design is one to two orders of magnitude lower in performance, space, energy, and memory bandwidth overhead compared to prior solutions.

Caches as data-parallel accelerators [2]: This work transforms large on-chip caches from passive to active compute units by enabling in-place computation in them. This transformation unlocks massive data parallelism (100X wrt SIMD processor) and saves significant amount of data movement energy (~10X wrt SIMD processor). This accelerates new-age applications, which process massive data in a data-parallel fashion considerably (1.9X performance, 2.4X energy savings).

Efficient fences for multi-cores [5, 8]: In this work, I designed and implemented an efficient fence instruction by decoupling coherence permission from data. Using this fence instruction we could enable stronger and more intuitive memory model like Sequential Consistency in hardware at a low cost (2.93%).

Stronger memory models for GPUs [3]: This work investigates memory model implications for GPUs wherein we propose a low-overhead GPU-specific non-speculative Sequential Consistency design.

- **Interim Engineering Intern,** *Qualcomm Research Silicon Valley (QRSV)* May 2014- August 2014
  Manager: *Calin Cascaval*

  Optimizing a heterogeneous benchmark: I worked here on optimizing a heterogeneous (CPU + mobile GPU) benchmark (ray tracing). Using algorithmic changes and ARM Neon instructions I attained 2-30X speedup. I also implemented an alternate algorithm which attained 40X speedup.

- **Intern,** *Pacific Northwest National* Laboratory June 2012- August 2012
  Mentor: *Sriram Krishnamoorthy*

  Smart runtime via optimistic concurrency: I worked here on improving the efficiency of Cilk runtime system. Cilk makes it easy for programmers to express parallelism yet synchronization primitives in Cilk tend to be over-constrained leading to poor performance. With speculation based approach and a smart predictor [4], I improved the performance of Cilk runtime system by upto 1.6X on 30 cores.

- **Senior Technology Associate**, *Morgan Stanley* January 2011 - July 2011
- **Technology Associate**, *Morgan Stanley* January 2010 - December 2011
  Manager: *Vinod Alva*

  Design and development of data warehouse: I was a part of Firm Market Risk Data Warehousing team here. My work primarily involved design and development of a Data Warehouse catering to regulatory (FED/FSA) requirement & analytical needs of the risk managers, optimizing queries and building analytical (OLAP) cubes for reporting purposes. I was a key contributor to a major re-structuring project (reduced the data transformation and load cycle by 65%).

  I also served as a mentor and I was involved in hiring initiatives as well.

- **Intern**, *NVIDIA Graphics Pvt Ltd* June 2008 - March 2009
  Manager: *Philips Koshy*

  Accelerating true motion estimation: I ported a True motion estimation algorithm onto the NVIDIA parallel computing platform CUDA to get 180X speedup.

Teaching Experience

- **Graduate Student Instructor,** *University of Michigan, Ann Arbor* Winter 2013, Winter 2014
  I taught Parallel Computer Architecture; a graduate course on recent advancements in parallel architectures.

Publications

[1] **S Aga** and S Narayanasamy. “InvisiMem: Smart Memory Defenses for Memory Bus Side Channel”. *To appear in 44th International Symposium on Computer Architecture **(ISCA)**, Toronto, ON, Canada, June 2017.*

[2] **S Aga**, S Jeloka, A Subramaniyan, S Narayanasamy, D Blaauw, and R Das. “Compute Caches”. *In IEEE Symposium on High Performance Computer Architecture (**HPCA**), Austin, Texas, February 2017.*

[3] A Singh**, S Aga**, S Narayanasamy. “Efficiently Enforcing Strong Memory Ordering in GPUs”. *In International Symposium on Microarchitecture (**MICRO**), Waikiki, Hawaii, December 2015.*

[4] **S Aga**, S Krishnamoorthy, S Narayanasamy. “CilkSpec: Optimistic Concurrency for Cilk”. In International Conference for High Performance Computing, Networking, Storage and Analysis *(**SC**), Austin, TX, November 2015.*

[5] **S Aga**, A Singh, S Narayanasamy. “zFence: Data-less Coherence for Efficient Fences”. *In 29th International Conference on Supercomputing (**ICS**), Newport Beach, CA, June 2015.*

Patents

[6] **S Aga**, S Narayansamy. "Trusted computing system with enhanced memory".
US Patent Pending.

[7] B Robatmili, **S Aga**, D Gracia, A Raman, A Natarajan, G C Cascaval, P M Ortego, H Zhao. "Method for exploiting parallelism in task-based systems using an iteration space splitter".
US Patent 9501328.

[8] **S Aga**, A Singh, S Narayansamy. "Ordering constraint management within coherent memory systems". *US Patent 9367461.*

Other Projects

- ***Speculatively relaxing memory model constraints by dynamic classification of cache blocks.***

  Using dynamic classification of cache blocks, I relaxed memory consistency model constraints to improve performance of Sequentially Consistent hardware. This project earned **top grade in Winter 2012 class of Parallel Computer Architecture** at University of Michigan.

- ***Design and implementation of P6 microarchitecture based core in Verilog.***

  I implemented the memory interface of the core and host of other components. I designed and implemented an **Adaptive Instruction Prefetcher** which gained us significant performance benefits. This project earned **top grade in Fall 2011 class of Computer Architecture** at University of Michigan.

- ***Parallel implementation of Maximum likelihood method of Phylogenetic Tree construction algorithm.***

  Phylogenetic tree construction algorithms are crucial in the field of drug design. Using Microsoft's Task Parallel library, I improved the performance of computationally intensive Maximum Likelihood method of Phylogenetic tree construction. This project won **Parallel Computing Award** at **Microsoft's Imagine Cup 2009**, a worldwide technical student competition.

Service

- **Moderator** for the **CELAB reading group** (2014-15) at University of Michigan, a reading group that meets weekly to discuss recent papers from top-tier computer architecture conference.
- **Mentor** to **incoming graduate women** students at University of Michigan as part of ECSEL, a small group of women in Computer Science and Engineering.
- **Co-ordinator** and **Member** of **Debate Club** at College of Engineering Pune, India.
- **Volunteer** with Akanksha (2008-09); a non-profit organization working for **education of under-privileged kids**.