Shaizeen Aga

4844 BBB, University of Michigan
2260 Hayward, Ann Arbor
MI, USA 48109-2121.

shaizeen@umich.edu
www.shaizeen.com

Research Interests

- **Near data computing**
  My research has focussed on investigating novel ways to exploit near data computing to demonstrate its performance, energy and security benefits.
- **Parallel architecture and computing**
  I have worked on design and implementation of efficient memory models and runtimes for multi-core systems.

Work Experience

- **Graduate Student Research Assistant,** *University of Michigan, Ann Arbor* — January 2012 - Present
- **Intern,** *Qualcomm Research Silicon Valley* — May 2014- August 2014
- **Intern,** *Pacific Northwest National Laboratory* — June 2012- August 2012
- **Senior Technology Associate***, Morgan Stanley* — January 2011 - July 2011
- **Technology Associate***, Morgan Stanley* — January 2010 - December 2011
- **Intern***, NVIDIA Graphics Pvt Ltd* — June 2008 - March 2009

Teaching Experience

- **Graduate Student Instructor,** *University of Michigan, Ann Arbor* — Winter 2013, Winter 2014
  I taught Parallel Computer Architecture; a graduate course on recent advancements in parallel architectures.

Education

- **PhD.** Computer Engineering**, University of Michigan, Ann Arbor** — Expected 2017
- **Master of Science**, Computer Engineering, **University of Michigan, Ann Arbor** — May 2013
- **Bachelor of Technology**, Information Technology, **College of Engineering**, **Pune, India** — May 2009

Awards and Achievements

- Awarded 1st place at **University of Michigan CSE Graduate Students Honors Competition 2016** for outstanding research.
- Won **Parallel Computing Award** at **Imagine Cup 2009** (a worldwide student technical competition) organized by Microsoft.
- Recipient of **K.C. Mahindra & Bharat Petroleum Corporation Scholarship** for graduate studies.
- **Microsoft Student Partner** at College of Engineering, Pune, India.
- Recipient of **Dhirubhai Ambani Scholarship** for undergraduate studies.
- Winner of elocution competitions at school and national level.

Publications

[1] **Shaizeen Aga**, Supreet Jeloka, Arun Subramaniyan, Satish Narayanasamy, David Blaauw, and Reetuparna Das. Compute Caches for Efficient Very Large Vector Processing. *To appear in 23rd IEEE Symposium on High Performance Computer Architecture (**HPCA**), Austin, Texas, February 2017.*

[2] Abhayendra Singh**, Shaizeen Aga**, Satish Narayanasamy. Efficiently Enforcing Strong Memory Ordering in GPUs. *In International Symposium on Microarchitecture (**MICRO**), Waikiki, Hawaii, December 2015.*

[3] **Shaizeen Aga**, Sriram Krishnamoorthy, Satish Narayanasamy. CilkSpec: Optimistic Concurrency for Cilk. In International Conference for High Performance Computing, Networking, Storage and Analysis *(**SC**), Austin, TX, November 2015.*

[4] **Shaizeen Aga**, Abhayendra Singh, Satish Narayanasamy. zFence: Data-less Coherence for Efficient Fences. *In 29th International Conference on Supercomputing (**ICS**), Newport Beach, CA, June 2015.*

Research Projects

Following is the brief summary of some of my research projects.

- ***Graduate Student Research Assistant*** January 2012 - Present

  I am working with Prof. Satish Narayanasamy. Some of my projects here are:

Near data computing for efficiency and security: Near data computing is a paradigm where in computation is moved to where data is stored saving both energy and delay expended in moving data over deep memory hierarchies. My work introduces a novel way to perform near data computing by exposing processor caches as viable compute units. I demonstrate how computation in caches unlocks massive amounts of data parallelism and reduces data movement costs.

Further, I am also working on harnessing logic layer in 3D stacked memories to provide low overhead security guarantees.

Stronger memory models using efficient fences: While Sequential Consistency (SC) is the most intuitive memory model for multi-core machines, its concomitant overheads preclude its adoption. In this work, I designed and implemented an efficient fence design using which I showed SC overhead to be minimal.

- ***Intern,*** *Qualcomm Research Silicon Valley (QRSV)* May 2014- August 2014

  I worked here on programming mobile GPUs. I also worked on optimizing ray tracing application which is a heterogeneous benchmark harnessing both CPU and GPU. I optimized its CPU phase using algorithmic changes and ARM Neon instructions to attain 2-30X speedup. I also implemented an alternate algorithm which attained 40X speedup.

- ***Intern,*** *Pacific Northwest National Laboratory* June 2012- August 2012

  I worked here on improving the efficiency of Cilk multi-core runtime system. Cilk programming language makes it easy for programmers to express parallelism though for certain class of algorithms, synchronization in Cilk programs tends to be over-constrained leading to poor performance. By employing optimistic concurrency, I improved the performance of Cilk multithreaded runtime system by upto 1.9X.

- ***Senior Technology Associate****, Morgan Stanley* January 2011 - July 2011
- ***Technology Associate****, Morgan Stanley* January 2010 - December 2011

  My work here primarily involved design and development of a Data Warehouse. I was a key contributor to a major re-structuring project (reduced the data transformation and load cycle by 65%). I served as a mentor to a new undergraduate joinee to the team and was involved in hiring initiatives as well.

- ***Intern****, NVIDIA Graphics Pvt Ltd* June 2008 - March 2009

  I worked here on NVIDIA's parallel computing platform CUDA. I ported a True motion estimation algorithm on the CUDA platform.

Other Projects

- ***Speculatively relaxing memory model constraints by dynamic classification of cache blocks.***

  Using dynamic classification of cache blocks, I relaxed memory consistency model constraints to improve performance of Sequentially Consistent hardware. This project earned **top grade in Winter 2012 class of Parallel Computer Architecture** at University of Michigan.

- ***Design and implementation of P6 microarchitecture based core in Verilog.***

  I implemented the memory interface of the core (load/store queue, store buffer) and host of other components. I designed and implemented an **Adaptive Instruction Prefetcher** which gained us significant performance benefits. This project earned **top grade in Fall 2011 class of Computer Architecture** at University of Michigan.

- ***Parallel implementation of Maximum likelihood method of Phylogenetic Tree construction algorithm using Microsoft's Task Parallel Library.***

  Phylogenetic tree construction algorithms are crucial in the field of drug design. Using Microsoft's Task Parallel library, I improved the performance of computationally intensive Maximum Likelihood method of Phylogenetic tree construction. This project won **Parallel Computing Award** at **Microsoft's Imagine Cup 2009**, a worldwide technical student competition.