10-bit CMOS ADC*

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***Abstract*—Tremendous growth in VLSI industry due to open-source tool has paved way for better system design. This paper is on designing 10-Bit CMOS ADC for obtaining better resolution, speed, power and find a system which matches our preference.**

***Index Terms*—ADC, S/H circuit, SAR ADC, binary-weighted capacitive DAC array, dynamic comparator**

I. Introduction

Technology is increasingly moving towards system on chip design(SoC). This necessities the use of a more compact ADC. S/H circuit plays a key role in ADC design. Nyquise criteria is strictly followed for the reconstruction of signal, which states that sampling frequency is greater than twice the maximum frequency in a band-limited signal.

II. ADCs commonly used

Successive approximation type ADC– advantage: it requires only n clock cycle; zero latency
drawback:expensive; complexity in design.
Pipeline ADC– advantage: high resolution (10-13 bits) at a relatively fast speed.
drawback: first digital output appears after N clock delay; if imperceptible error seep into first stage, it propagates through the converter,it leads to a massive error in the result.

III. SAR ADC Architecture

Successive approximation type ADC work on the binary search algorithm. Whenever SAR switches ON, MSB is set. The DAC along with the shift register generates an approximate analog input signal. The output of DAC is fed to the comparator which compares the signal with a reference voltage. The output of the comparator is then fed to the logic circuit for farther manipulation(if Vin is greater than the Vref then the next bit is set and if Vin is less than Vref then the present bit is reset and the next bit is set). The result of every stage is stored in the code register. The process is repeated unless an EOC signal is generated and the digital output is read.

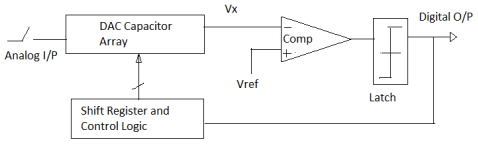

Fig. 1. SAR ADC block diagram [3]

IV. SAR circuit design consideration

For the circuit design, we are using differential architecture. DAC logic– It has synchronous SAR logic. It comprises of ring counter and code register. In the first clock cycle, the first D flip flop is set and sampling takes place.MSB is set in the second clock pulse. In code register for every clock pulse, one of the ring counter output set the D flip flop. At the final stage, an End of conversion signal is generated to read the bits from the code register.
Dynamic comparator– It has two stage, a pre-amplifier stage followed by a two-stage NAND type SR latch. During the reset phase, when the clock pulse is low,the latch is turned off. At the rising edge, first stage is turn ON and the transistor gets discharge. When either of the first stage transistor's voltage drops below supply voltage, amplification takes place and positive feedback occurs. The output of the first stage finally latched and fed to shift registers.
Capacitive DAC– It enables sampling of an input signal and generate an error signal(the difference between an input voltage and digital approximated voltage)
Sampling switch– It is made of transmission gates with low on-resistance to reduce voltage drop

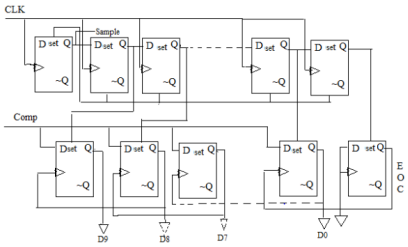

Fig. 2. DAC control logic block [3]

V. Conclusion

SAR ADC can be used for designing a 10-Bit ADC which has application in biomedical imaging and monitoring, optical communication, industrial process and many more.

References

[1] R. Jacob Baker, "CMOS circuit design, layout and simulation", 3rd edition.
[2] Indranil Sengupta, Dept.of CSE,IIT Kharagpur,"switching circuit and logic design", NPTEL lecture
[3] K. Yadav, P. Patra and A. Dutta, "A 43-nW 10-bit 1-kS/s SAR ADC in 180nm CMOS for biomedical applications,"IEEE Conference Paper .