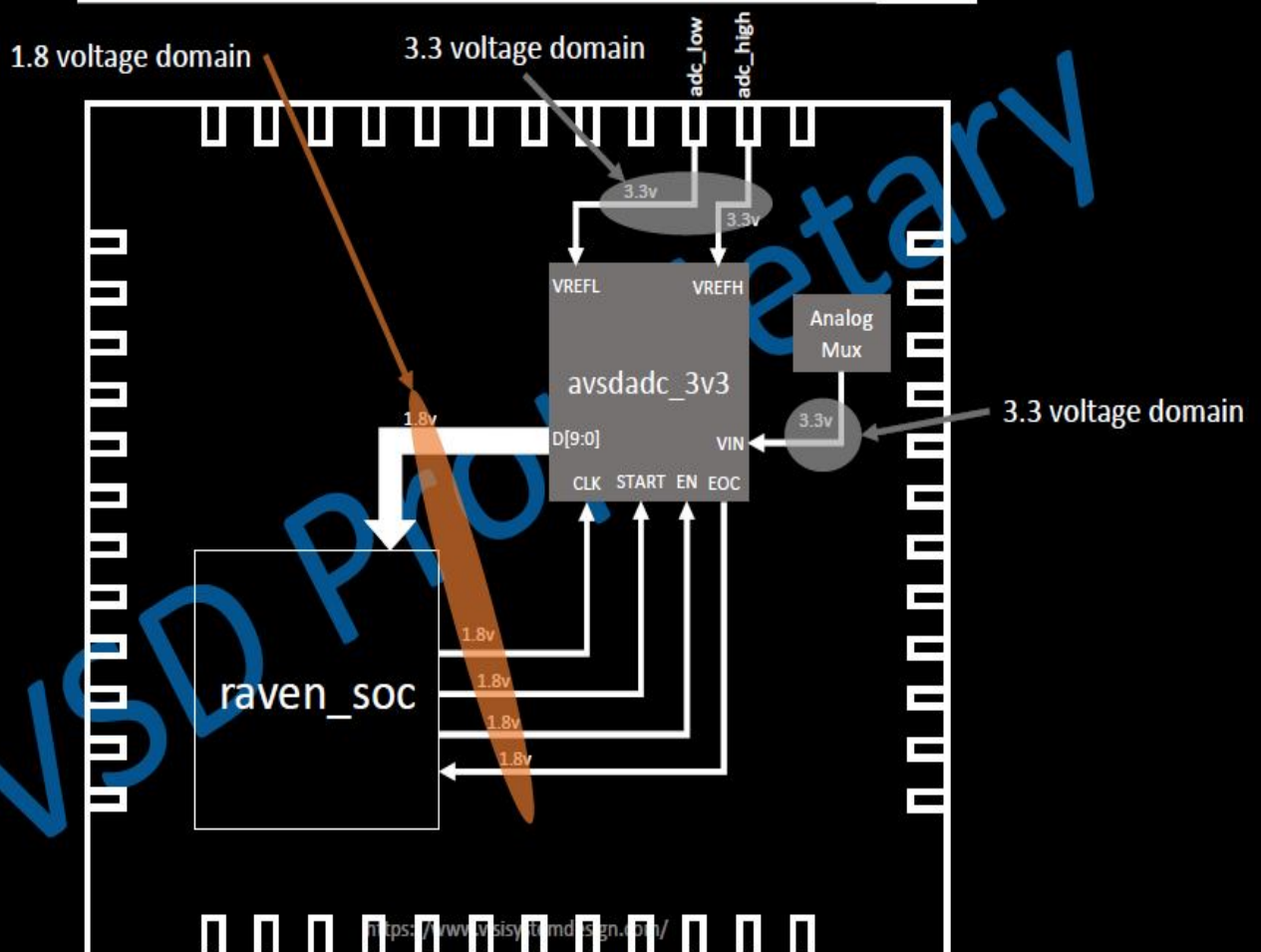


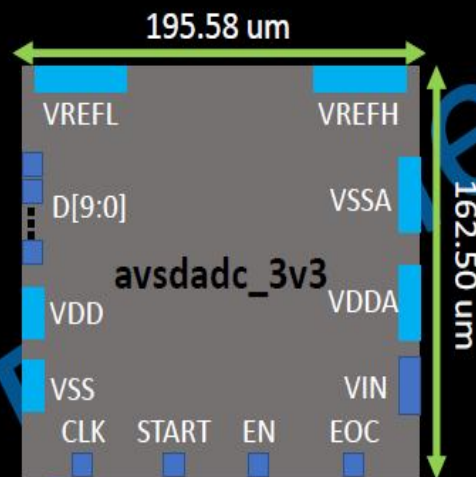
DISCLAIMER by VSD Corp. Pvt. Ltd.

- ADC (avsdadc_3v3) spec sheet for 180nm tech node
- Original Specs from XFAB and Recreated by VSD Corp. Pvt. Ltd.
- To be used only for Educational purposes
- Please contact Kunal at kunalpghosh@gmail.com in case of any doubts

Application Note for adc (avsdadc_3v3)



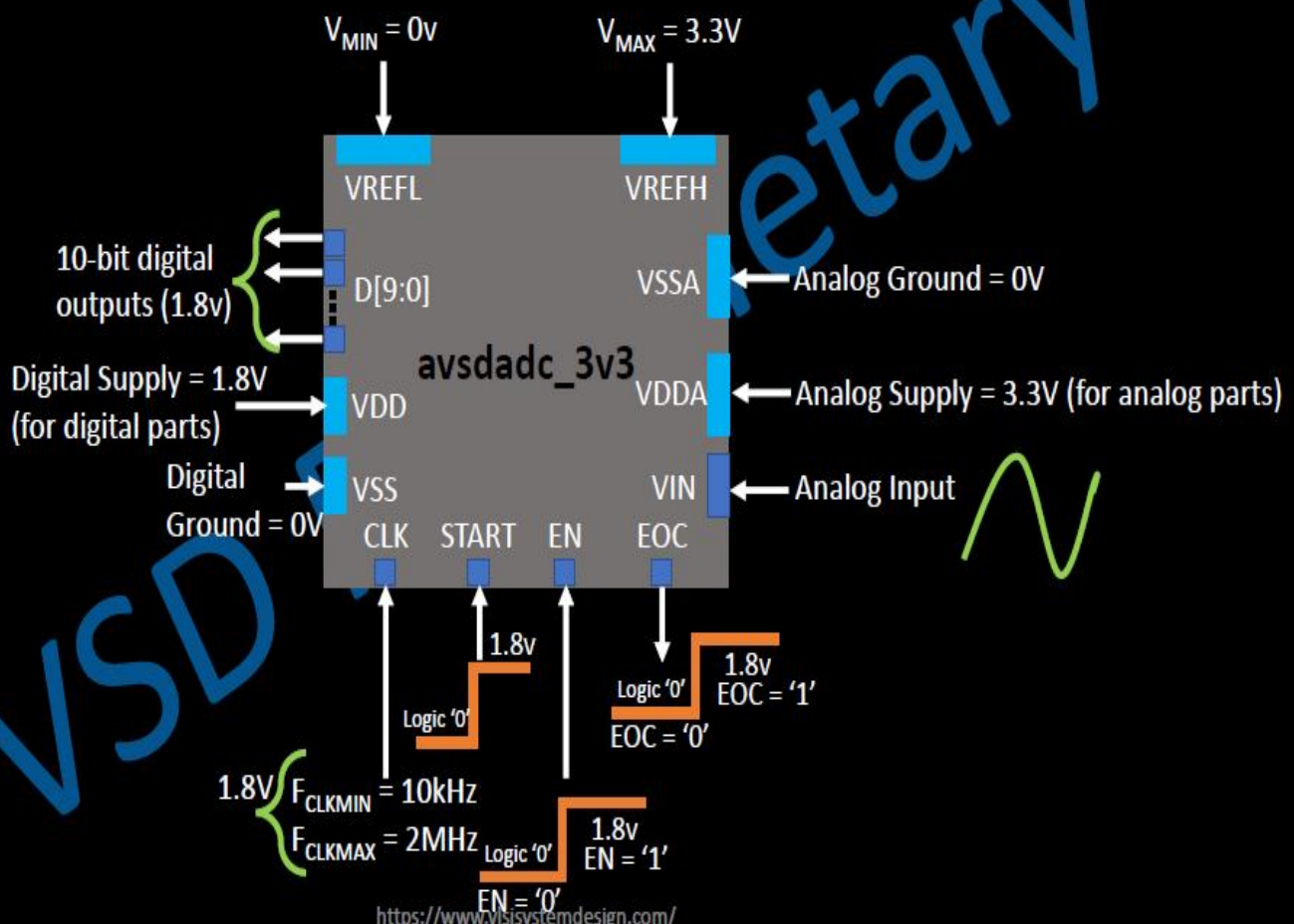
avsdadc_3v3 preferred dimensions, pin locations and metal layers



- D[9-0], EN, EOC, CLK, START pins (metal3) – 0.28um x 0.28um
- VDDA, VSSA pins (metal2) – 0.4um x 3um
- VREFL, VREFH pins (metal2) – 9.48um x 0.4um
- VDD, VSS pins (metal2) – 0.4um x 1.5um

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avsdadc_3v3 operating modes



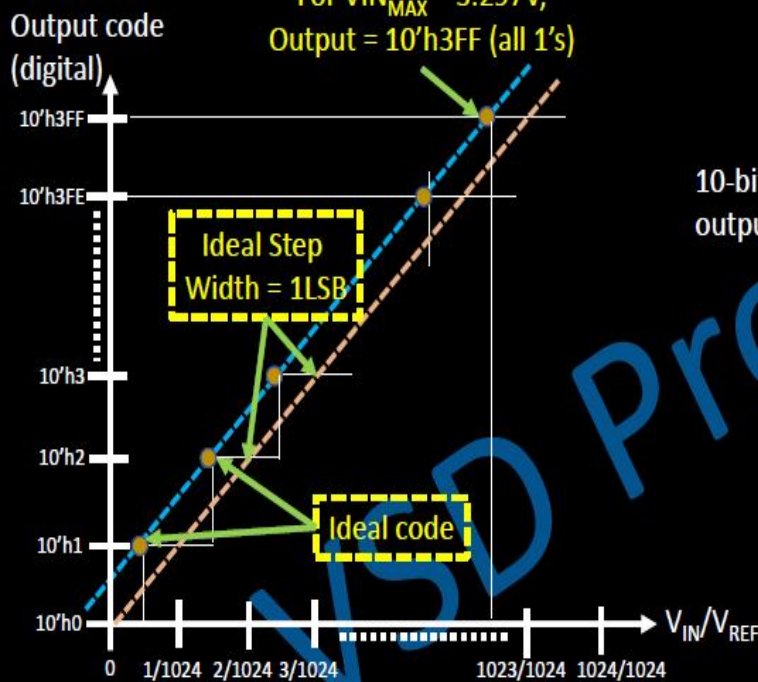
<https://www.vlsisystemdesign.com/>

avsdadc_3v3 operating modes (For $F_{CLK}=1\text{MHz}$)

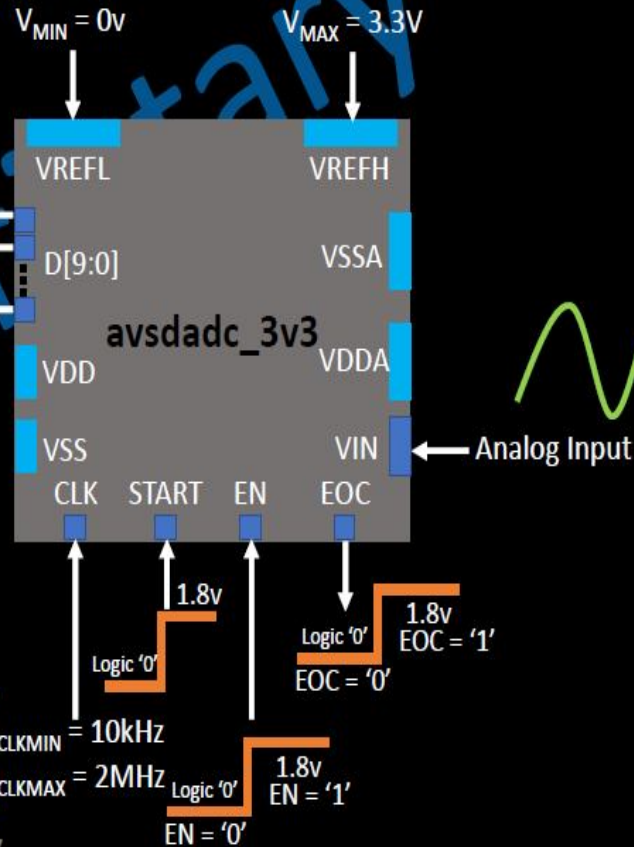
$$1\text{LSB} = 0.00322\text{V or } 3.2\text{mV} (1\text{LSB} = V_{REF}/2^N)$$

$$\text{Resolution} = 10\text{bits (For } V_{REF}=3.3\text{V)}$$

For $V_{IN_MAX} = 3.297\text{V}$,
Output = $10'h3FF$ (all 1's)



10-bit digital
outputs (1.8v)



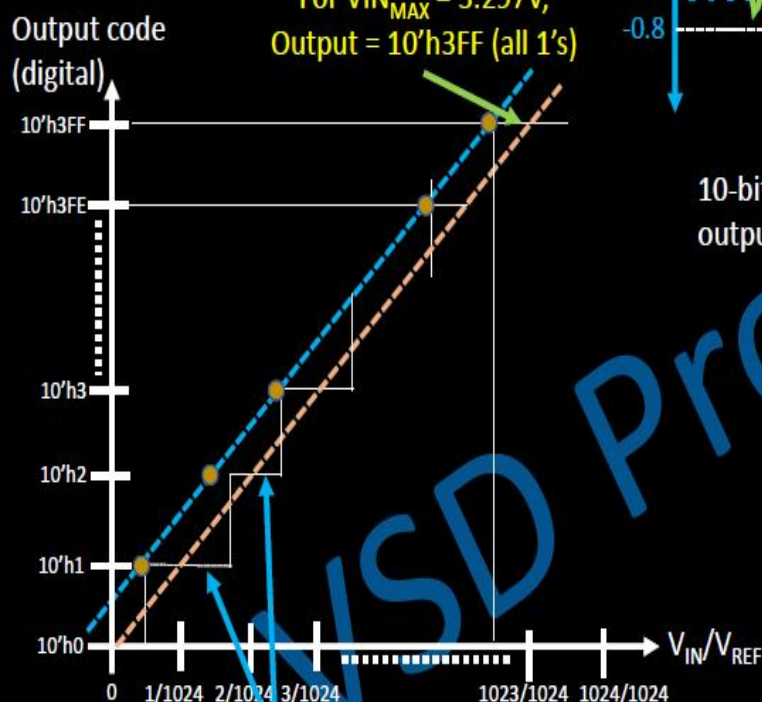
<https://www.vlsisystemdesign.com/>

avsdadc_3v3 operating modes (For $F_{CLK}=1\text{MHz}$)

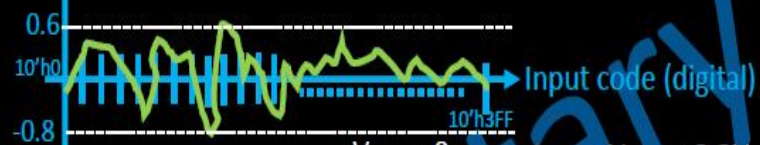
$$\text{Differential nonlinearity (DNL)} = 0.8\text{LSB}$$

$$\text{DNL} = \text{Actual step width} - \text{Ideal step width}$$

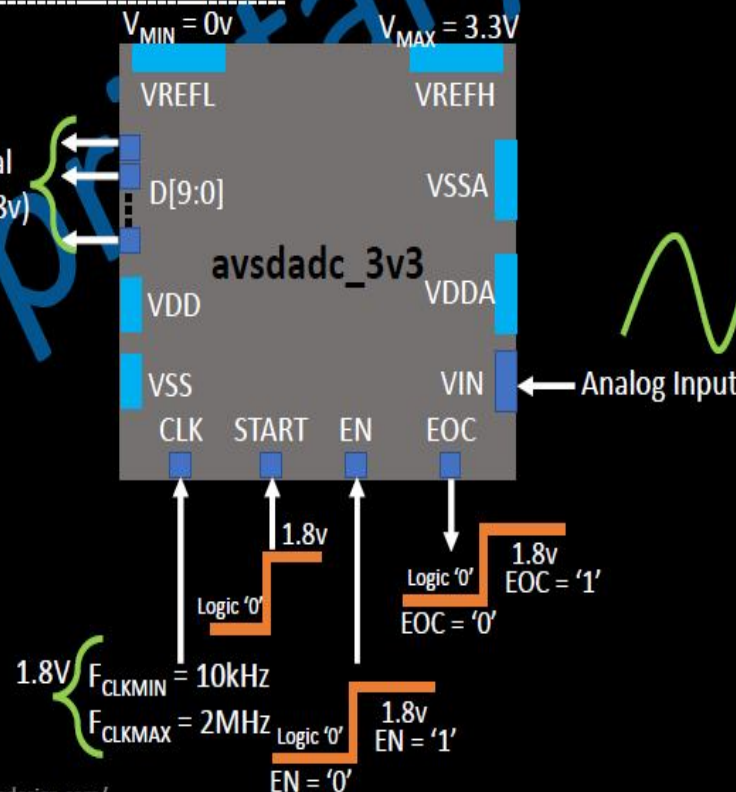
For $V_{IN_MAX} = 3.297\text{V}$,
Output = $10'h3FF$ (all 1's)



DNL (LSBs)



10-bit digital
outputs (1.8v)



<https://www.vlsisystemdesign.com/>

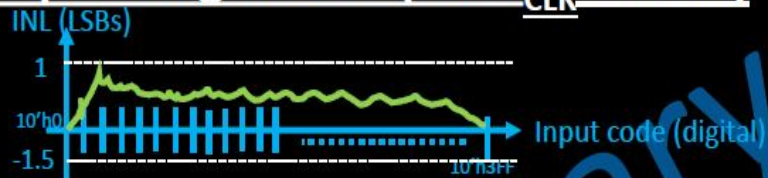
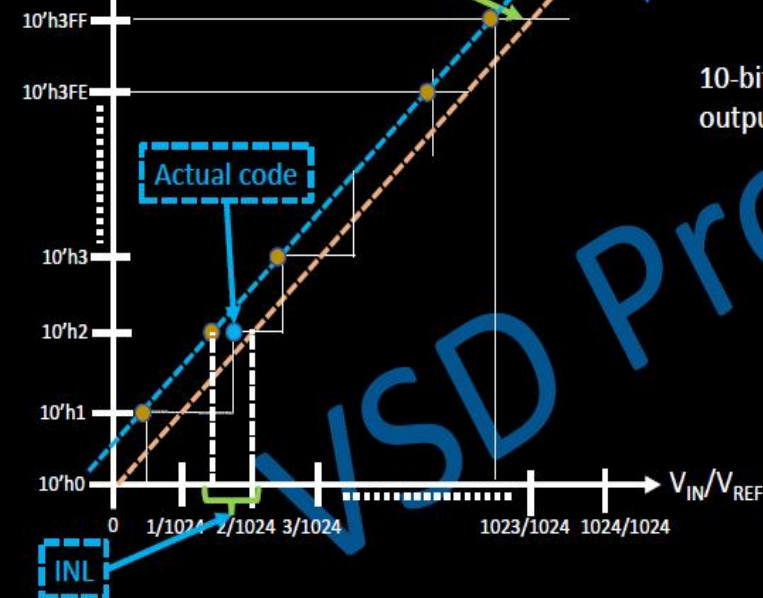
avsdadc_3v3 operating modes (For $F_{CLK}=1\text{MHz}$)

Integral nonlinearity (INL) = 1.5LSB

INL = Actual code - Reference code

For $V_{IN_MAX} = 3.297\text{V}$,
Output = $10'h3FF$ (all 1's)

Output code (digital)



10-bit digital outputs (1.8v)

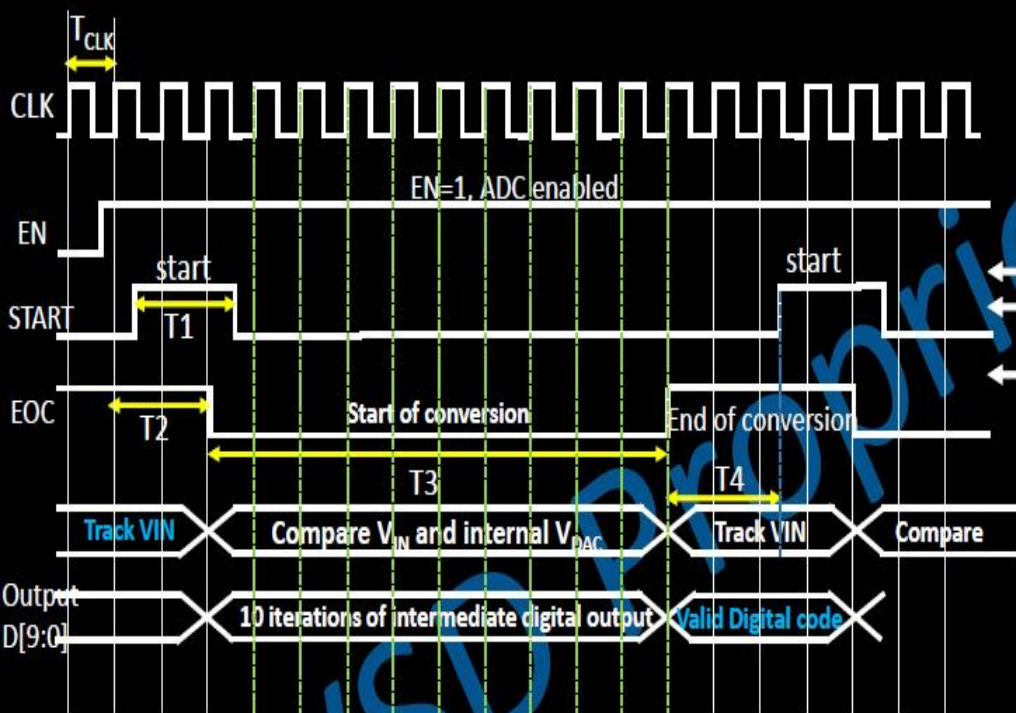


1.8V $F_{CLKMIN} = 10\text{kHz}$
1.8V $F_{CLKMAX} = 2\text{MHz}$
Logic '0' EN = '0'

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avsdadc_3v3 operating modes (For $F_{CLK}=1\text{MHz}$)

Total conversion time = SAR prep time (2 clock cycles) + Conversion time (10 clock cycles)

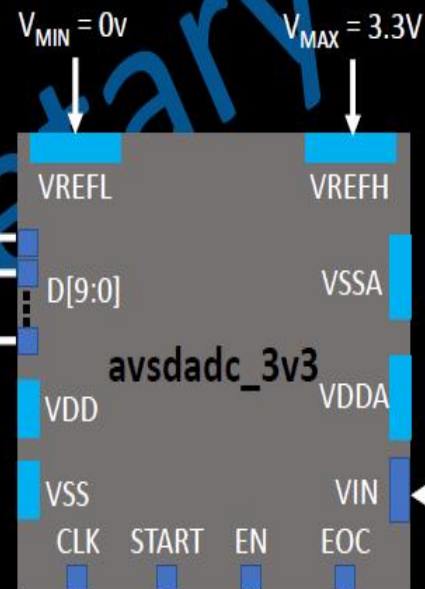


T_1 = START signal duration min 2 clock cycles

T_2 = SAR preparation time is up to 2 clock cycles

T_3 = Conversion time is 10 clock cycles

T_4 = At least 1us needed to track V_{IN}



1.8V $F_{CLKMIN} = 10\text{kHz}$
1.8V $F_{CLKMAX} = 2\text{MHz}$
Logic '0' EN = '1'

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avsdadc_3v3 plots and values needed

- 1) DNL vs Digital code at $V_{REF}=V_{DD}=3.3V$; $F_{CLK}=2MHz$ and $T=20C$
- 2) INL vs Digital code at $V_{REF}=V_{DD}=3.3V$; $F_{CLK}=2MHz$ and $T=20C$
- 3) DNL vs Digital code at $V_{REF}=1.25V$, $V_{DD}=3.3V$; $F_{CLK}=2MHz$ & $1MHz$ and $T=20C$
- 4) INL vs Digital code at $V_{REF}=1.25V$, $V_{DD}=3.3V$; $F_{CLK}=2MHz$ & $1MHz$ and $T=20C$