MINISTRY OF SCIENCE AND HIGHER EDUCATION OF THE RUSSIAN FEDERATION

FEDERAL STATE AUTONOMOUS EDUCATIONAL INSTITUTION OF HIGHER EDUCATION

"NOVOSIBIRSK NATIONAL RESEARCH UNIVERSITY STATE UNIVERSITY"

(NOVOSIBIRSK STATE UNIVERSITY, NSU)

15.03.06 - Mechatronics and Robotics Focus (profile): Artificial intelligence

TERM PAPER

Nazarov Danila Alekseevich Kalugina Anastasia Vladimirovna

The theme of the paper:

"The game of Life"

Contents

1.	Introduction	3
2.	Analogues	
3.	Problem statement and division into subtasks	5
4.	Hardware	ϵ
5.	Software	14
6.	Conclusion	18
7.	Sources	19

Introduction

Games are quite in demand in the 21st century, and more and more people are immersed in them. But very few people think about how they work from the inside. And in order to create a game, you need to understand it. Your own implementation of the game will help to understand this.

We chose "The game of life" as the theme of the project. In previous years there was no such theme, so we became interested in implementing this game. In addition, the documentation for the project is given in Russian).

Rules:

- Any "living" cell with less than two "living" neighbors dies, as if caused by an insufficient population;
- Any "living" cell with two or three "living" neighbors lives on for the next generation;
- Any "living" cell with more than three "living" neighbors is dying, as if due to overpopulation;
- Any "dead" cell that has exactly three "living" neighbors becomes a "living" cell by reproduction.

The games stops if:

- There will not be a single "living" cell left on the field;
- The configuration in the next step will repeat itself exactly (without shifts and rotations) in one of the earlier steps (a periodic configuration is formed);
- At the next step none of the cells changes its state (a special case of the previous rule, a stable configuration is formed).

The player does not actively participate in the game. He only arranges or generates the initial configuration of "living" cells, which then change according to the rules. Despite the simplicity of the rules, a huge variety of shapes can arise in the game.

Analogues

"The game of Life" is not as popular a game as tanks or tennis, but it is the most interesting. The main task is to set up such a configuration at the beginning so that at the end of each epoch there are still living cells that can continue the lineage. (figure 1).

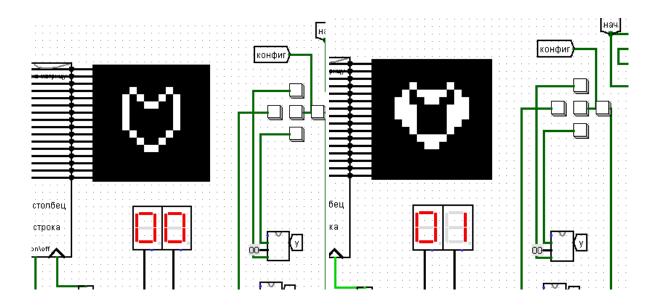


Figure 1 – The birth of a new "living" cell

But there are cases where after a few epochs there may be no living cells left at all and they will die of loneliness. (figure 2).

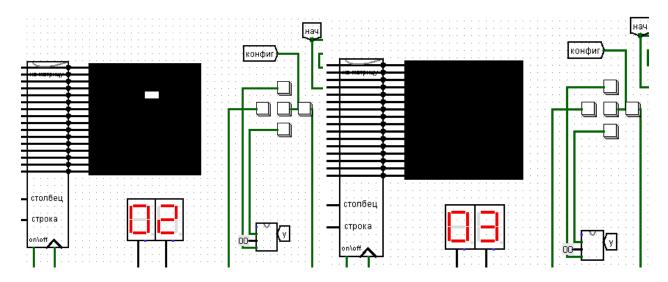


Figure 2 – The cell "dies" because of loneliness

Problem statement and division into subtasks

In order to implement all of the above, we have set tasks that will lead to the realization of "The game of Life".

Tasks:

- 1. Simulation of the device, which is built on logic circuits in the program Logisim;
- 2. Using and connecting to the CDM-8 processor circuitry.

For a clear understanding of all stages of work, we have divided tasks into subtasks.

Subtasks:

- 1. Dividing the game implementation into Hardware and Software parts;
- 2. Hardware design and implementation;
- 3. Development and implementation of the Software;
- 4. Checking Software and Hardware collaboration;
- 5. Fixing bugs and optimizing the game (if it's possible).

Hardware

Start screen

We have implemented the game (figure 3). The player sees the control buttons, the check button and the field of 16x16. The edges of the field are connected to each other as if they were "stitched".

There are two circuits connected to the matrix, which are responsible for memory and buffer. They are used to write to the cells and output to the matrix. The circuit closest to the matrix is responsible for blinking red of the cell where the player is at the moment. The location of the live cell and its state can be selected using the controls on the right side of the playing field. After setting the initial configuration, the player can start the game by clicking on the button to the right of the navigation. The process will be started.

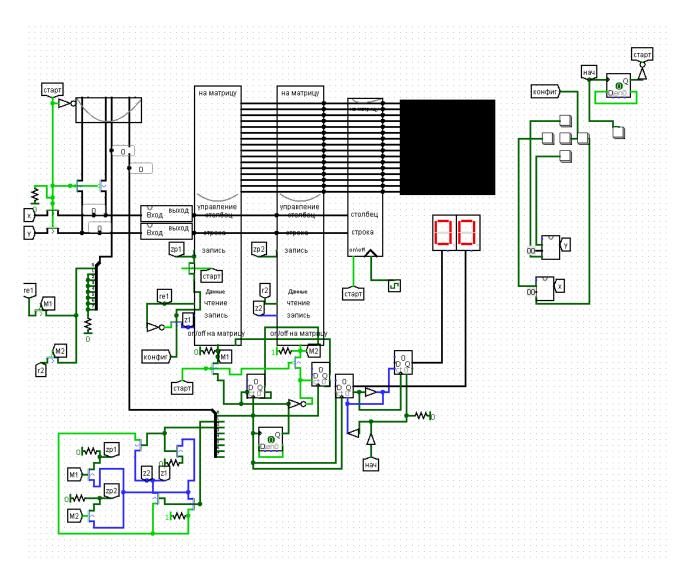


Figure 3 – startup screen

CDM

Here is an implementation of CDM. When an attempt is made to write something to RAM, Hardware intercepts communication with the CDM and RAM. Then certain cell addresses are assigned to the memory and as soon as the address on the address bus matches the address that is defined for a particular device, it appears as a memory cell for the CDM.

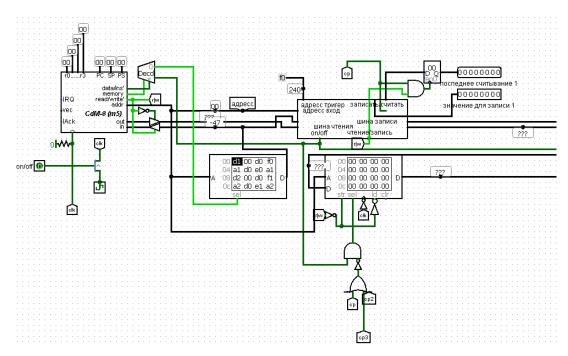


Figure 4 – first part of the CDM

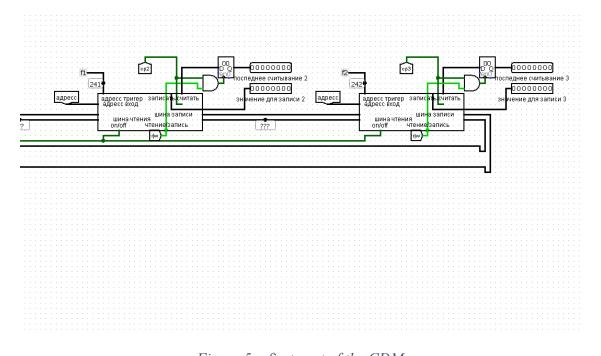


Figure 5 – first part of the CDM

Filed coordinated

In memory the values are stored by coordinates which we set manually at the beginning. They are set by columns and rows. The minimum coordinate value is (0;0) and the maximum is (15:15).

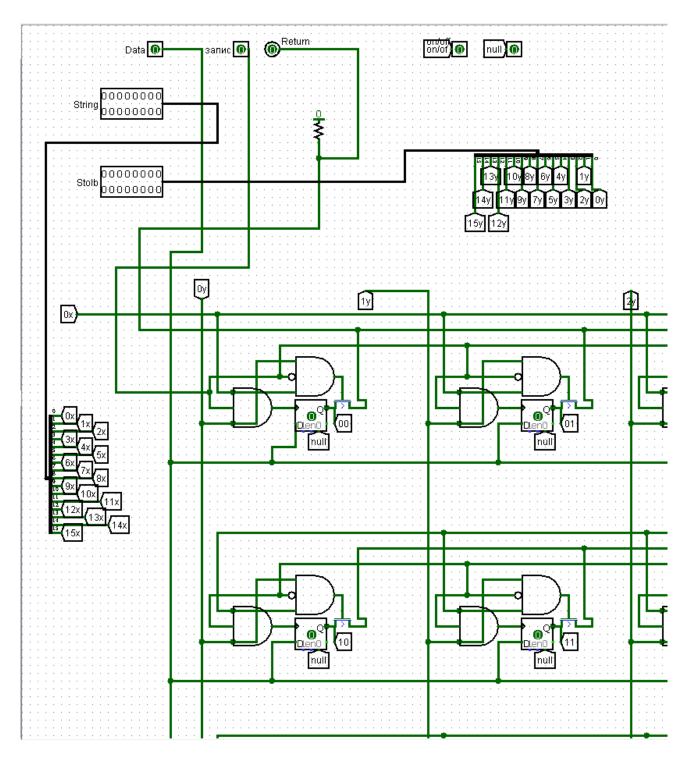


Figure 6 – the state of the field coordinates at the beginning

As an example, let's choose the initial coordinates. Let it be (0;0) (figure 7). In Data comes the value to be written to the memory cell. Record is the input to which the cycles come. On the rising cycle the value is written. And Return is where the value that is currently in the cell comes in.

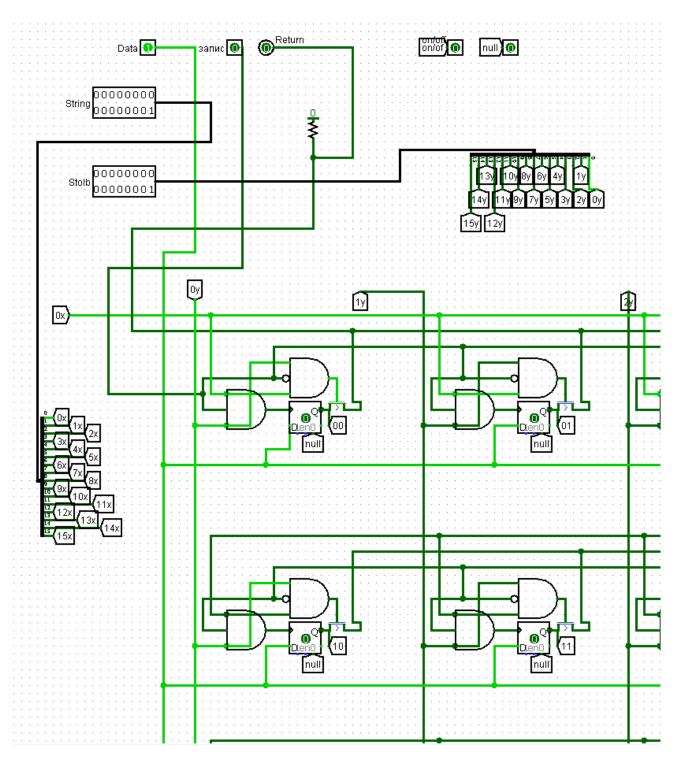


Figure 7 – ehe state of the field cell with the selected coordinate

Conversion from 8 bits to 16 for coordinates

For the correct operation of the game it is necessary to set the coordinate state by a hexadecimal number. In the diagram (figure 8) the number translation from octal to hexadecimal number system is realized.

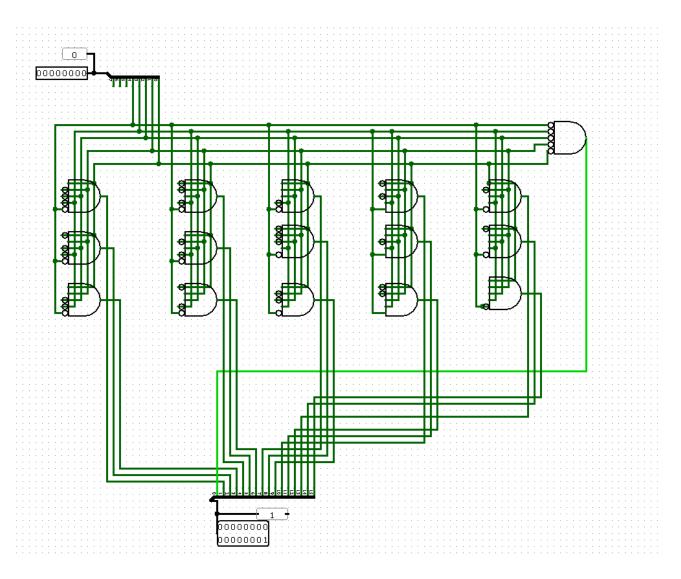


Figure 8 – conversion from octal to hexadecimal

Flashing of the selected cell in red

Flashing a square in red only works when the game is not running. Each "square" is responsible for a cell specified by coordinates. When the beat is 0, no error is caused (figures 9 and 10). When the measure becomes 1, an error occurs and the square becomes red (figures 11 and 12). Since the measures change, the state of the cell will also change.

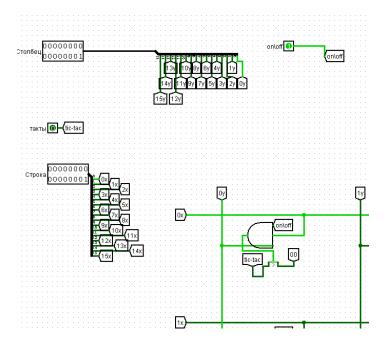


Figure 9 – the cycle is 0

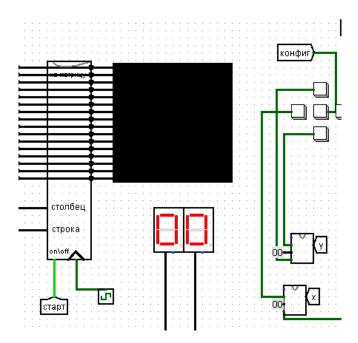


Figure 10 - the state of the cell when the cycle is 0

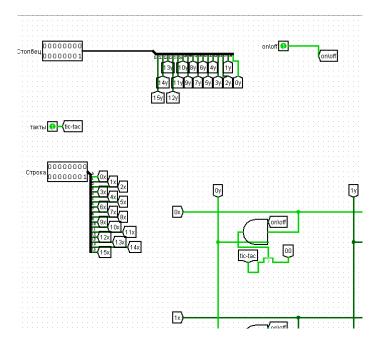


Figure 10 – the tact equals 1

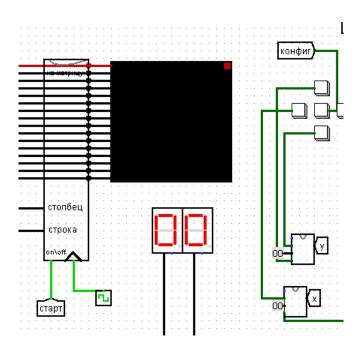


Figure 11 - cell state when the cycle is 1

There are 3 buses from the CDM and the address given to the device. If the device address and the address on the bus match, the transistors lock the bus. They then check to see if it is a read or write. They then write data to the CDM that came to the device or write data to the device from the CDM.

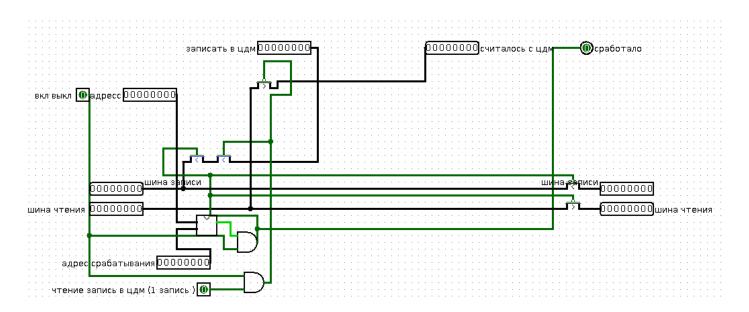


Figure 12 - work with CDM

Software

This part of the project is implemented with the CocoIDE development environment. It is based on the Assembler programming language, which is designed to write instructions on the Harvard architecture for the CdM-8 processor from the CdM-8-mark-5-banks library.

Our code starts by assigning memory locations to variables (figure 13). The first 4 lines are the memory cells to which the hard devices are bound.

Then we start the enumeration of cells (figure 14). In the first iteration it zeroes in on X and Y, and in subsequent iterations it only zeroes in on X. It also records the coordinates of the current cell in the X and Y variables, and records the state of that cell (alive or dead) in the "sost" variable.

```
asect
                                       0x00
     asect 0xf0
                          23
                               start:
2
     yadr: ds l
                          24
                               ldi r1, 0
3
     xadr: ds 1
                          25
                               ##ldc r1, r1
4
     ypradr: ds 1
                          26
                               parsy:
5
     asect 0xe0
                          27
                               ldi r0, yadr #r1 y
     y: ds l
                          28
                               st r0, r1
7
     x: ds l
                          29
                               ldi r0, y
                          30
                               st r0, r1
     ypl: ds l
                          31
                               #ld r1, r2 #r1 y
     xpl: ds 1
                          32
                               ldi r2, 0
10
     ymi: ds 1
                          33
                               ##1dc r1, r1
11
     sost:ds 1
                          34
                               parsx:
12
     sums: ds 1
                          35
                               ldi r0, xadr
13
     #razm: ds 1
                          36
                               st r0, r2
                                           #r2 x
14
     sum: ds 1
                          37
                               ldi r0, x
15
                          38
     schx:ds 1
                               st r0, r2
                          39
16
     schy: ds 1
                               ldi r0, 0
                          40
                               ldi r3, sums
17
     #asect Oxfc
                          41
                               st r3, r0
18
     #xmax: dc 15
                          42
                               ldi r3, xadr
19
     #ymax: dc 15
                          43
                               ld r3, r3 #r3 sost
20
     #xstart: dc 0
                          44
                               ldi r0, sost
21
     #ystart: dc 0
                          45
                               st r0, r3
```

Figure 13, 14 - variable labels

These parts are responsible for enumerating the neighbors of a cell (figure 15). They find neighbor coordinates while checking for edges. For example, if the current cell has a Y coordinate of 15, then its Y+1 coordinate will be 0. This is how the edges are "stitched" together.

```
67
46
                                   47
    if
                               68
                                   if
                                                                     if
                                                                                       ldi r3, y
48
    tst r1
                               69
                                   ldi r3, 15
                                                                     tst r2
                                                                                      jsr extra
49
    is eq
                               70
                                   ##1dc r3, r3
                                                                     is eq
                                                                                      ldi r0, 15
                                                                        ldi r0, 15
50
                               71
                                   cmp r1, r3
51
       ##1dc r3, r0
                               72
                                   is eq
                                                                        ##1dc r3, r0
                                                                                      112 ldi r3, ymi
52
       ldi r3, yadr
                               73
                                       ldi r0, 0
                                                                        ldi r3, xadr
                                                                                      113 jsr extra
53
       st r3, r0
                               74
                                       ldi r3, yadr
                                                                        st r3, r0
54
       ldi r3, ymi
                               75
                                       st r3, r0
                                                                    else
                                                                                     ########## x+1
55
       st r3, r0
                               76
                                       ldi r3, ypl
                                                                        ldi r3, x
                                                                                     if
56
    else
                               77
                                       st r3, r0
                                                                        ld r3, r0
                                                                                     ldi r3, 15
57
       ldi r3, y
                               78
                                                                        dec r0
                                                                                      ##1dc r3, r3
58
                                                                        ldi r3, xadr
       ld r3, r0
                               79
                                       ldi r3, y
                                                                                      cmp r2, r3
59
       ldi r3, yadr
                               80
                                       ld r3, r0
                                                                        st r3, r0
                                                                                      is eq
60
       dec r0
                               81
                                       ldi r3, yadr
                                                                                        ldi r0, 0
       st r3, r0
61
                               82
                                       inc r0
                                                                                         ldi r3, xadr
62
       ldi r3, ymi
                               83
                                       st r3, r0
                                                                                         st r3, r0
63
       st r3, r0
                               84
                                       ldi r3, ypl
                                                                                      else
64 fi
                               85
                                       st r3, r0
                                                                                         ldi r3, x
                               86 fi
                                                                                         ld r3, r0
136 ########## y +1
                                                                                         inc r0
137 ldi r3, ypl
                                                                                         ldi r3, xadr
138 jsr extra
                                                                                         st r3, r0
                                                                                      ldi r3, xpl
141 ########## y
142 ldi r3, y
                                                                                      st r3, r0
143 jsr extra
```

Figure 15 - search for neighbors' coordinates

These parts are used to check the state of the cell neighbors (figure 16). If the neighbor is alive, they increment the variable sums.

```
prov:
229
     ldi r3, xadr
230
231
     ld r3, r0
     if
232
     tst r0
233
     is ne
234
235
         ldi r3, sums
         ld r3, r0
236
         inc r0
237
         st r3, r0
238
     fi
239
240
     rts
###########
jsr prov
#############
```

Figure 16 - neighborhood check

Here we optimized the code to fit into memory (figure 17).

```
216 extra:
217 ld r3, r3
218 ldi r0, yadr
219 st r0, r3
220 rts
221
222 extraq:
223 ldi r3, ypradr
224 st r3, r0
225 ldi r0, 0b000000000
226 st r3, r0
227 rts
```

Figure 17 - code optimization

A cell becomes alive if its number of neighbors and current state satisfy the rules of cell life (figure 18).

This is where it goes to the next iteration of the cell enumeration. If all the cells have already been searched, it sends a signal to change the fields and clear the field to be written, and then starts the enumeration again (figure 19).

```
******
146 #######################
                                         sled:
147
    ldi r0, x
                                         #pop r1
148
    ld r0, r0
                                         if
149
    ldi r3, xadr
                                         ldi r0, 15
150
    st r3, r0
                                         ##1dc r0, r0
151
    ldi r0, sost
152
    ld r0, r0
                                         cmp r0, r2
153
    ldi r3, sums
                                         is eq
154
    ld r3, r3
                                             if
155
    #push r1
                                             ldi r0, 15
156
    if
                                             ##1dc r0, r0
157
    tst r0
                                             cmp r0, r1
158
    is ne
                                             is eq
159
        if
                                                 br fin
160
        ldi r0, 2
                                             else
161
        cmp r0, r3
                                                 ldi r3, ypl
162
        is eq
                                                 ld r3, r1
163
            ldi r0, 0b00000010
                                                 br parsy
164
            jsr extraq
                                             fi
165
        else
                                         else
166
            if
167
                                             ldi r3, xpl
            ldi r0, 3
168
            cmp r0, r3
                                             ld r3, r2
169
            is eq
                                             br parsx
170
                ldi r0, 0b00000010
                                         fi
171
                jsr extraq
                                         fin:
172
            else
                                         ldi r0, 0b00000001
173
                br sled
                                         jsr extraq
174
            fi
                                         br start
175
        fi
```

Figure 18, 19 - "birth" of a cell, go through the cells

Conclusion

The result of this work was the implementation of the "Game of Life". We implemented the project with the help of logic circuits, which we created in the program Logisim, and wrote the software in the programming language Assembler in the development environment CocoIDE.

In the process of implementing the project, we were able to understand how our game works from the inside. Thanks to this we fixed some bugs and errors that were either preventing our game from working or slowing it down.

By implementing the project, we have improved our programming skills and our understanding of circuitry. Also, it is an invaluable experience that will stay with us forever.

Sources

http://www.cburch.com/logisim/docs/2.7/ru/html/libs/index.html
http://www.ccfit.nsu.ru/~fat/