CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Telecommunication Engineering

VLSI Technology Sessional

ETE 404

Experiment No:03

Design and Performance Analysis of an Inverter Using Cadence Virtuoso

---

Submitted by:

Shamanza Chowdhury

ID: 1908008

Submitted to:

Arif Istiaque Rupom

Lecturer

Dept. of ETE,CUET

June 2, 2024

1 Objectives:

- To familiarize with Cadence tools and library creation.
- To familiarize with inverter design and implementation.
- To familiarize with transient analysis and performance measurements.

2 Apparatus:

- **Software:** VMware Workstation v10
- **Hardware:** PC

3 Design Process:

3.1 Opening Cadence:

- VMware Workstation 10 had launched from the start menu.
- Then **"Open a Virtual Machine"** had been selected where the **Cadence.vmx** file had located from our storage media.
- The configuration had been changed as needed and started the VM, selecting "I Copied It" when prompted.

3.2 Starting Virtuoso:

- The **"Terminal"** was started from the home screen.
- To bring up the Command Interpreter Window (CIW).**"Virtuoso"** was typed and entered.

3.3 Creating and Attaching Library:

- To create new library, **File** $>$ **New** $>$ **Library** was executed in the Command Interpreter Window (CIW).
- The name **"vlsi3_4"** was entered in the 'New Library' form.
- **"Attach to an existing technology library"** was selected, and then OK was clicked.
- Then **gpdk090** technology library was chosen and confirmed.

3.4 Schematic Entry:

3.4.1 Creating New Cellview:

- In the CIW, **File** $>$ **New** $>$ **Cellview** was executed.
- The **'New File'** form was set up with **Library**: 'vlsi3_4', **Cell**:'inverter', **View**: 'schematic', **Type**: 'schematic', **Open with**: 'Schematics L'.

3.4.2 Creating Instances:

- In the Virtuoso schematic editor window, **Create** $>$ **Instance** was executed (or the shortcut key "**i**" was used).
- To select a library component, **"Browse"** was clicked from where **Library:**"gpdk090", **Cell:**"nmos1v", **View:**" symbol" was chosen and the component was placed.
- After the form is completed, the cursor is moved to the schematic window and the left mouse button is clicked to place the component.

- After entering the components, the '**Create Instance**' form is canceled or Esc is pressed while the cursor is in the schematic window.
- The pmos1v cell was similarly added.
- If a component is placed in the wrong location, **'m'** is pressed, the component is clicked to select it, and the mouse is moved to reposition it.

3.4.3 Editing Properties of the Components:

- The sizes of the transistors can be adjusted by editing instance properties.
- The NMOS is selected with a left click, and its properties are modified by pressing **"q"** or executing **Edit** $>$ **Properties** $>$ **Object** in the schematic editor window. The Library Name, Cell Name, and property values are updated as each component is placed.
- For NMOS, the Total Width is set to 240n, and pressing **'Tab'** sets the Finger Width to the same value. For PMOS, the Total Width and Finger Width are set to 480n.
- To deselect any object, **"ctrl+d"** is pressed.

3.4.4 Adding Power Nets:

- Power nets (vdd and gnd) were instantiated from **'analogLib'** library.

3.4.5 Adding Pins:

- **Create** $>$ **Pin** was executed or **'p'** was pressed on the keyboard to add pins for input as **'in'** and output as'**out'** with the appropriate directions.

3.4.6 Wiring the Schematic:

- **Add** $>$ **Wire** was used or **'w'** was pressed to enter wiring mode and connect the components. The work was saved periodically.

3.4.7 Checking and Saving:

- Check and Save was clicked, and the CIW was checked for errors or warnings.
- There were no significant errors, only some license warnings which were ignored.

The schematic diagram of a inverter is given below:

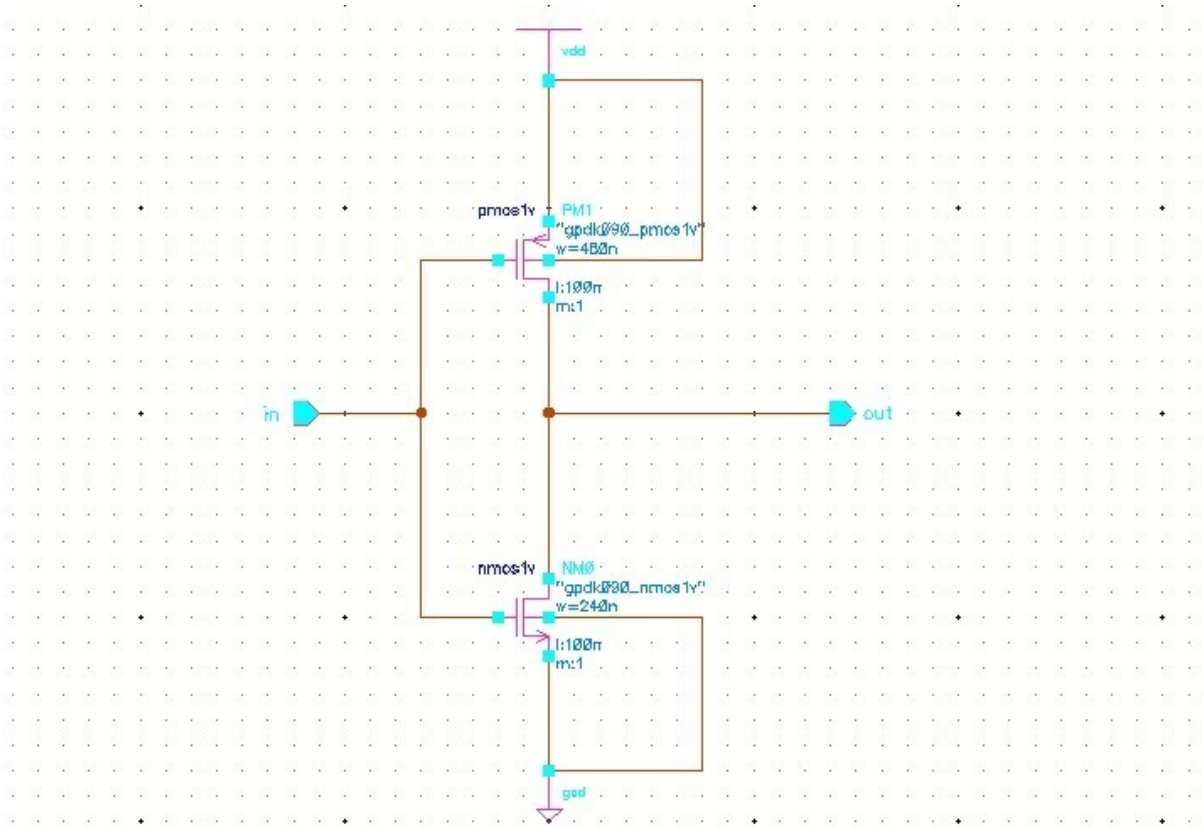

Figure 1: Schematic diagram of a inverter .

3.5 Netlist and Simulation:

3.5.1 Launching ADE L:

- In the Schematic editor window, **Launch** > **ADE L.** was executed and the Analog Design Environment (ADE) L window was arrived.

3.5.2 Setting Up Model Libraries:

- **Setup**>**Model Libraries** was executed, **'gpdk090_mos.scs'** was selected, and the section **'TT_s1v'** was chosen.

3.5.3 Assigning Signals:

- **Setup** > **Stimuli** was executed to assign signals to the inverter pins.
- **'Global Sources'** is selected, revealing the global power net vdd!.
- **'Enabled'** is clicked, **'dc'** is selected under Function, and **'Voltage'** is selected under Type. A value of **'1.2'** is entered in the DC voltage box.

- The form for '**vdd!**' is filled out accordingly and Apply is clicked (clicking OK would close the window and require it to be reopened to set up inputsand configuring a pulse waveform for the input pin 'in'.)
- For the input pin **'in'**, a pulse waveform needs to be set.
- In the Setup Analog Stimuli window, Inputs are selected.
- Enabled is clicked, and Function is set to **'pulse'** with Type as **'Voltage'**. Parameters for the pulse source are as follows: **Voltage1 = 0V**, **Voltage2 = 1.2V, Period = 40n, Delay time = 3n, Rise time = 3n, Fall time = 3n, Pulse width = 20n.**
- Apply is clicked, followed by OK.

3.5.4 Choosing Analysis:

- **Transient (tran)** analysis was selected with a stop time of 100n.

3.5.5 Selecting Outputs:

- **Outputs** > **To be plotted** > **Select on Design** was executed, and **'out'** and **'in'** were chosen.

3.5.6 Saving Design Settings:

- Design settings were saved by executing **Session** > **Save State.**

3.5.7 Running Simulation:

- **Simulation**>**Netlist and Run** was executed, successfully running the simulation and displaying the output in the Virtuoso Visualization & Analysis XL window.

The simulation output of a inverter is given below:

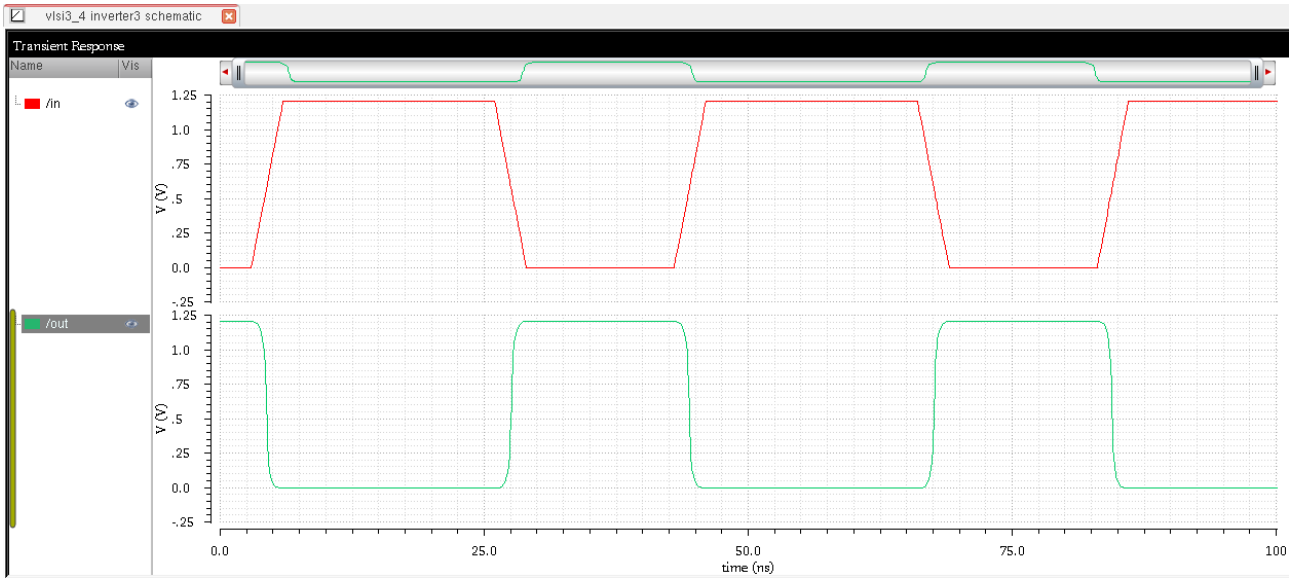

Figure 2: Output of a inverter .

3.6 Measurement:

The three primary timing parameters associated with CMOS devices—rise time, fall time, and propagation delay—are typically discussed using the system response of an inverter. To measure these parameters and perform various waveform calculations, the Waveform Calculator in the **Virtuoso Visualization & Analysis X**L window can be utilized by executing **Tools** > **Calculator**

3.6.1 Propagation Delay Measurement:

Propagation delay refers to the time difference between approximately 50% of the input transition and approximately 50% of the output transition.

- The 'vt' is selected. In the Schematic editor window, the input node 'in' is clicked, resulting in the appearance of an expression (e.g., VT("/in")).
- In the Function Panel, **'Special functions**' is selected, and **'delay'** is chosen.
- This time Signal1 and Signal2 was **VT("/in")** and **VT("/out")**
- Threshold value 1 and 2 should be 0.6 (50% of 1.2 V supply) and 0.6 (50% of 1.2 V supply) respectively.
- By clicking the Evaluate the buffer icon,the propagation delay was found.

The measurement of propagation delay a inverter is given below:

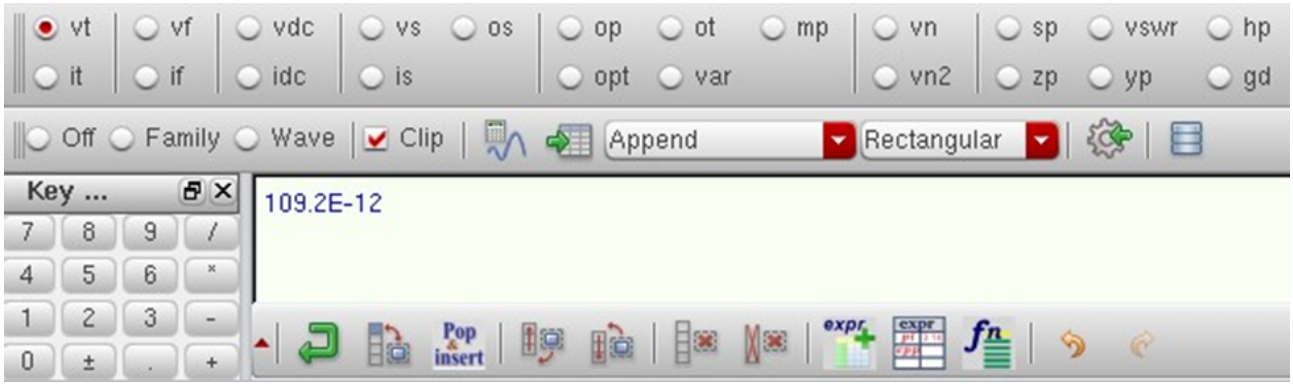

Figure 3:Measurement of propagation delay of a inverter .

3.6.2 Rise/Fall Time Measurement:

The rise and fall time are usually measured from 10% to 90% and from 90% to 10% of the steady state value of a waveform, respectively.

- This time Signal1 and Signal2 both was **VT("/out")**
- Threshold value 1 and 2 was 0.12 (10% of 1.2 V supply) and 1.08 (90% of 1.2 V supply) respectively for 10% to 90% rise time calculation. These values would be swapped for fall time calculation.
- For rise time/fall time calculation, both the Edge numbers was the same.

- By clicking the Evaluate the buffer icon,the propagation delay was found.
- The Edge types would be rising for rise time calculation and falling for fall time calculation.

The measurement of rise time of a inverter is given below:

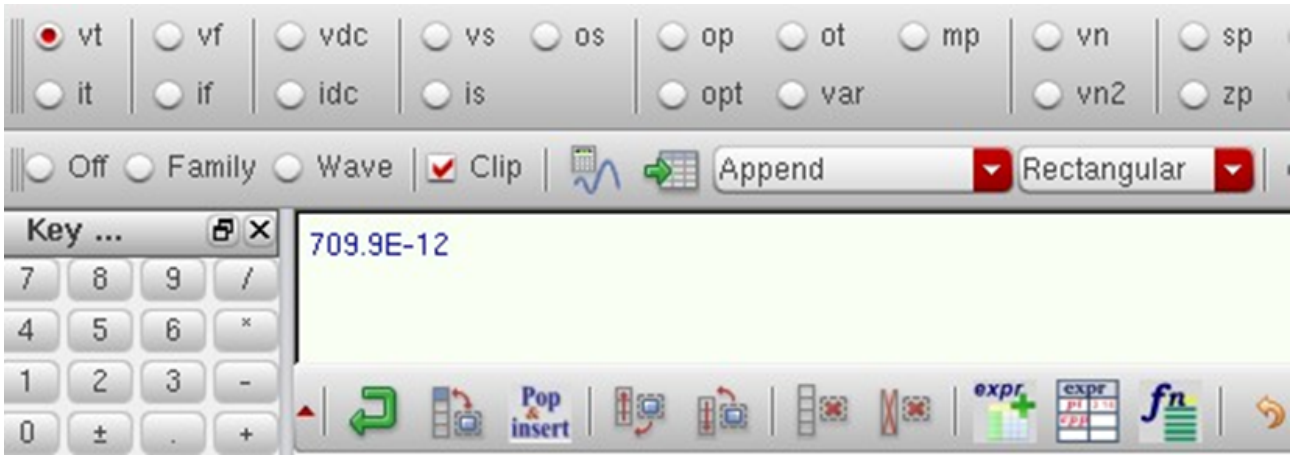

Figure 4:Measurement of rise time of a inverter .

3.6.3 Power Measurement:

- Before running the simulation, the **Outputs** > **Save** All option had been selected in the ADE L window. In the '**Save Options**' window, the '**Select power signals to output (pwr)**' option had been ticked, and OK had been clicked.
- The circuit had been simulated by executing **Simulation ¿ Netlist and Run**.
- had been executed in the ADE L window, and the **'Result Browser'** window had appeared on the left side of the 'Virtuoso Analysis and Visualization XL' window.
- **"Tran"** had been double-clicked, and from the signals list, **"pwr"** had been double-clicked.
- The waveform display window had shown the instantaneous power consumed by the circuit along with 'in' and 'out' signals.
- The Waveform calculator window had been opened, ensuring the **"Wave" and "Clip"** options were selected.
- **'Average'** had been selected from the 'Special Functions' menu.
- The **Evaluate the buffer icon** had been clicked, and the average power dissipation in the time window had been displayed.

The measurement of average power of a inverter is given below:

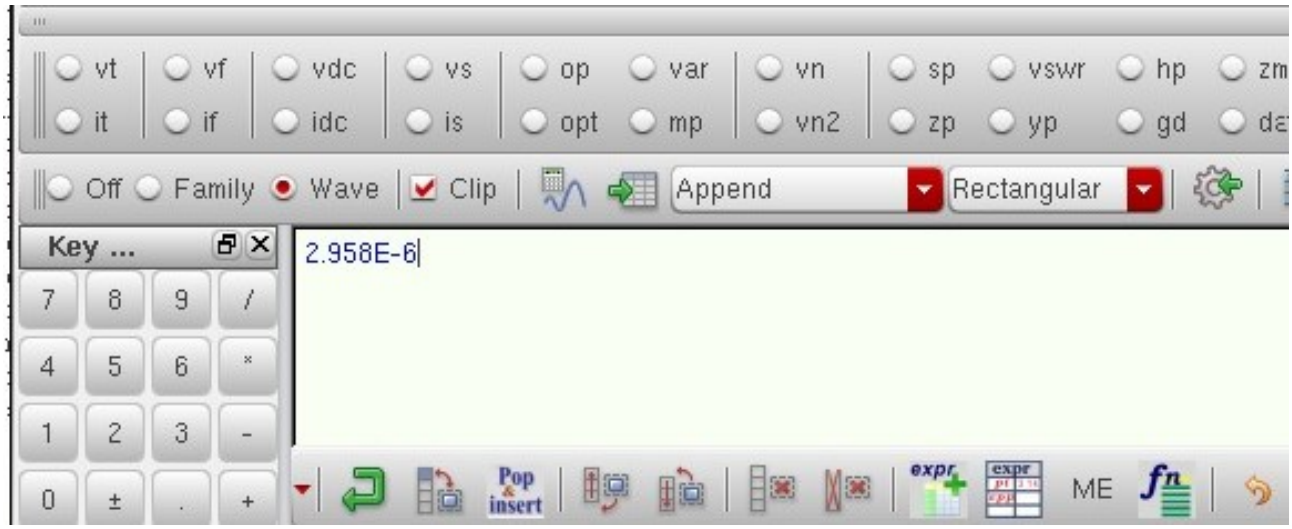

Figure 5:Measurement of average power of a inverter .

4 Behaviour Analysis:

The CMOS inverter had demonstrated specific behavior that could be analyzed in terms of its voltage transfer characteristics (VTC), transient response, and power consumption. The output of a inverter is given below:

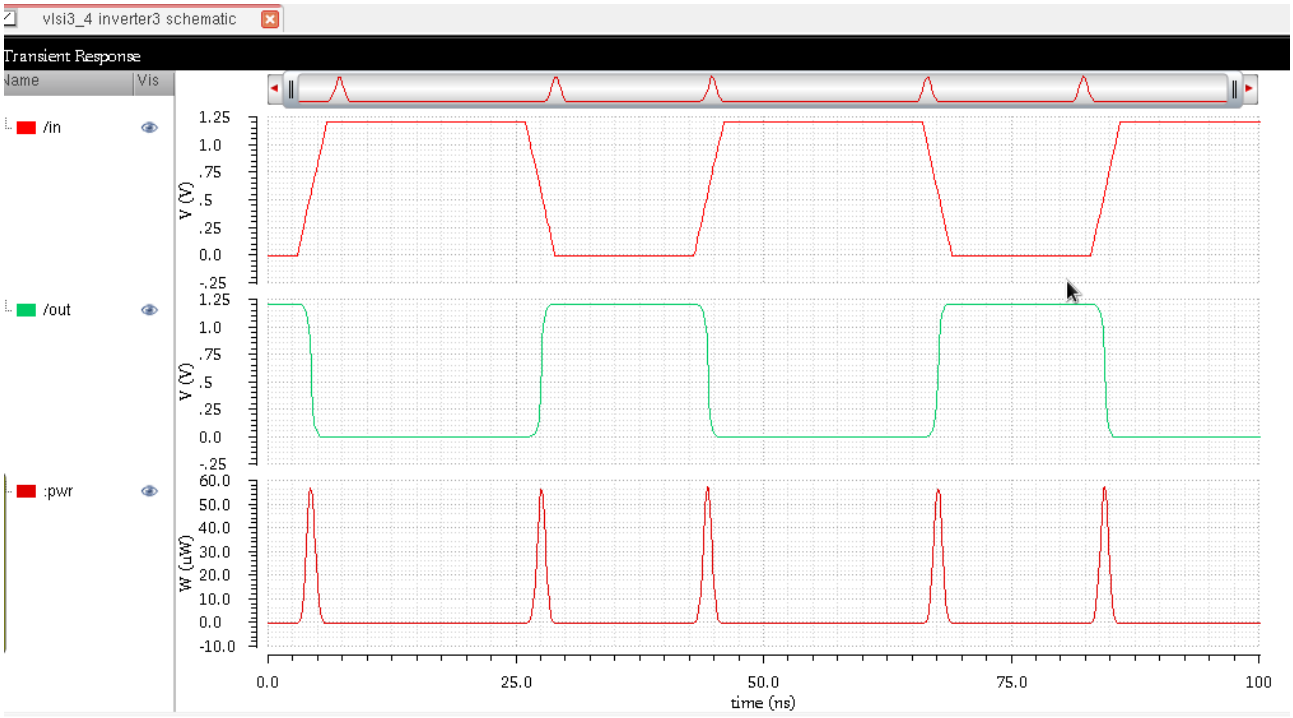

Figure 6:Output of average power of a inverter .

4.1 Input-Output Relationship:

The output of the inverter(as shown in figure 6) had illustrated the relationship between the input voltage (Vin) and the output voltage (Vout), highlighting three main regions:

Cut-off Region:

- When Vin had been low (close to 0V), the PMOS transistor had been fully on, and the NMOS transistor had been fully off.
- Vout had been high, close to the supply voltage (Vdd)

Transition Region:

- As Vin had increased, both transistors had operated in their saturation regions, leading to a sharp transition in Vout.So,a quick switch from high to low output.

Saturation Region:

- When Vin had been high (close to Vdd), the NMOS transistor had been fully on, and the PMOS transistor had been fully off.
- Vout had been low, close to 0V.

4.2 Transient Response:

The transient response had been analyzed by measuring the rise time, fall time, and propagation delays:

Rise Time (tr):

- The rise time(Vout to rise from 10% to 90% of its final value) had been determined from the transient simulation waveform was **709.9E-12** .

Fall Time (tf):

- The rise time(Vout to fall from 90% to 10% of its final value) had been determined from the transient simulation waveform was **709.9E-12** .

Propagation Delay (tp):

- Propagation delays(Time difference between the 50% transition points of the input and output waveforms) had been determined using the delay function in the waveform calculator was **109.2E-12**.

4.3 Power Consumption

Power consumption had been analyzed by breaking it down into dynamic and static components.In ideal CMOS technology, static power consumption had been negligible.Only dynamic power consumption was in account.

Average Power Dissipation:

- During the transition period, there was a brief moment when both NMOS and PMOS transistors conduct simultaneously.The load capacitance at the output need to be charged or discharged, causing a current from Vdd to ground ,leading to a significant spike in current and, consequently inpower consumption.
- Approximately **2.598E-6 W** for the given input conditions and a supply voltage of 1.2V.

5 Discussion:

- In this experiment, the Cadence environment had successfully initiated within VMware Workstation and set up the necessary libraries and cells for our VLSI design.
- An inverter schematic had created using the gpdk090 technology library, ensuring the correct placement and sizing of NMOS and PMOS transistors.
- Testing procedures had been provided to verify circuit design.
- The simulation process had involved configuring the Analog Design Environment (ADE) L, assigning stimuli, and running a transient analysis.
- The switching threshold and output voltage levels had been clearly defined, showing distinct cut-off, transition, and saturation regions.
- Using the waveform calculator, transient response such as rise time, fall time, and propagation delay had been measured.
- The speed of the inverter had been indicated by the measured rise and fall times, as well as propagation delays.
- Additionally,the average power consumption had been calculated during the simulation period.
- In conclusion, the experiment had successfully achieved its objectives of familiarizing with Cadence tools and library creation ,and designing and simulating the inverter through the utilization of VMware Workstation software.