
**CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY**

**Department of Electronics and Telecommunication Engineering**

**VLSI Technology Sessional**

**ETE 404**

**Experiment No:04**

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# DC Analysis and Symbol Creation of Inverter and AND Gate

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# 1 Objectives:

- To familiarize with DC sweep and parametric simulation in ADE L.
- To familiarize with symbol creation from schematic view.

# 2 Apparatus:

- **Software:** VMware Workstation v10
- **Hardware:** PC

# 3 Design Process:

## 3.1 TCC of Inverter with Changing PMOS width:

### 3.1.1 Initialization and Setup

- The Cadence VM was activated, and Virtuoso was initiated by typing **'virtuoso**' in the terminal.
- The existing inverter schematic was opened through **File**$>$ **Open** in CIW.

### 3.1.2 Schematic Entry:

- The schematic editor opened, and the inverter schematic was saved as 'inverter2' via File $>$ Save a Copy. The original editor was closed, and 'inverter2' was reopened from CIW.
- The PMOS transistor was selected in the schematic editor. Its properties were accessed by pressing 'q' or right-clicking and choosing 'Properties', where the total width (w) was entered, updating the 'Finger Width' field automatically.
- Two vdc instances from analogLib were added. The first was set to 'DC Voltage' value of vin, connected between 'in' and 'gnd!'. The second was set to 1.2V, connected between 'vdd!' and 'gnd!'. The input pin and 'vdd!' instance were removed, finalizing the schematic.
- The schematic was checked for errors and saved.

The schematic diagram of a inverter is given below:

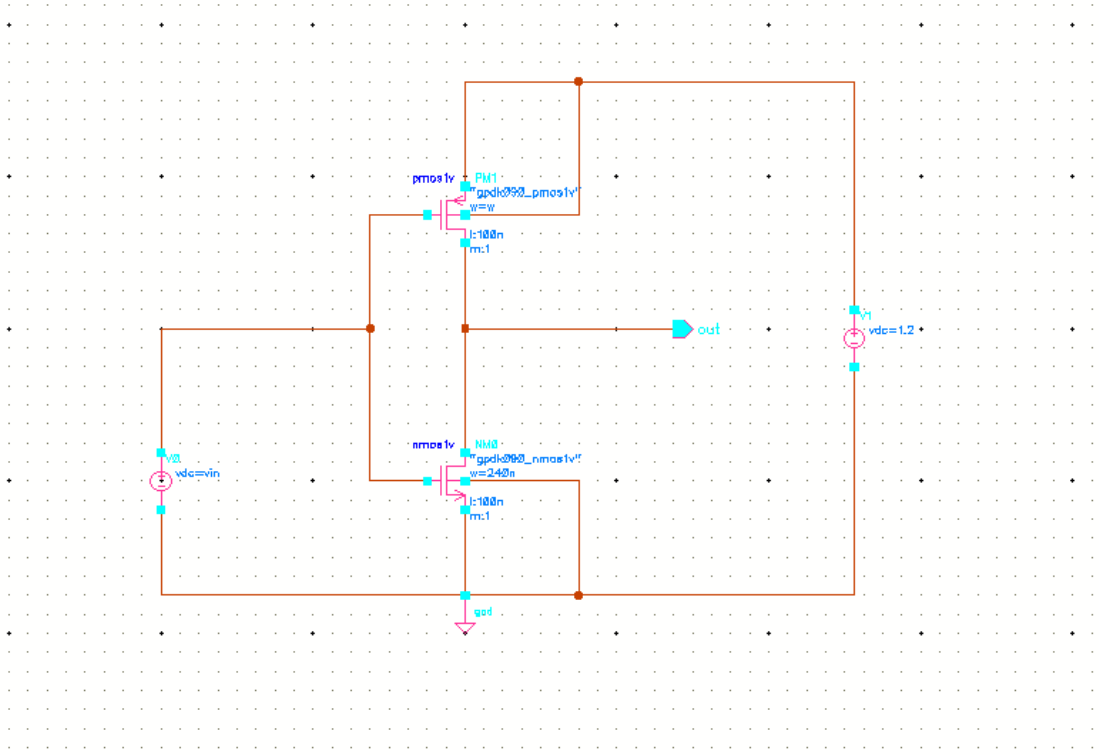



**Figure 01: Schematic diagram of a inverter with varying PMOS total width .**

### 3.1.3 Setting Up ADE L:

- ADE L was launched, and the Model Library was set to **gpdk090_mos.scs**, section Configuring DC Analysis Design variables **'w'** and **'vin'** were copied from the schematic, with default values of 480n and 0.6, respectively.

### 3.1.4 Configuring DC Analysis:

- 'dc' analysis was chosen in the Configuring DC Analysis menu, and Configuring DC Analysis was selected. The sweep variable was set to 'vin' with a range from 0 to 1.2 and a step size of 0.01.

### 3.1.5 Plotting and Running DC Simulation:

- The 'out' pin was selected to be plotted, and Simulation >Netlist and Run was executed to simulate the TCC for the PMOS width of 480n. The Transfer Characterstics Curve(TCC) of a inverter is given below:

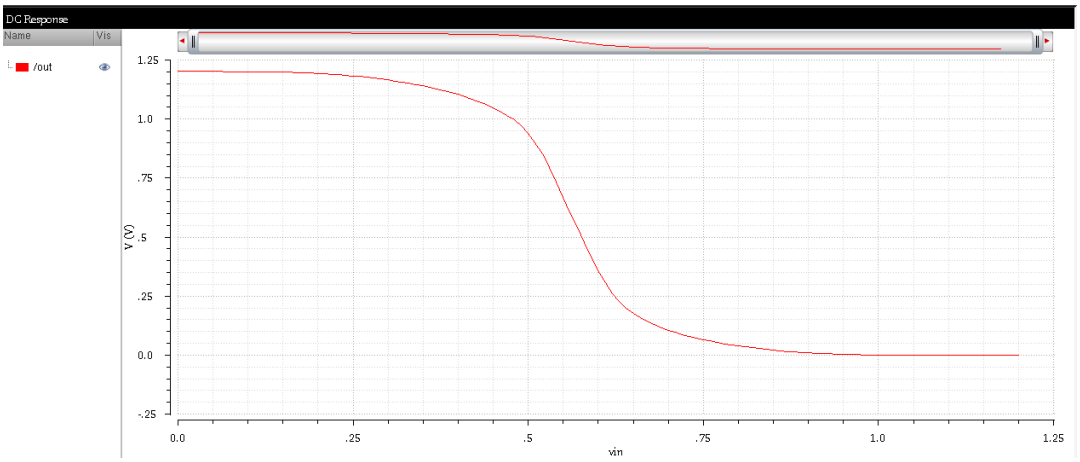



Figure 02: Transfer Characterstics Curve(TCC)of a inverter .

### 3.1.6 Configuring Parametric Analysis:

- **Tools**> **Parametric Analysis** was selected. 'w' was added as a variable, with a range from 240n to 720n and a step size of 120n. Simulations were run by clicking the green 'Run Selected Sweep' icon.
- The parametric file and the ADE L window state were saved for future use.

The effect of changing PMOS width on the TCC of an inverter is given below:

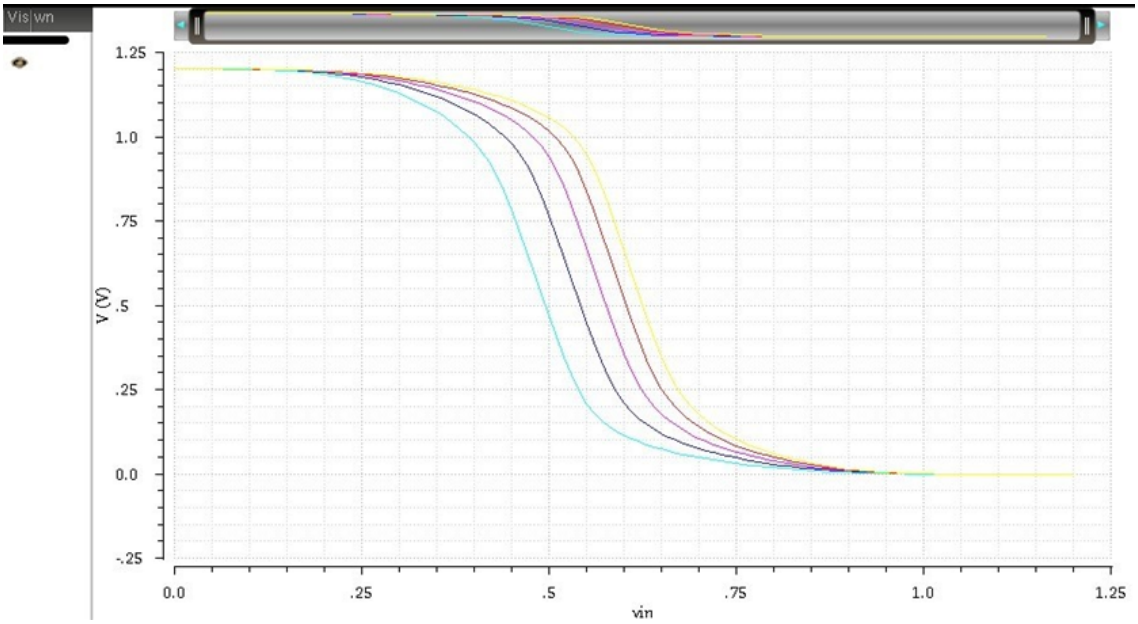



Figure 03:Output of effect of changing PMOS width on the TCC of an inverter.

## 3.2 Symbol Creation of Inverter:

- In the schematic editor window cell 'inverter', Create > Cellview >From Cellview had been executed, and the 'Cellview From Cellview' window had been confirmed by clicking OK.
- In the 'Symbol Generation Options' window, pin locations had been chosen, and OK had been clicked.
- The outer red and green rectangles had been deleted. A triangle shape had been drawn using Create > Shape > Polygon, and a circle had been added at the triangle's end using Create> Shape > Circle. Pin names had been adjusted accordingly.
- An automatic red selection box had been added by Create > Selection Box . The symbol had been saved using the save icon, and File > Check and Save had been executed. Finally, the symbol editor window had been closed.

The symbol of an inverter is given below:

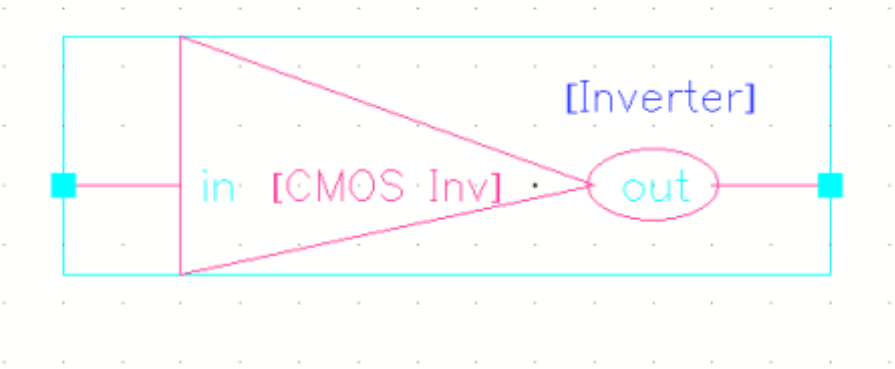



Figure 04:Symbol of an inverter.

## 3.3 AND Gate Creation:

### 3.3.1 Initialization and Setup

- The Cadence VM was activated, and Virtuoso was initiated by typing **'virtuoso'** in the terminal.
- The existing vlsi3_4 library was opened through **File**> **Open** in CIW and created new cell 'and'.

### 3.3.2 Schematic Entry:

- The schematic editor opened,two PMOS transistors was selected in the schematic editor. Its properties were accessed by pressing 'q' or right-clicking and choosing 'Properties', where the total width (480n) was entered, updating the 'Finger Width' field automatically.
- Similarly two NMOS transistors were created with total width 240n.
- Two PMOS were connected in series while two NMOS were connected in parallal.
- The vdd and gnd instances from analogLib were added.
- Create > Pin was executed or 'p' was pressed on the keyboard to add pins for input as 'A' and 'B' output as 'Y'with the appropriate directions.
- The output of the transistors was going to the inverter instance to create AND gate.
- The schematic was checked for errors and saved.

The schematic diagram of a AND gate is given below:

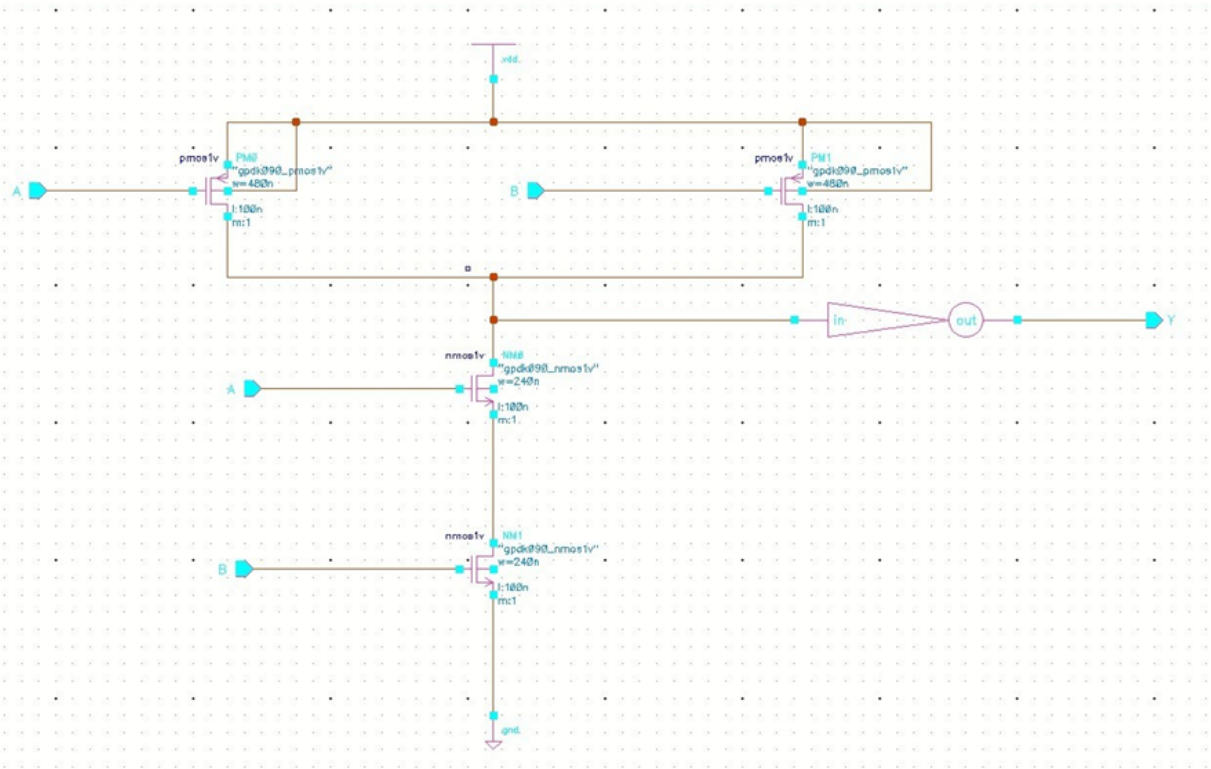



Figure 04: Schematic diagram of a AND gate .

### 3.3.3 Setting Up ADE L:

- ADE L had been set up following the previous steps in inverter.
- The stimuli for inputs A and B had been configured such that the pulse width and period of input B were set to be half of those for input A. This configuration ensured that all four input combinations could tested.

### 3.3.4 Running the Simulation:

- The simulation had been executed, and the expected output waveform had been generated, showing the results for all input combinations. The output of an AND gate is given below:

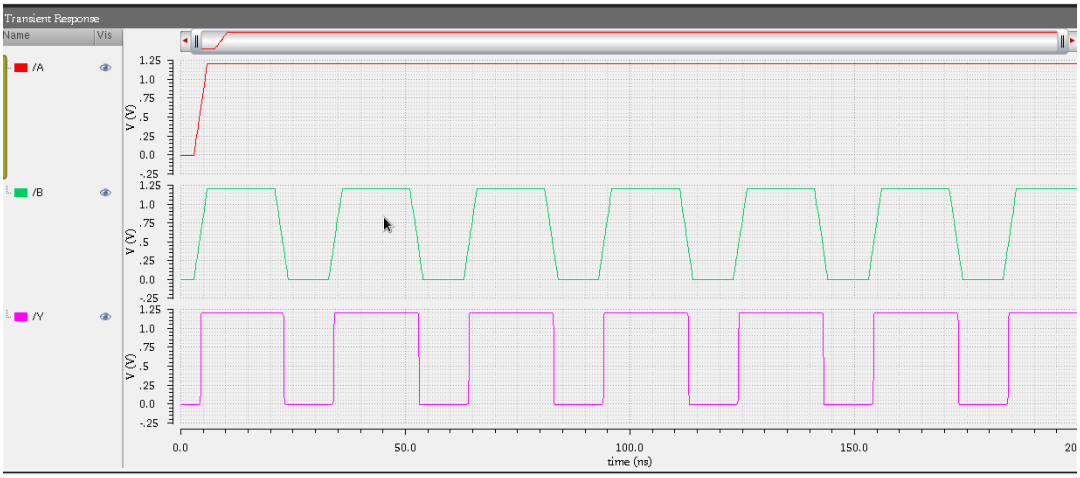



Figure 05: The output of an AND gate .

## 3.4 Symbol Creation of AND Gate:

- In the schematic editor window cell 'and', Create > Cellview >From Cellview had been executed, and the 'Cellview From Cellview' window had been confirmed by clicking OK.
- In the 'Symbol Generation Options' window, pin locations had been chosen, and OK had been clicked.
- The outer red and green rectangles had been deleted. Execute Create > Shape > Polygon and draw a shape similar to the AND gate symbol (a semicircle with straight lines on the left and a curved line on the right). Pin names had been adjusted accordingly.
- An automatic red selection box had been added by Create > Selection Box . The symbol had been saved using the save icon, and File > Check and Save had been executed. Finally, the symbol editor window had been closed.

The symbol of an AND gate is given below:

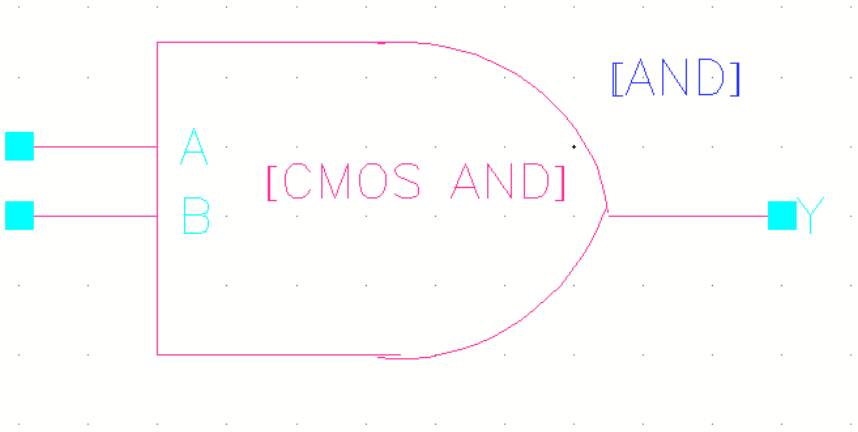



Figure 6:Symbol of an AND gate.

# 4 Home Task

## 4.1 TTCC of an Inverter with Changing NMOS width:

### 4.1.1 Initialization and Setup

- The Cadence VM was activated, and Virtuoso was initiated by typing '**virtuoso**' in the terminal.
- The existing inverter schematic was opened through **File**$>$ **Open** in CIW.

### 4.1.2 Schematic Entry:

- The schematic editor opened, and the inverter schematic was saved as 'inverter2' via File $>$ Save a Copy. The original editor was closed, and 'inverter2' was reopened from CIW.
- The PMOS transistor was selected in the schematic editor. Its properties were accessed by pressing 'q' or right-clicking and choosing 'Properties', where the total width (w) was entered, updating the 'Finger Width' field automatically.
- Two vdc instances from analogLib were added. The first was set to 'DC Voltage' value of vin, connected between 'in' and 'gnd!'. The second was set to 1.2V, connected between 'vdd!' and 'gnd!'. The input pin and 'vdd!' instance were removed, finalizing the schematic.
- The schematic was checked for errors and saved.

The schematic diagram of a inverter with varying NMOS total width is given below:

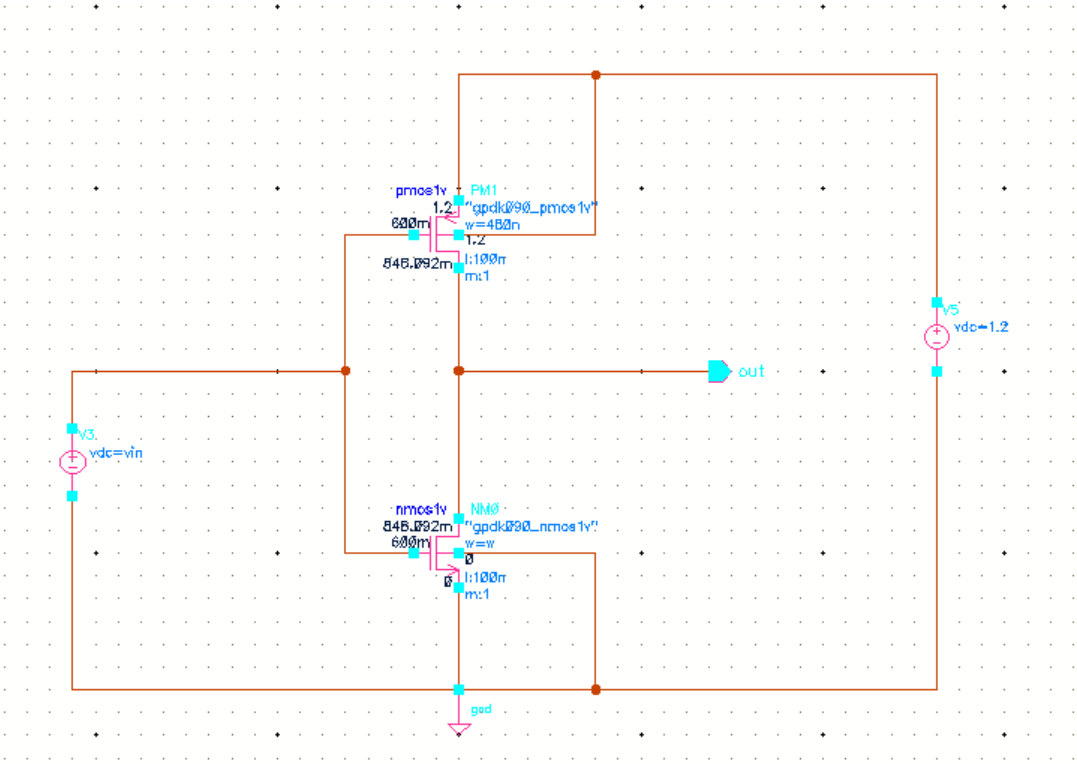



Figure 07: Schematic diagram of a inverter with varying NMOS total width .

#### 4.1.3 Setting Up ADE L:

- ADE L was launched, and the Model Library was set to **gpdk090_mos.scs**, section Configuring DC Analysis Design variables **'w'** and **'vin'** were copied from the schematic, with default values of 240n and 0.6, respectively.

#### 4.1.4 Configuring DC Analysis:

- 'dc' analysis was chosen in the Configuring DC Analysis menu, and Configuring DC Analysis was selected. The sweep variable was set to 'vin' with a range from 0 to 1.2 and a step size of 0.01.

#### 4.1.5 Plotting and Running DC Simulation:

- The 'out' pin was selected to be plotted, and Simulation $>$ Netlist and Run was executed to simulate the TCC for the PMOS width of 240n. The Transfer Characterstics Curve(TCC) of a inverter is given below:

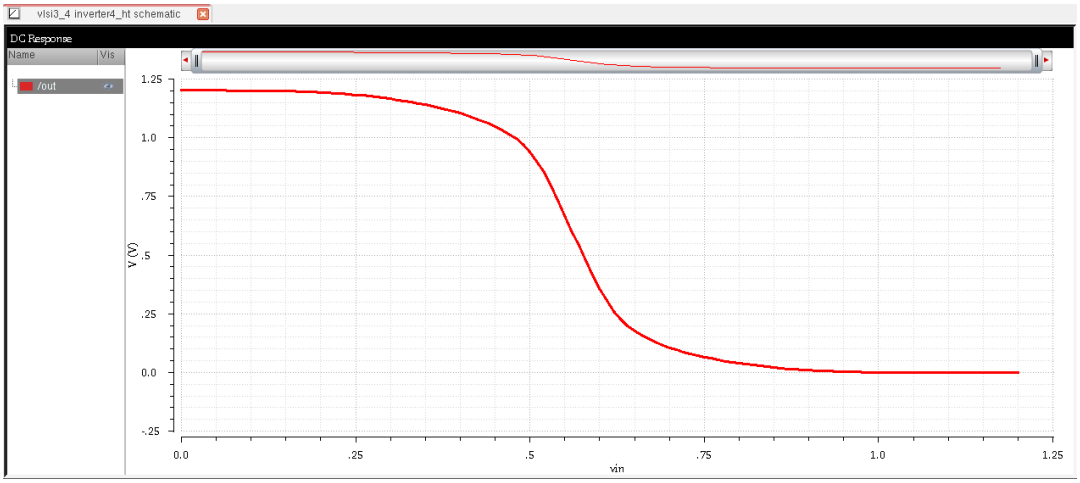



Figure 08: Transfer Characterstics Curve(TCC)of a inverter .

### 4.1.6 Configuring Parametric Analysis:

- **Tools**> **Parametric Analysis** was selected. 'w' was added as a variable, with a range from 120n to 480n and a step size of 80n. Simulations were run by clicking the green 'Run Selected Sweep' icon.
- The parametric file and the ADE L window state were saved for future use.

The effect of changing NMOS width on the TCC of an inverter is given below:

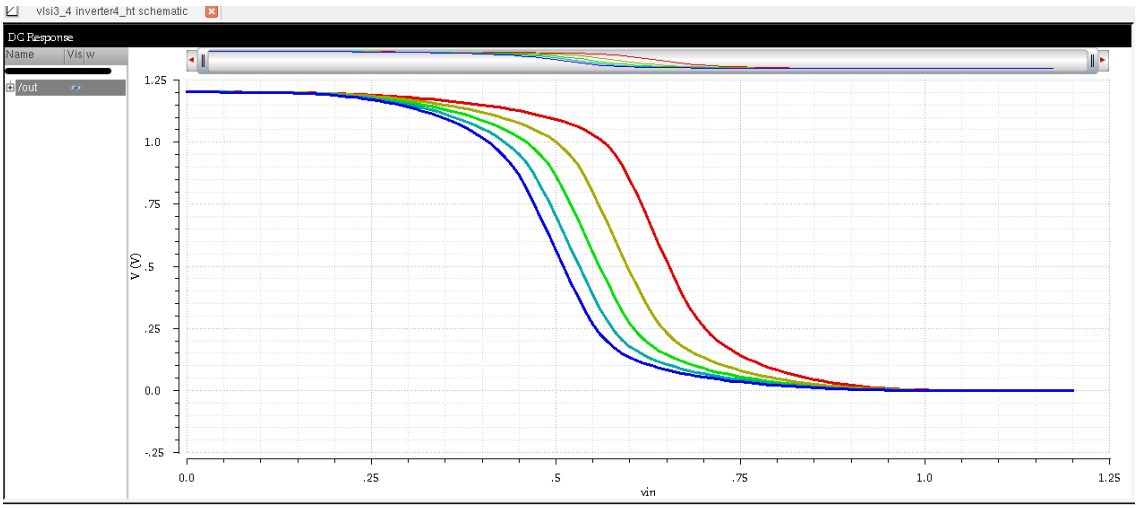



Figure 09:Output of effect of changing NMOS width on the TCC of an inverter.

## 4.2 OR Gate Creation:

### 4.2.1 Initialization and Setup

- The Cadence VM was activated, and Virtuoso was initiated by typing **'virtuoso'** in the terminal.
- The existing vlsi3_4 library was opened through **File**> **Open** in CIW and created new cell 'or'.

### 4.2.2 Schematic Entry:

- The schematic editor opened,two PMOS transistors was selected in the schematic editor. Its properties were accessed by pressing 'q' or right-clicking and choosing 'Properties', where the total width (480n) was entered, updating the 'Finger Width' field automatically.
- Similarly two NMOS transistors were created with total width 240n.
- Two PMOS were connected in parallel while two NMOS were connected in series.
- The vdd and gnd instances from analogLib were added.
- Create > Pin was executed or 'p' was pressed on the keyboard to add pins for input as 'A' and 'B' output as 'Y' with the appropriate directions.
- The output of the transistors was going to the inverter instance to create OR gate.
- The schematic was checked for errors and saved.

The schematic diagram of a OR gate is given below:

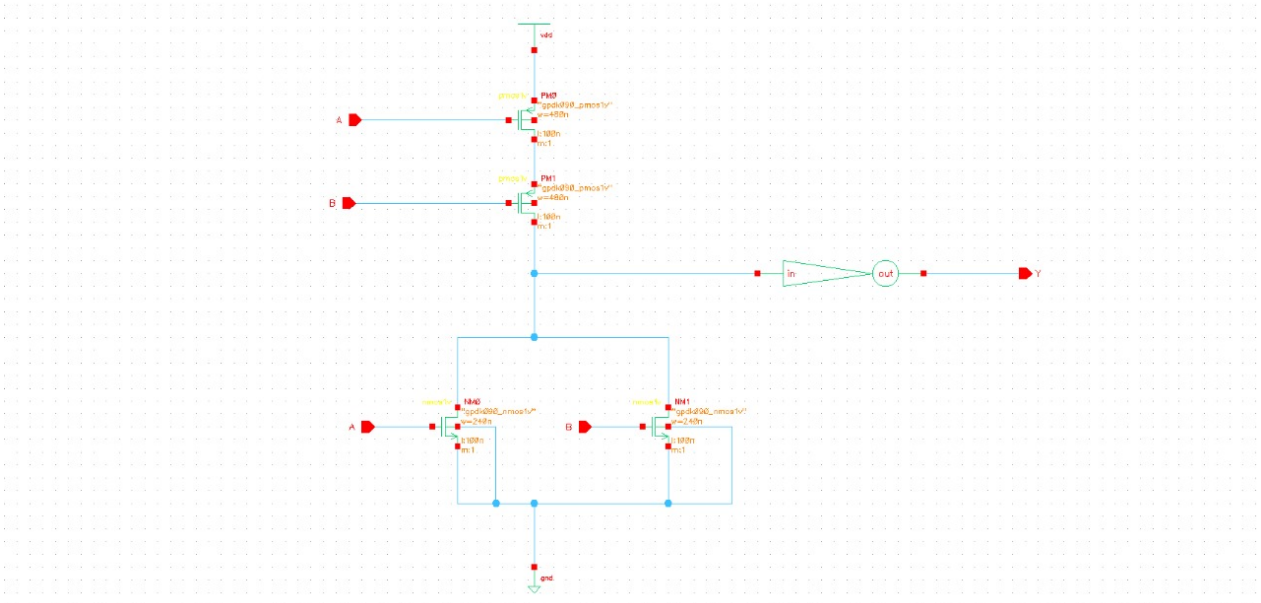



Figure 10: Schematic diagram of a OR gate .

### 4.2.3 Setting Up ADE L:

- ADE L had been set up following the previous steps in inverter.
- The stimuli for inputs A and B had been configured such that the pulse width and period of input B were set to be half of those for input A. This configuration ensured that all four input combinations could tested.

### 4.2.4 Running the Simulation:

- The simulation had been executed, and the expected output waveform had been generated, showing the results for all input combinations. The output of an OR gate is given below:

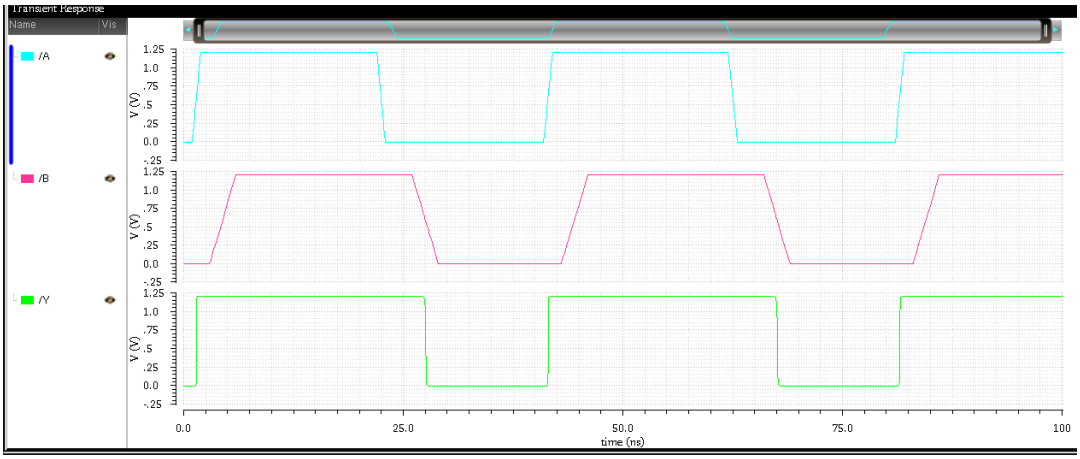



Figure 11: The output of an OR gate .

## 4.3 Symbol Creation of OR Gate:

- In the schematic editor window cell 'and', Create > Cellview >From Cellview had been executed, and the 'Cellview From Cellview' window had been confirmed by clicking OK.
- In the 'Symbol Generation Options' window, pin locations had been chosen, and OK had been clicked.
- The outer red and green rectangles had been deleted. Execute Create > Shape > Polygon and draw a shape similar to the OR gate symbol ( Drawing a line on the left,and a convex curved line on the right to form the characteristic OR gate shape. Drawing two more lines from the top and bottom to complete the shape)Pin names had been adjusted accordingly.
- An automatic red selection box had been added by Create > Selection Box . The symbol had been saved using the save icon, and File > Check and Save had been executed. Finally, the symbol editor window had been closed.

The symbol of an OR gate is given below:

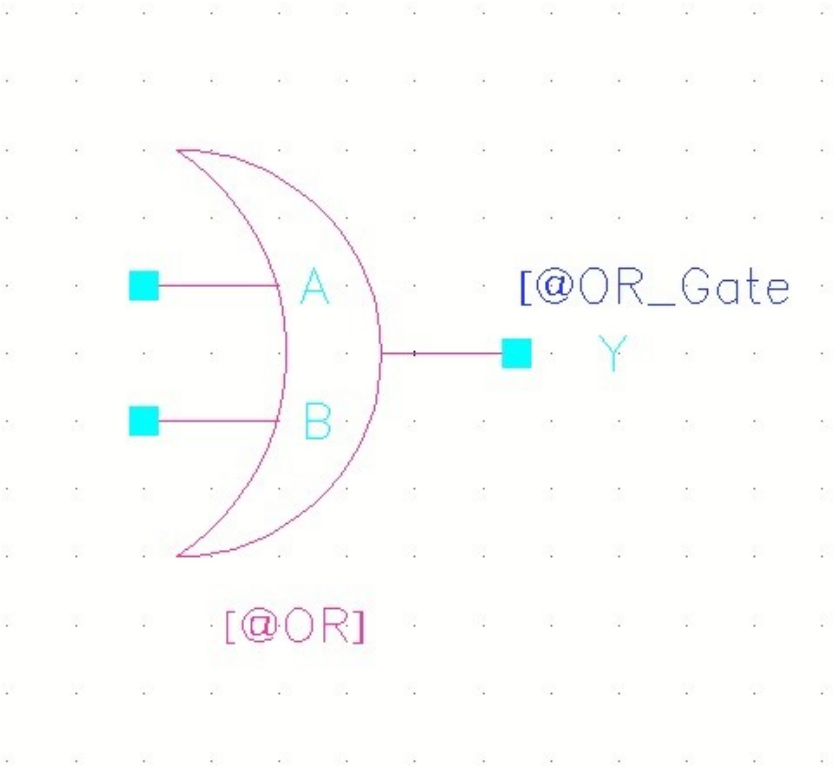



Figure 12:Symbol of an OR gate.

# 5 Behaviour Analysis with Varying PMOS and NMOS Width:

The CMOS inverter had demonstrated specific behavior that could be analyzed in terms of its Transfer transfer characteristics (TTC).

## 5.1 Input-Output Relationship:

**Cut-off Region:**

- When Vin had been low (close to 0V), the PMOS transistor had been fully on, and the NMOS transistor had been fully off.
- Vout had been high, close to the supply voltage (Vdd)

**Transition Region:**

- As Vin had increased, both transistors had operated in their saturation regions, leading to a sharp transition in Vout.So,a quick switch from high to low output.

**Saturation Region:**

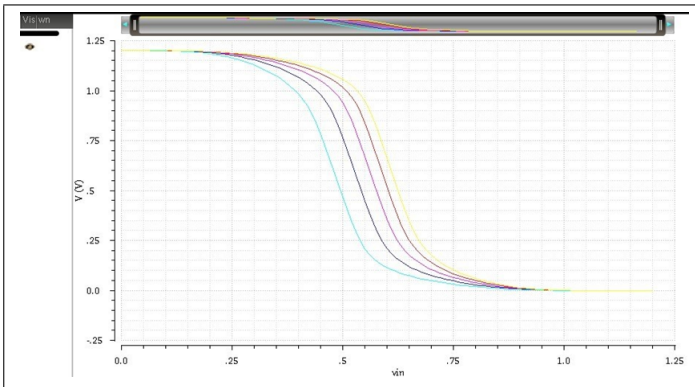
- When Vin had been high (close to Vdd), the NMOS transistor had been fully on, and the PMOS transistor had been fully off.
- Vout had been low, close to 0V.

## 5.2 TCCs for Varying PMOS Width Setting:

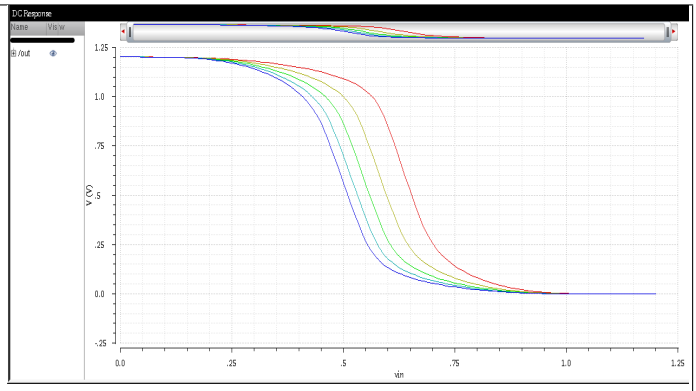
- The switching threshold voltage shifted towards a higher value. A wider PMOS transistor allows more current to flow for the same gate voltage, making the PMOS transistor turn on more easily(as shown in figure 13(a)).
- The transition region became steeper. .

## 5.3 TCCs for Varying NMOS Width Setting:

- With decreasing NMOS Width,the switching threshold voltage shifted towards a higher value. A narrower NMOS transistor requires a higher gate voltage to conduct the same amount of current.(as shown in figure 13(b)).
- A wider NMOS resulted in a lower Vin, meaning the inverter switches at a lower input voltage.
- The transition region became less steep.




(a)TCCs for Varying PMOS Width Setting




(b)TCCs for Varying NMOS Width Setting

**Figure 13: TCCs for for an Inverter**

# 6 Behaviour Analysis of AND Gate:

An AND gate have been analyzed in terms of its truth table, voltage transfer characteristics (VTC).

## 6.1 Truth Table:

- The truth table for a 2-input AND gate have been indicated that the output was high (1) only when both inputs were high (1).

Table 1: Truth Table for AND Gate

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## 6.2 Voltage Transfer Characteristics (VTC)

The VTC curve of the AND gate had been analyzed by plotting the output voltage (Y) against one of the input voltages (A and B), while the other input had been fixed at logical high (1) or low (0).(as shown in figure 15)

**When Input B= Low (0):**

- The output Y had always been low (0) regardless of the value of input A.
- VTC had been a flat line at 0V.

**When Input B =High (1):**

- The output Y had followed the behavior of input A.
- When both inputs were high,then Y would be high.

The VTC of an AND gate is given below:

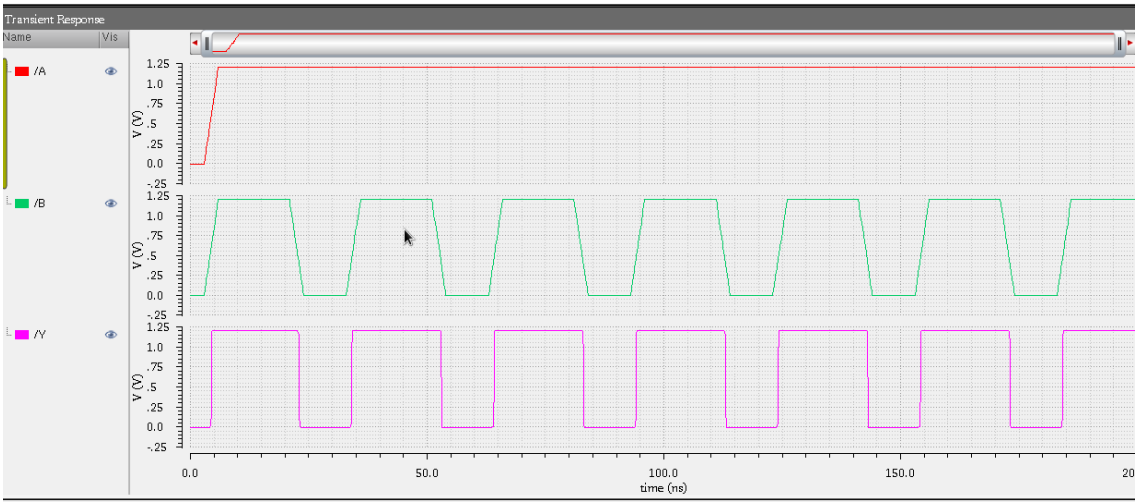



Figure 14: The VTC of an AND gate .

# 7 Behaviour Analysis of OR Gate:

An AND gate have been analyzed in terms of its truth table, voltage transfer characteristics (VTC).

## 7.1 Truth Table:

- The truth table for a 2-input ORgate have been indicated that the output was high (1) only when any one of the inputs were high (1).

Table 2: Truth Table for OR Gate:

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

## 7.2 Voltage Transfer Characteristics (VTC)

The VTC curve of the OR gate had been analyzed by plotting the output voltage (Y) against input voltages (A and B)(as shown in figure 15)

**When Input A=Input B= Low (0):**

- The output Y had always been low (0)
- VTC had been a flat line at 0V.

**When Input A=Input B =High (1):**

- The output Y had always been high (1)
- VTC had been a flat line at 1.2V.

**When Only One Input=high(1):**

- The output Y had always been high (1)
- VTC had been a flat line at 1.2V.

The VTC of an OR gate is given below:

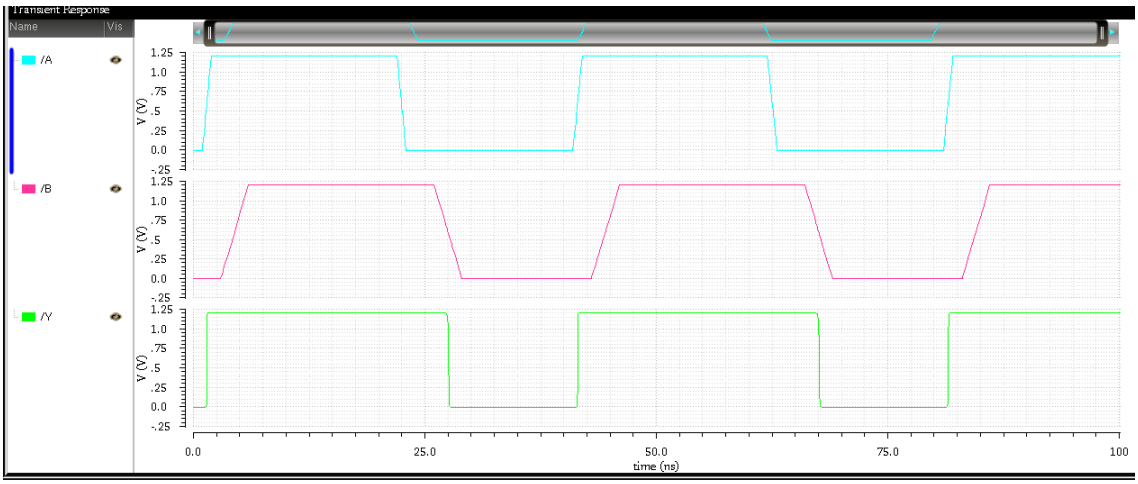



Figure 15: The VTC of an OR gate .

# 8 Discussion:

- In this experiment, the behavior of an inverter, AND gate, and OR gate in terms of their transfer characteristics curve (TCC), and symbolic representations hed been examined.
- The effect of changing NMOS and PMOS width on the inverter's Transfer Characteristic Curve (TCC) was investigated, demonstrating how varying transistor widths influenced the switching threshold and transition region.
- The switching threshold and output voltage levels had been clearly defined, showing distinct cut-off, transition, and saturation regions.
- With increasing NMOS Width resulted in lowers switching threshold and steeper transition while increasing PMOS Width resulted in in highers switching threshold and steeper transition.
- The TCC for a 2-input AND gate have been indicated that the output was high (1) only when both inputs were high (1).
- The TCC for a 2-input AND gate have been indicated that the output was high (1) only when any one of the inputs were high (1).
- In conclusion, the experiment had successfully achieved its objectives of familiarizing with DC sweep and parametric simulation and with symbol creation from schematic view.through the utilization of Cadence in VMware Workstation software.