CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Telecommunication Engineering

VLSI Technology Sessional

ETE 404

Experiment No:05

Layout Generation of an Inverter using Virtuoso L

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June 23, 2024

1 Objectives:

- To create a layout view of the basic inverter in Virtuoso Layout Editor.
- To design the layout keeping basic design rules in mind.
- To design cell layout of a constant height for use in hierarchical design.

2 Apparatus:

- **Software:** VMware Workstation v10
- **Hardware:** PC

3 Design Process:

3.1 Initialization:

- The Virtuoso software was initiated from the terminal, and a new file was created with the cell name ”inverter” and type ”layout”.

3.2 Display Settings Adjustment:

- The ’Layers’ panel was reviewed to ensure the display corresponded to the gpdk090 layers. The layout display configuration was set by executing **Options** > **Display** (or pressing ’e’). The following values were configured:

  Minor Spacing: 0.01 µm

  Major Spacing: 0.1 µm

  X Snap Spacing: 0.005 µm

  Y Snap Spacing: 0.005 µm

  Display Levels: Stop at 10

3.3 DRD Notification Setting:

- The Design Rule Driven (DRD) notify was turned on to ensure adherence to design rules.

3.4 NMOS Transistor Layout:

- A rectangle of the ’Cont (drw)’ layer with dimensions 0.12 µm x 0.12 µm was created using **Create** > **Shape** > **Rectangle** (or pressing ’r’).
- This contact was copied at a distance of 0.3 µm using a ruler tool (invoked by pressing ’k’).

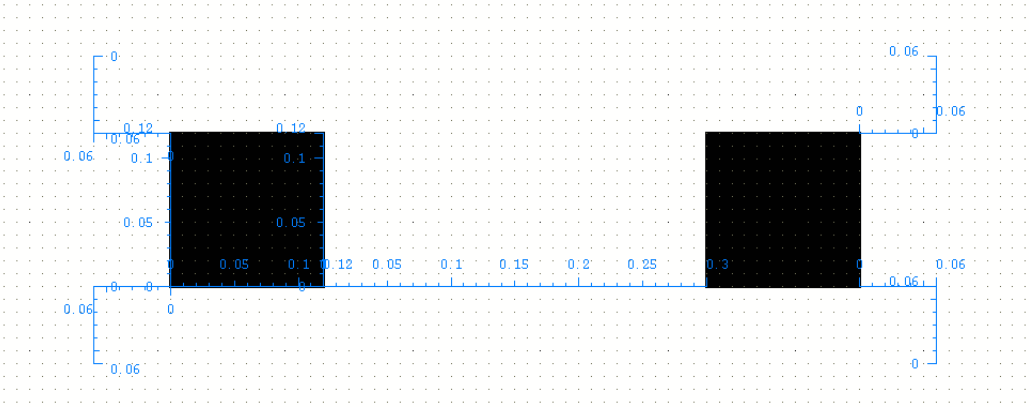

Figure 1.1:Layout of contact layer of NMOS transistor.

- An ’Oxide (drw)’ layer rectangle was drawn to cover both contacts, extending by 0.06 µm on each side.

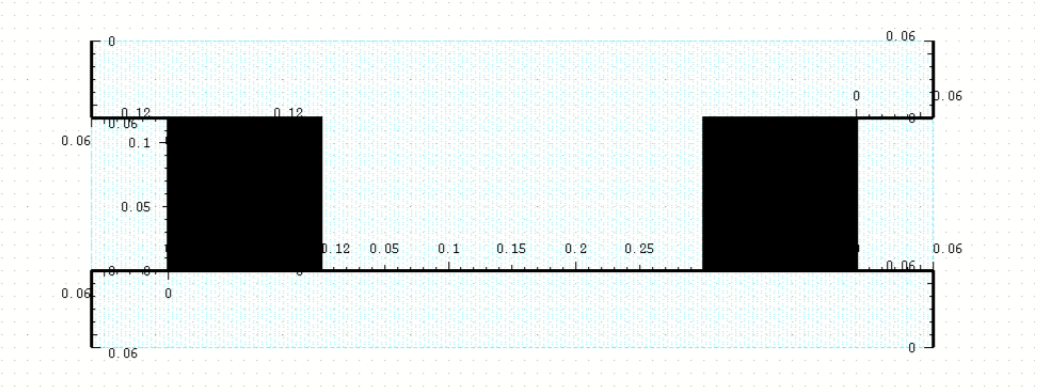

Figure 1.2:Layout of Oxide layer of NMOS transistor.

- An ’Nimp (drw)’ layer was extended from the oxide layer by a minimum of 0.14 µm using the stretch tool (’s’).

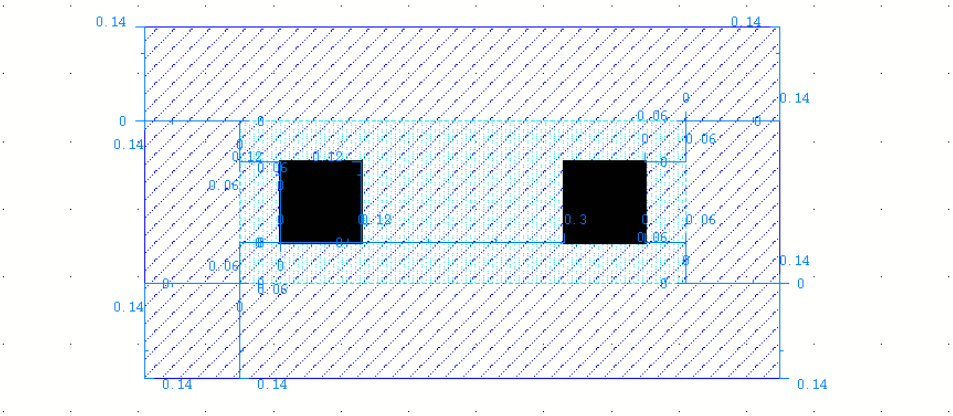

Figure 1.3:Layout of Nimp layer of NMOS transistor.

3.5 PMOS Transistor Layout:

- Another set of layers (Cont, Oxide, Poly) was created 2.0 µm away from the NMOS layout.
- The ’Nimp (drw)’ layer of the copied structure was modified to ’Pimp (drw)’ using the edit properties function (’q’).

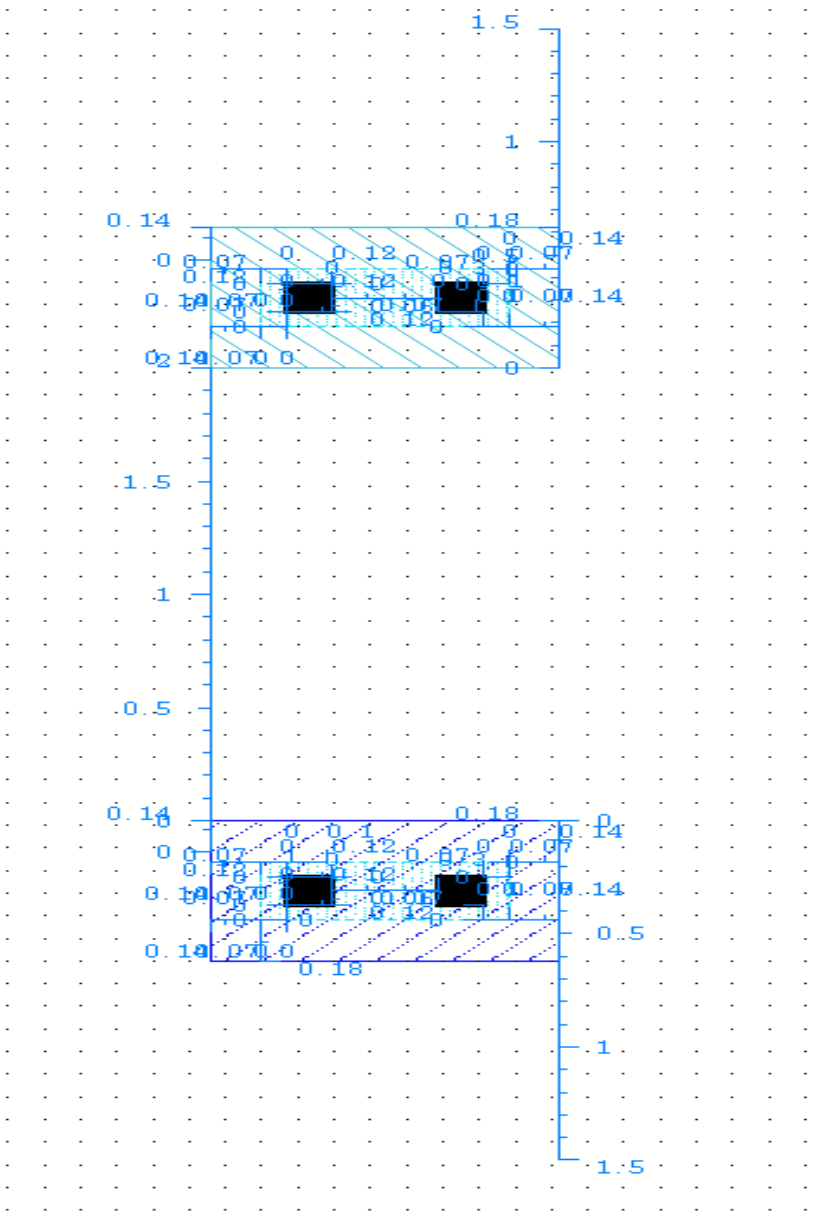

Figure 2:Layout of p-type and n-type portion.

3.6 Creating Poly Layer:

- The NMOS and PMOS were positioned 2 µm apart, maintaining a total cell height of 5 µm.
- A 'Poly (drw)' path was created(invoked by pressing 'p'), ensuring a 0.18 µm extension from the oxide layer and a minimum width of 0.1 µm.

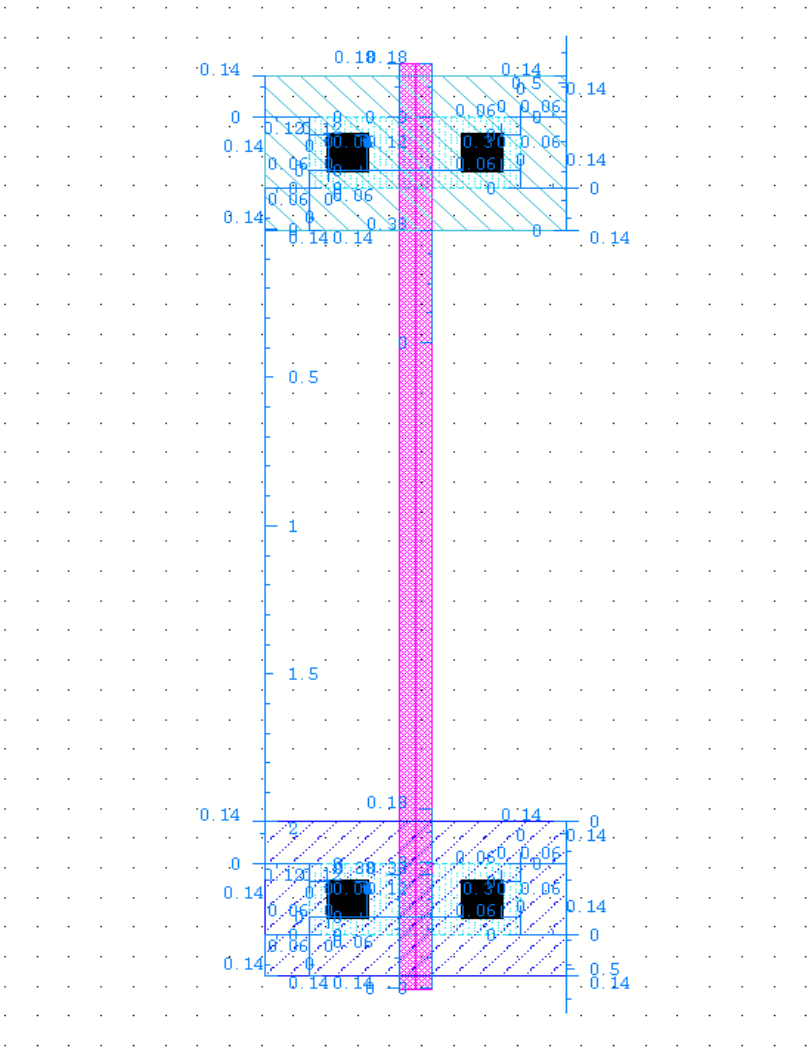

Figure 3:Layout of p-type and n-type portion with poly layer.

3.7 Body Terminals and Connections:

- Contacts for body terminals were created using Cont, Oxide, and Nimp/Pimp layers, ensuring compliance with DRD notifications.

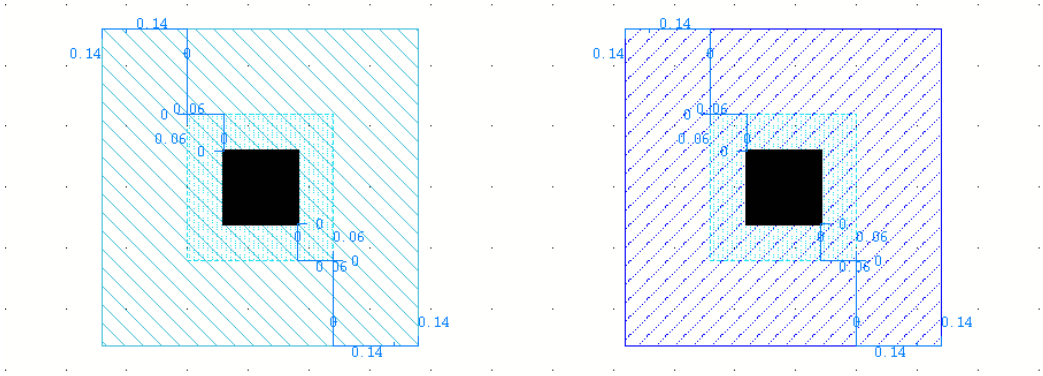

Figure 4.1:Layout of body terminals of NMOS and PMOS transistor.

- The drains of the NMOS and PMOS were connected using 'Metal1 (drw)' layer, with sources connected to their respective body terminals.
- An 'Nwell (drw)' rectangle was drawn around the PMOS and its body contact.

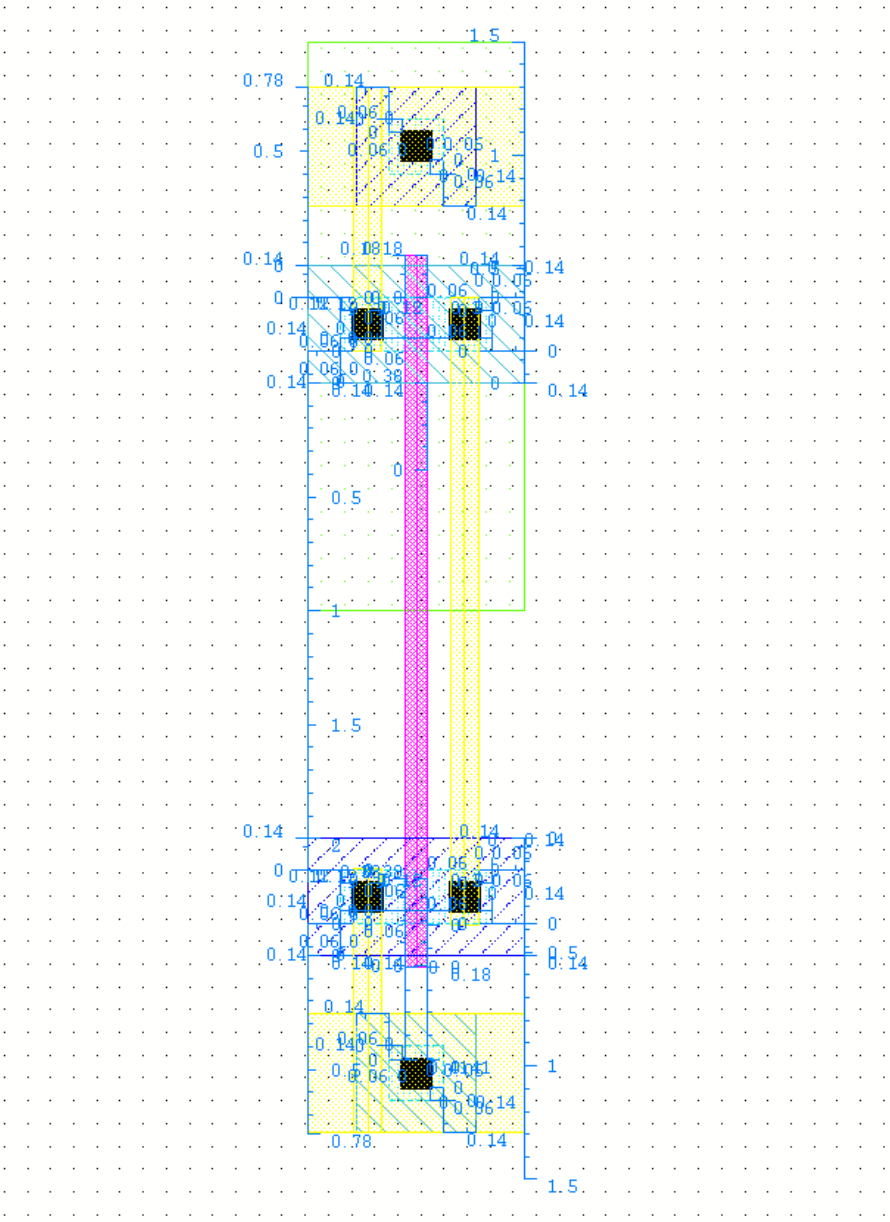

Figure 4.2: Layout of connection of drain,source and body terminals of PMOS and NMOS transistor.

3.8 Placing Pins and Final Connections:

- A via between the Poly and Metal1 layers was created at the gate for the "in" pin using 'M1_POv' via definition.
- Additional Metal1 rectangles were drawn on the vias to meet the minimum required area.
- Pins for vdd!, gnd!, in, and out were created using **Create** > **Pin**,selecting 'input' for vdd!, gnd!, and in, and 'output' for out.

- Rectangles for these pins were drawn on the appropriate layers.
- Finally, Metal2 paths with a width of 0.5 µm were added for power rails, connecting them to power nets in Metal1 using Metal1 to Metal2 vias. The final layout was completed according to these steps.

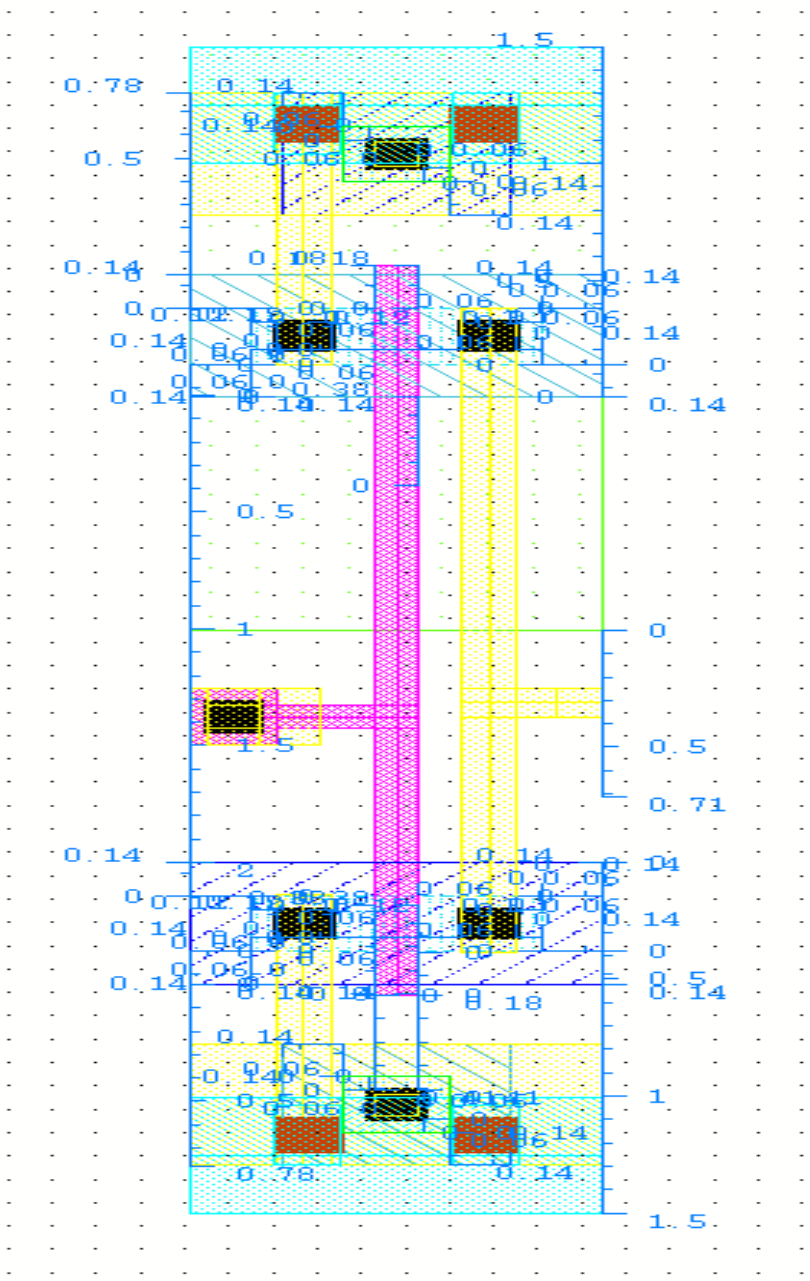

Figure 5:Final layout of an inverter.

4 Home Task:

4.1 P-Substrate Contact:

- The 'Cont (drw)' layer was selected from the Layers panel, and a contact rectangle with dimensions 0.12 µm x 0.12 µm was created.
- An oxide layer was then drawn with a minimum spacing of 0.06 µm from the contact.
- An Pimp layer was drawn, extending a minimum of 0.07 µm in width and of 0.075 µm in height from the oxide layer.
- A Metal1 path with a minimum width of 0.1 µm was added in the oxide layer.

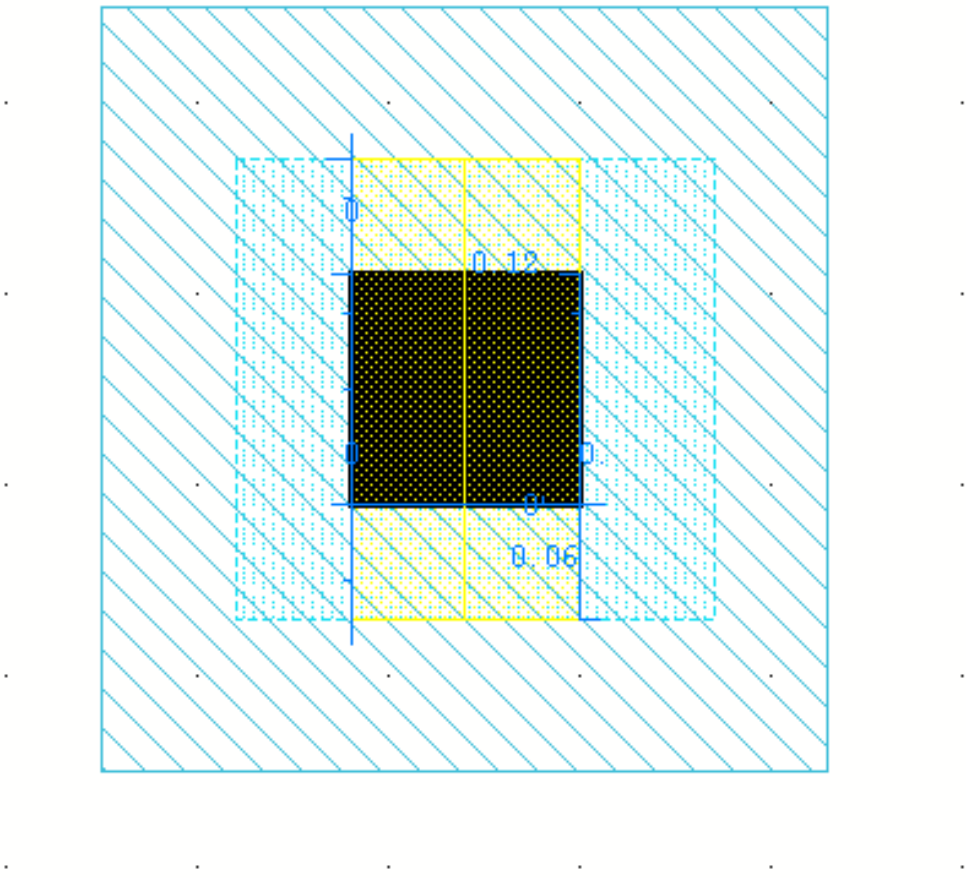

Figure 6.1:Layout of an p-subratre ontact.

4.2 N-Substrate Contact:

- The 'Cont (drw)' layer was selected from the Layers panel, and a contact rectangle with dimensions 0.12 µm x 0.12 µm was created.
- An oxide layer was then drawn with a minimum spacing of 0.06 µm from the contact.
- An nimp layer was drawn, extending a minimum of 0.07 µm in width and of 0.075 µm in height from the oxide layer.
- A Metal1 path with a minimum width of 0.1 µm was added in the oxide layer.

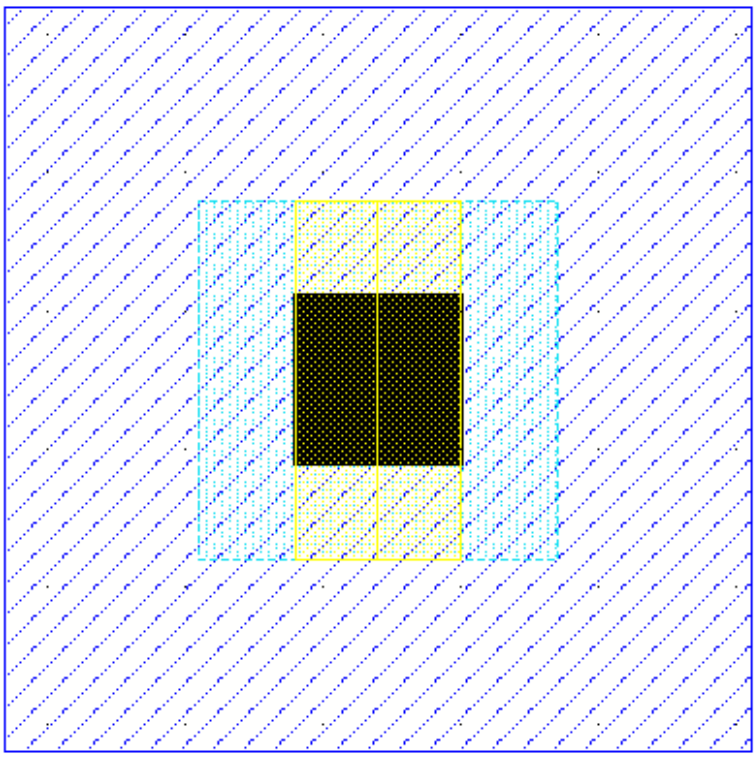

Figure 6.2:Layout of an n-subratre ontact.

5 Discussion:

- In this experiment, the layout design process for an inverter was methodically carried out using the Virtuoso Layout Suite L Editor.
- To ensure the correct placement and sizing of NMOS and PMOS transistors, the inverter layout was created using the gpdk090 technology library.
- DRD Notify was utilized to promptly identify and rectify any design rule violations, thereby maintaining the integrity of the layout.
- The NMOS and PMOS transistors were accurately constructed by layering contact,oxide, polysilicon, Nimp and Pimp,and metal appropriately.
- The connections for the source, drain, and gate terminals were meticulously established using Metal1 and Metal2 layers, following standard cell physical design principles.
- The final layout included all necessary connections and pins, with power and ground rails appropriately routed using higher metal layers.
- Although a full-custom IC design flow was followed, same cell height was maintained throughout our cell library.
- In conclusion, the experiment had successfully achieved its objectives of creating a layout view of the basic inverter with keeping basic design rules in mind through the utilization of VMware Workstation software.