DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY

CHATTOGRAM – 4349, BANGLADESH

Experiment No. 6

DRC, LVS, RCX and Post-Layout Simulation of an Inverter

PRECAUTIONS:

- Students must carefully read the lab manual before coming to lab to avoid any inconveniences.
- Students must carry a flash drive to transfer files and lab manuals.
- Use of mobile phone in lab is strictly prohibited and punishable offence.
- Experiment files must be uploaded to GitHub including home tasks.

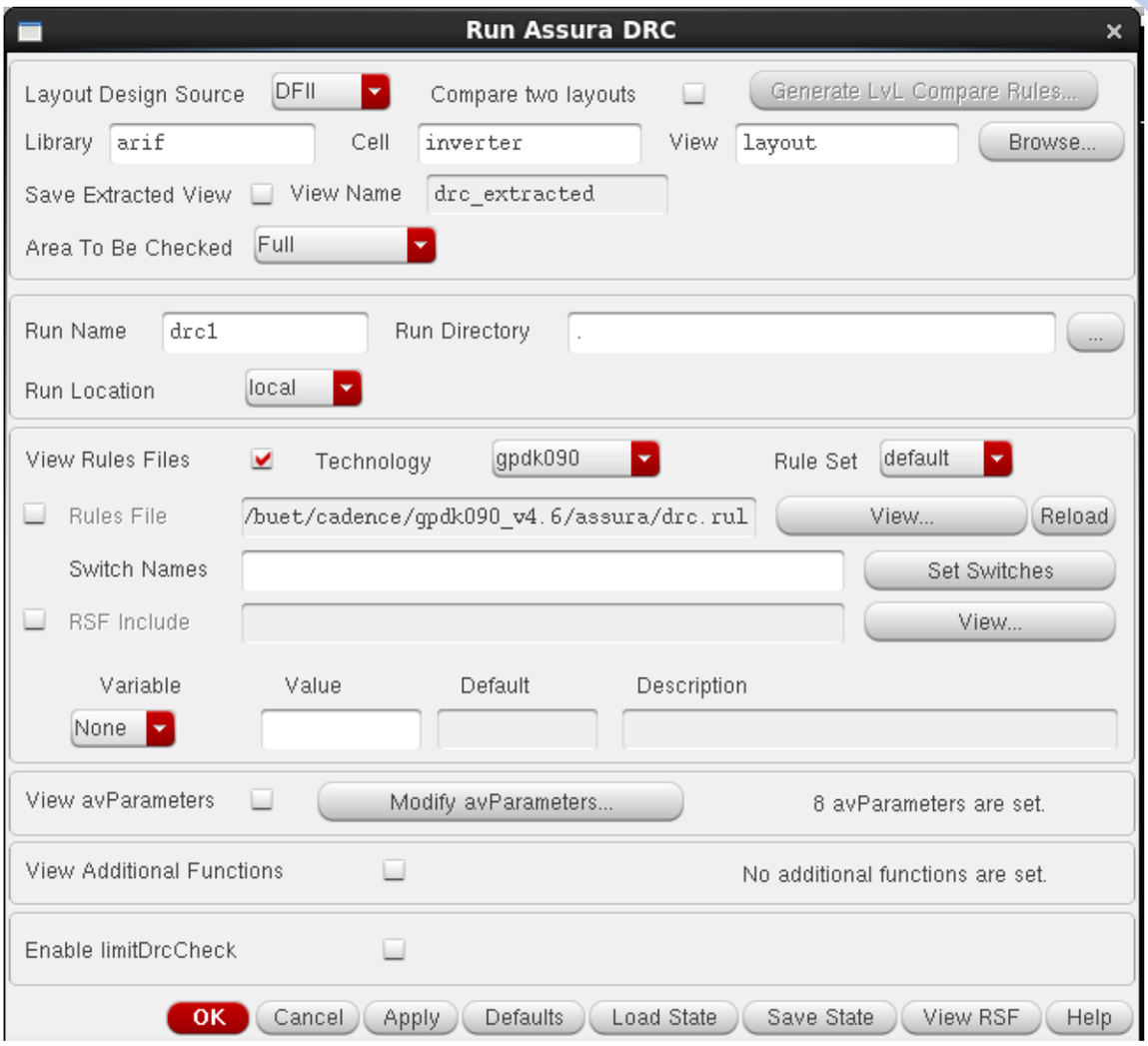
OBJECTIVES:

- To perform Design Rules Check (DRC) and Layout vs. Schematic (LVS).
- To extract parasitic resistance and capacitance from layout.
- To perform transient simulation of extracted view.

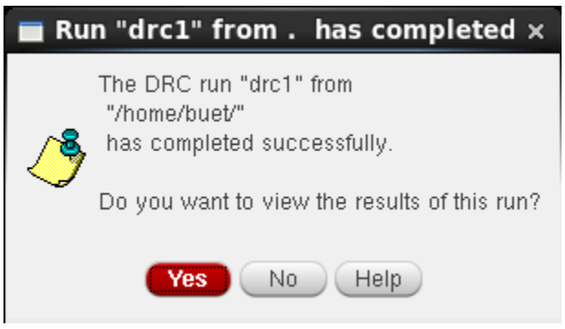
DRC USING ASSURA:

1. Open the previously created layout of an inverter in Virtuoso Layout Suite L. Execute **Assura > Technology**. In the following window, type the path of **'Assura Technology File'** as shown. Click **OK**.

2. Execute **Assura > Run DRC**. A DRC window appears as shown below. Fill the form as indicated in the picture. Give a **Run Name**. Select **'gpdk090'** under **'Technology'**. Then click **OK**.

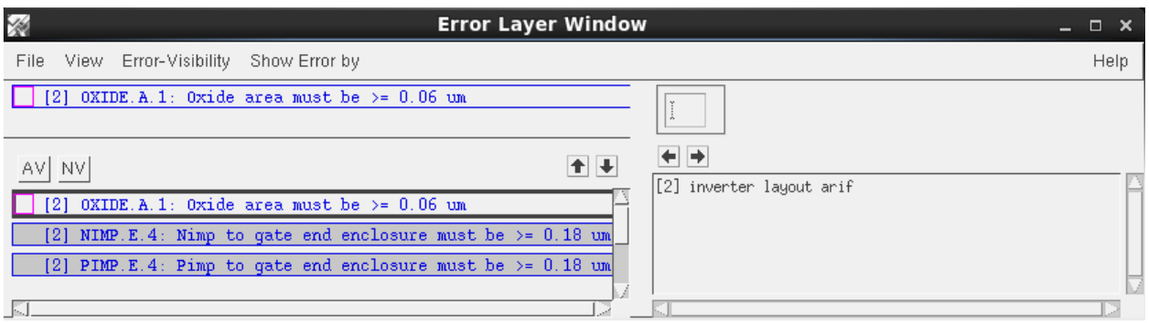


3. A DRC completed window appears as shown below, after completion of DRC run:



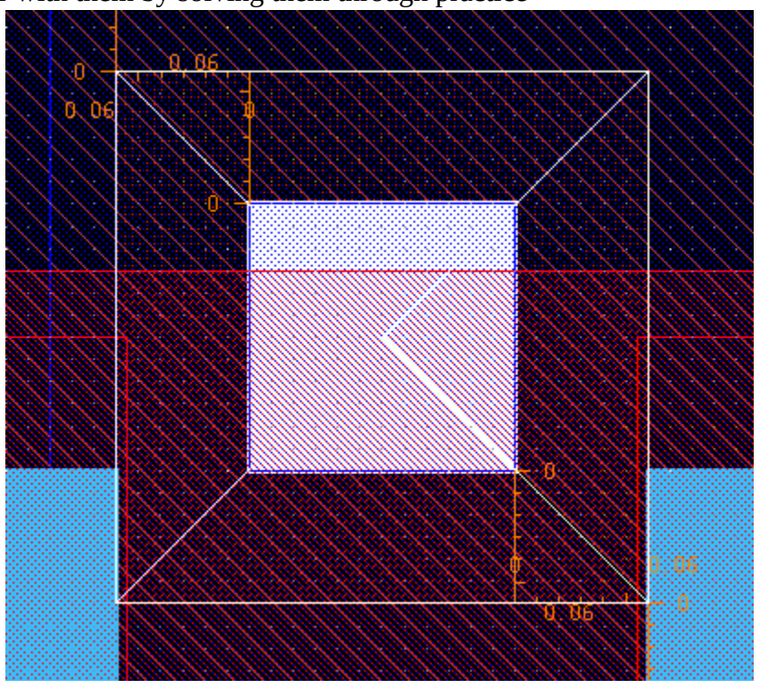
Click **Yes**.

4. **'Error layer Window'** (ELW) appear as shown below with inverter layout window which shows the errors.



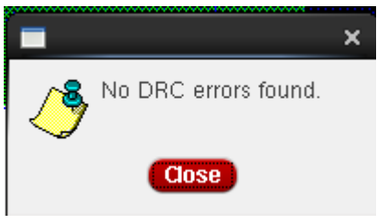
5. To correct the errors, find the error location by clicking on the error and then clicking on the right arrow key on ELW. To hide all the errors, click on **'NV'** (no Layers visible) button. The particular error in the following figure is due to a lower than 0.06 µm area for the Oxide. Correct the size of the Oxide by using the ruler and stretch tool. Similarly, do this for all errors

in your layout. No one can list all the errors one may commit, try correcting one after another and be familiar with them by solving them through practice



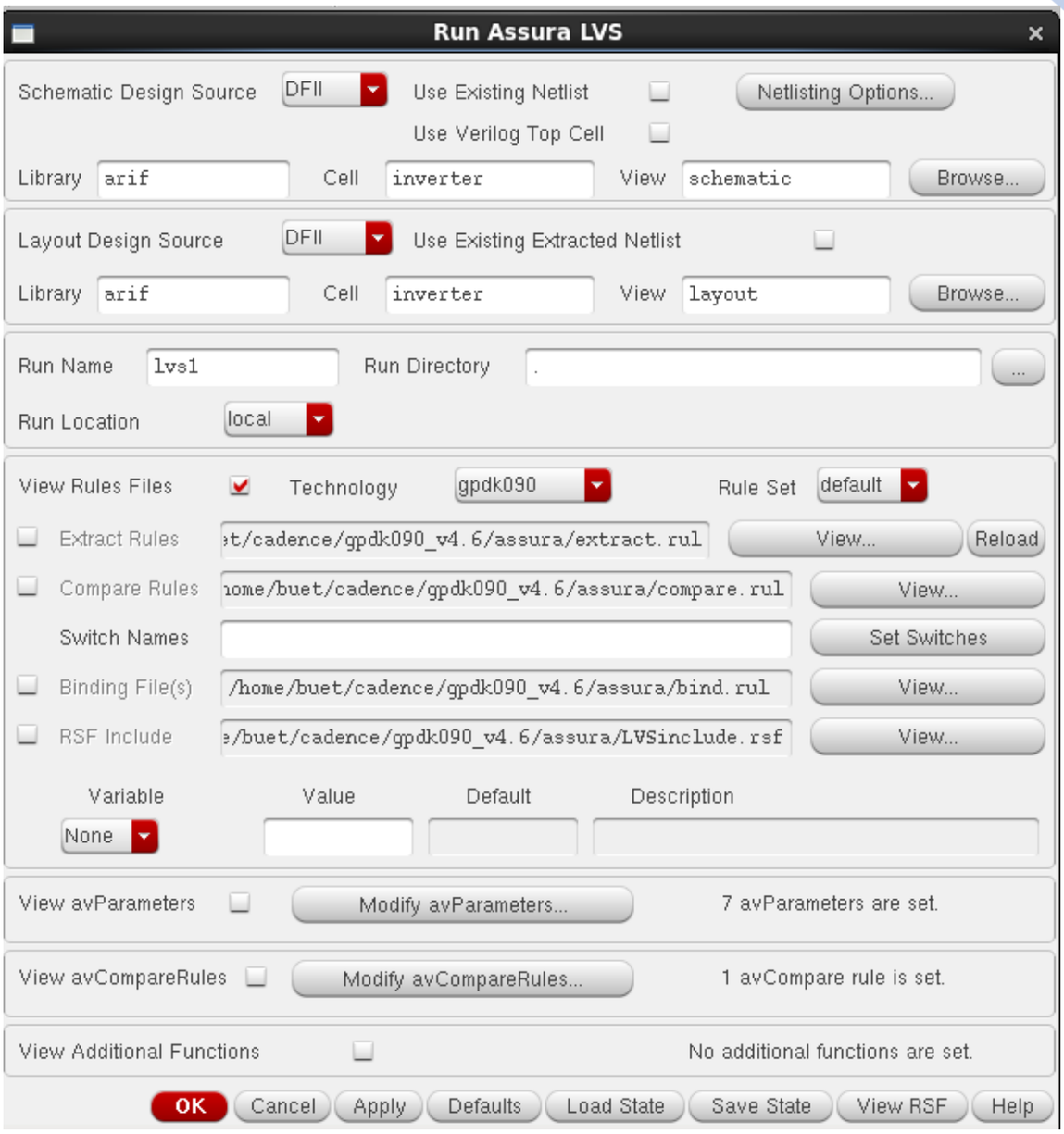
After correcting all the errors, run the DRC again.

6. If your design is error free, you should get the following message.

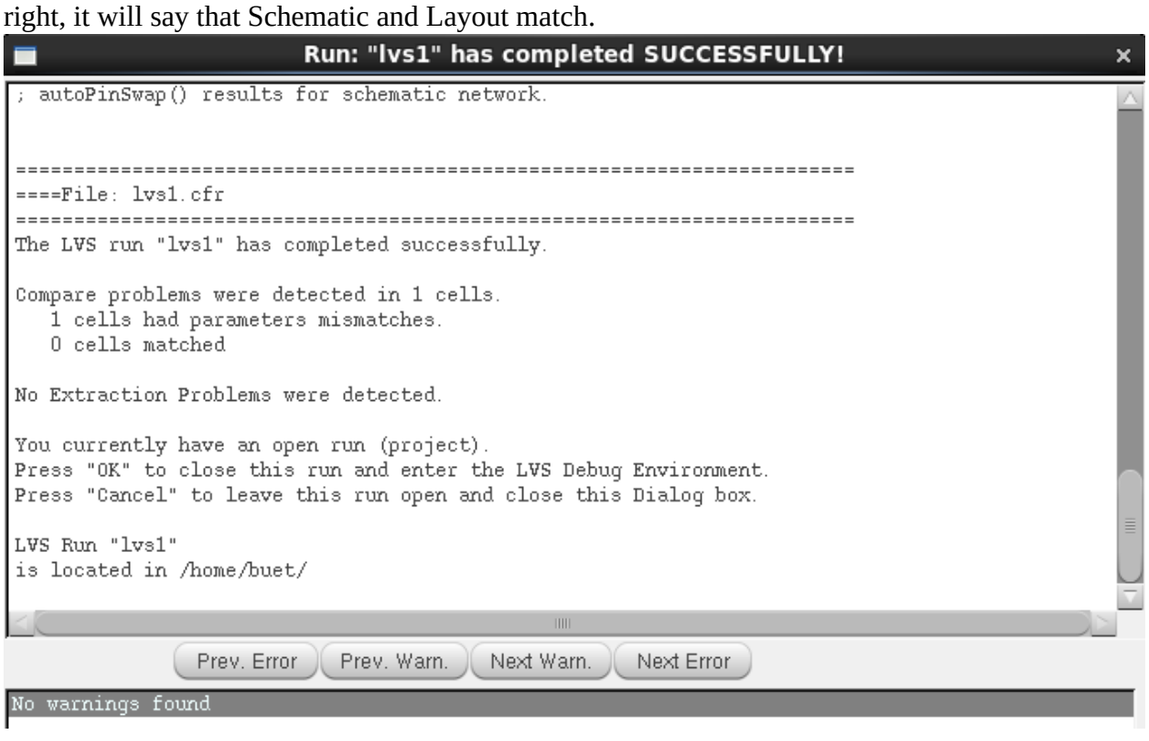


LVS USING ASSURA:

1. Execute **Assura > Run LVS**. Select gpdk090 and give a **Run Name**. Click **OK**.

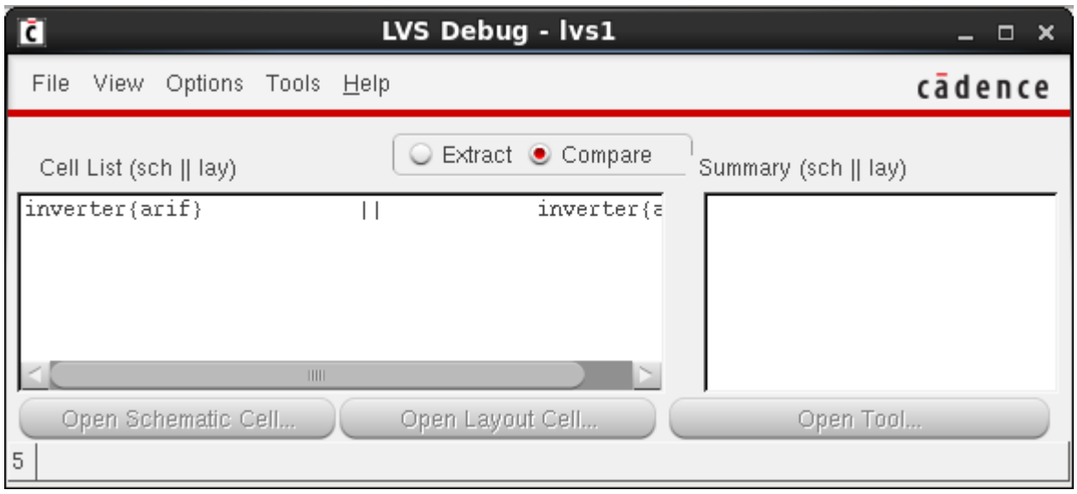


2. After completion of **LVS** run, you will get a result window. If you have done everything right, it will say that Schematic and Layout match.

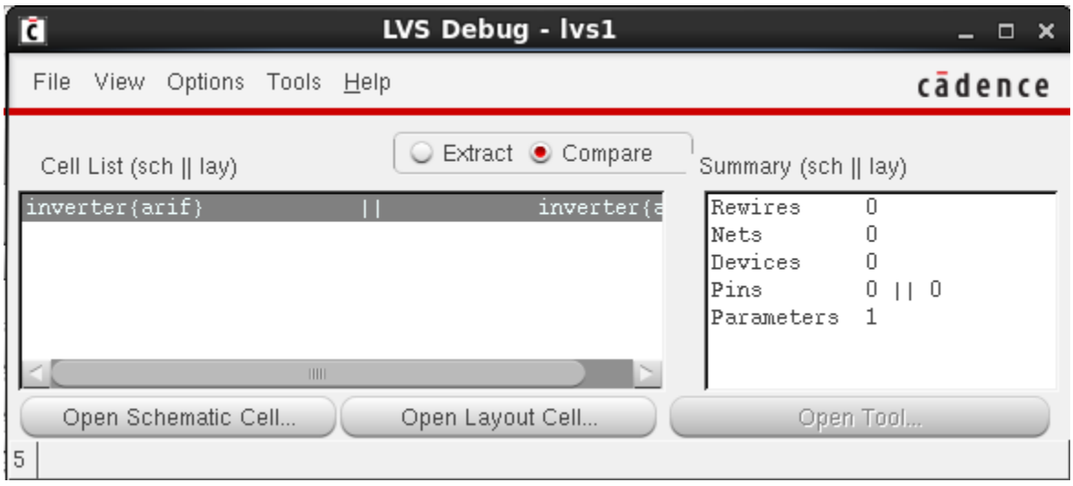


Note that, LVS report says that 1 cell had parameter mismatch. That means one cell had two

different dimensions in schematic and layout. Click **OK**. **'LVS Debug'** window will appear:

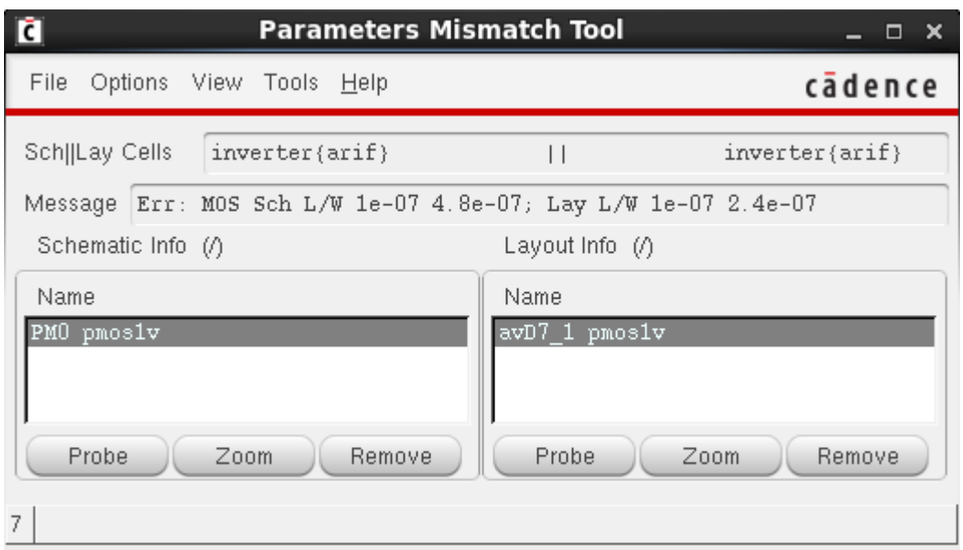


3. Select inverter {arif}. Notice that the summary window now shows the list of errors.

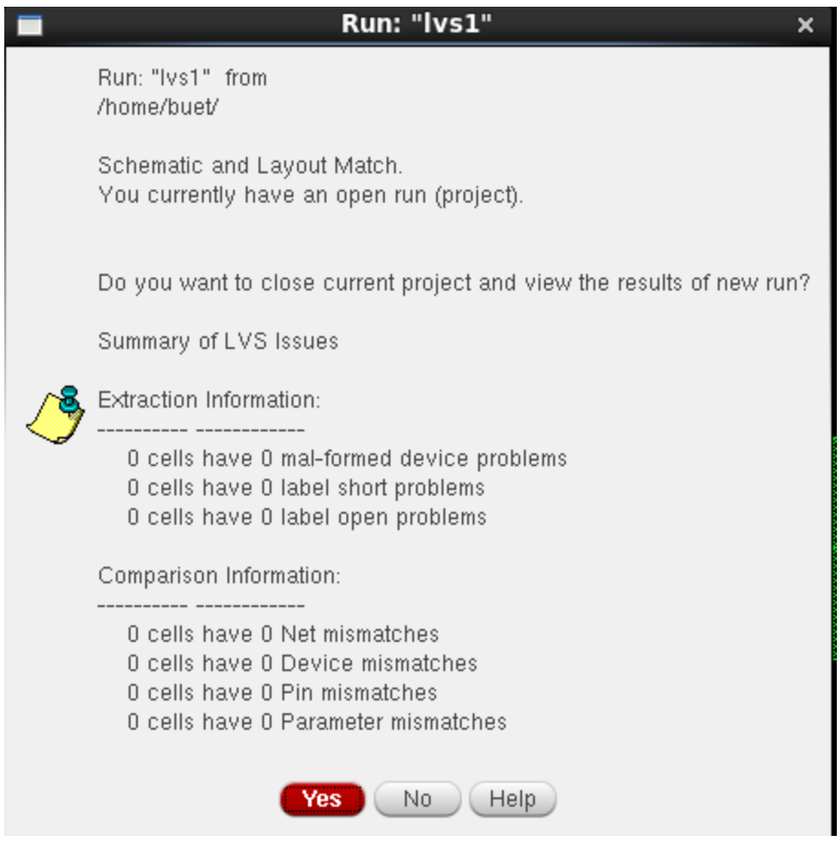


Click on **Parameters** and **Open Tool**.

4. 'Parameters Mismatch Tool' will open. Select PMO pmos1v. Now in the **Message** box, you can see the mismatch error.

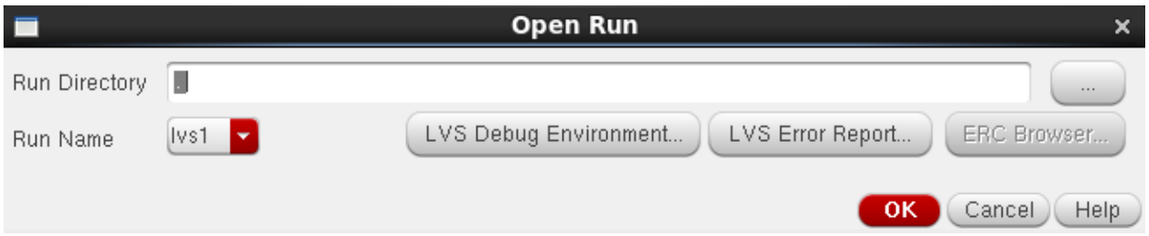


5. Change the width of PMOS to the value of width in layout and run LVS again. This time you will get an LVS match.

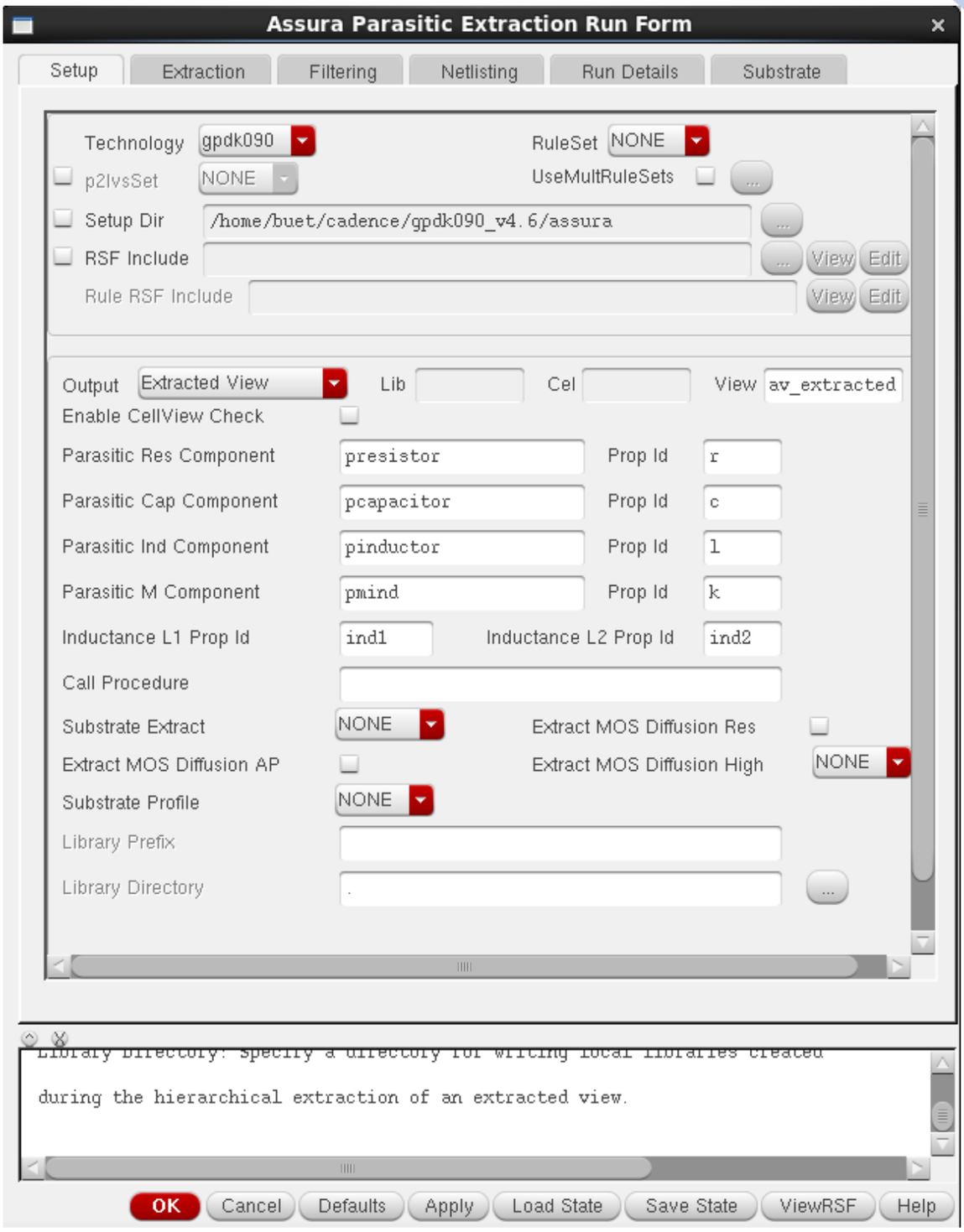


RCX USING ASSURA:

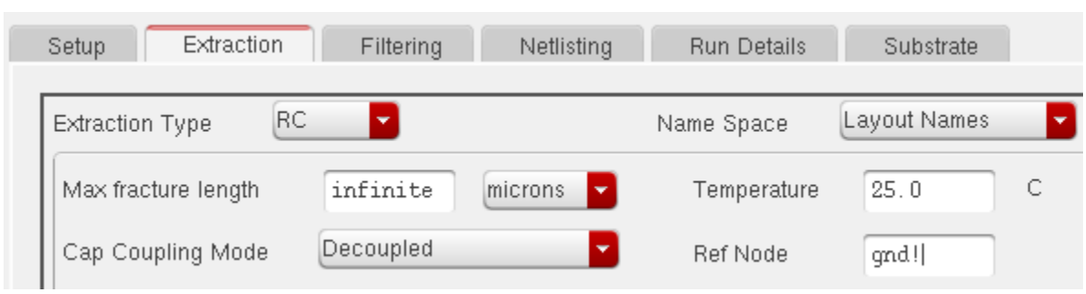
1. Execute **Assura > Open Run**. Select the final error free LVS run name in the run name field (it automatically loads the last LVS run). Click **OK**.



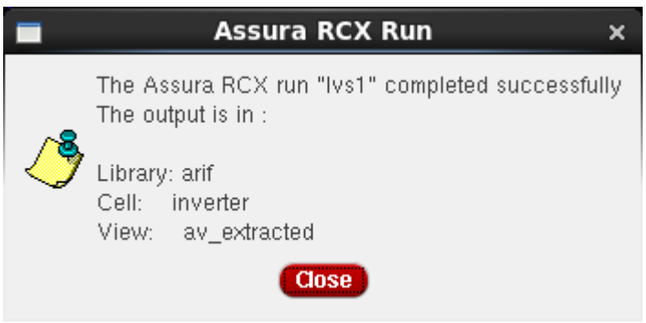
2. Execute **Assura > Run RCX**. Select **Extracted View** in the output field under **Setup** tab.



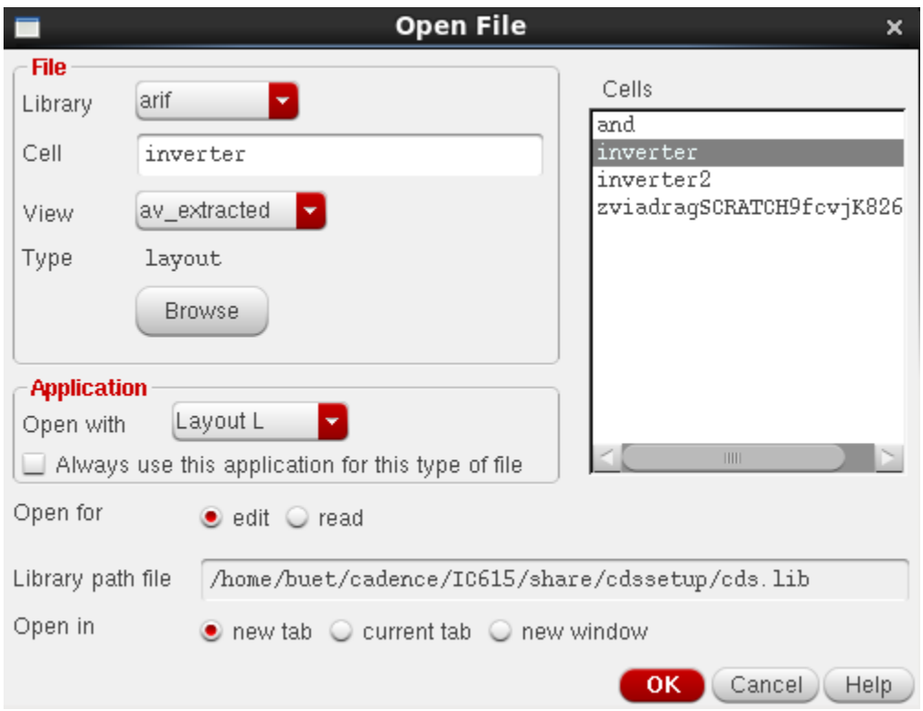
3. Go to **Extraction** tab. Select **RC** as **Extraction Type** and put the name of your reference node (**gnd!** in the given case) and click **OK.**



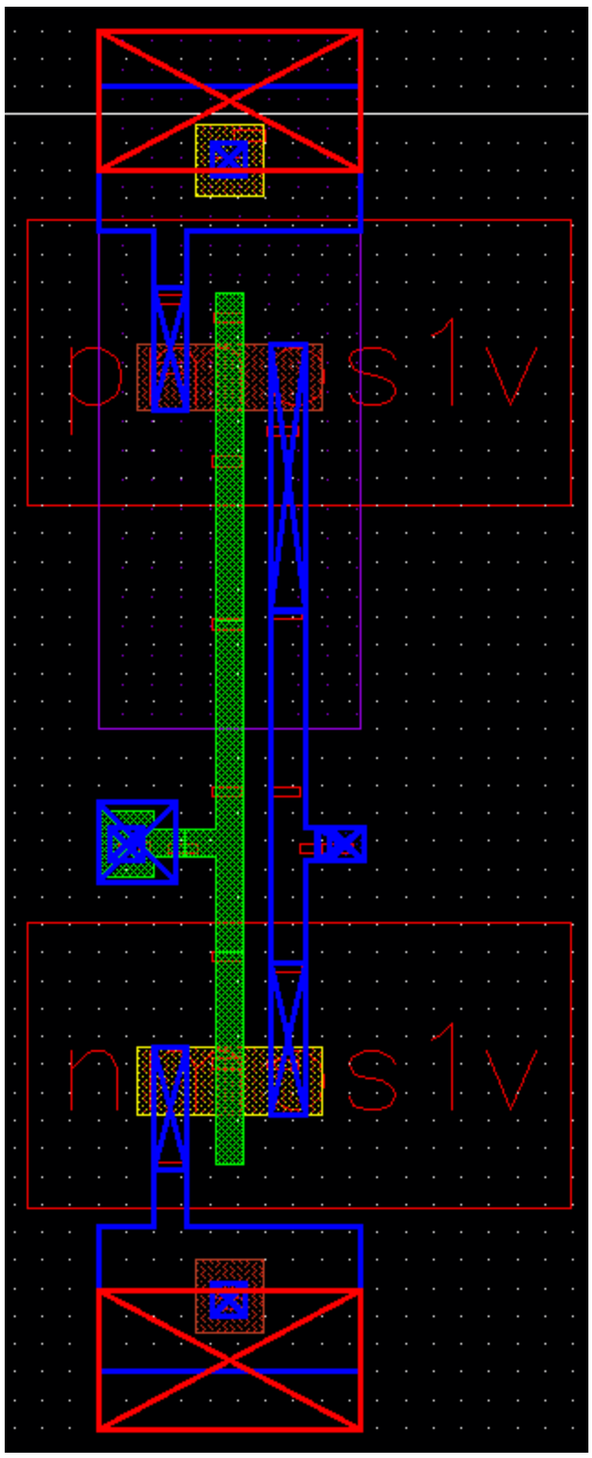
4. After completion of the run, you will get the following message:



5. Execute **File > Open** and fill in the form as follows. Click **OK.**



The extracted view will open.



6. Now launch ADE L from the **av_extracted** view and setup everything other than outputs to be plotted in the same way as you have done in Lab 1. After setting everything else, execute **Outputs > To be plotted > Select on design**. Go to **av_extracted** view. Click on the **in** pin location on that view. The following window will appear. Select pin name **in** and click **OK**. Do the same for **out** pin.

7. Now run the simulation and observe the output waveforms. Then measure the power and delay using waveform calculator. Delay should be 116ps and maximum power draw should be 38.5µW.

HOME TASK:

1. Analyze the effect of parasitic RC elements on the power consumption and propagation delay of an inverter.

Rubrics:

Criteria	Below Average (1)	Average (2)	Good (3)
Formatting	Report is not properly formatted, missing objectives, discussions and references.	Report is somewhat formatted but missing proper references.	Report is properly formatted.
Design	Design steps are somewhat followed and results have errors.	Design steps are properly followed and the results are flawless.	
Writing	Writing is poor and not informative. It does not address the design decisions and contains high plagiarism.	Writing is average and original. Design decisions are somewhat explored.	Writing is excellent with every design decision adequately explored.
Diagram	Diagrams are of bad quality and unreadable.	Diagrams are clear and of high quality.	