CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Telecommunication Engineering

VLSI Technology Sessional

ETE 404

Experiment No:08

Hierarchical Design of AND Gate Using a NAND Gate and a NOT Gate

---

Submitted by:

Shamanza Chowdhury

ID: 1908008

Submitted to:

Arif Istiaque Rupom

Lecturer

Dept. of ETE,CUET

October 6, 2024

1 Objectives:

- To familiarize with hierarchical design.
- To perform schematic-level verification, layout generation, DRC and LVS.
- To perform post-layout simulation of top-level design.

2 Apparatus:

- **Software:** VMware Workstation v10
- **Hardware:** PC

3 Design Process:

3.1 Schematic Entry:

- A new cell view named ”AND” was created in the CIW to intiate the hierarchical design process.
- The previously designed NAND gate and inverter symbols were instantiated from the library.
- Input and output pins were added appropriately to form an AND gate at the schematic level.
- The final schematic was saved and verified for connection accuracy.The schematic diagram of a AND gate is given below:

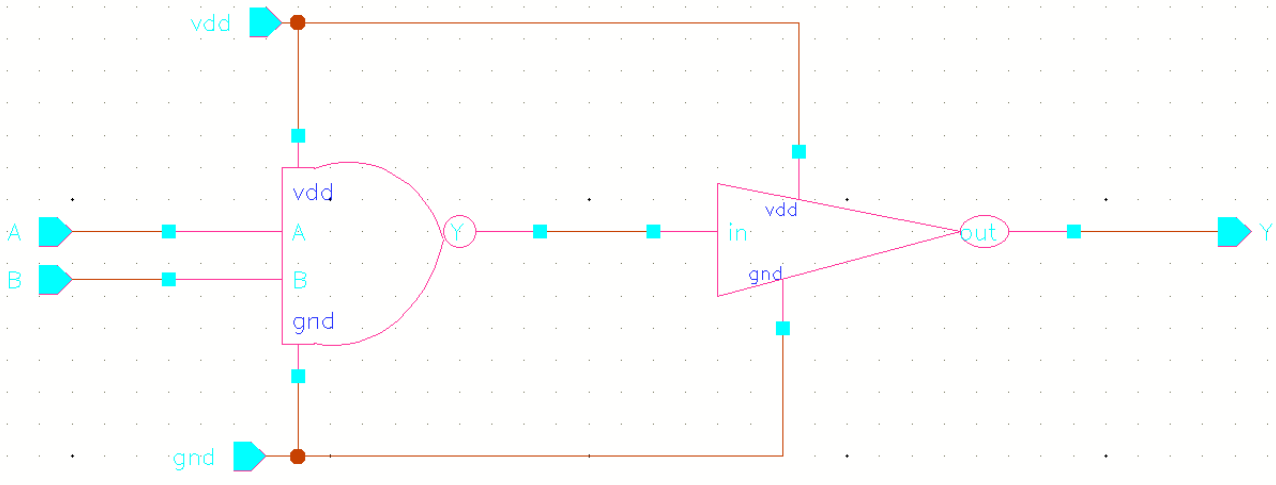

Figure 01: Schematic diagram of an AND gate.

3.2 Symbol Creation:

- A symbol was generated from the newly created AND gate schematic to facilitate its use in higher-level designs. The symbol of a AND gate is given below:

Figure 02: Symbol of an AND gate.

3.3 Schematic-Level Simulation:

- Analog analysis was performed by launching the ADE L simulation environment.
- The stimuli for inputs A and B had been configured such that the pulse width and period of input B were set to be half of those for input A.
- The simulation had been executed, and the expected output waveform had been generated, showing the results for all input combinations. The output of an AND gate is given below:

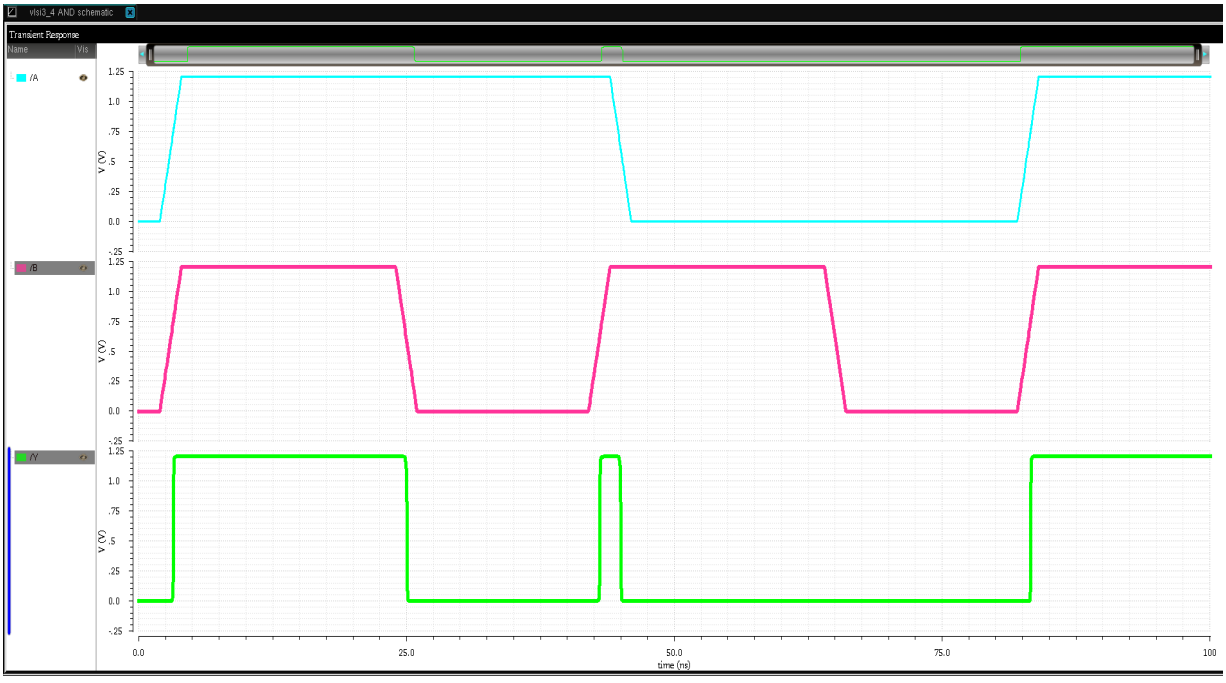

Figure 03:Output waveform of an AND gate.

- A small glitch appears at the output of the AND gate due to unequal delays in the two input paths. When input A transitions from high to low, input B takes some time to switch to high because of the inverter delay. As input A falls but remains above the NMOS threshold of 1V, the NMOS transistor connected to A stays on. Meanwhile, input B has already risen above 1V, turning the NMOS transistor connected to B on as well. During this overlap, both NMOS transistors conduct briefly, causing a glitch at the AND gate's output

3.4 Layout Generation:

- Layout XL was launched from the schematic view of the AND gate.
- Instances of the NAND and inverter were generated and placed in the layout window.
- Display options were adjusted to visualize the layout properly.
- The individual components were then interconnected as required to implement the AND gate layout.

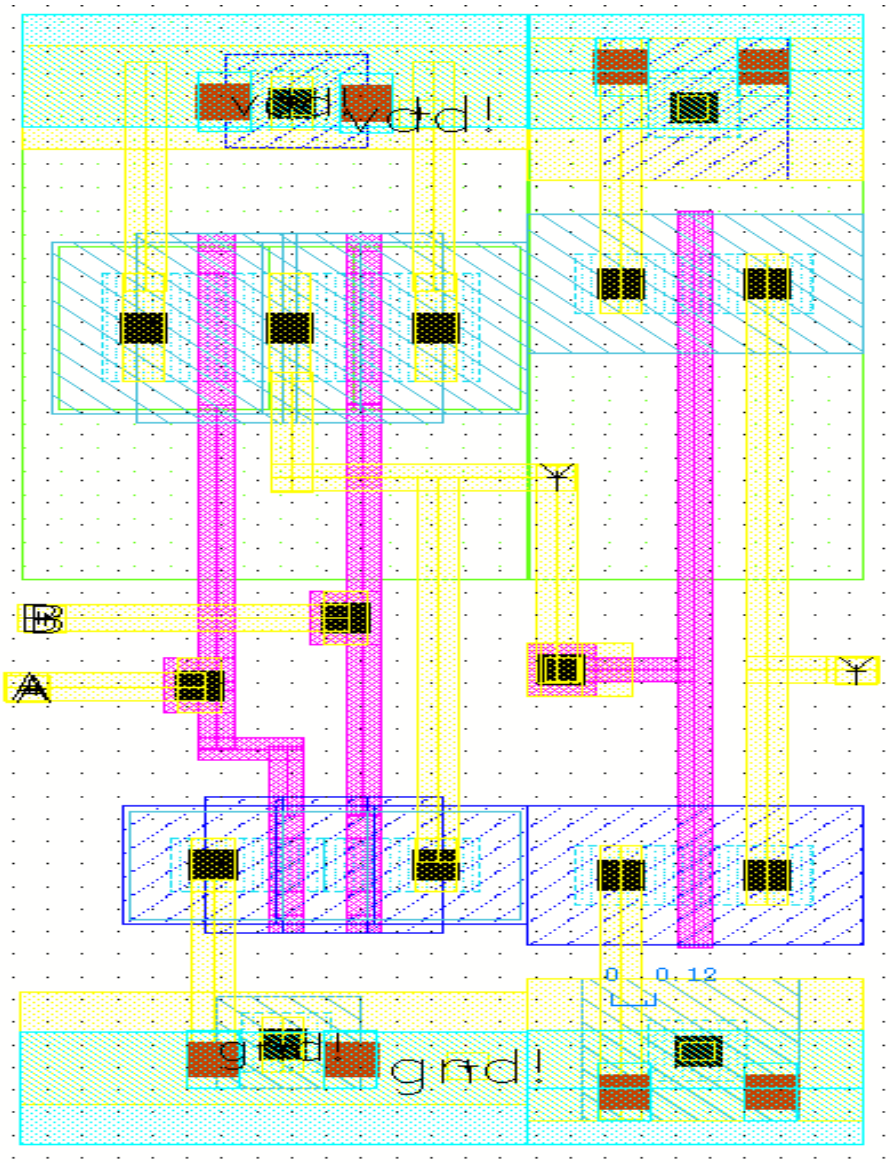

Figure 04:Layout of an AND gate.

3.5 Design Rules Check (DRC) Verification:

- Design Rule Check (DRC) was performed to ensure that the layout adhered to the foundry's design rules.
- The errors identified during the DRC run were corrected, and a successful DRC completion was achieved.

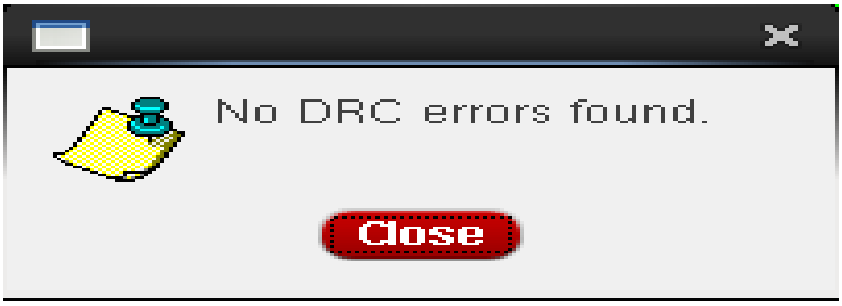

Figure 05: DRC Completion Window.

3.6 Layout vs. Schematic (LVS) Verification:

- Layout vs. Schematic (LVS) verification was conducted to ensure that the netlist generated from layout matched the schematic design. Any mismatch errors were resolved by verifying the interconnections and pin placements.

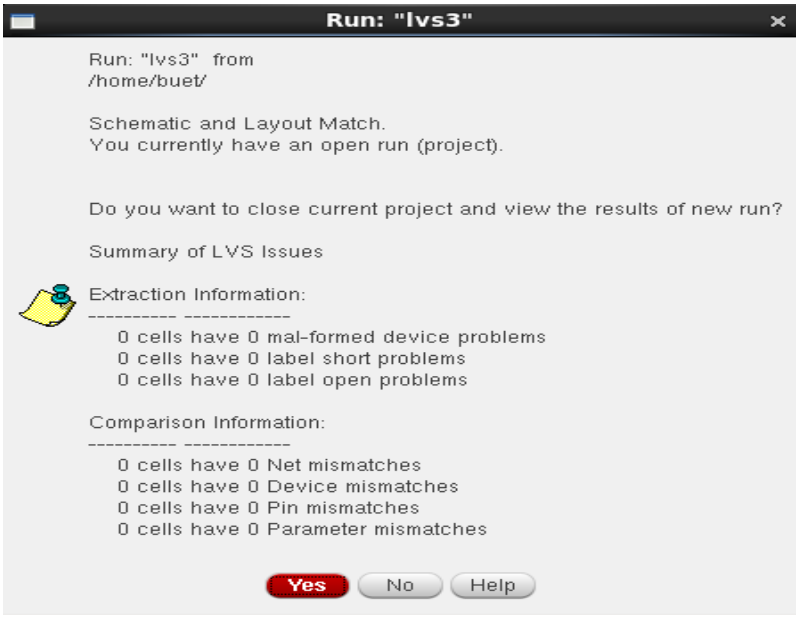

Figure 06: LVS Completion Window.

3.7 RCX Verification:

- After the final error-free LVS run, parasitic resistance and capacitance extraction (RCX) was performed to create an extracted view of the layout, which included parasitic elements.

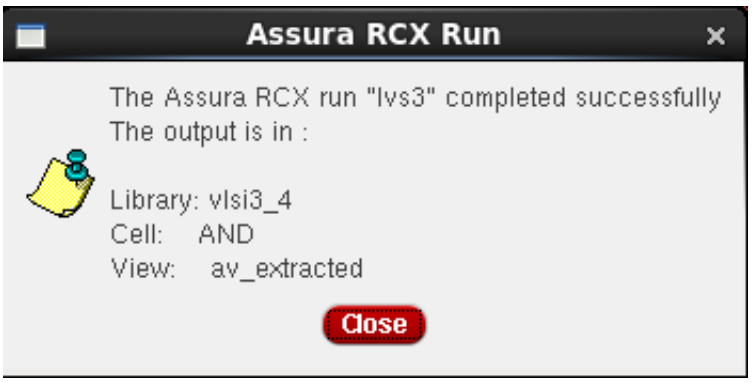

Figure 07:RCX Completion Window.

- Upon completion, the extracted view was opened using File > Open.

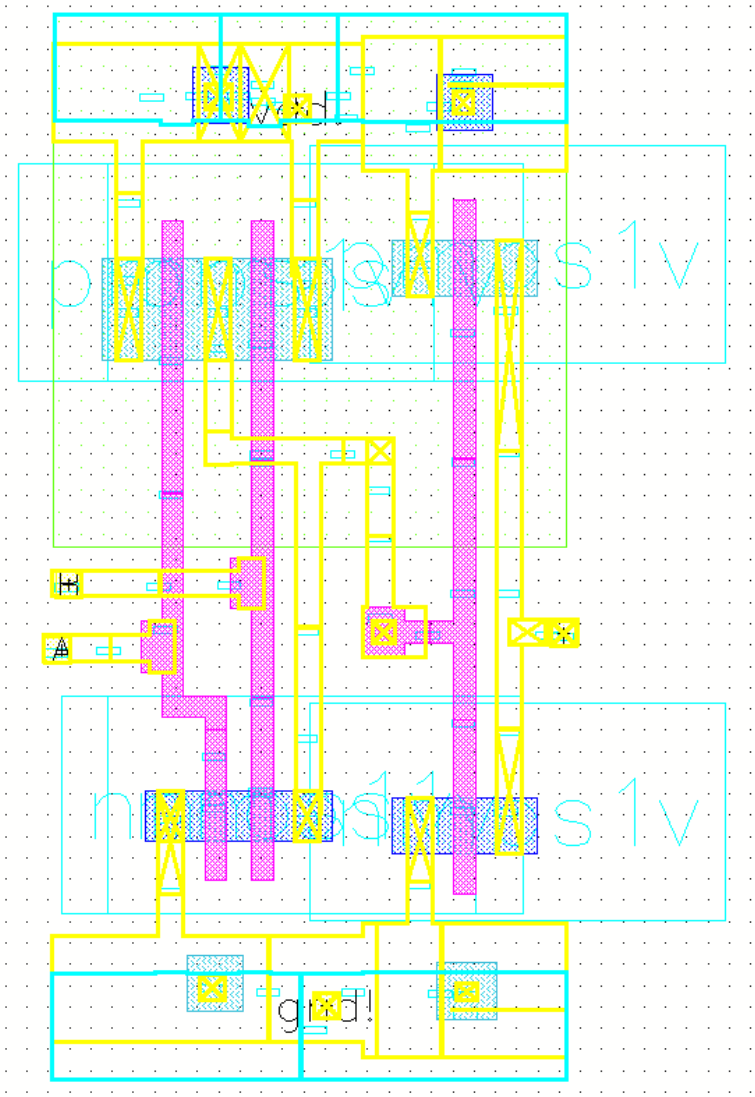

Figure 08:Extracted view of the AND gate.

3.8 Post-Layout Simulation:

- The av_extracted view was opened for post-layout simulation. Inputs were applied to the AND gate, and the output waveform was analyzed to ensure that the circuit's behavior matched the expected functional-

ity.

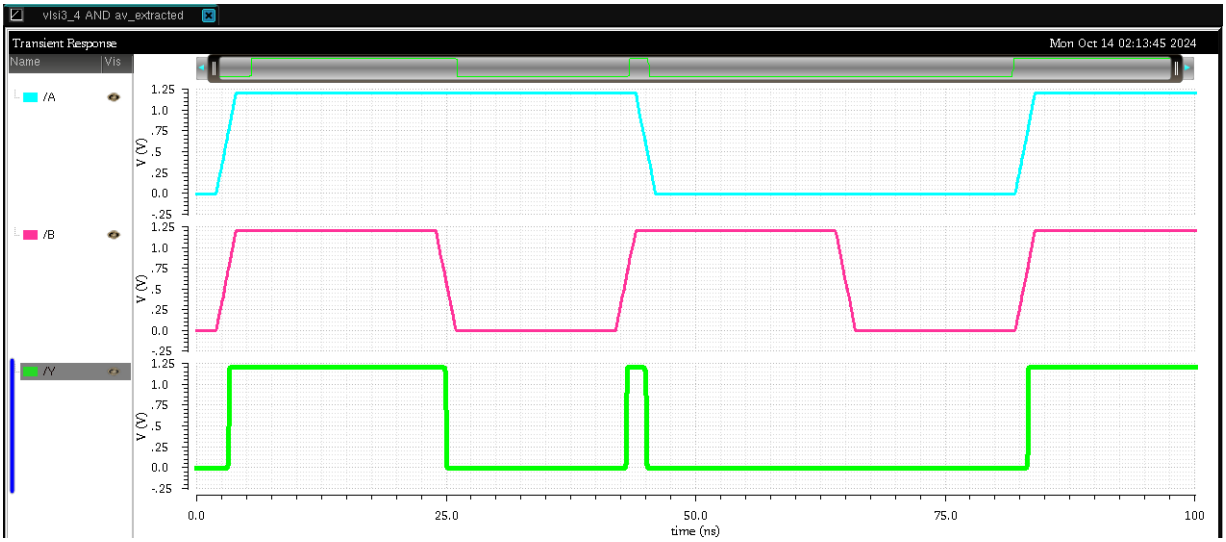

Figure 09:Output waveform of an AND gate.

- A small glitch appears at the output of the AND gate due to unequal delays in the two input paths. When input A transitions from high to low, input B takes some time to switch to high because of the inverter delay. As input A falls but remains above the NMOS threshold of 1V, the NMOS transistor connected to A stays on. Meanwhile, input B has already risen above 1V, turning the NMOS transistor connected to B on as well. During this overlap, both NMOS transistors conduct briefly, causing a glitch at the AND gate's output.

4 Discussion:

- In this experiment,the hierarchical design of the AND gate was successfully carried out by using a previously created NAND gate and an inverter.
- Schematic-level verification ensured that the logic of the AND gate was correct, while the layout generation involved connecting the pre-designed layouts of the NAND gate and inverter.
- The DRC and LVS checks helped to identify and resolve any layout inconsistencies or rule violations.
- After correcting minor errors in the layout, the design passed all verification steps.
- Parasitic elements were extracted, providing insights into their impact on the AND gate's performance.
- The transient analysis of the extracted view confirmed that the AND gate operated as expected, with the output being a correct logical AND of the inputs.
- Overall, this experiment demonstrated the importance of hierarchical design techniques, along with meticulous verification and extraction processes, to ensure correct functionality and performance in VLSI circuits.