DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY

CHATTOGRAM – 4349, BANGLADESH

Experiment No. 4

DC Analysis and Symbol Creation of Inverter and AND Gate

PRECAUTIONS:

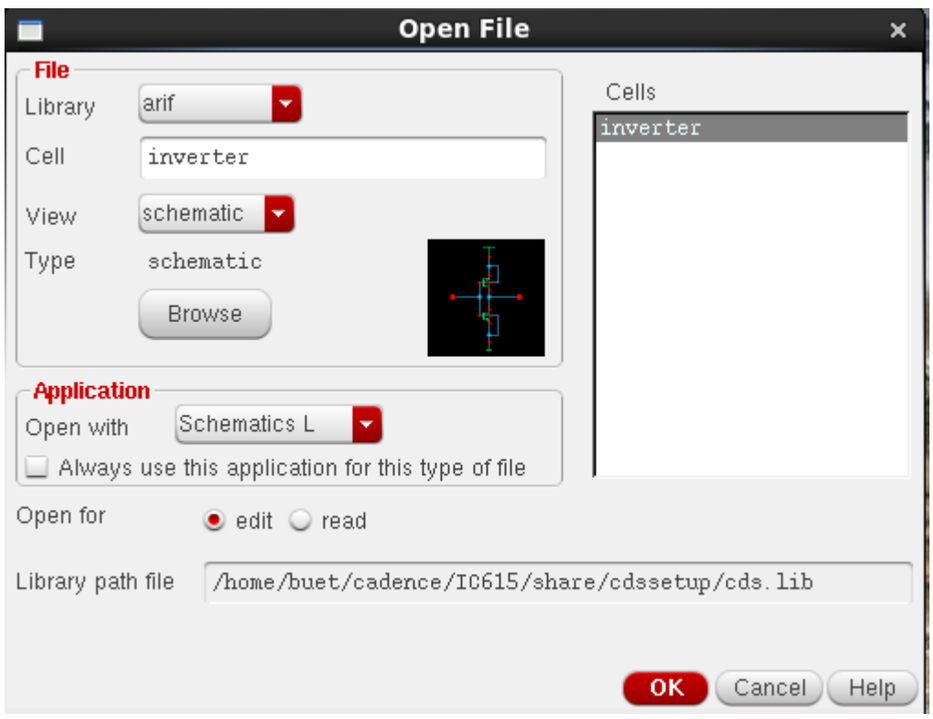
- Students must carefully read the lab manual before coming to lab to avoid any inconveniences.
- Students must carry a flash drive to transfer files and lab manuals.
- Use of mobile phone in lab is strictly prohibited and punishable offence.
- Experiment files must be uploaded to GitHub including home tasks.

OBJECTIVES:

- To familiarize with DC sweep and parametric simulation in ADE L.
- To familiarize with symbol creation from schematic view.

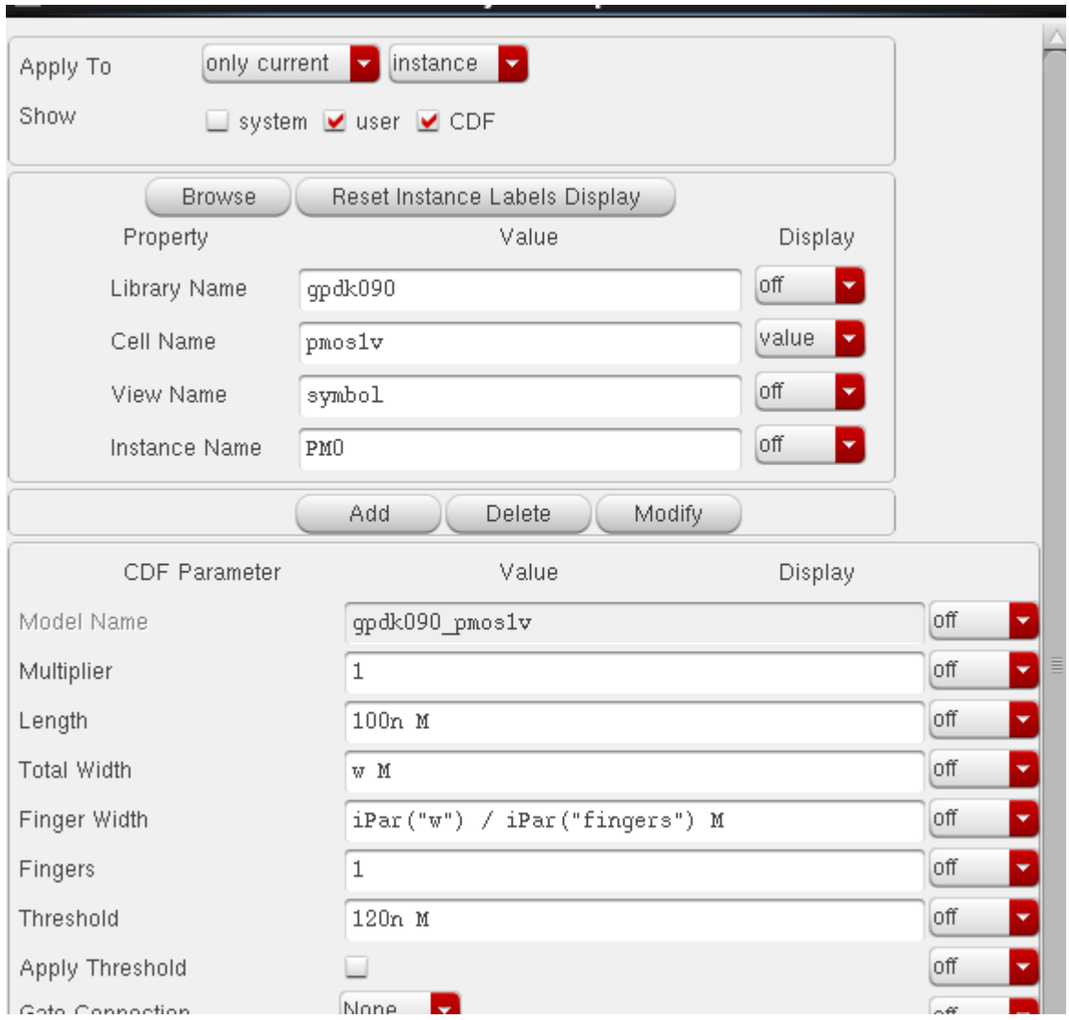
DC SIMULATION:

1. Start by turning on the Cadence VM and starting Virtuoso by typing **'virtuoso'** on the terminal.
2. Execute **File > Open** in **CIW**. In the 'Open File' windows, select the inverter schematic you previously built in your library.

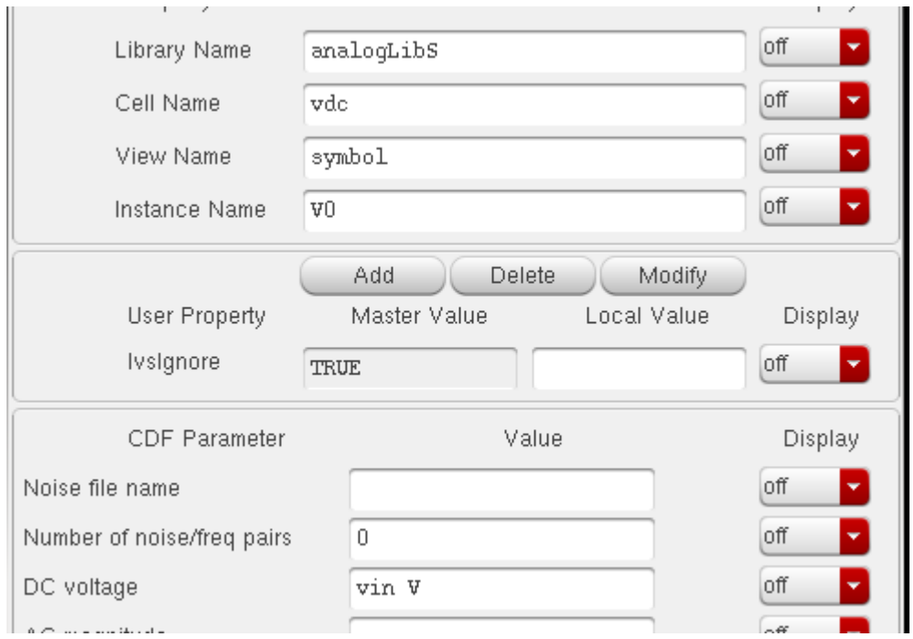


3. The schematic editor window will open. Execute File > Save a Copy. In the following window, change the name of the cell to inverter2. Click OK. Close the schematic editor window and open the inverter2 cell from CIW.

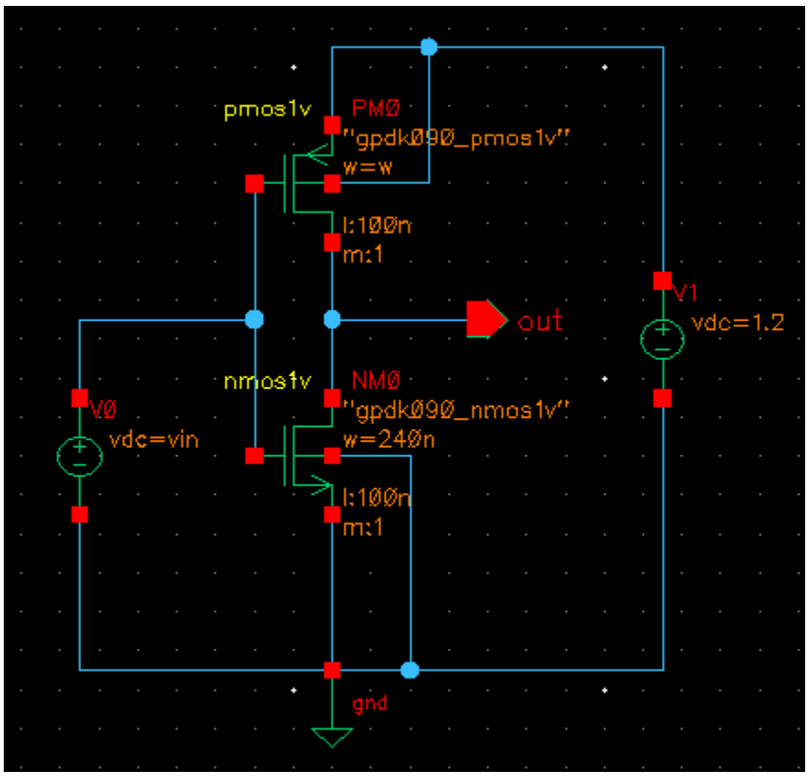
4. This time we will perform both DC and parametric simulation at the same time on the inverter schematic. We will obtain the transfer characteristics curve (TCC) of the inverter from DC simulation and by varying the width of the PMOS transistor; we will observer its effect on the transfer characteristics.
   Select the PMOS transistor in the schematic editor window, click 'q' or right click the body and click 'Properties'; the Edit Object Properties window will open. Place ***w*** under 'Total Width' and press tab on keyboard. The 'Finger Width' field will be changed automatically.



5. Place symbol of an instance vdc from analogLib on the schematic. Edit its properties and in the 'DC Voltage' field, type ***vin*** and press tab on the keyboard. Connect it between the 'in' and 'gnd!' terminals.

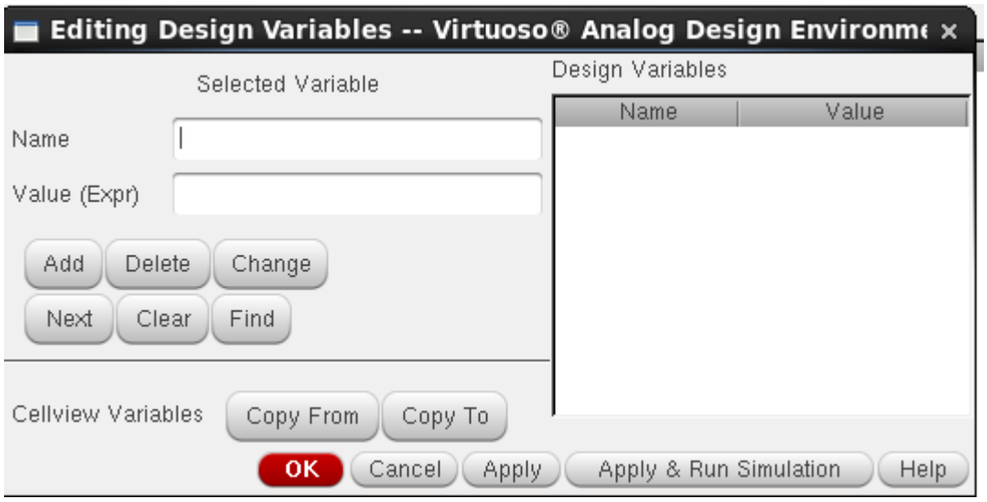


6. Now place another instance of vdc on the schematic. Edit its properties and in the ‘DC Voltage’ field, type **1.2** and press tab on the keyboard. Connect it between the ‘vdd!’ and ‘gnd!’ terminals. Now remove the input pin and the ‘vdd!’ instance. The final schematic should look like this:

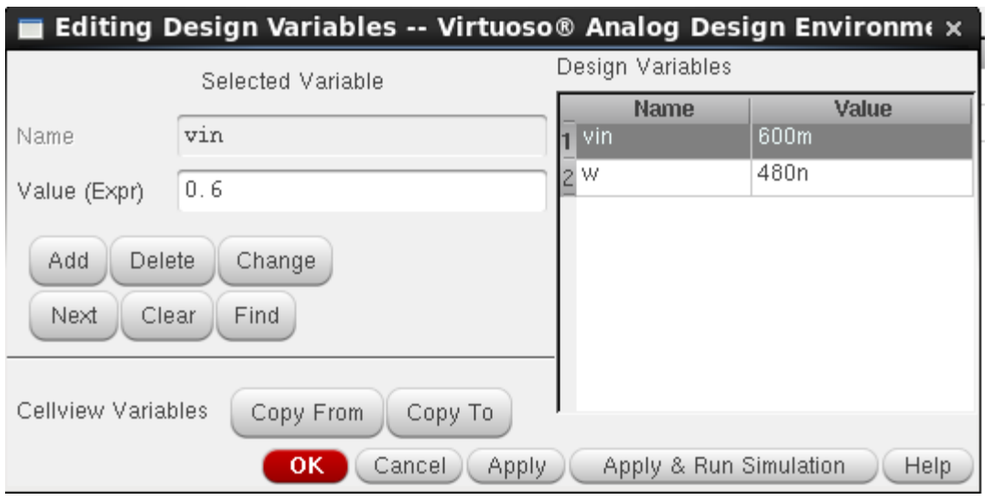


Click Check and Save.

7. Execute Launch > ADE L and setup Model Library to gpdk090_mos.scs and section to TT_s1v similar to previous lab.
8. Execute Variables > Edit and the following ‘Editing Design Variable’ window will open.

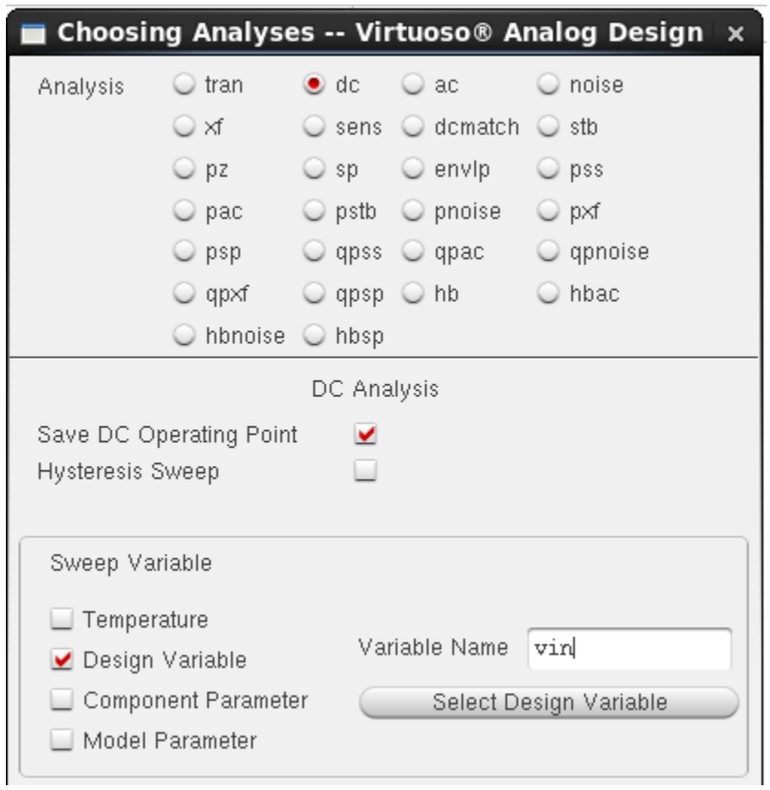


9. Select ‘Copy From’. You will see ‘w’ and ‘vin’ appear in the ‘Design Variables’ window. Click on ‘w’ and in ‘Value (Expr)’ field, put a default value of 480n. Click Apply. Similarly click on ‘vin’ and in the ‘Value (Expr)’ field, put a default value of 0.6. Then click OK.

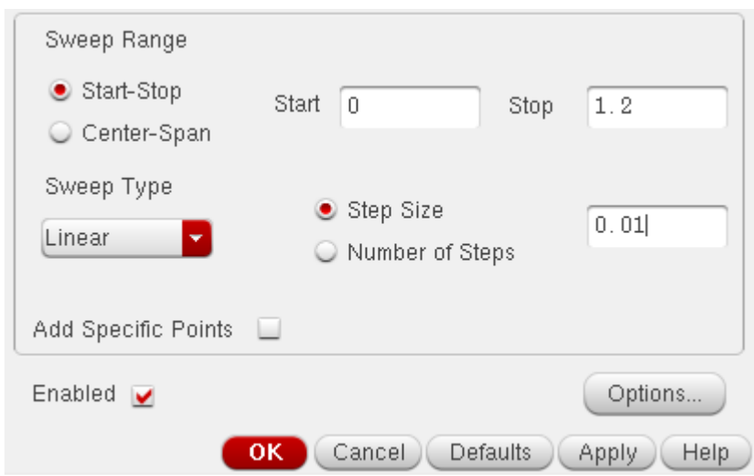


10. Execute Analysis > Choose and in the 'Choosing Analysis' form, select 'dc'. Click on 'Save DC Operating Point'.

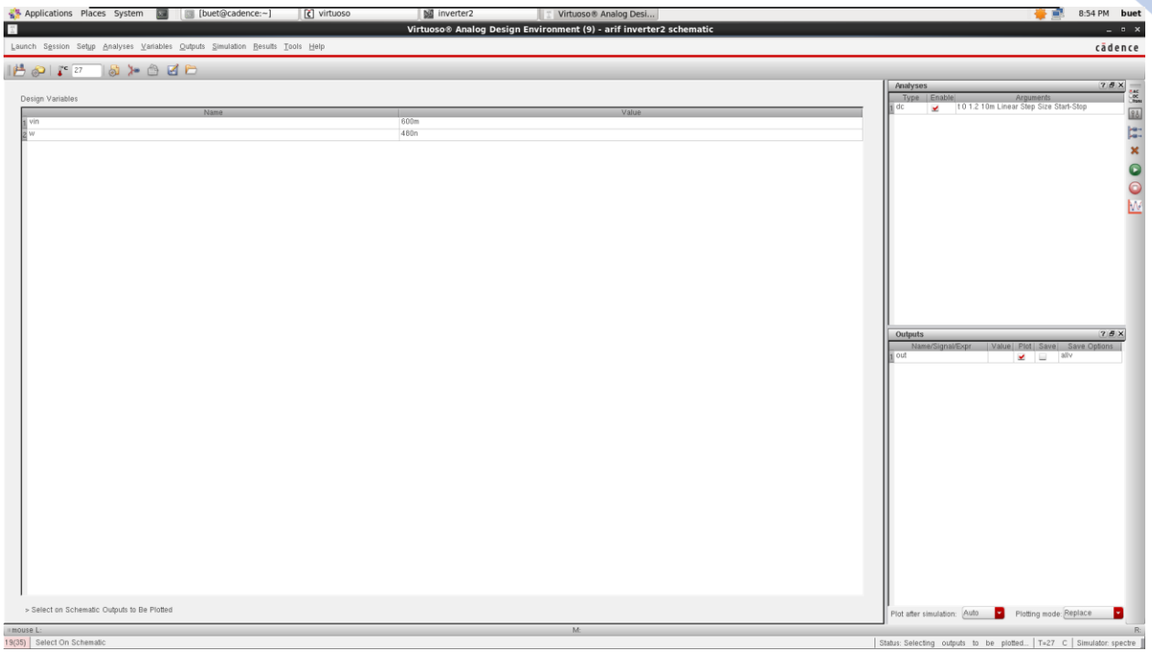
11. Under 'Sweep Variable', select 'Design Variable' and click on 'Select Design Variable'. Select 'vin' and click OK.



12. Under 'Sweep Range', select 'Start-Stop' and put a start value of 0 and a stop value of 1.2. Select 'Sweep Type' to be 'Linear' and 'Step Size' to be 0.01. Click OK.

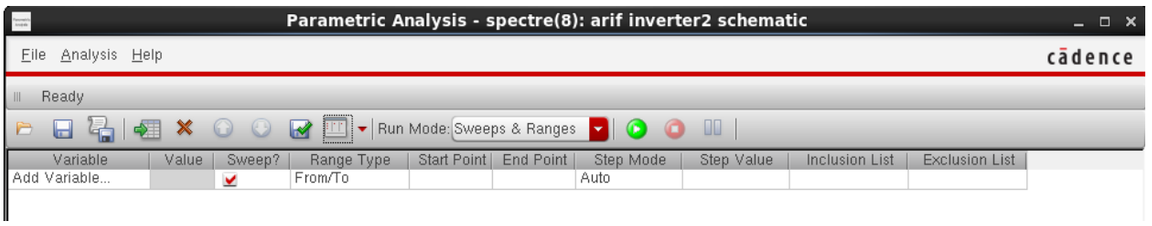


13. Execute Outputs > To Be Plotted and select 'out' pin from the schematic. ADE L should look like the following:

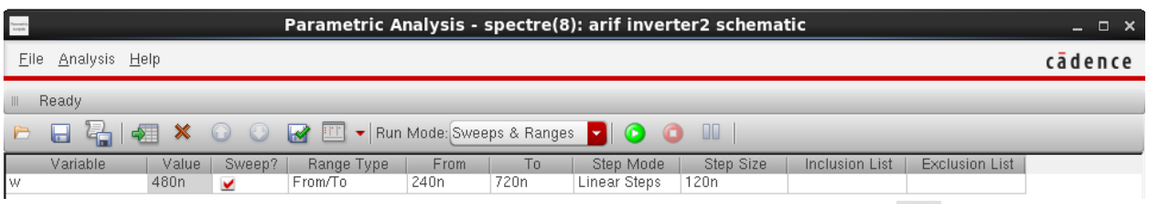


14. Execute Simulation > Netlist and Run to simulate a single TCC for the given default PMOS width of 480n.

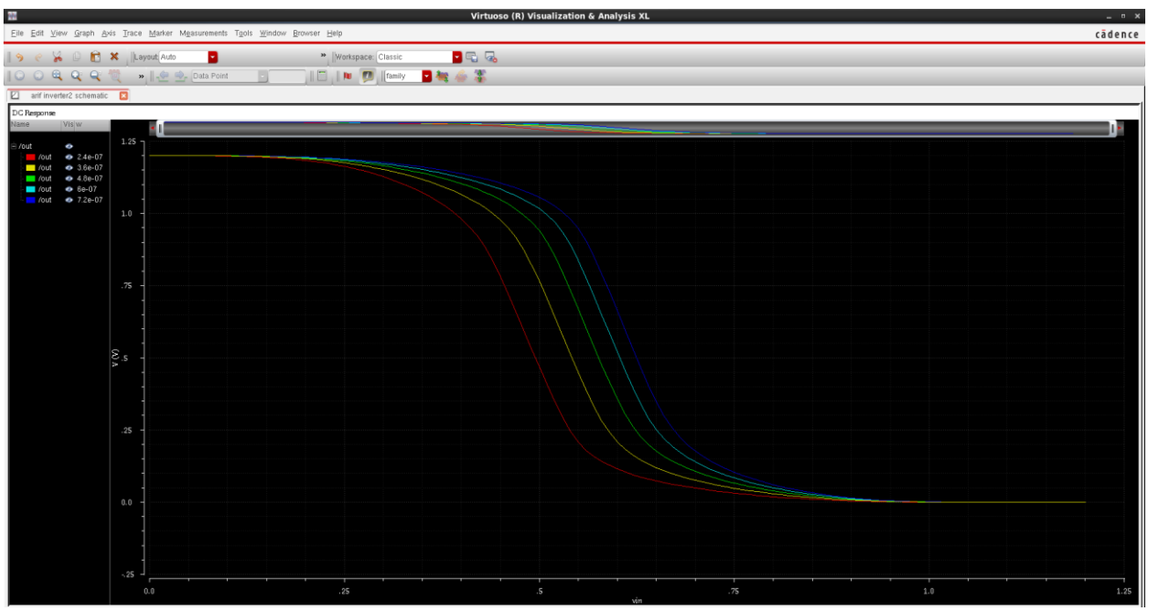
15. In ADE L, execute Tools > Parametric Analysis. 'Parametric Analysis' window will appear.



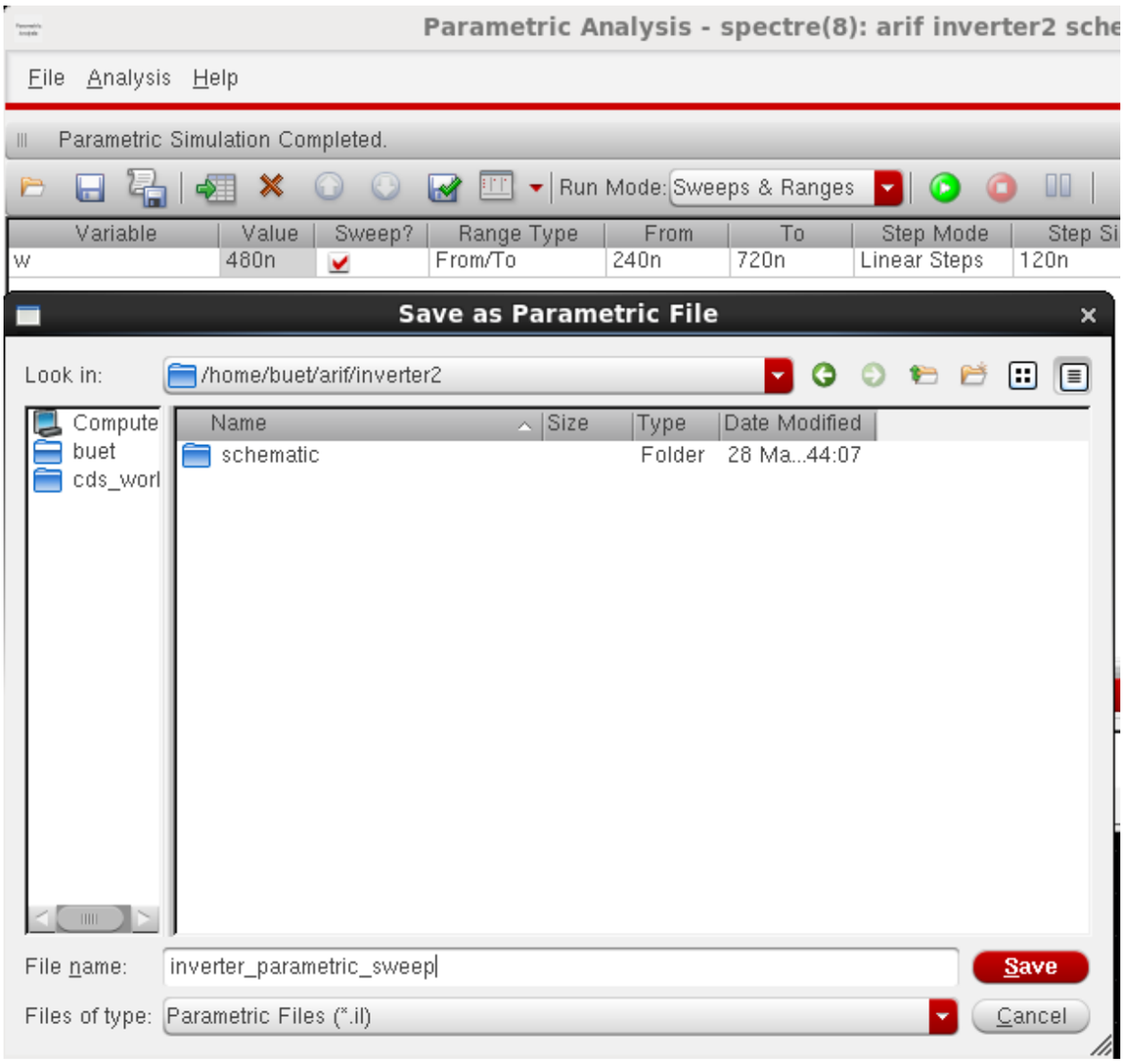
16. Click on 'Add Variable'. From the dropdown menu select 'w'. Put From: 240n and To: 720n. Select Step Mode: Linear Steps from the dropdown and put Step Size: 120n.



Now click on the green, 'Run Selected Sweep' icon to start the simulations.
The following waveforms will be displayed:



17. This parametric file can be saved for later use by clicking on the save icon. In the following windows, select appropriate destination path and an appropriate name and click Save.

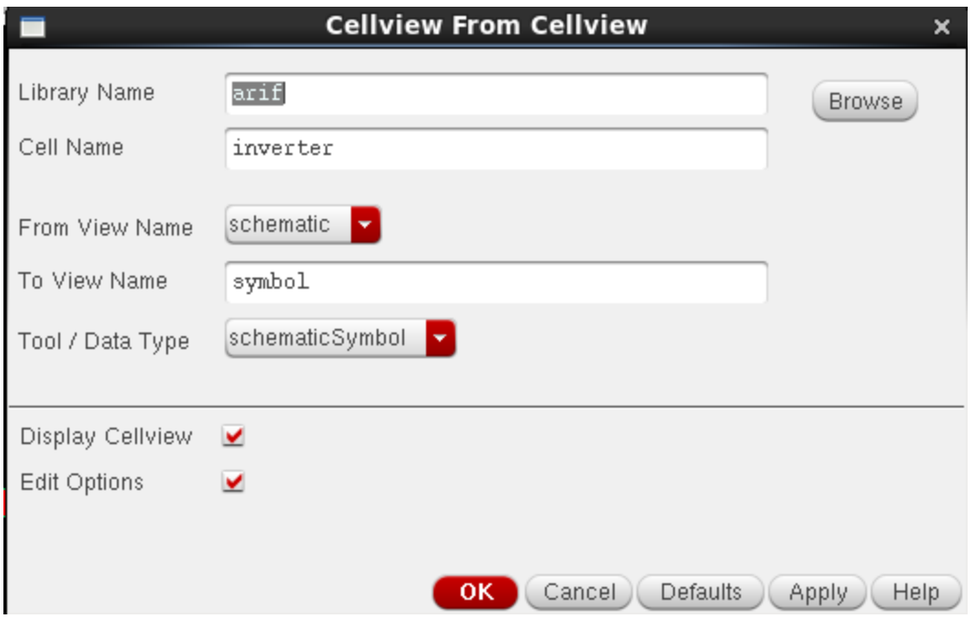


18. Also save the state of the ADE L window.

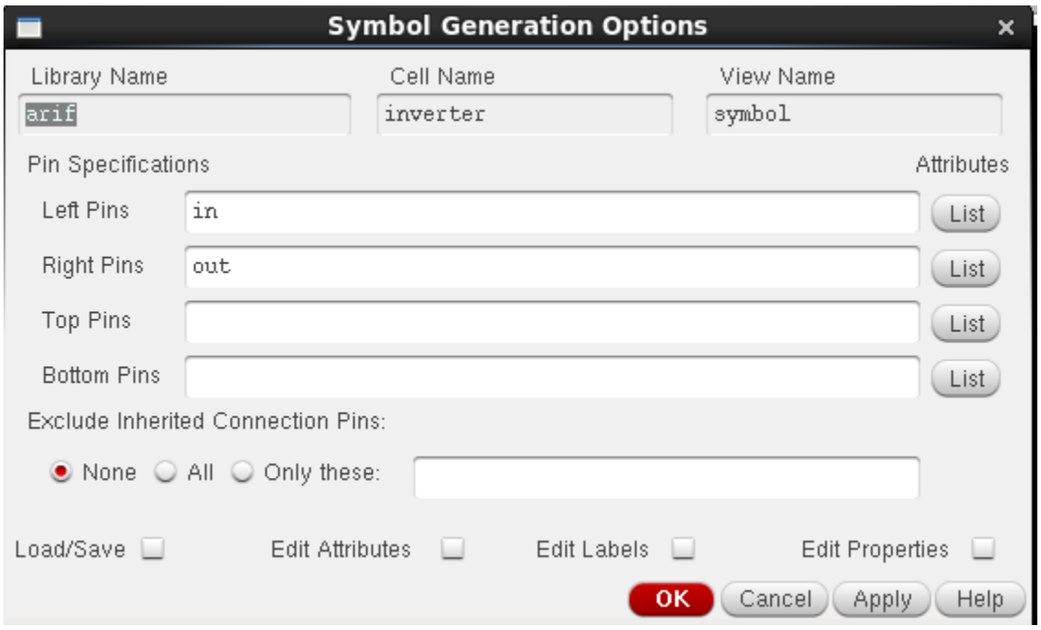
SYMBOL CREATION:

In this section, we will create a symbol for our inverter design so that we can use this symbol view for the schematic in a hierarchical design. In addition, the symbol has attached properties (cdsParam) that facilitate the simulation and the design of the circuit.

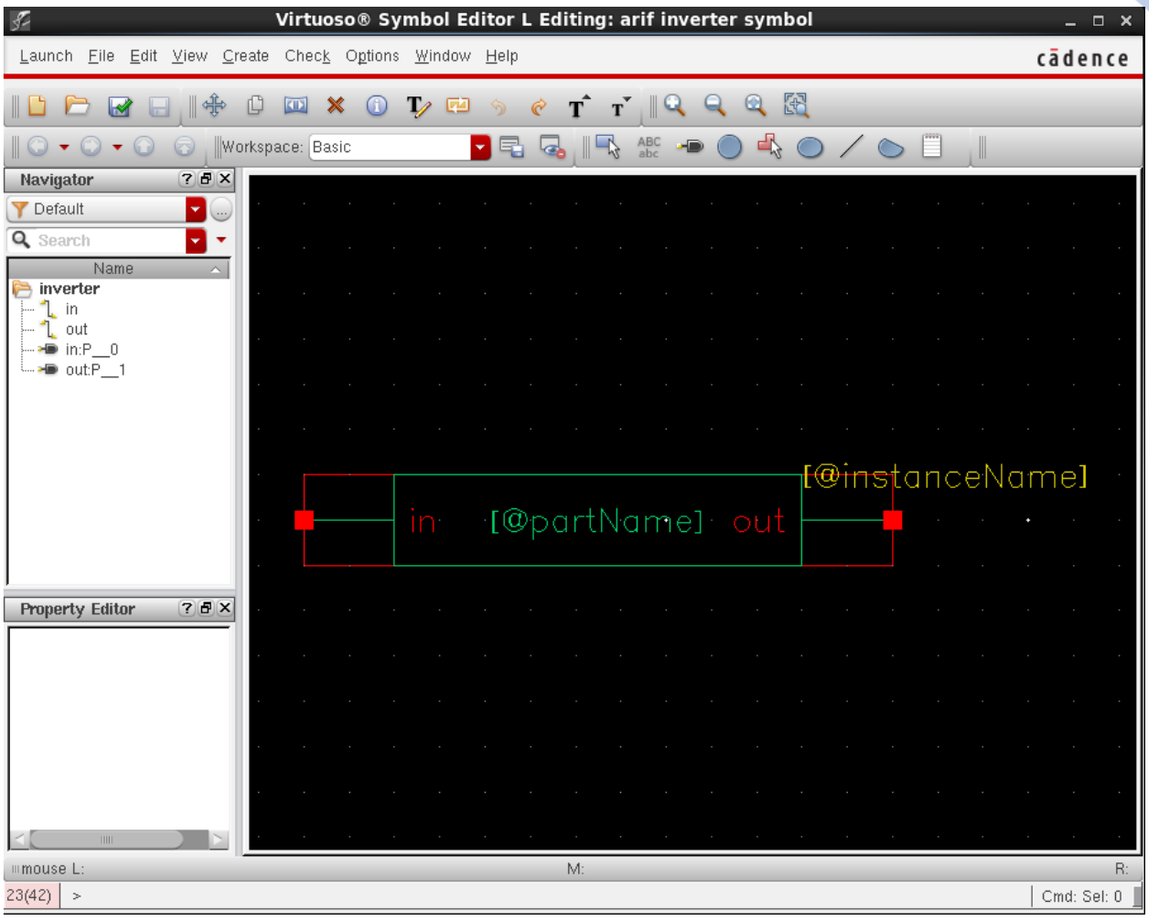
1. Open the schematic of the cell ‘inverter’ from your own library.
2. In the schematic editor window for ‘inverter’, execute Create > Cellview > From Cellview. ‘Cellview From Cellview’ window will appear. Click OK.



3. In the 'Symbol Generation Options' window, you can choose the location of the pins.

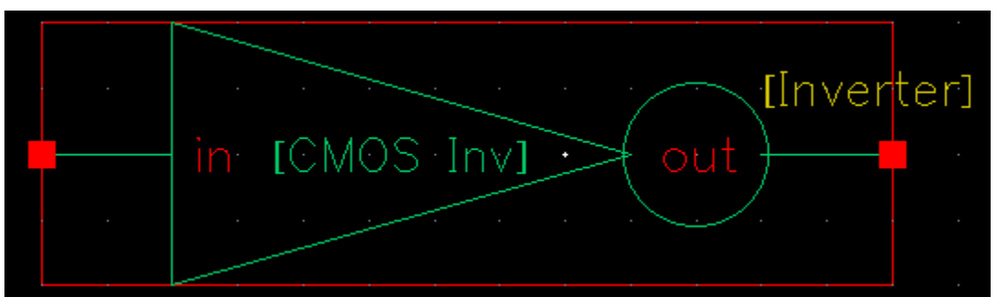


Click OK and the Symbol Editor window will now open.



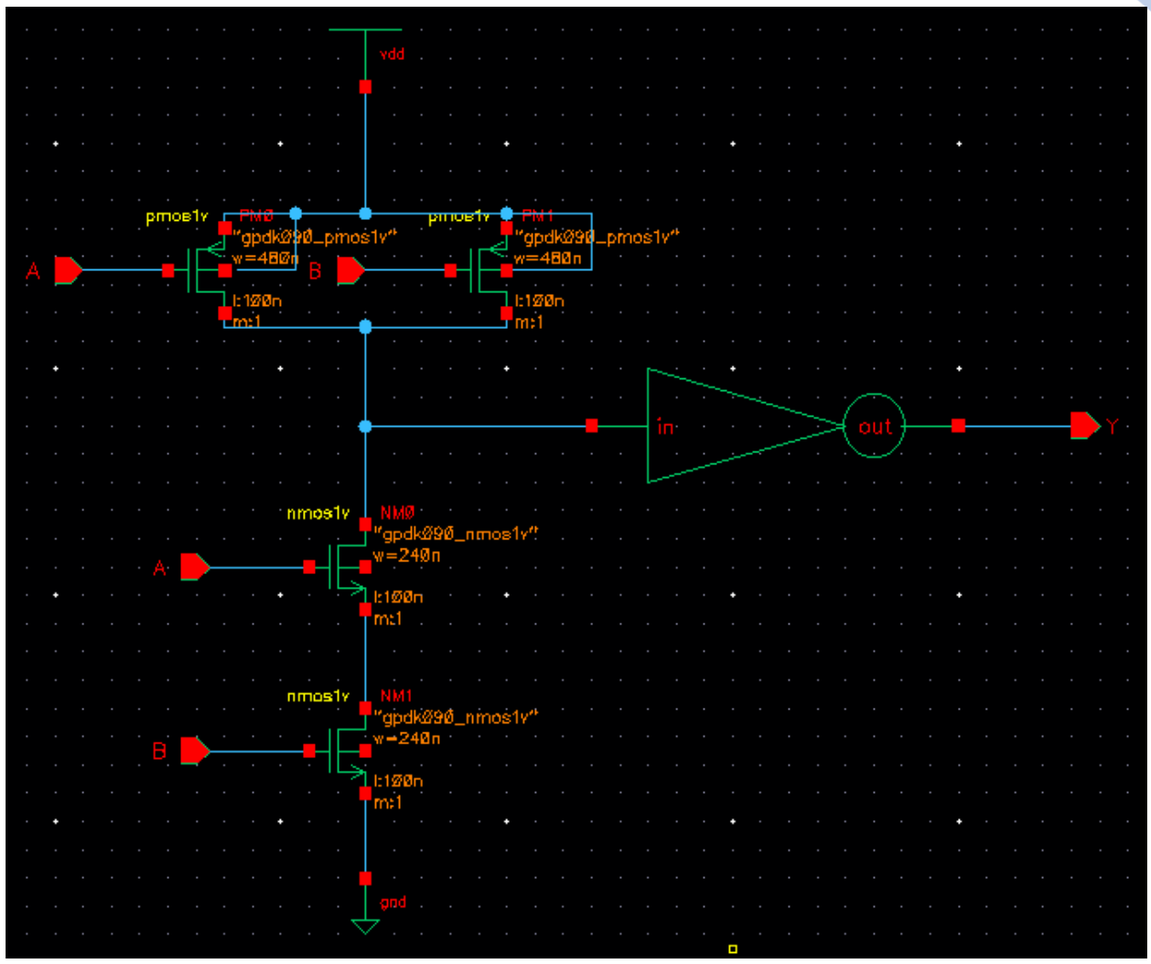
4. Click Delete icon in the symbol window, delete the outer red rectangle and green rectangle.

5. Execute Create > Shape > Polygon, and draw a shape similar to triangle. After creating the triangle, press Esc key.
6. Execute Create > Shape > Circle to make a circle at the end of the triangle. You can move the pin names according to the location.
7. Execute Create > Selection Box. In the 'Add Selection Box' form, click 'Automatic'. A new red selection box is automatically added.
8. After creating symbol, click on the save icon in the symbol editor window to save the symbol. In the symbol editor window, execute File > Check and Save. Then close the symbol editor window.



AND GATE CREATION:

1. Similar way to the inverter, create a schematic on an AND gate using the inverter we just built. It should look like the following:



2. Setup ADE L as before. During the setup stimuli part, set pulse width and period of B to be half of A so that all four input combinations can be tested.

3. Now run the simulation and your output should look like this:

4. Now create a symbol for the AND gate.

HOME TASK:

1. Show the effect of changing NMOS width on the TCC of an inverter.
2. Design a 2-input OR gate along with its symbol.

Rubrics:

Criteria	Below Average (1)	Average (2)	Good (3)
Formatting	Report is not properly formatted, missing objectives, discussions, and references.	Report is somewhat formatted but missing proper references.	Report is properly formatted.
Design	Design steps are somewhat followed, and results have errors.	Design steps are properly followed, and the results are flawless.	
Writing	Writing is poor and not informative. It does not address the design decisions and contains high plagiarism.	Writing is average and original. Design decisions are somewhat explored.	Writing is excellent with every design decision adequately explored.
Diagram	Diagrams are of bad quality and unreadable.	Diagrams are clear and of high quality.	