CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY

Department of Electronics and Telecommunication Engineering

VLSI Technology Sessional

ETE 404

Experiment No:06

DRC, LVS, RCX and Post-Layout Simulation of an Inverter

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1 Objectives:

- To perform Design Rules Check (DRC) and Layout vs. Schematic (LVS).
- To extract parasitic resistance and capacitance from the layout.
- To perform transient simulation of the extracted view.

2 Apparatus:

- **Software:** VMware Workstation v10
- **Hardware:** PC

3 Design Verification:

3.1 Design Rules Check (DRC) Using Assura:

- The previously created inverter layout was opened in Virtuoso Layout Suite L.
- Assura Technology was executed by navigating to Assura > Technology, and the path for the Assura Technology File was specified.
- The DRC was initiated by executing Assura>Run DRC. The required fields were completed, selecting 'gpdk090' under Technology and providing a run name.
- Upon completion of the DRC run, a DRC completion window was displayed. Errors were displayed in the Error Layer Window (ELW).

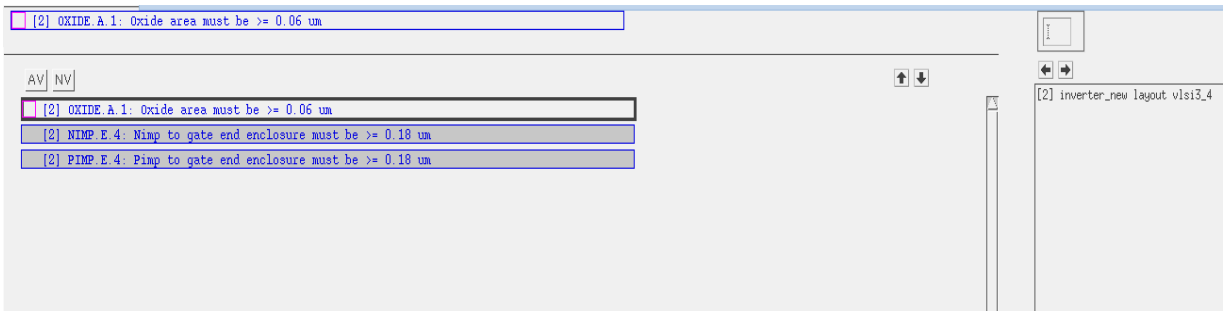


Figure 3.1.1: Error Layer Window.

- Errors were corrected by locating them via the ELW, adjusting dimensions using the ruler and stretch tools, and re-running the DRC until the design was error-free.
- After solving all errors,the following window was appeared:

Figure 3.1.2: DRC Completion Window.

3.2 LVS Using Assura:

- The LVS was executed by navigating to Assura > Run LVS, selecting gpdk090, and providing a run name.
- After the LVS run,the LVS Debug window was used to identify the mismatch.

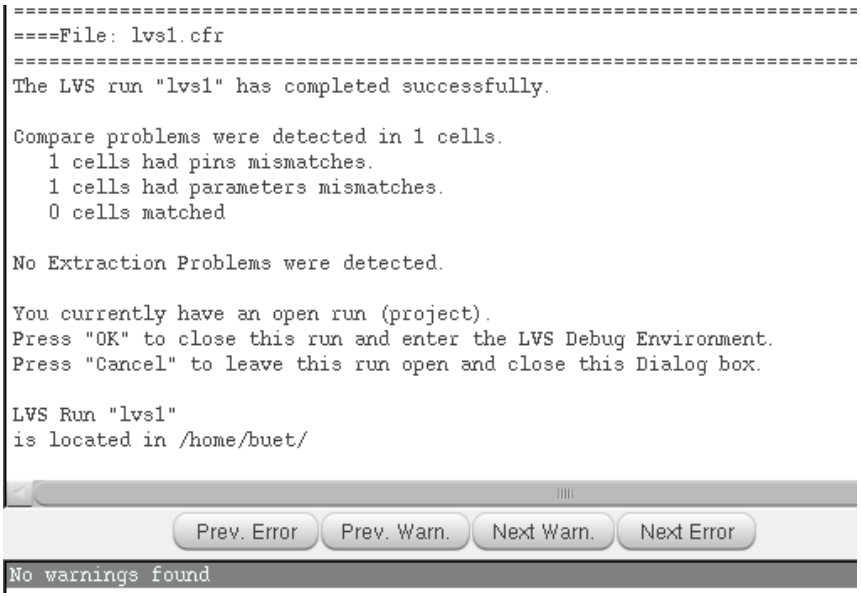


Figure 3.2.1:LVS Completion Window.

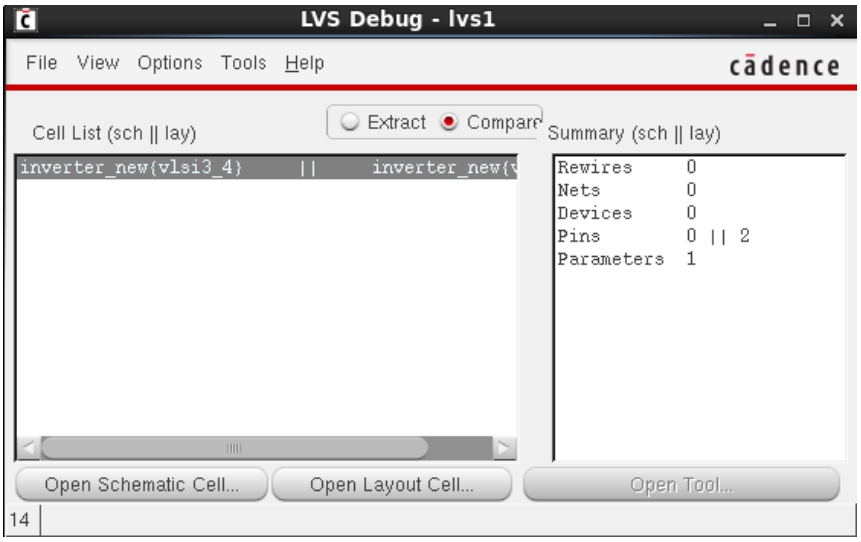
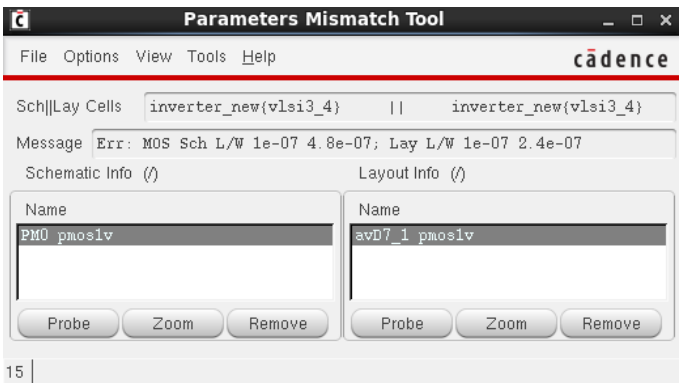
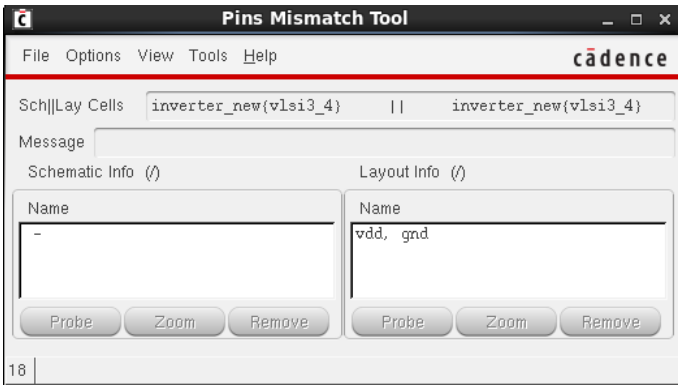


Figure 3.2.2:LVS Debug Window.

- Initially, a parameter mismatch and two pin mismatch was noted.



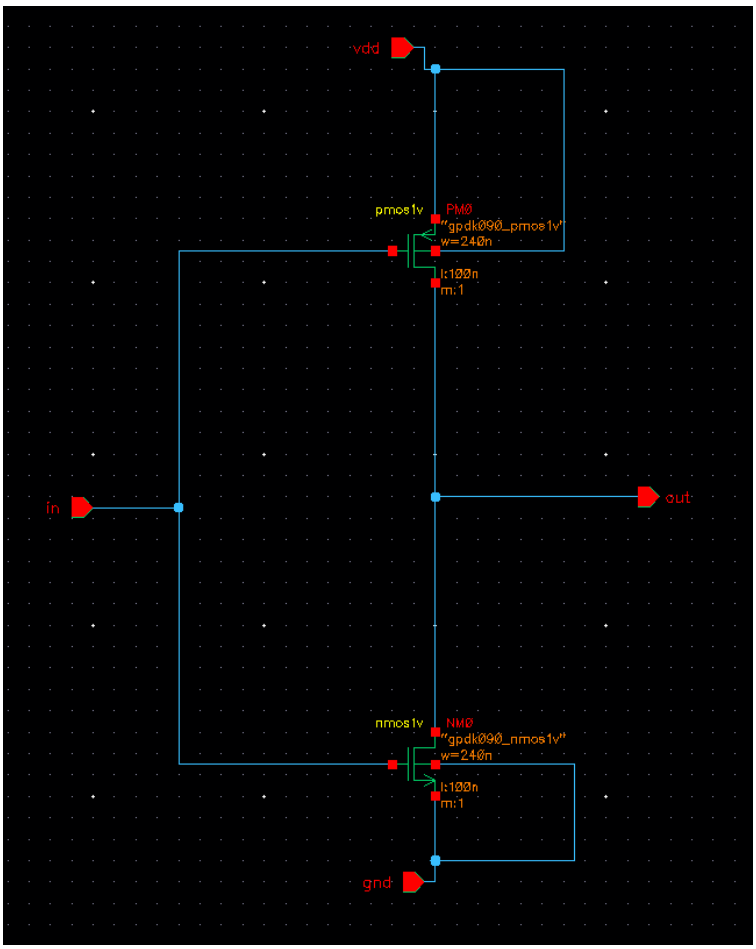
(a) Parameter Mismatch Window



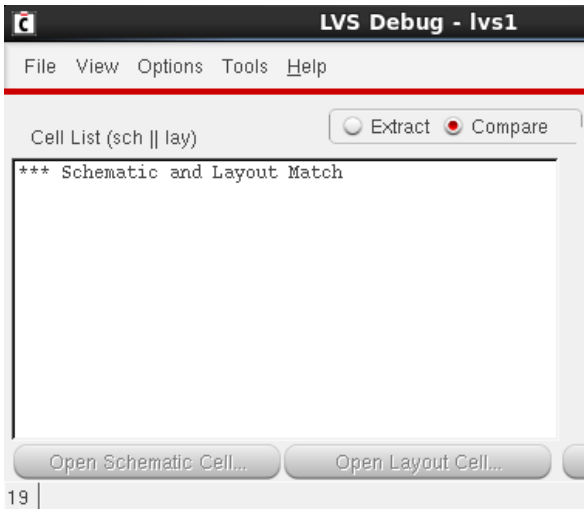
(b) Pins Mismatch Window

Figure 3.2.3: Mismatch Tool Window of LVS

- The PMOS width was adjusted and pin of vdd and gnd was created in schematic design to match the layout, and the LVS was re-run, resulting in a match.



(a) Schematic of the inverter



(b) LVS Debug Window

Figure 3.2.4: Verification of LVS

3.3 RCX Using Assura:

- The final error-free LVS run was selected via Assura < Open Run.
- RCX was initiated by executing Assura < Run RCX, selecting Extracted View in the output field.
- Under the Extraction tab, RC was selected as the Extraction Type, and 'gnd!' was set as the reference node.

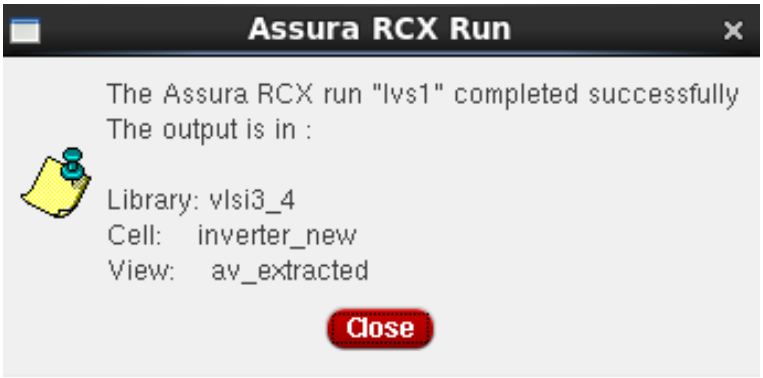


Figure 3.3.1:RCX Completion Window.

- Upon completion, the extracted view was opened using File > Open.

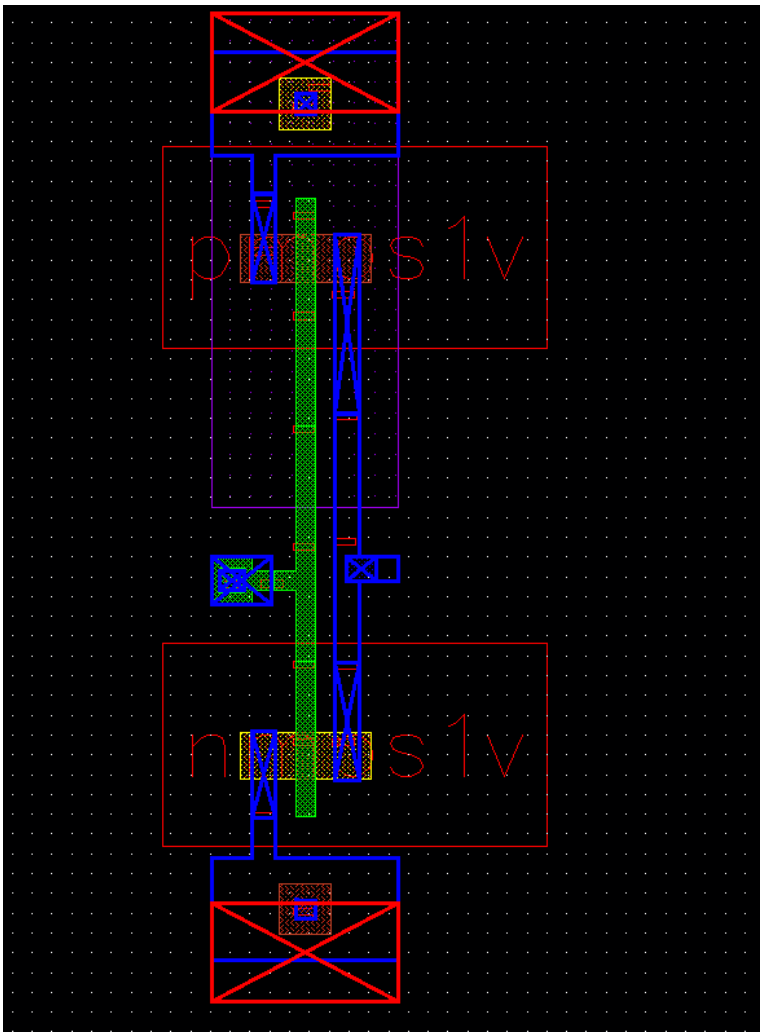


Figure 3.3.2:Extracted view of the inverter.

- ADE L was launched from the av_extracted view.
- The simulation setup was configured similarly to previous labs. Inputs and outputs were plotted by selecting the respective pin locations. The simulation was run, and the output waveforms were observed.

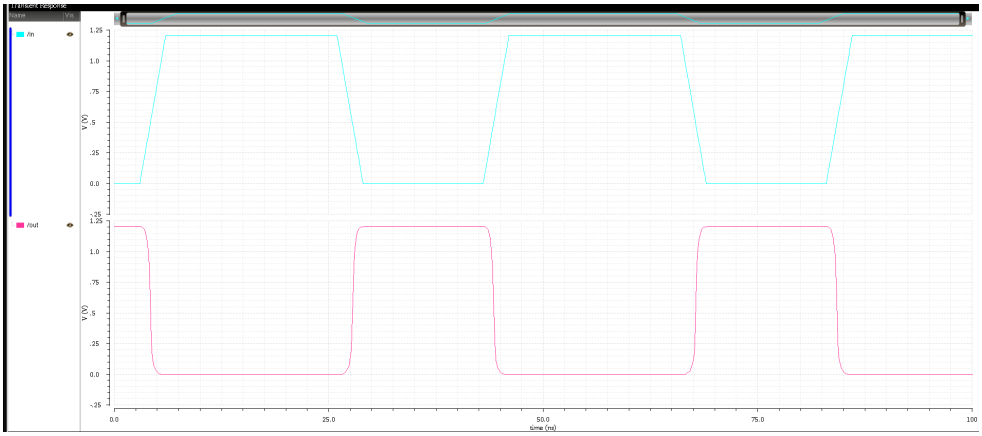


Figure 3.3.3:Input and Output waveforms of the inverter.

3.4 Measurements:

To measure various parameters and perform various waveform calculations, the Waveform Calculator in the **Virtuoso Visualization & Analysis X**L window can be utilized by executing **Tools** > **Calculator**

3.4.1 Propagation Delay Measurement:

- The propagation delay was found by selecting the input node 'in' as VT("/in"), choosing 'delay' in the Special functions panel, setting Signal1 and Signal2 as VT("/in") and VT("/out"), setting both threshold values to 0.6(50%), and clicking the Evaluate buffer icon.

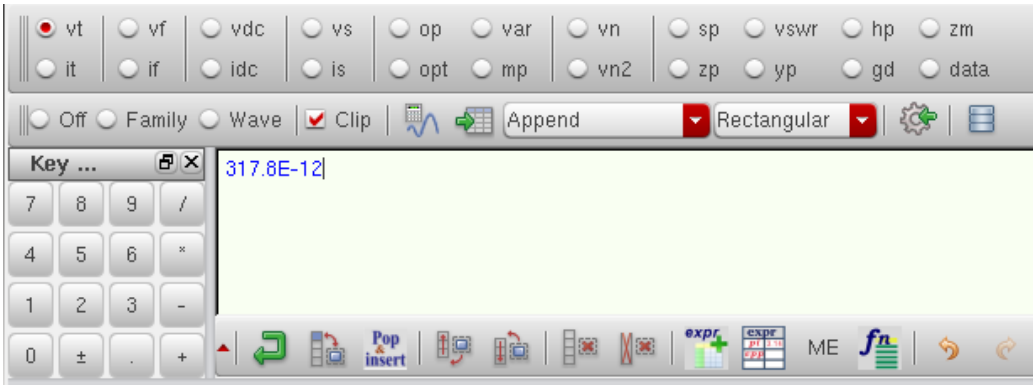


Figure 3.4.1:Measurement of propagation delay of an inverter .

3.4.2 Rise/Fall Time Measurement:

- The rise fall was found by setting Signal1 and Signal2 to VT("/out"), using thresholds of 0.12 and 1.08 for rise time (swapped for fall time), ensuring the same edge numbers for rise/fall time calculation, and selecting rising/falling edge types accordingly before clicking the Evaluate buffer icon'.

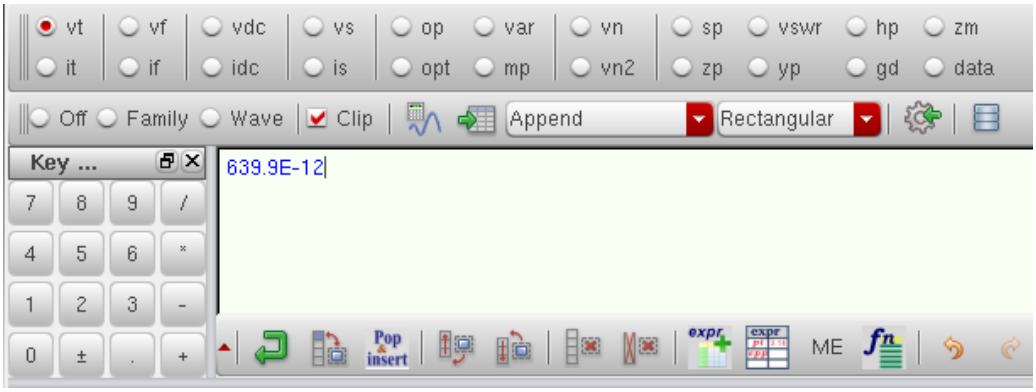


Figure 3.4.2:Measurement of rise time of an inverter .

3.4.3 Power Measurement:

- Before running the simulation, power signals were saved in the ADE L window, the circuit was simulated, and the instantaneous power consumption along with ’in’ and ’out’ signals were displayed in the waveform window.

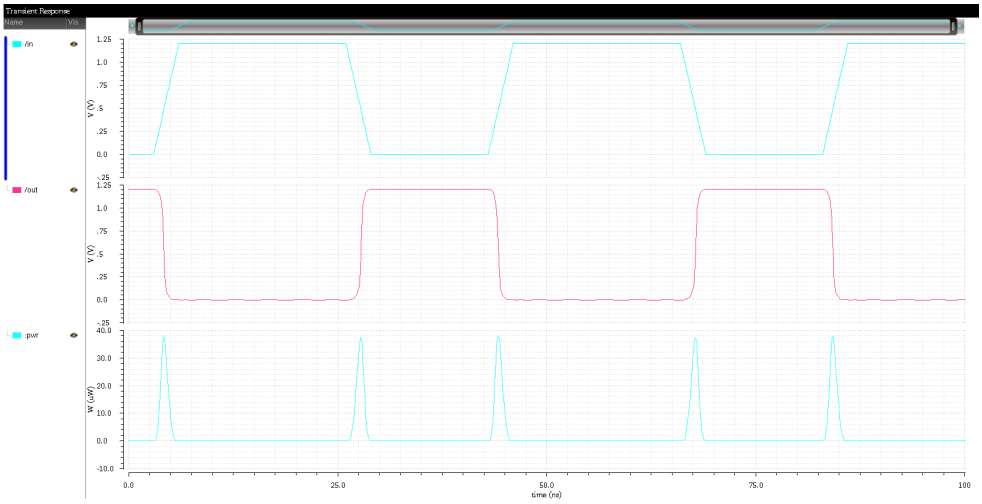


Figure 3.4.3:Output of average power of an inverter .

- The Waveform calculator window was opened with ”Wave” and ”Clip” selected, ’Average’ was chosen from the ’Special Functions’ menu, and the average power dissipation in the time window was displayed after clicking the Evaluate buffer icon.

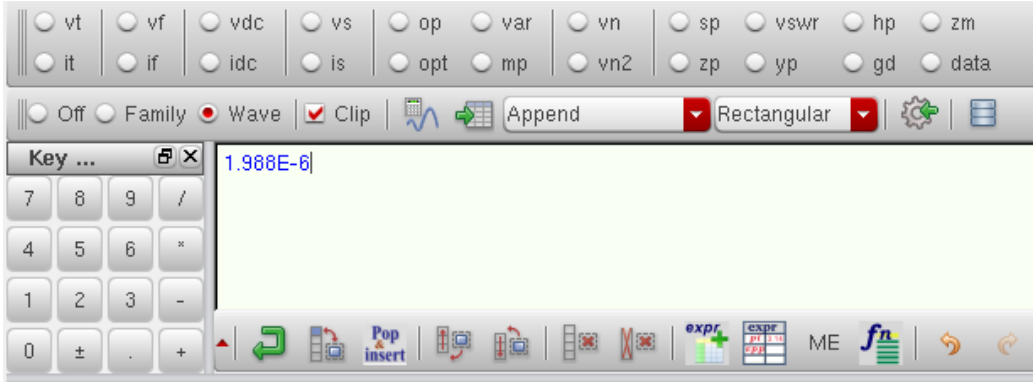


Figure 3.4.4:Measurement of average power of a inverter .

4 Home Task:

4.1 Effects of Parasitic RC Element:

- The effect of parasitic RC elements on the power consumption and propagation delay of an inverter was analyzed.
- It was observed that parasitic resistances and capacitances increase the propagation delay and power consumption, due to the additional load they introduce to the circuit.
- The resistive effects contributed to static power dissipation and impacted the signal rise and fall times.
- The capacitive effects slowed down the charging and discharging of the output node and increased dynamic power dissipation.
- To reduce the influence of these parasitic effects throughout the design phase,the layout and interconnect lengths can be optimized, and strategies such as buffering, shielding, and impedance matching can be applied.

5 Discussion:

- In this experiment, DRC, LVS, RCX, and post-layout simulation of an inverter were performed,to ensure compliance with design rules and consistency between schematic and layout views.
- The DRC and LVS processes helped identify and correct errors in the layout.
- After running DRC, three errors appeared in the Error Layer Window and were corrected by locating the error through the ELW and made the necessary adjustments.
- During the layout vs. schematic check, two mismatches were found: pin and parameter mismatches.
- The parameter mismatch was due to a discrepancy in the width of the PMOS between the layout and schematic ,then adjusted thw width in the inverter's schematic.
- Parasitic elements were extracted, providing insights into their impact on the inverter's performance.
- The transient simulation of the extracted view allowed for the measurement of propagation delay, rise/fall time and average power.
- It was observed that parasitic resistances and capacitances increase the propagation delay and power consumption, due to the additional load they introduce to the circuit.
- In conclusion, the experiment demonstrated the importance of thorough verification and extraction processes in VLSI design, highlighting how parasitic elements can affect circuit performance.