DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

CHITTAGONG UNIVERSITY OF ENGINEERING AND TECHNOLOGY

CHATTOGRAM – 4349, BANGLADESH

Experiment No. 8

Hierarchical Design of AND Gate Using a NAND Gate and a NOT Gate

PRECAUTIONS:

- Students must carefully read the lab manual before coming to lab to avoid any inconveniences.
- Students must carry a flash drive to transfer files and lab manuals.
- Use of mobile phone in lab is strictly prohibited and punishable offence.
- Experiment files must be uploaded to GitHub including home tasks.

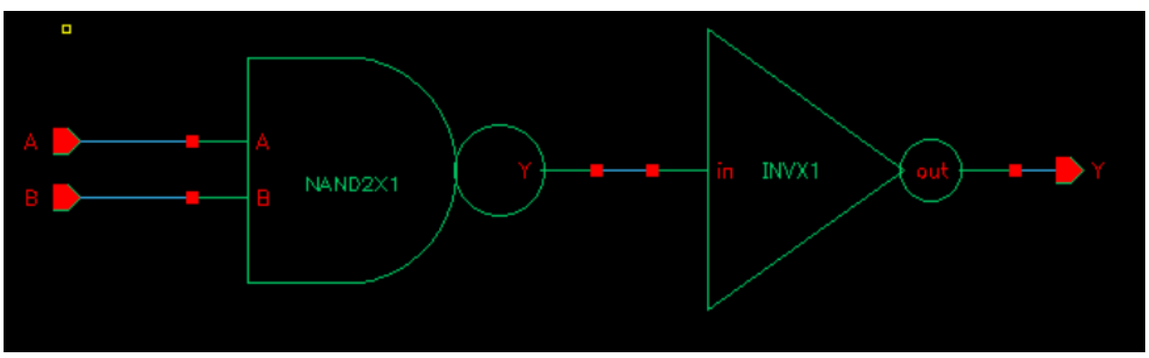
OBJECTIVES:

- To familiarize with hierarchical design.
- To perform schematic-level verification, layout generation, DRC and LVS.
- To perform post-layout simulation of top-level design.

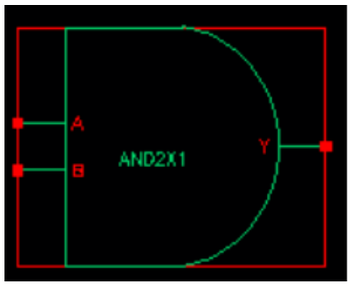
HIERARCHICAL DESIGN:

By this point, we have already created the schematic, symbol and layout of an inverter and a NAND Gate. We will now be using these to create an AND Gate.

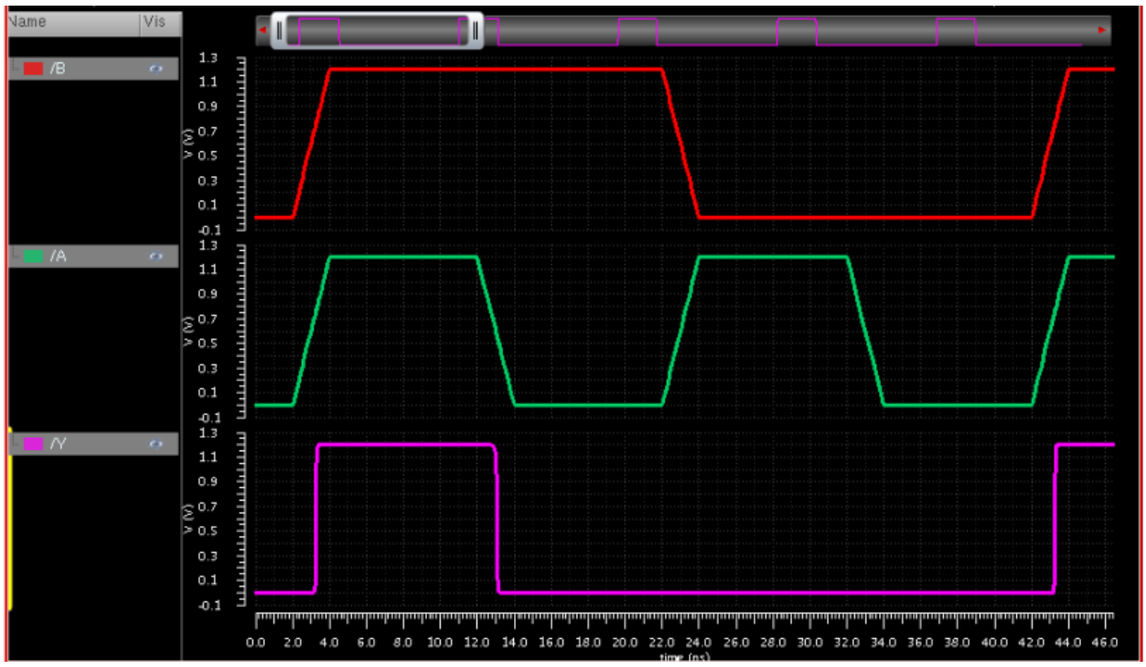
1. From **CIW**, create a new **cellview** and name it "AND".
2. Instantiate the NAND and inverter you already designed by their symbol from your own library into the new schematic. Your final schematic should look like the following:



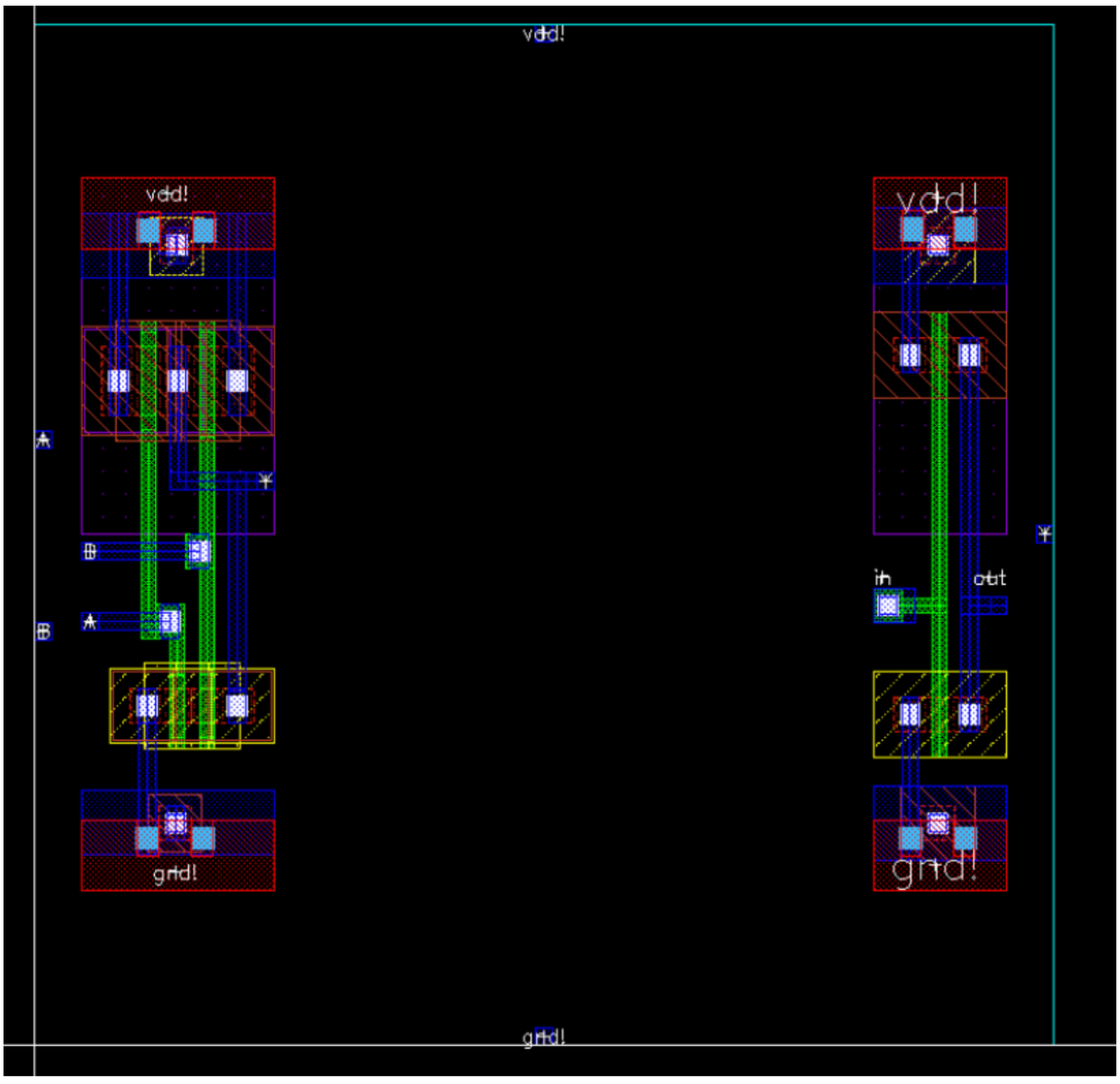
3. Now create a symbol from the newly created schematic.



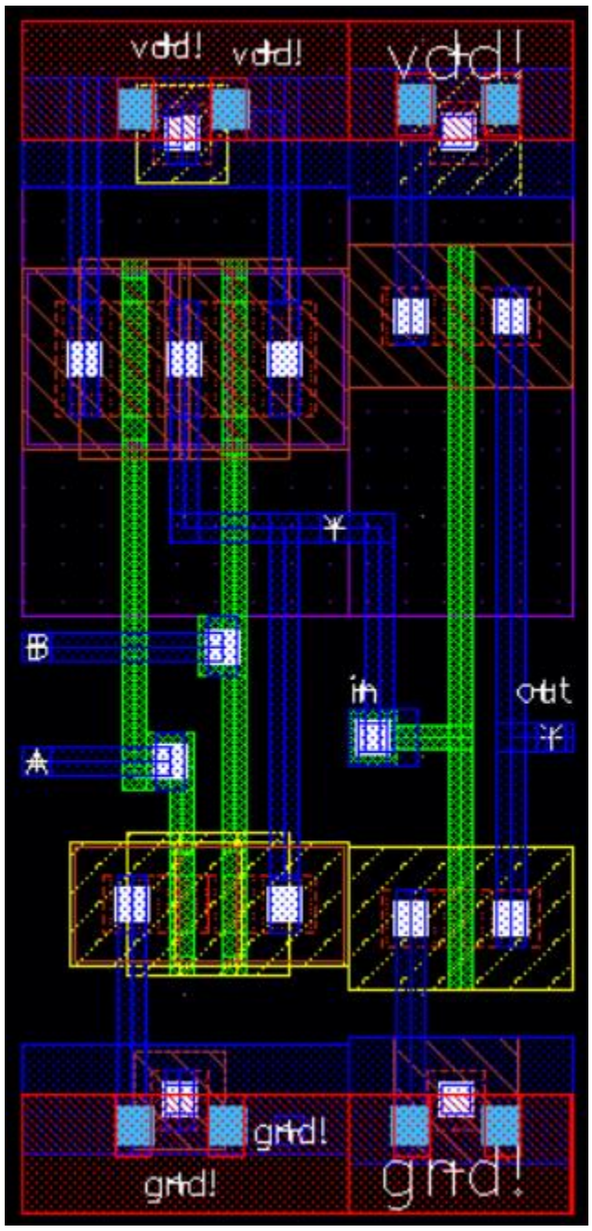
4. Now add **input** and **output** pins, launch **ADE L** and perform an analog analysis following all the proper steps. The result should look like the following:



5. Now execute **Launch > Layout XL** from the schematic view. Now generate the instances and set the display options as you did in the previous labs. You should get something similar to the following:



6. Now connect them as required to build an AND Gate. Your design should look similar to the following:



7. Now perform **DRC**, **LVS** and **QRC** similar to previous labs. Now perform a post-layout simulation from the **av_extracted** view and verify the results.

Rubrics:

Criteria	Below Average (1)	Average (2)	Good (3)
Formatting	Report is not properly formatted, missing objectives, discussions and references.	Report is somewhat formatted but missing proper references.	Report is properly formatted.
Design	Design steps are somewhat followed and results have errors.	Design steps are properly followed and the results are flawless.	
Writing	Writing is poor and not informative. It does not address the design decisions and contains high plagiarism.	Writing is average and original. Design decisions are somewhat explored.	Writing is excellent with every design decision adequately explored.
Diagram	Diagrams are of bad quality and unreadable.	Diagrams are clear and of high quality.	