SYNOPSYS®

DATASHEET

IC Validator WorkBench

High Speed Layout Visualization

Synopsys IC Validator WorkBench is a powerful, hierarchical layout visualization and analysis tool

Overview

Synopsys IC Validator™ WorkBench allows viewing and editing GDSII, OASIS®, and LEF/DEF layouts from small IP blocks to full chip databases.

Benefits

- Quickly opens large GDSII, OASIS, and LEF/DEF files with low memory overhead. Additionally, cache files can drastically decrease the time for subsequent sessions
- Opens Optimized OASIS files instantly
- Provides easy debugging of the hierarchy and placement of cells and shapes
- Quickly determines and displays shape connectivity interactively with cut layer capabilities
- Provides improved support of the Synopsys IC Validator (VUE) application to review and correct DRC and LVS errors
- Provides various modes for merging layouts of mixed formats and DBUs
- Compares layouts, cells, and generates difference reports/layouts
- Defines TCAD simulation domains in hierarchical layouts for Synopsys Sentaurus™

High Speed, High Capacity View and Editing

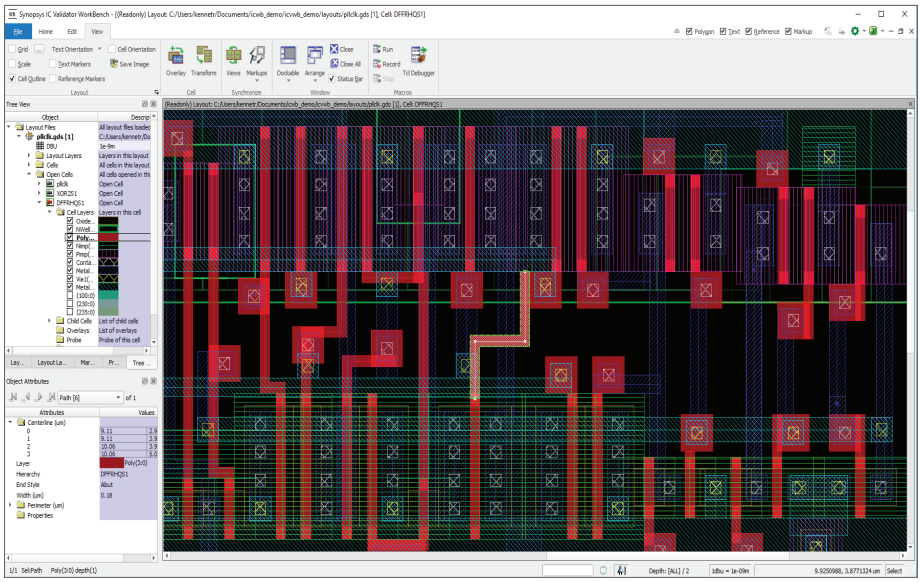

Figure 1: Hierarchical selection and editing in ICVWB

Synopsys IC Validator WorkBench loads gigabytes of data in minutes and has unlimited file size capacity on 64-bit platforms. Fast zooming and panning ease exploration and analysis of the largest layout patterns. In addition, Synopsys IC Validator WorkBench can overlay two or more layouts in a single view without merging the underlying layout files.

Hierarchical selection and editing allow Synopsys IC Validator WorkBench to select and edit shapes deep in the hierarchy without requiring the sub-cell to be opened as shown in Figure 1. Edit operations have undo and redo support.

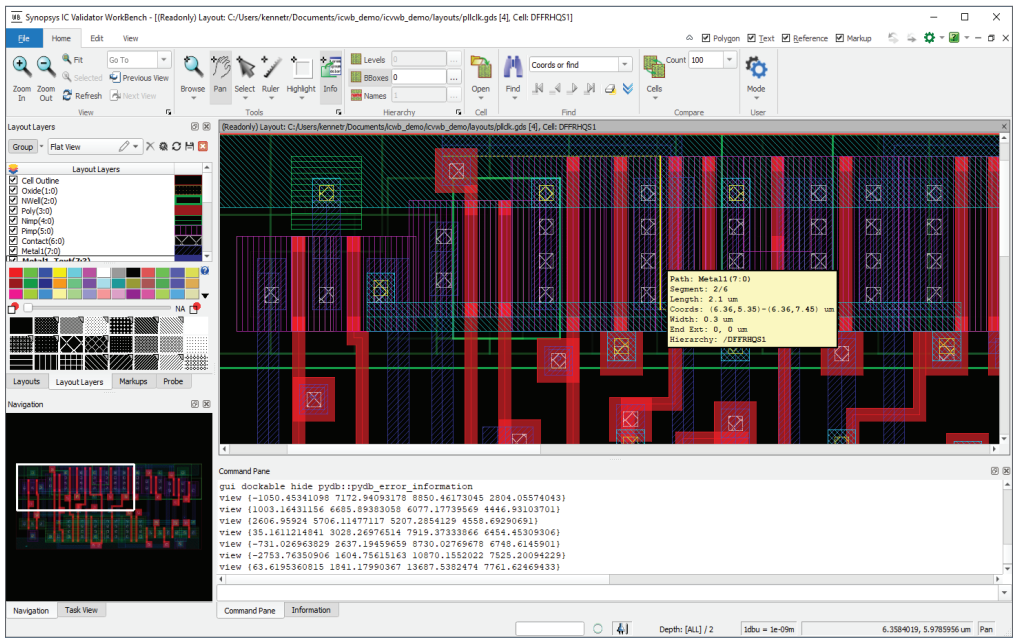

Figure 2: Shape information tool tip and probe showing the hierarchy of layout shapes

Hierarchy Debug

Debugging layouts and their hierarchy is critical for the final design of large chips and Synopsys IC Validator WorkBench provides several tools to do this as shown in Figure 2.

- Control of the levels of hierarchy shown: select the level or range of levels of the hierarchy to be shown to better determine the source of shapes
- Shape information tool tip: Synopsys IC Validator WorkBench includes a shape information tool tip to allow quick determination of the hierarchy of shapes and cells
- Probe: Synopsys IC Validator WorkBench allows to get complete information of the hierarchy at a location including the cell placement information and properties

Advanced Features

Synopsys IC Validator WorkBench implements the latest in user interface technology and is architected to make the powerful Synopsys IC Validator WorkBench capabilities easy and intuitive to use.

Key features include:

- Net tracing—Synopsys IC Validator WorkBench can trace touching shapes based on a user- defined connectivity list. This allows a quick check of opens/ shorts in a layout
- Automated configurable HTML reporting of violation errors
- Support automation with both Tcl and Python languages
- Hierarchical folder representation of all objects including layouts, rulers, and other markups, such as SEM images
- Browser-like forward and back view history
- User and site-level customization:
  - Customizable hot keys for menus and commands
  - Customizable window and toolbar positions
  - Customizable menus and context-menus
- Custom buttons to run user-created macros
- Features to query layout databases instantly from a batch mode interface

Common Platform and User Modes

Synopsys IC Validator WorkBench is built on the same code base as the Synopsys Proteus™ WorkBench product, but without the lithographic simulation. All lithography markup types are available for review in Synopsys IC Validator WorkBench.

Synopsys IC Validator WorkBench can be used as a cockpit for rigorous lithography simulation and resist calibration.

Synopsys IC Validator WorkBench has user modes for different users including:

- Synopsys IC Validator: default set up and connections to Synopsys IC Validator VUE through a single toolbar button
- Synopsys Sentaurus: additional markups to support TCAD simulations, including stretch, and toolbar buttons to generate simulation domain information for Synopsys Sentaurus

Interfaces

- Inputs and Outputs
  - GDSII (including compressed GDSII)
  - LEF/DEF
  - OASIS (including compressed OASIS)
  - Optimized OASIS

User Interfaces

- GUI-based user interface
  - Tcl-based user interface with TK widgets available
  - Python interface for scripting Synopsys IC Validator WorkBench
- Including a powerful layout processing iLayout Python module—an automation API for reading/writing full-chip layouts
- Socket communication
- Supported platforms
  - Linux64, Win64, Suse64, Linux on PowerPC, Linux on ARM64