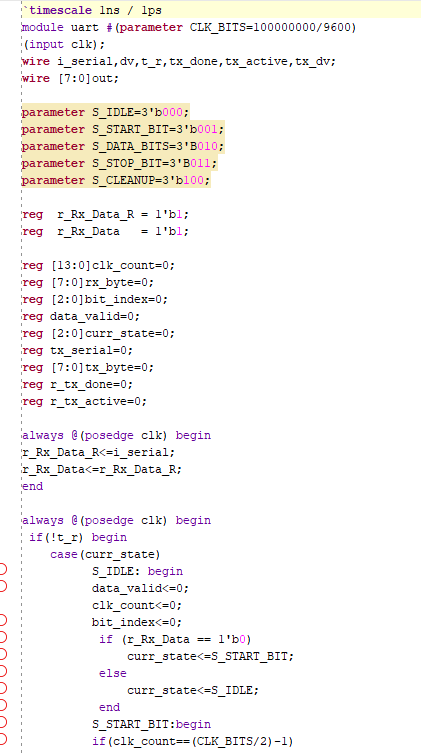
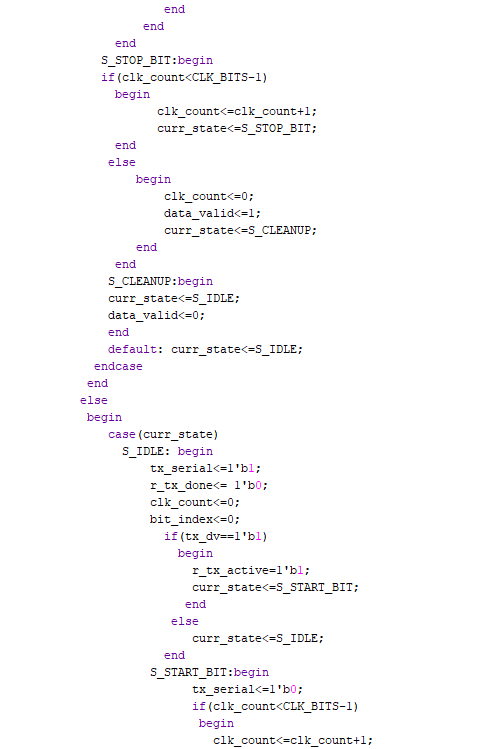
ASSIGNMENT 4

1.Implement a simple UART protocol using verilog HDL and test using ILA & VIO

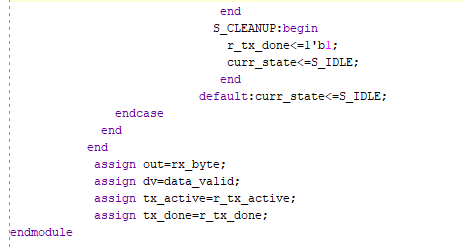
1 START BIT, 1 STOP BIT, 8 DATA BITS

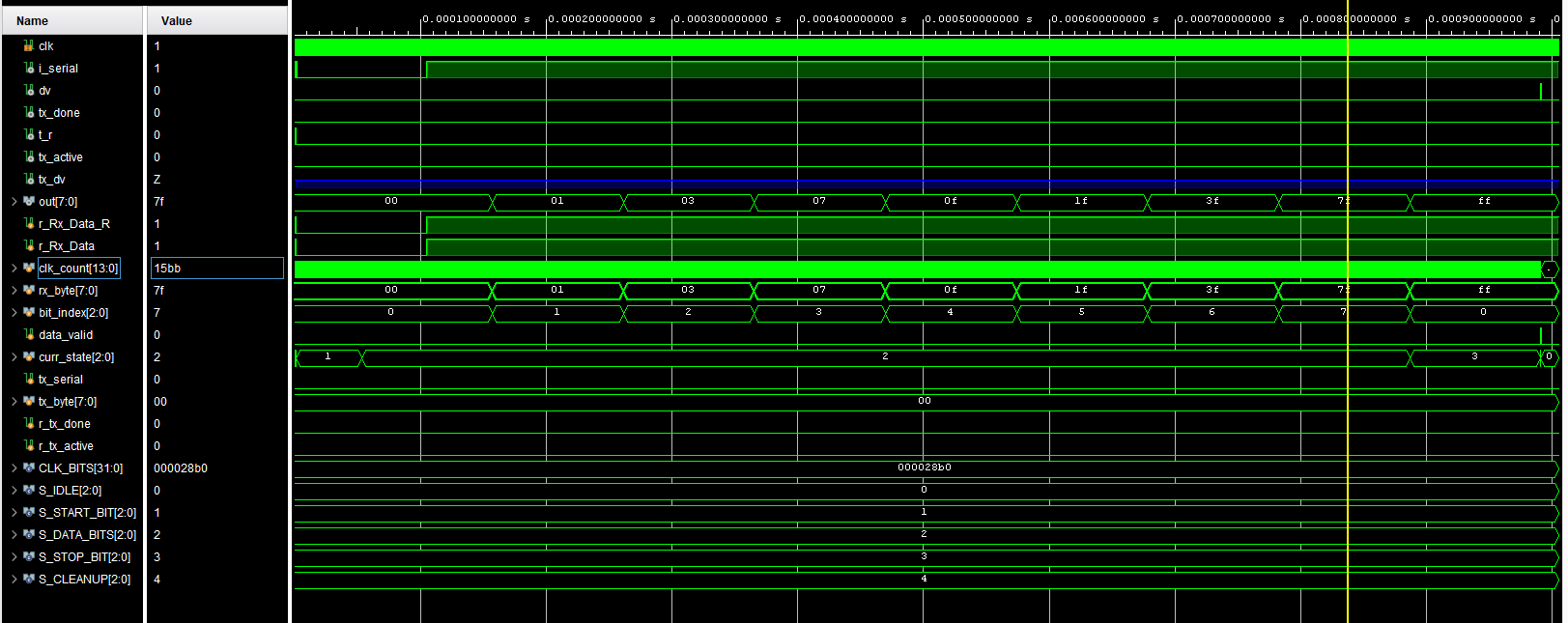




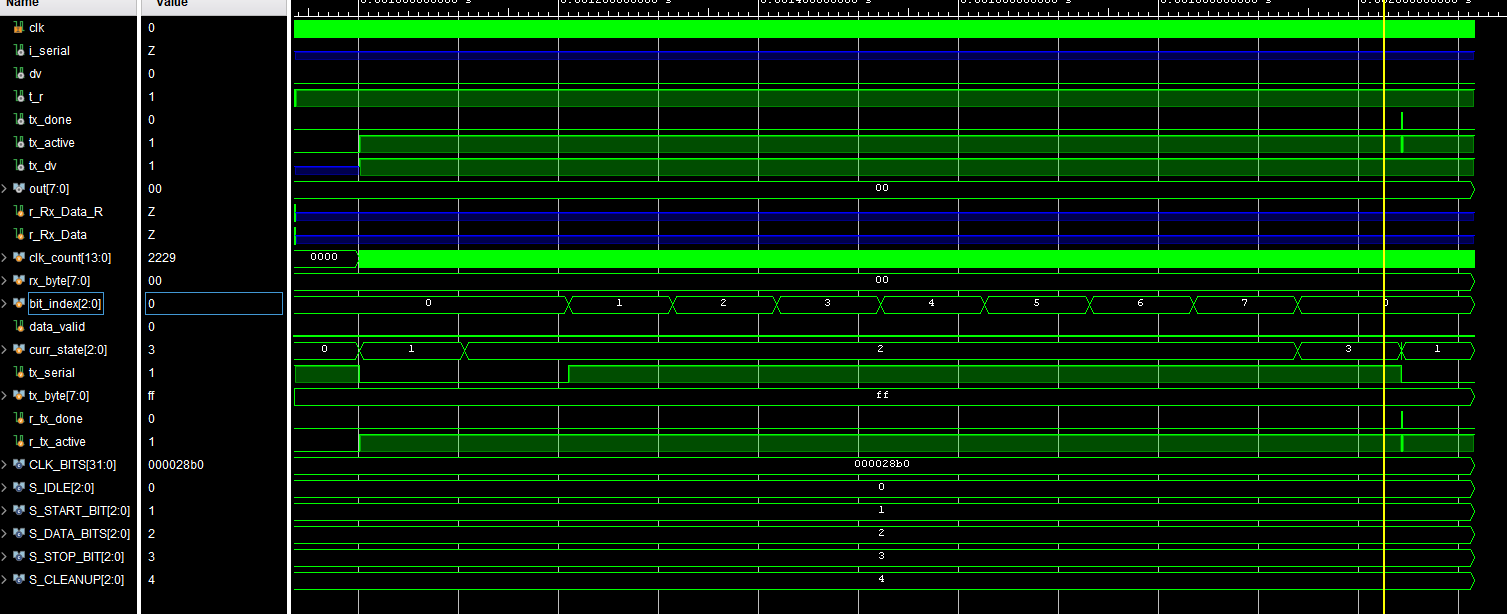






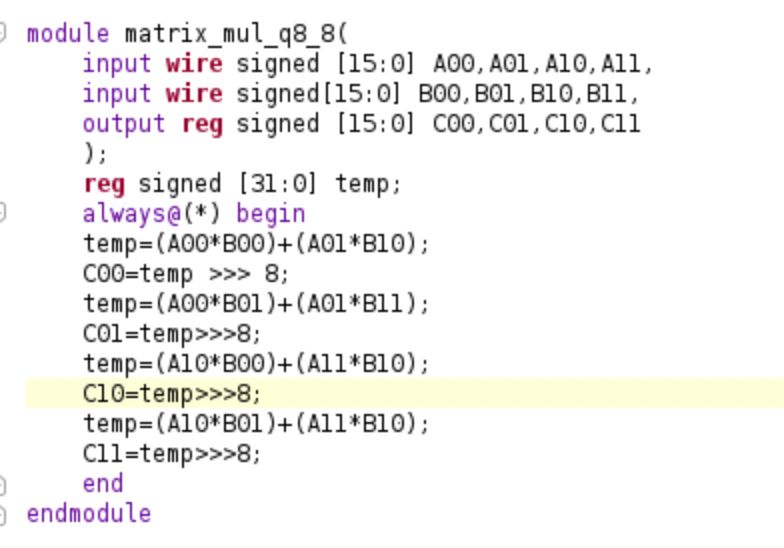
RECEIVER

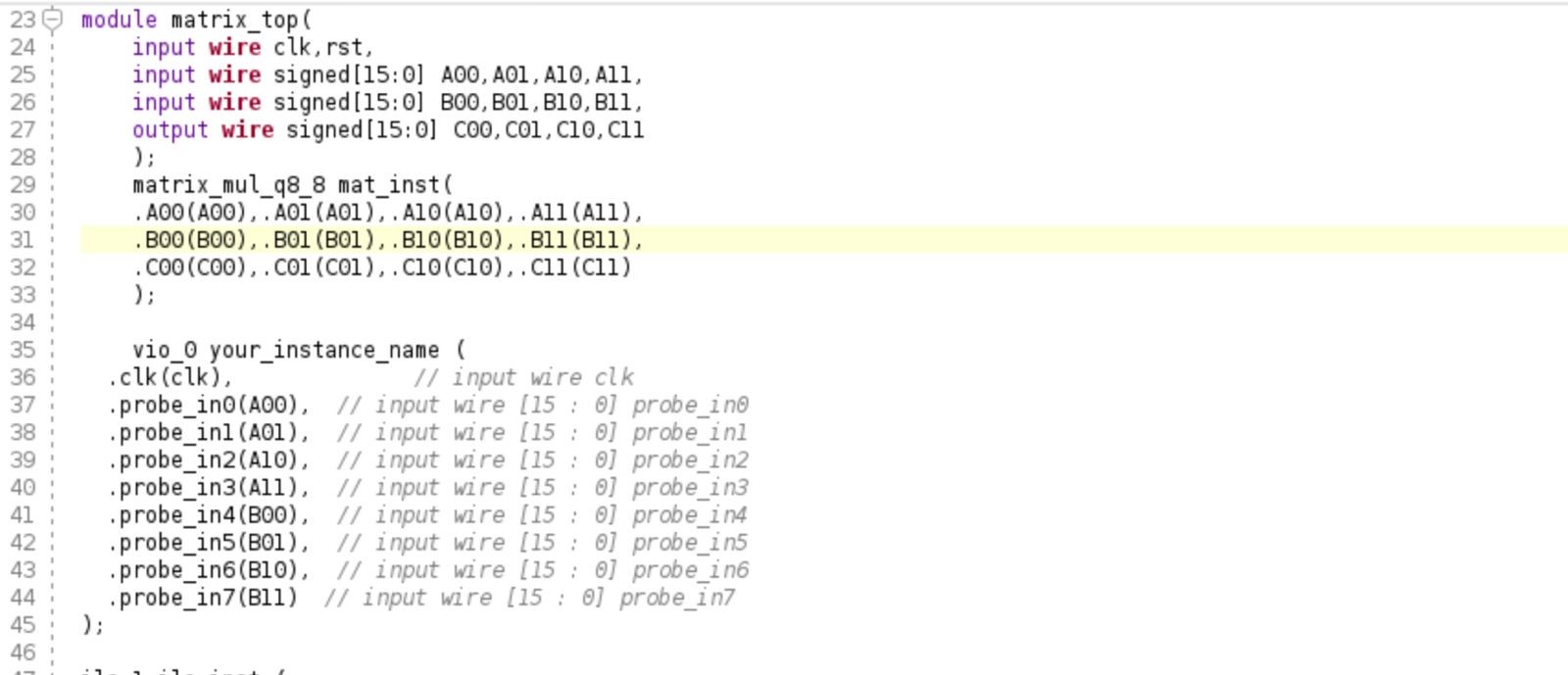
RECEIVED BYTE = 0xFF

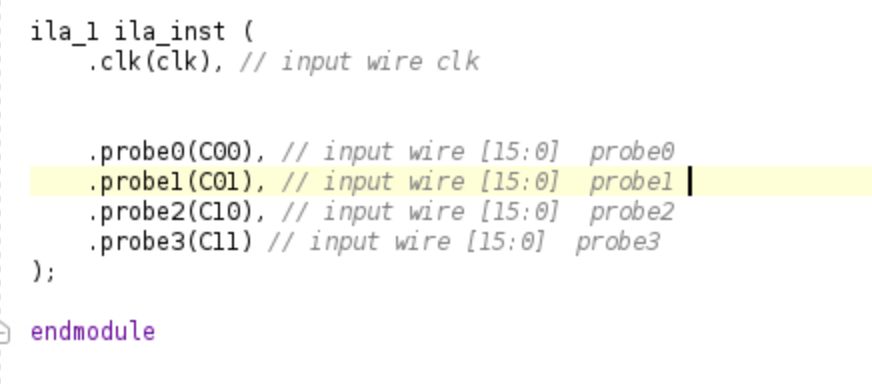
TRANSMITTER

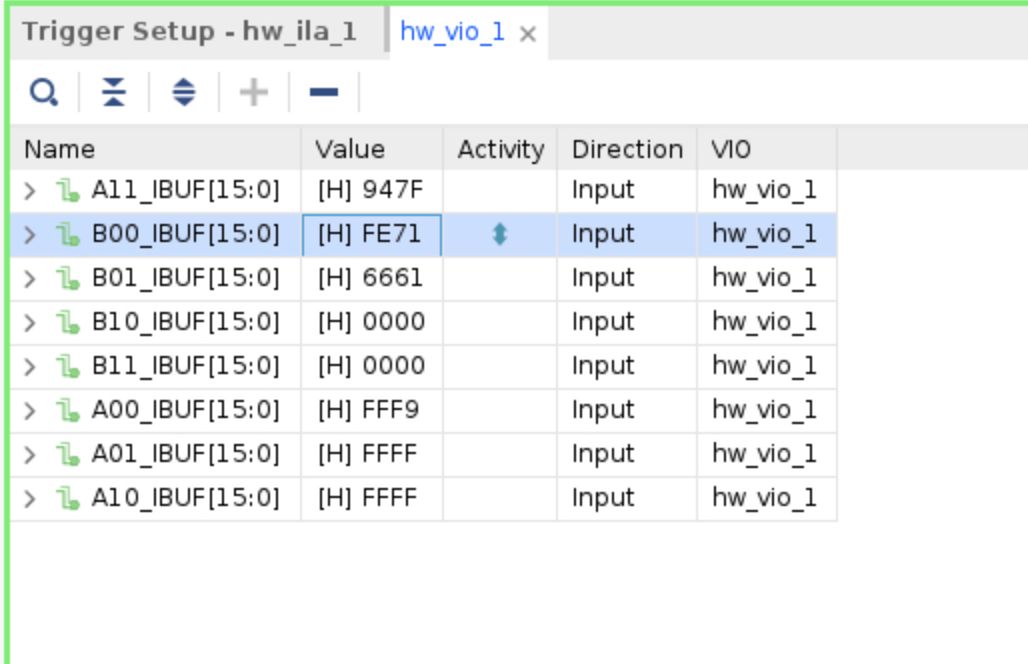
TRANSMITTED BYTE = 0xFF

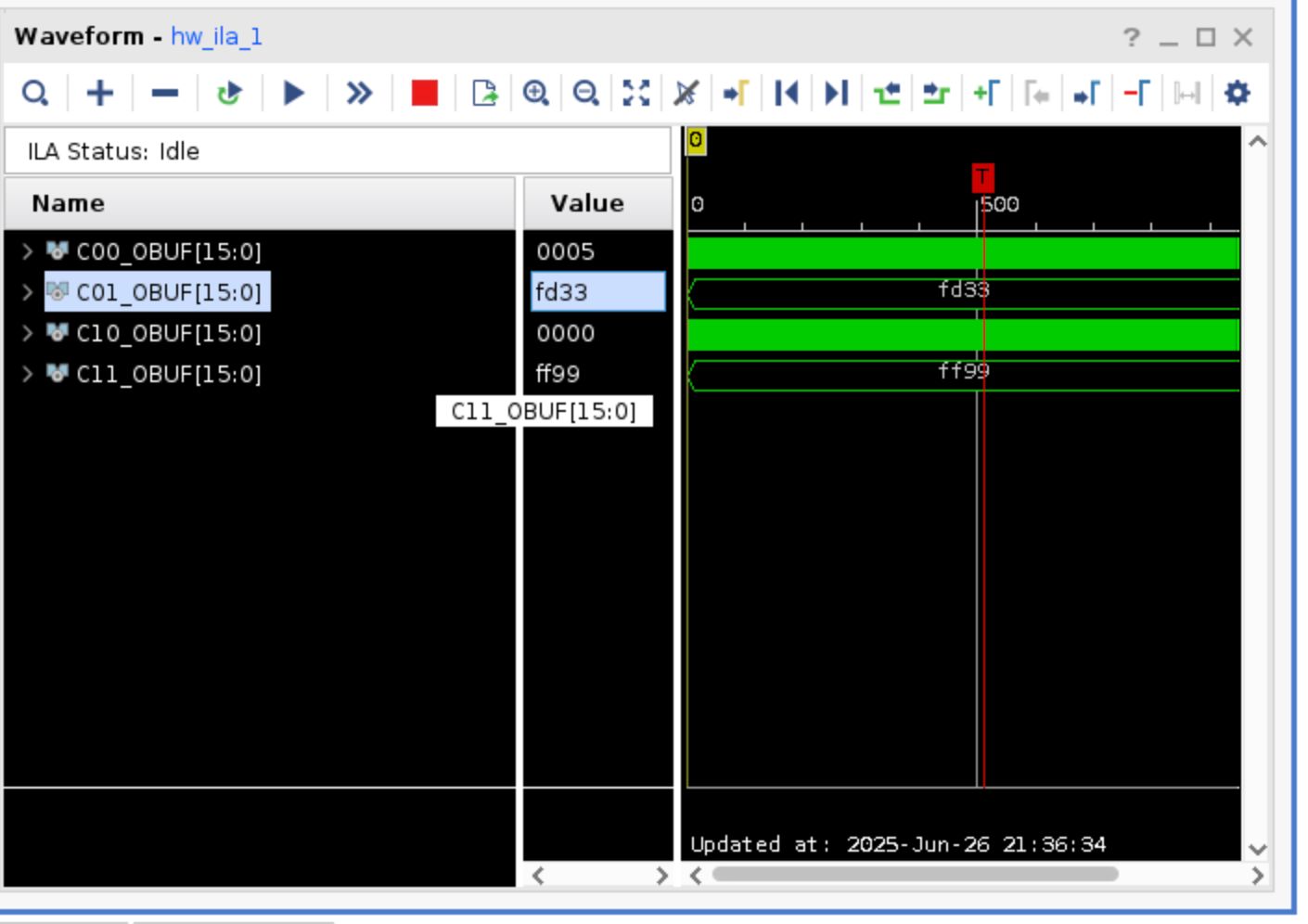
2. Implement a Fixed Point Matrix Multiplication on FPGA using Verilog

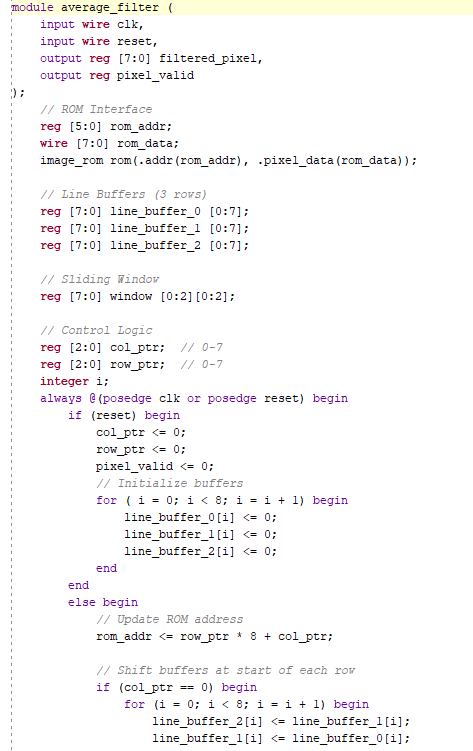










3.How to load text file or image into FPGA? Try to read a small size image into an FPGA and apply a basic filter (like a 3x3 average or Sobel filter).

