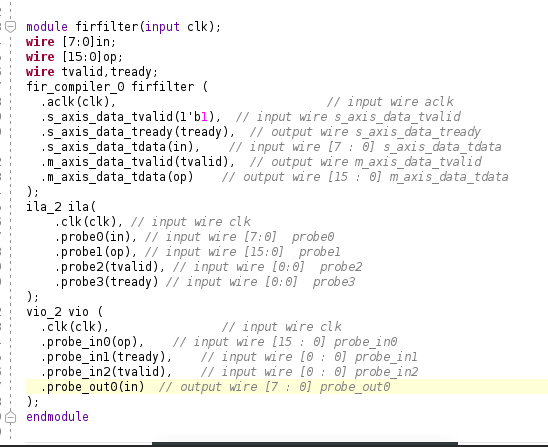
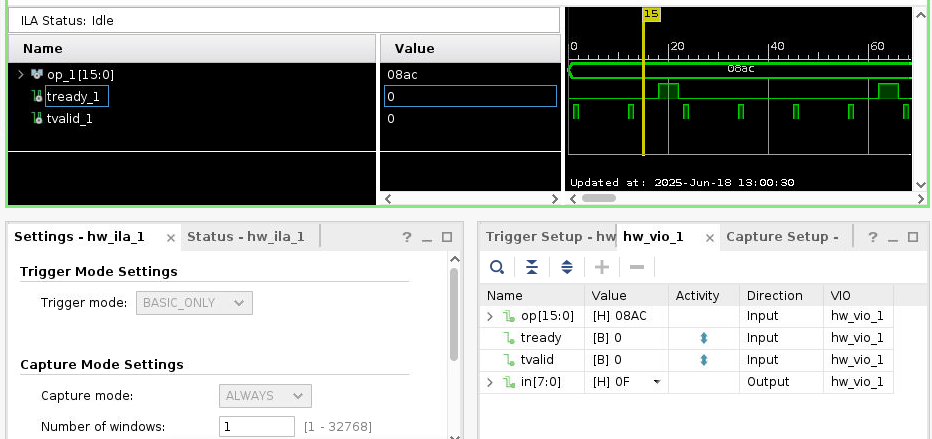
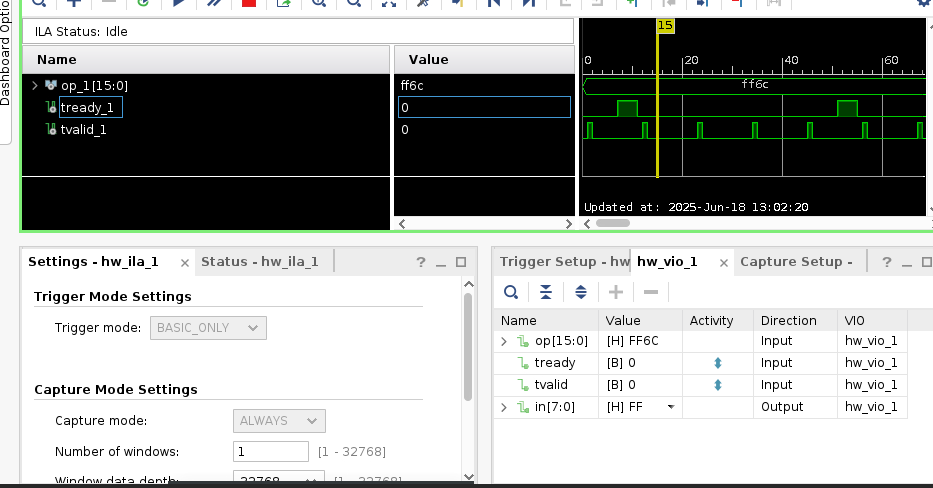
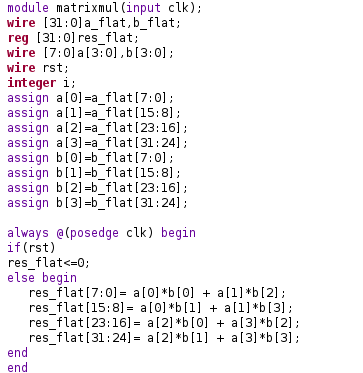
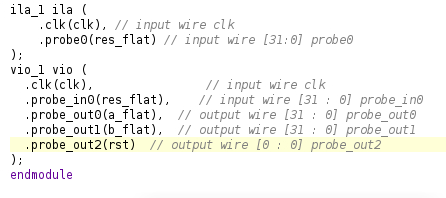
ASSIGNMENT 3

1. Model a simple FIR Filter using verilog HDL and implement on Arty 7 FPGA. Using ILA and VIO, observe the waveforms and mathematical results.



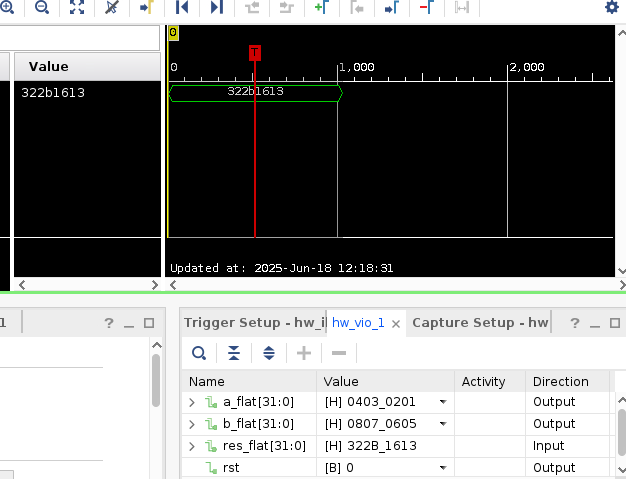
2. Model a simple 8 bit Matrix Multiplication using the array concept ( A[7:0] ) in verilog HDL and using the Debugging cores, observe the results.



Input= [01 02] , [05 06]

[03 04] , [07 08]

(a\_flat = 0x04030201, b\_flat=0x08070605)

(res\_flat=0x322b1613, which when taken 2 digits at a time from the left and changed to decimal gives the result)

Output= [19 22]

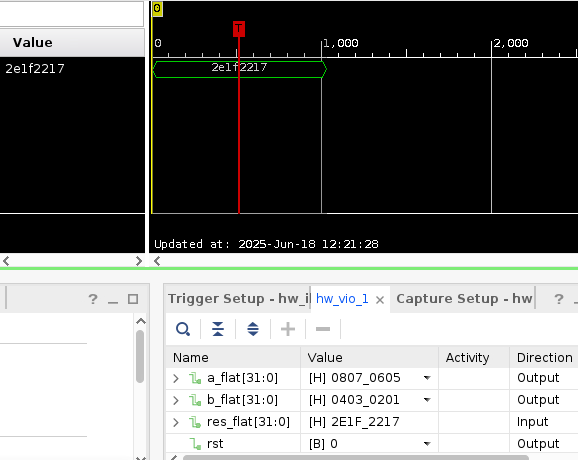
[43 50]

Input= [05 06] , [01 02]

[07 08] , [03 04]

(a\_flat = 0x08070605, b\_flat=0x04030201)

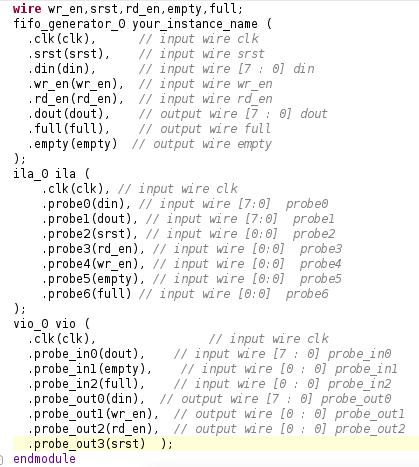
(res\_flat=0x2e1f2217, which when taken 2 digits at a time from the left and changed to decimal gives the result)

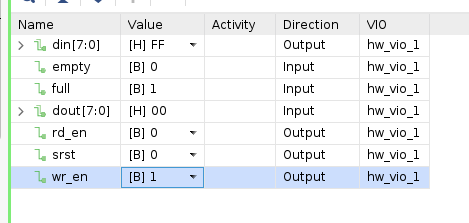


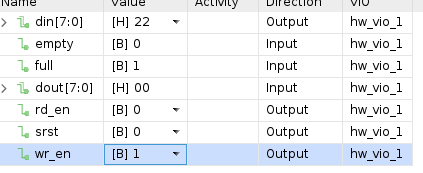
Output= [23 34]

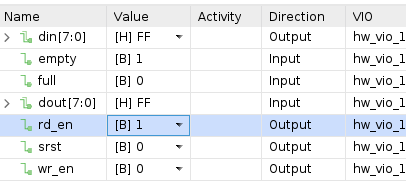
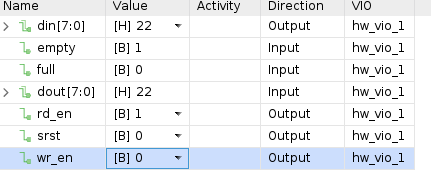
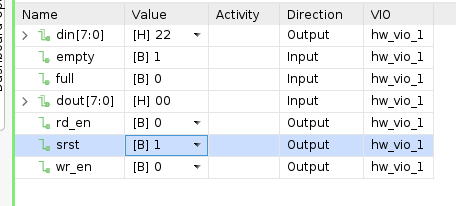
[31 46]

3. Model a simple 8 bit FIFO and observe the results using ILA & VIO.



Writing into FIFO

Reading from FIFO

Resetting the FIFO