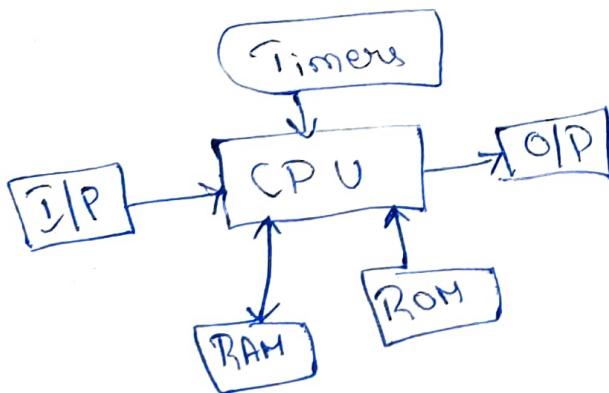


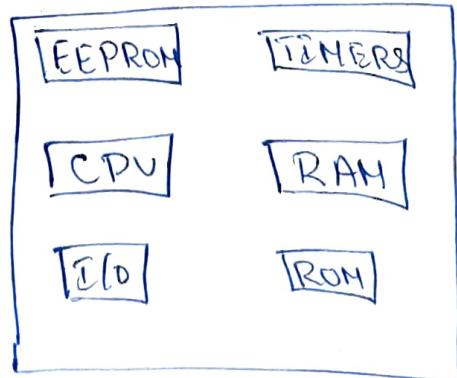
IV Micro processor

- * CPU is stand alone, RAM, ROM, I/O, timer are separate.
- * Designer can decide on the amt. of ROM, RAM & I/O ports.
- * Acts as heart of computer system.
- * It has less no. of registers.
- * It is a processor in which memory & I/O output is connected externally.
- * As it is connected externally, connection is more complex.
- * Cannot be used in complex compact system.
- * General-purpose



Micro controller

- * CPU, RAM, ROM, timer & I/O are all on a single chip.
- * Fix amt. of on-chip ROM, RAM & I/O ports.
- * Acts as heart of embedded System.
- * It has more no. of registers.
- * It is a processor in which memory & I/O output is connected internally.
- * As it is connected internally, connection is less complex.
- * Can be used in compact System.
- * Single purpose.

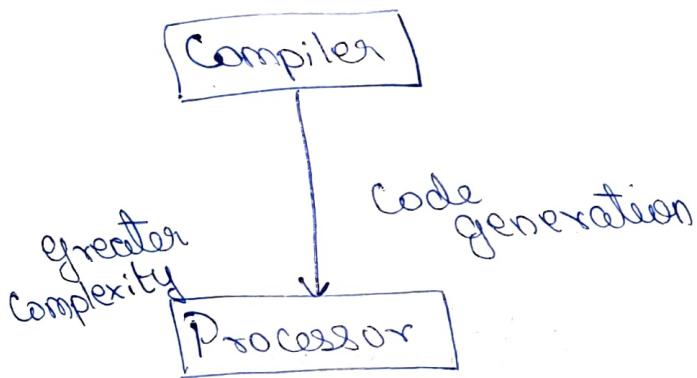


CISC

on Hardware

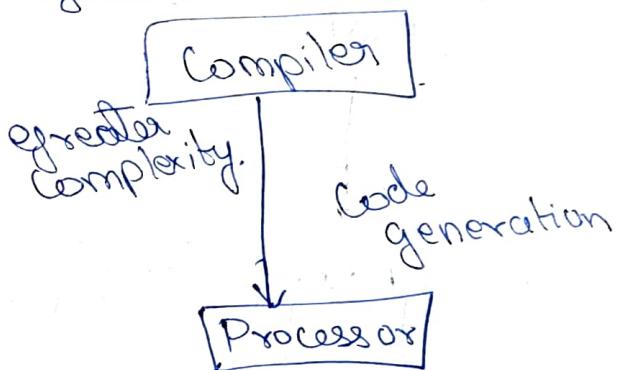
- * Emphasis on Hardware
- * Multiple instruction size & format
- * Less register
- * More addressing Modes
- * Pipelining is difficult

* Instruction take a varying amt. of cycle time

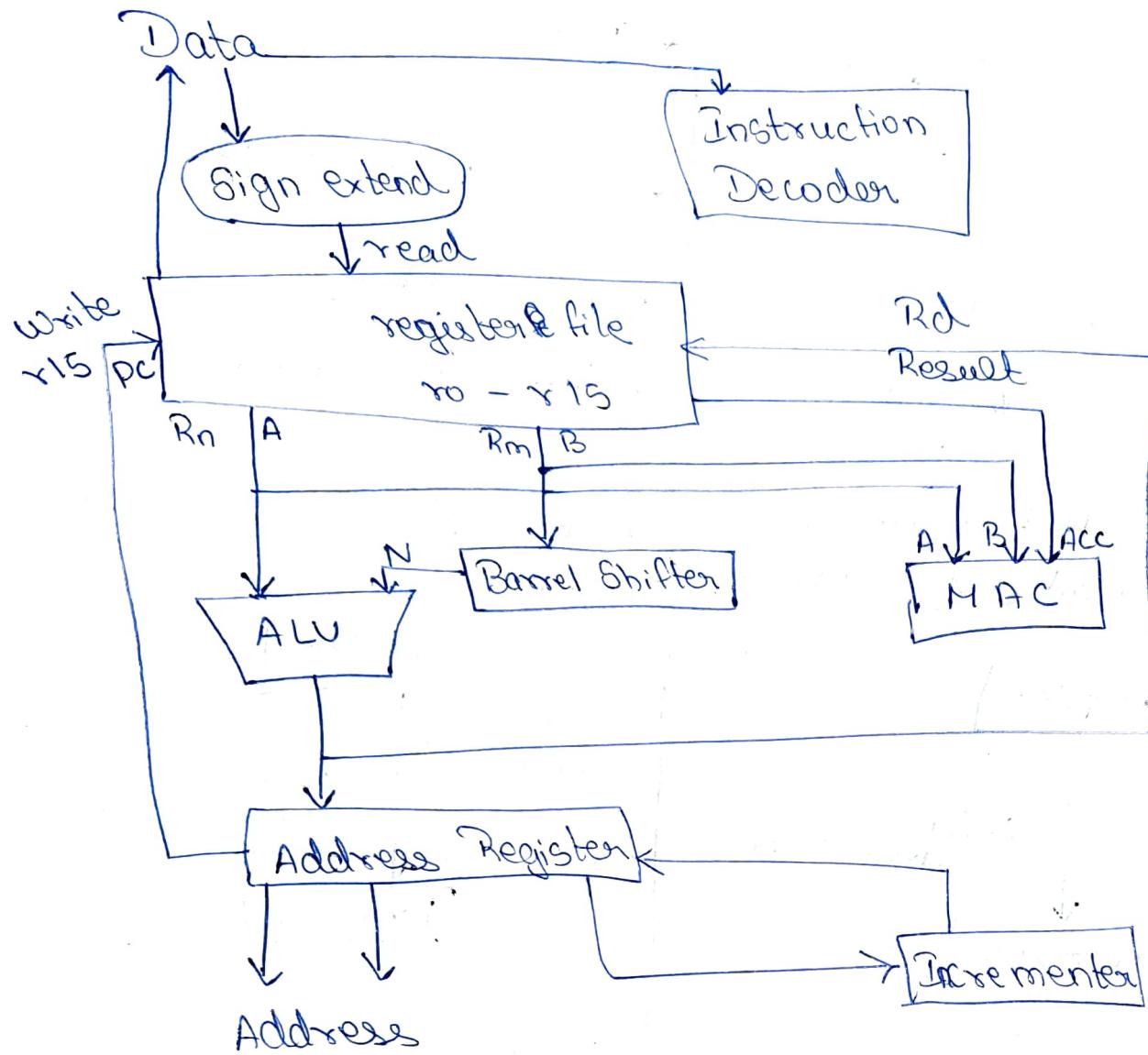


RISC

- * Emphasis on Software
- * Instruction of same size & few format.
- * Uses More Registers.
- * Few addressing Mode.
- * ~~Pipe~~ Pipelining is easy.
- * Instructions take one cycle time.



47 Data Flow Model

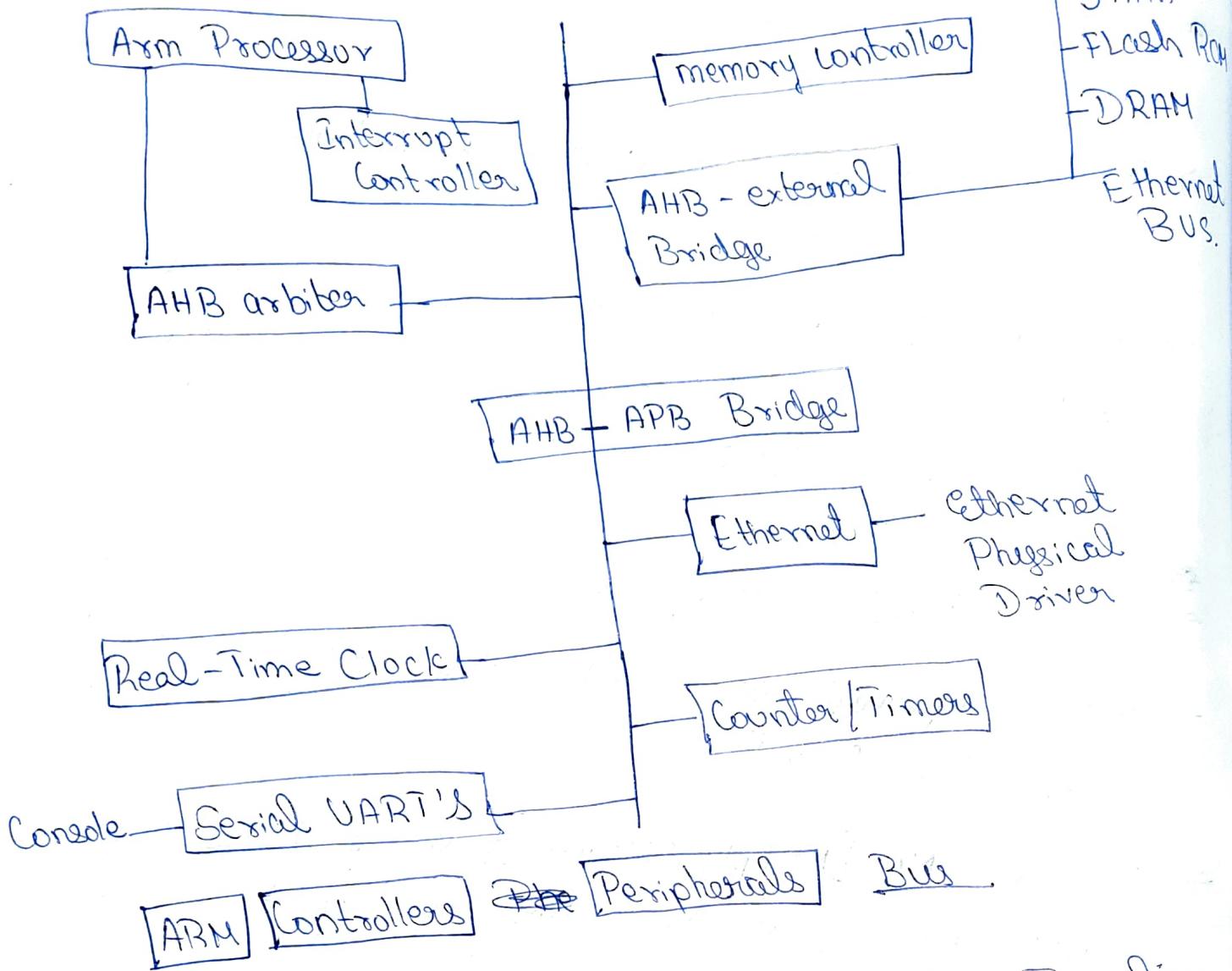


- * A data flow model is a diagrammatic representation of how data moves or is used within a system.
- * Arrows represent the flow of data, the lines represent the buses.
- * boxes represent either an operation unit or a storage area.

Working

- Data :- Data enters the processor ~~core~~ through the date bus.
- Instruction Decoder :- Translates the instruction before they are executed.
- Sign extend :- ~~Hardware~~ Hardware converts signed 8-bit or 16-bit values to 32-bit values as they are needed from memory & placed in register.
- Arm instruction have 2 source register - Rn & Rm
- Source operand are read from register file using internal bus A & B
- ALU or MAC [Multiply accumulate unit] :- Takes the register value from Rn & Rm via bus A & B. & then computes the result.
- Load & store instruction :- Data processing instruction write the result in Rd directly to the register file, it uses the ALU to generate an address to be held in Address register & broadcast onto address bus.
- The incrementer or PC updates the address register before the ~~processor~~ core reads or writes the next register value.

5) Embedded System Hardware.



→ Each box represents a feature or function. The lines connecting the boxes are the buses carrying data.

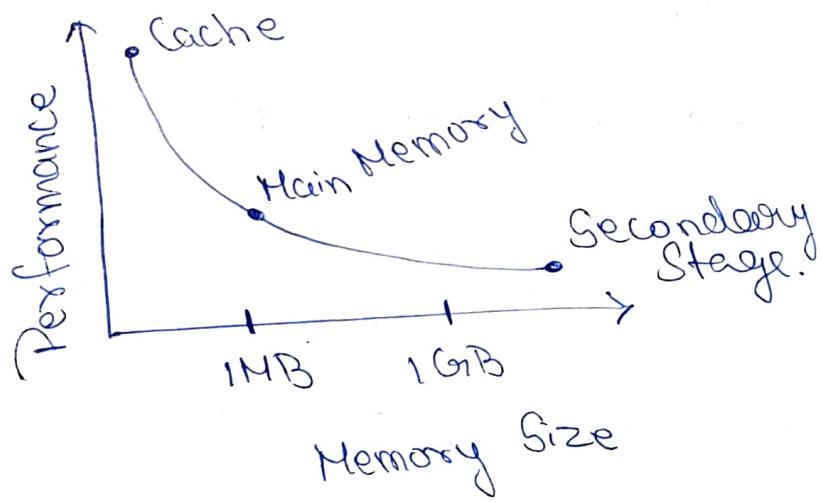
→ The device is separated into 4 main hardware components

- * **ARM Processor** :- Controls the embedded device
 - An Arm comprises of a core (The execution engine that processes instruction & manipulates data) plus the surrounding ~~surrounding~~ components that interface it with a bus.
 - Components may include memory management caches.

- Controllers :- Co-ordinate important functional blocks of a system.
- 2 commonly used controller are interrupt controller & memory controller.
- Peripherals :- Provide all the I/O capability external to the chip.
- Bus :- Used to communicate b/w different parts of the device.

7) Memory Hierarchy :-

→ The fastest memory cache is physically located nearer to the CPU processor core & the slowest secondary memory is set further away.



- Cache is placed b/w main memory & core
- Used to speed up data transfer b/w processor & main memory.
- A cache provides an overall increase in performance
- Main memory is large - around 256 KB to 256 MB
- Secondary memory is the largest & slowest form of memory.
- Memory width has a direct effect on the overall performance & cost ratio.

Instruction Size	8 bit Memory	16-bit memory	32 bit
ARM 32 bit	4 cycles	2 cycles	1 cycle
Thumb, 16 bit	2 cycles	1 cycle	1 cycle

Different Types of Memory

ROM, RAM, DRAM, SDRAM, SRAM, PROM, EEPROM, EEPROM.

~~8) Pipeline~~

- Speeds up the execution by fetching the next

Q7 Core Extension:-

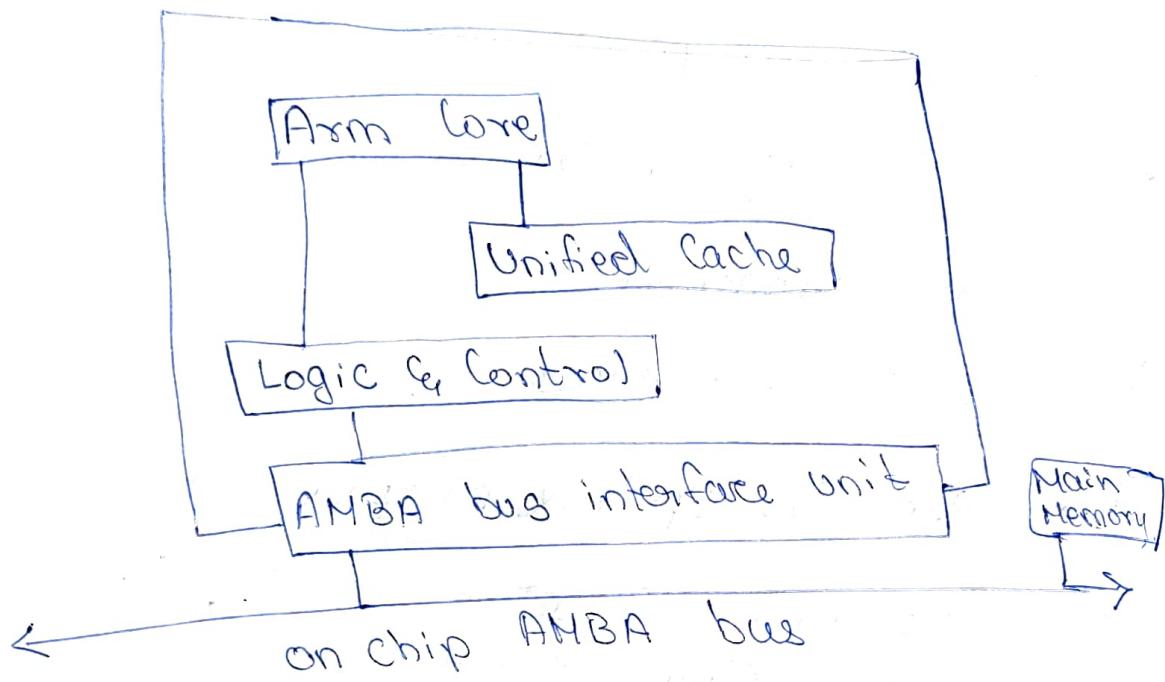
- The hardware extension are standard components placed next to the ARM core.
- They improve performance, manage resource by provide extra functionality and are designed to provide flexibility in handling particular application.
- 3 hardware extensions:
 - * Cache & Tightly coupled memory.
 - * Memory management
 - * Co-processor interface.

Q8 List ~~some~~ the Special purpose register.

- There are upto 18 active register, 16 data register & 2 processor status register.
- All the registers are 32 bits in size
- The data register are visible to programmer as r0 to r15.
- The register from r13 to r15 are special purpose register.
- r13 [Stack pointer] = Stores the head of the stack in current processor mode.

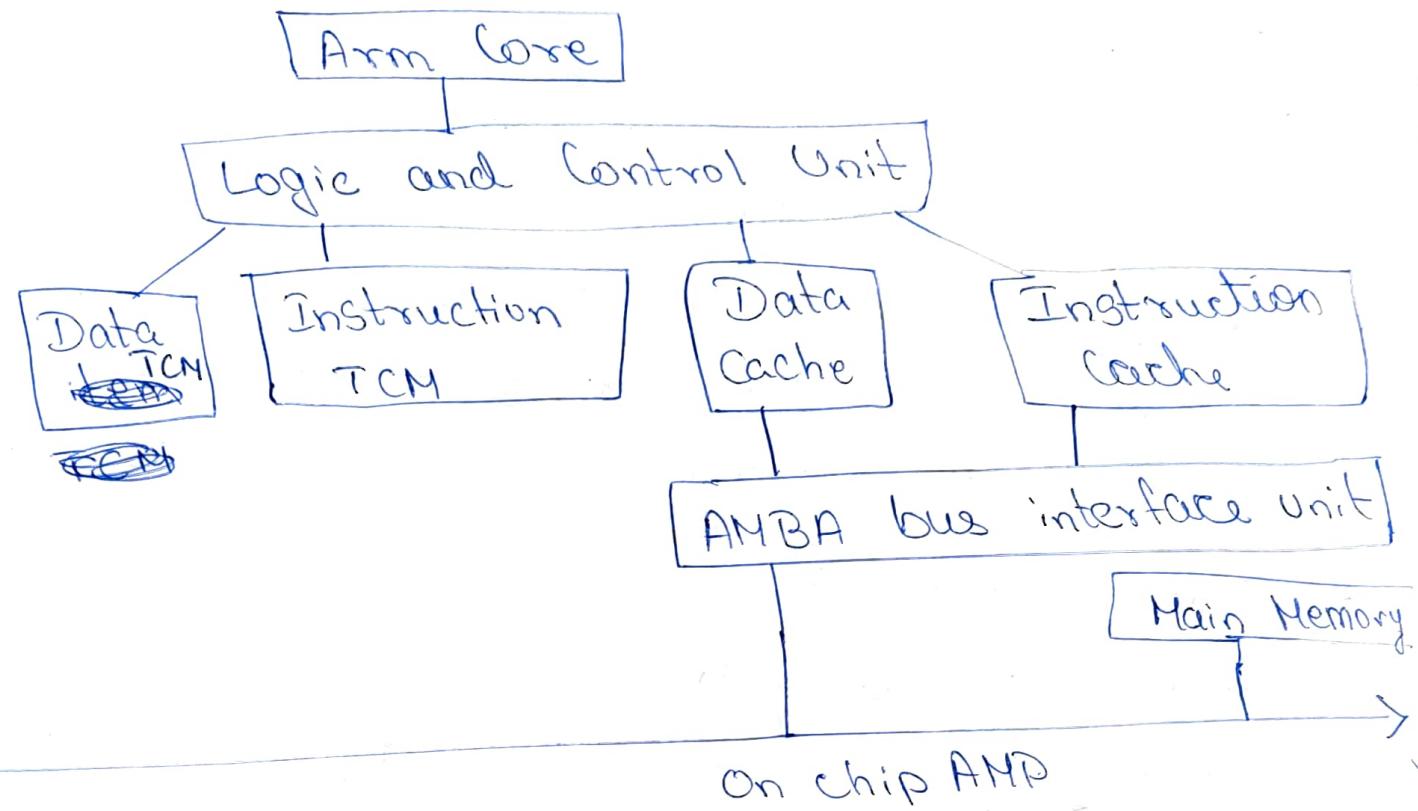
- r14 :- [link register] : where the core puts the return address whenever it calls a subroutine
- r15 :- [program counter] : contains the address of the next instruction to be fetched by the processor.

157 Von Neumann



In Von Neuman architecture, it combines both data and instruction into a single unified cache. The glue logic connects the memory system to the AMBA bus logic & control.

→ Harvard Architecture.



A cache provides small overall increase in performance but at the expense of predictable execution but for real time systems, the time taken for execution of instruction should be predictable.

RISC Philosophy

→ Instruction :-

- * RISC processors have a reduced no. of instruction classes.
- * Simple operation can be executed in a single cycle.
- * Instruction are fetched from memory, executed and the results are stored in a single cycle.

→ Pipeline.

- * The processing of instruction is broken down into smaller units that can be executed in parallel by pipelines.
- * Improves the efficiency of data processing.

- Registers
- * They have large general purpose register set.
- * Registers acts as the fastest local memory store for all data.
- Load store architecture

Processor and memory transfer depends on how fast.

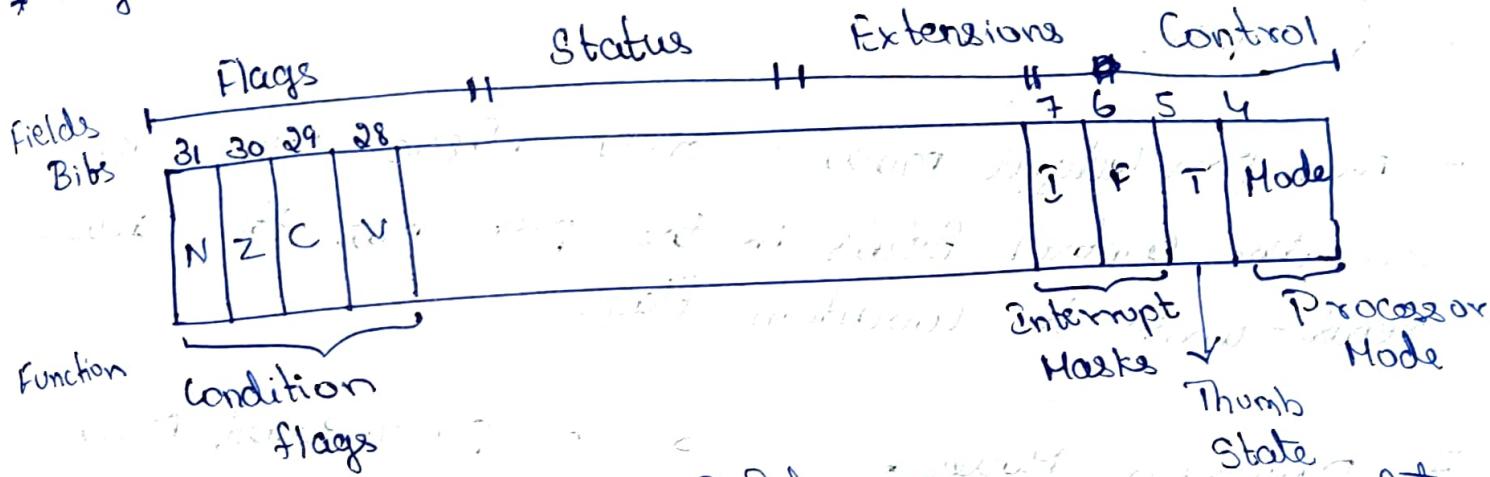
- * The speed of the processor depends on how fast data transfer b/w memory & processor.
- * Separate Local & store instruction transfer data b/w the register bank and external memory.

The Arm Design Philosophy :- What the manufacturer wants

- Smaller system are price sensitive & use below and low-cost memory devices.
- Price:- Embedded System needs a better memory for less and low-cost memory devices.
- Size of chip :- To reduce the area of the die taken up by the embedded processor.
- The ARM processor has been specifically designed to be small to reduce power consumption.

CPSR

- ⇒ Dedicated 32-bit register it resides in the register file.
- ⇒ Func. :- To monitor or control internal operations.
- ⇒ The CPSR is divided into 4 fields, each 8 bits wide.
- * flag * status * extensions * control.
- * flag



- ⇒ The extension and status fields are reserved for future use.
- ⇒ The control field contains the processor mode, state & interrupt mask bit.

N = -ve result from ALU. hence sign bit = 1
 Z = Zero " "
 C = ALU operation carried out overflowed.
 V = " "

Processor Modes

- determines which registers are active and the access rights to the CPSR itself.
- Modes are
- privileged mode :- allows full read - write access to CPSR.
 - Non-privileged mode :- only allows read access to the control fields in the CPSR but still allows read - write to condition flags.

7. Processor Modes

6 in privileged mode

1 in Non-privileged mode

Privileged Mode

- Abort
- Fast interrupt request [FIR]
- Interrupt request [IR]
- Supervisor
- System
- Undefined

Non-Privileged Mode

- User.

- Abort mode :- when there is a failed attempt to access memory.
- FIR & IR modes correspond to 2 interrupt levels available on the ARM processor
- System mode :- is a special version of user mode that allows full read - write access to the CPSR.
- Undefined mode is used when processor encounters an instruction that is undefined or not supported by the implementation.
- User mode is used for pgms in API
- Supervisor mode is the mode that the processor is in after reset and is generally the mode that an O.S kernel operates in.

Banked Registers

- All 37 registers in the register file, where 20 registers are hidden from a pgm at different times.
- These are available only when the processor is in a particular mode.
- e.g.: Abort mode has banked registers r13-abt, r14-abt & Spsr-abt.

- ~~→ Every processor mode except user mode can change mode by writing directly to the mode bits of the CPSR~~
- There is no SPSR available in user mode
- Another feature is that the CPSR is not copied into the SPSR when a mode change is forced due to a pgm writing directly to the CPSR.
- The saving of the CPSR only occurs when an exception or interrupt is raised: it is not saved in user mode.
- Every processor mode except user mode can change mood by writing directly to the mode bits of the CPSR.
- All processor modes except System mode have a set of associated banked registers that are a subset of the main 16 registers. One register maps one to one onto a user mode register.
- If change in processor mode, a banked register from the new mode will replace an existing register.

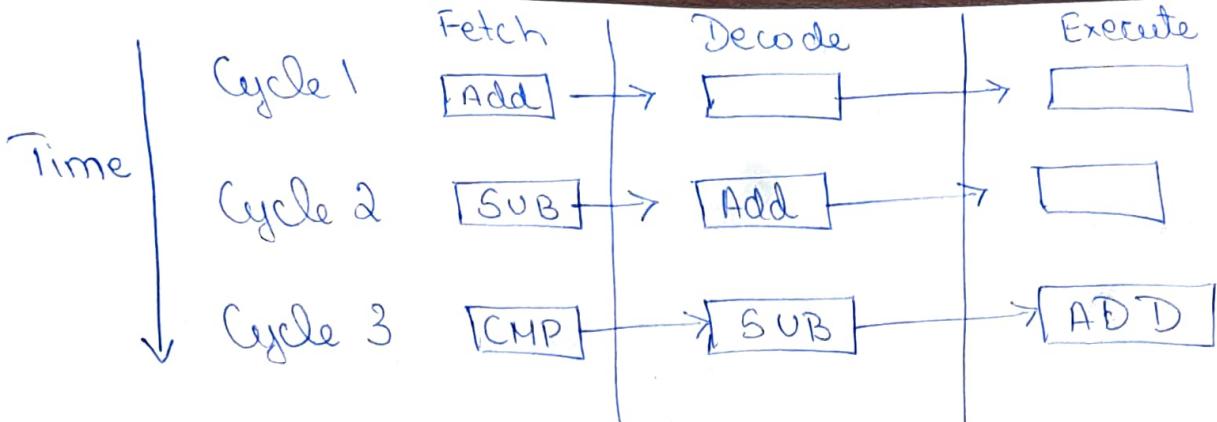
State and Instruction Sets

- ARM
- Thumb
- Jazelle

- The ARM instruction set is only active when the processor is in ARM state.
- The Jazelle T and Thumb T bits in the CPSR reflect the state of the processor.
 - When both T and T bits are 0, the processor is in ARM state and executes ARM instruction
 - When the T bit is 1, then the processor is in Thumb state.
 - Jazelle executes 8-bit instructions and is a hybrid mix of software and hardware designed to speed up the execution of java bytecodes.
 - Hardware portion of Jazelle only supports a subset of the java bytecodes.

Pipeline

- Fetch loads an instruction from memory.
- Decode identifies the instruction to be executed.
- Execute processes the instruction and writes the result back to a register.



- It shows a sequence of three instructions being fetched, decoded and executed by the processor.
- Each instruction takes a single cycle to complete after the pipeline is filled.
- The 3 instructions are placed into the pipeline sequentially.
- In the first cycle the core fetches the Add instruction from memory.
- In second cycle the core fetches the SUB instruction and decodes the ADD instruction.
- In 3rd cycle, both the SUB and ADD instruction are moved along the pipeline. The ADD instruction is executed, the SUB instruction is decoded & CMP instruction is fetched.

6) Arm Bus Technology.

- Most common bus tech. connects device such as video cards & harddisks controller to the ~~the~~ x86 processor bus.
- Embedded devices such as on-chip bus that is internal to the chip allows different peripheral devices to be interconnected with an arm core.
- 2 diff classes of device attached to the bus.
 - * Arm processor core in a Bus master:- Logical device capable of initiating data transfer with another device across the same bus.
 - * Peripherals tends to be bus slaves:- A logical device capable only of responding to a request from a bus master.
- First is a physical level :- That covers the electrical characteristics and bus width.
- Second level deals with a protocol :- The logical rules that govern the communication b/w a processor & a peripheral.

- 16) AMBA [Advanced Microcontroller Bus architecture]
 - First AMBA bus introduced were ARM System Bus (ASB) & Arm Peripheral bus (APB)
 - Later Arm High performance Bus was introduced (AHB)
 - AHB provides higher throughput than ASB because it is based on centralized multiplexed bus Scheme rather than ASB bidirectional bus design.
 - This change allows the AHB bus to run at higher clk speed and to be the 1st Arm bus to support widths of 64 bits Arm has introduced 2 variations on AHB bus.
 - * Multilayered AHB :- allows multiple active bus masters.
 - * AHB lite :- as a subset of the AHB bus and is limited to single bus master.