Design of an FPGA Integrated Circuit with 20 Configurable I/O Pins and 16 Logic Units

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***Abstract*-Due to a high degree of flexibility, faster operation and reasonable price FPGAs are very popular over other available in-place programmable devices. They are widely used in data centers, computer vision systems, real-time systems and most importantly for designing ASICs. In this project, an FPGA integrated circuit have been developed consisting 16 configurable logic blocks and 20 configurable input/output pins. Each configurable logic block can replicate any 4-input logic equation. Verilog HDL has been employed to design the RTL of the FPGA integrated circuit. For synthesis of the designed RTL and physical design of the integrated circuit, Cadence® Genus and Cadence® Encounter software has been used. The design has undergone static timing analysis to see whether the designed FPGA has any timing errors. During simulation, some violations have been identified, and the optimization process took care of them. Despite the completion of the optimization process we still got max_fanout violation, which indicates that our system only supports higher fanouts. Finally, the physical verification tests have been performed to check whether there are any physical errors.**

BACKGROUND

The first FPGA was developed in 1985 [5]. Since the first production it has gone through enormous development. Today's FPGAs even contains dedicated digital signal processing blocks and micro controlling units. The main building blocks of the design we have achieved are,

- Configurable Logic Block
- Switch Block
- Connection Block
- Input/Output Block
- Memory Controller
- Serial Input Parallel Output Shift Registers
- Interconnects

a. Configurable Logic Block: In the proposed design customized 4 input Configurable Logic Blocks (Fig. 1) are used as the main logic unit. The CLBs also contain a memory element (D Flip-flop). 2 LUT (Look-up Table) with 3 input pins are used as basic logic elements [4]. So, the CLB has two modes. One is 3 input mode and another is 4 input mode. The main building block of LUTs is MUX. We use the selector pin of the MUX as the input of desired digital logic equation. The MUX input pins are connected to the output of the dedicated SIPO (Serial Input Parallel Output Shift) block, which mainly contains the configurable bits used for constructing the desired logic. Also, two MUXs are implemented in the design so that the clock modes and output modes can be configured.

b. Switch Block: The Switch Block (Fig. 2) contains 64 sub-blocks called Switch Unit, which create routes between the interconnects. The switching operation inside each Switch Units is done using 6 transmission gates.

c. Connection Block: The Connection Block (Fig. 3) contains 48 sub-blocks called Connection Unit, which latches the CLB pins to the interconnects. The latching operation inside each Connection Units is done using 2 transmission gates.

d. Input/Output Block: This Input/Output Blocks (Fig. 4) contains 10 transmission gates that help the input/output pad to form connection with the logic cells.

e. Memory Controller: This Memory Controller Block (Fig. 5) is very important to decide the direction of the bitstream while programming the FPGA. It actually contains two 1 to 128 DEMUX. The selector pin of these DEMUXs is the 7-bit address pin. One DEMUX is used for redirecting the bitstream and another one is for selecting where to write the bitstream. It also consists of a dedicated output flag to indicate that the programming is completed. The 7-bit address is generated using a address generator block. The address block changes the address whenever a write operation is completed for a selected block.

f. Serial Input Parallel Output Shift Register: This Block (Fig. 6) is used as the memory device in our design. While programming with each clock pulses the input bitstream is shifted until the last bit is reached. The parallel output of SIPO helps to reach every necessary configuration pin at a time.

g. Interconnects: They are basically a net of 8-bit buses which offers any other block to get connected to it. It actually connects all the necessary blocks to attain desired logic.

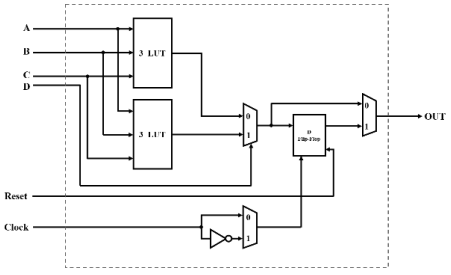

Fig. 1. Configurable Logic Block

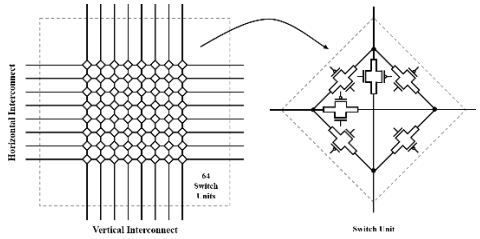

Fig. 2. Switch Block

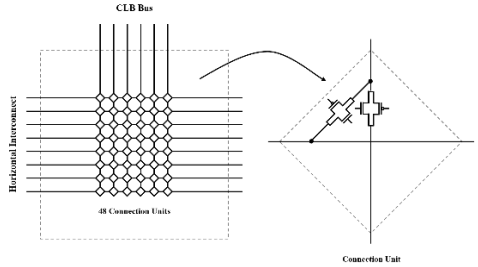

Fig. 3. Connection Block

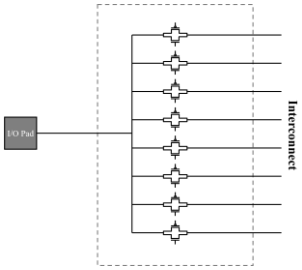

Fig. 4. Input/Output Block

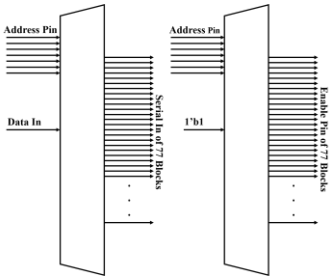

Fig. 5. Memory Controller Block

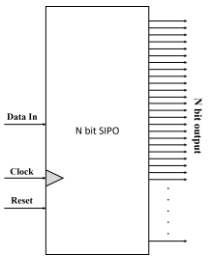

Fig. 6. SIPO Block

FUTURE ASPECTS

The future aspect of our design depends on several factors, including the continuing development of technology and the needs of the market. However, some possible future developments for such a device might include:

a. Increased Capabilities: The number of I/O pins and logic units in our FPGA are likely to increase in the future, allowing for greater functionality and more complex designs.

b. Increased Integration: It is possible that our future FPGAs will be integrated with more advanced components, such as MCU, DSP units, SRAM as memory element to form more advanced processing solution.

c. Increased I/O Block Functionality: Our future design might include multiple logic voltage adaptability feature and protection schemes.

d. Advancement of CLB: In future design the configurable logic blocks might consist more input and output pins and an adaptive design might be achieved with carry chain feature.

CONCLUSION

We have successfully implemented our RTL design and completed the Synthesis, PNR operation, Static Timing Analysis and finally the Physical Verification.

In this project we couldn't use SRAM for configuration bits because of complexity and shortage of time. Instead, we have used SIPO shift registers. During synthesis we figured out that genus does not support switch level RTL. So, we had to design transmission gates using and buffers. Also, we had to figure out which clock to use as the base clock. After executing the project and it successfully run. During Physical Verification we faced DRV violation as max_fanout violation. We let the design undergo another iteration of synthesis with max_fanout value of 60. But still got the violation. Also, we got 136 DRC violations due to vias placement, but was not able to fix those because of selection issue.

REFERANCE

[1] https://www.elprocus.com/fpga-architecture-and-applications/#:~:text=The%20general%20FPGA%20architecture%20consists,interconnection%20between%20the%20logic%20blocks
[2] https://www.nowpublishers.com/article/Details/EDA-005
[3] https://doi.org/10.1007/978-1-4614-3594-5_2
[4] https://www.wikiwand.com/en/Logic_block
[5] https://digilent.com/blog/history-of-the-fpga

TABLE I
SDC CONSTRAINTS

Initial Clock frequency (MHz)	Maximum transition (ns)	Driving cell	Operating conditions	Output delay (ns)	Max Fanout
66.67	3	BUFX16	slow	0.6	18

TABLE II
DESIGN CONSTRAINTS

Distance between Die and Core	Ring (Width, Distance)	Stripe (Number of sets)	Initial Placement Density	Offset
11	3,2	3	50	1

TABLE III
RESULT

Parameter	Value
Initial density (%)	51.149
Final density (%)	102.11
Total placed cells	63570
Dynamic power (nW)	8063237.998
Leakage power (nW)	5739.881
Total power (nW)	8068977.879
Initial timing violations	0
Remaining timing violations	0
Initial DRV violations	2 (max_cap), 24 (max_tran), 2 (max_fanout)
Remaining DRV violations	37 (max_fanout)
Physical verification violations	0
Power analysis violations	0

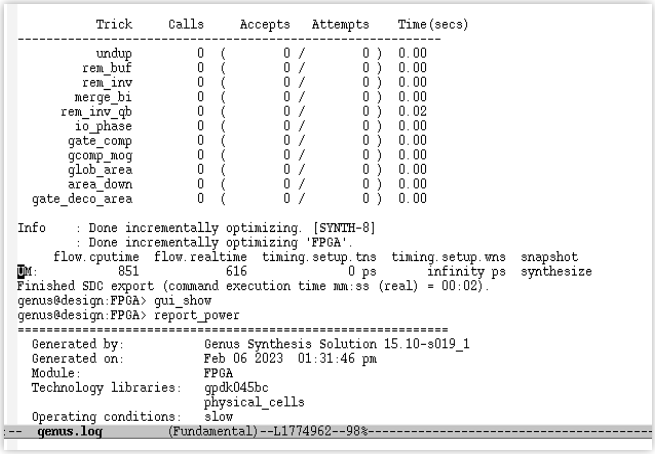

Fig. 7. Synthesis Result

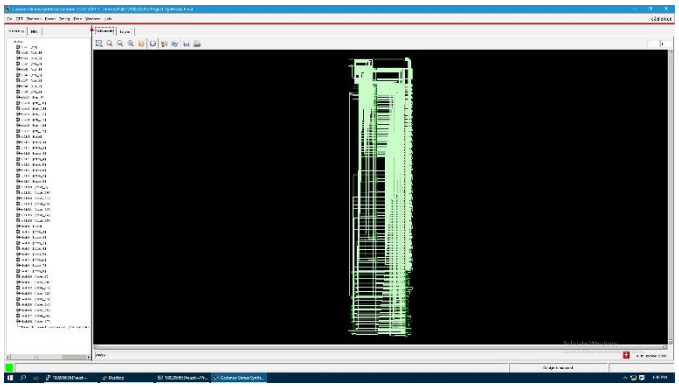

Fig. 8. Synthesized Circuit

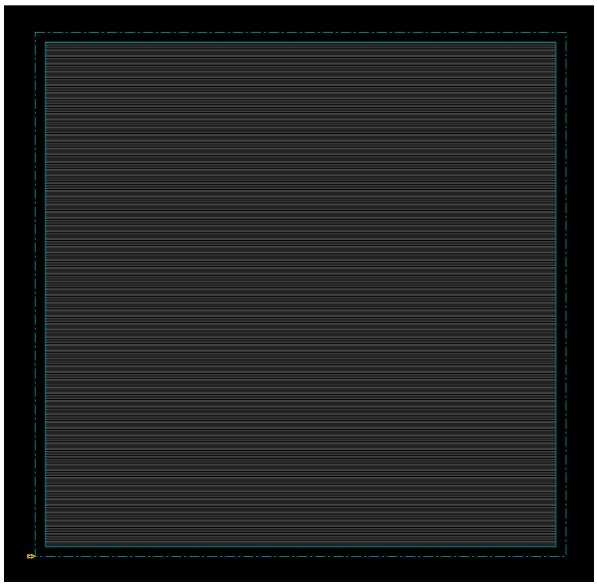

Fig. 9. Floorplan

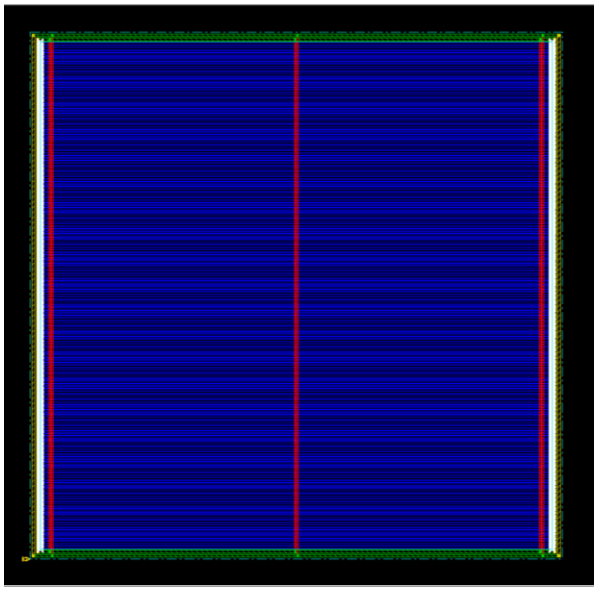

Fig. 10. Power Plan

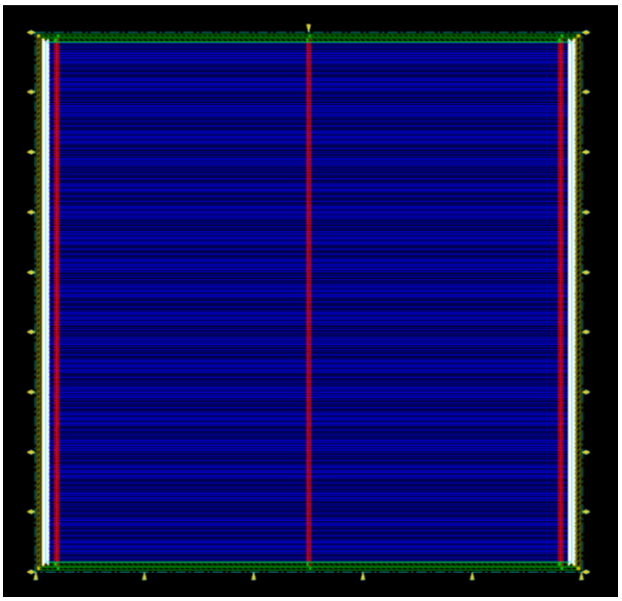

Fig. 11. Pin Placement

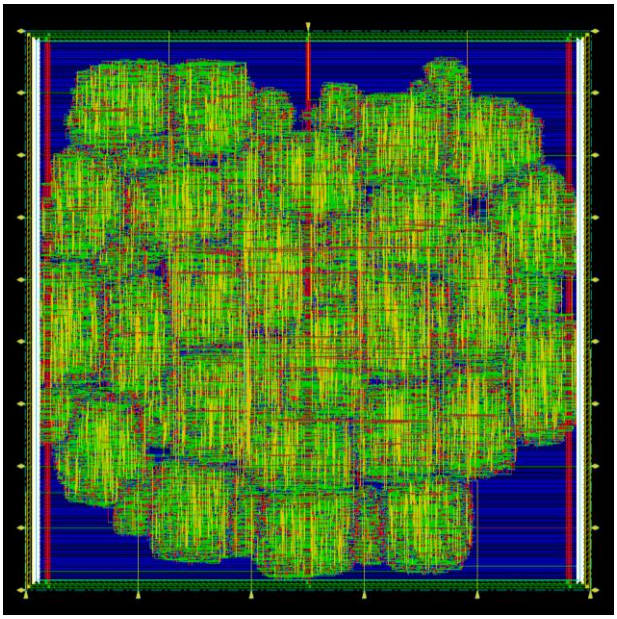

Fig. 12. Placement

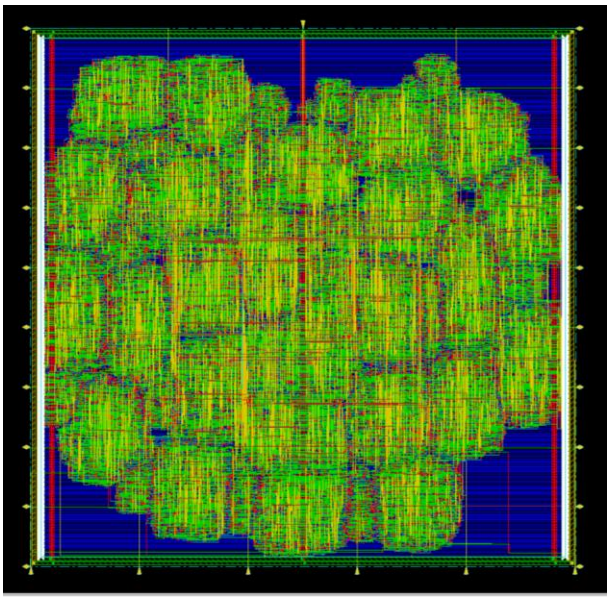

Fig. 13. Placement (Optimized)

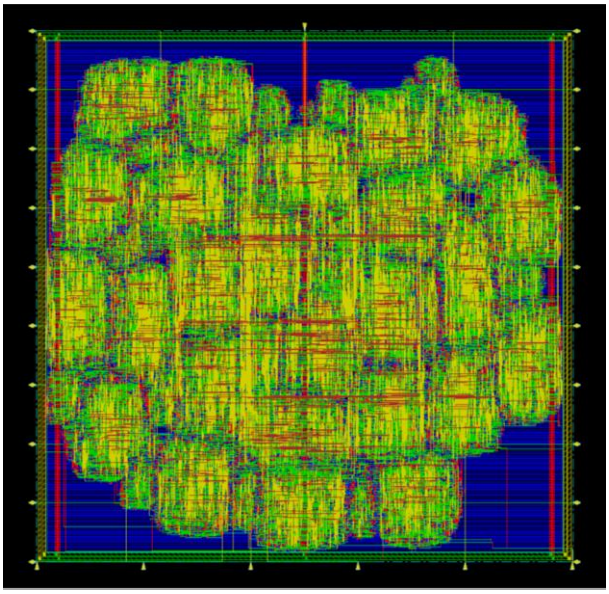

Fig. 14. Placement (Post Route)

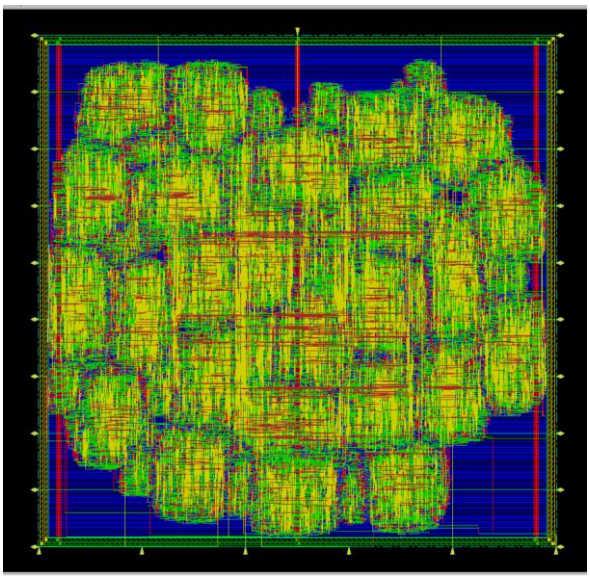

Fig. 15. Placement Optimized (Post Route)

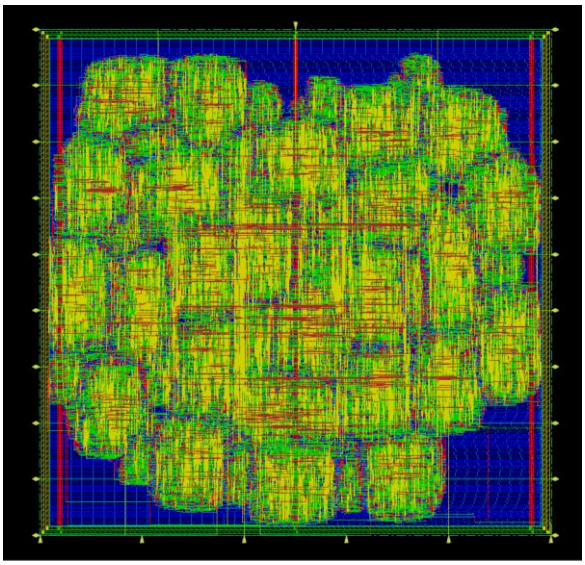

Fig. 16. Filler Cell Added

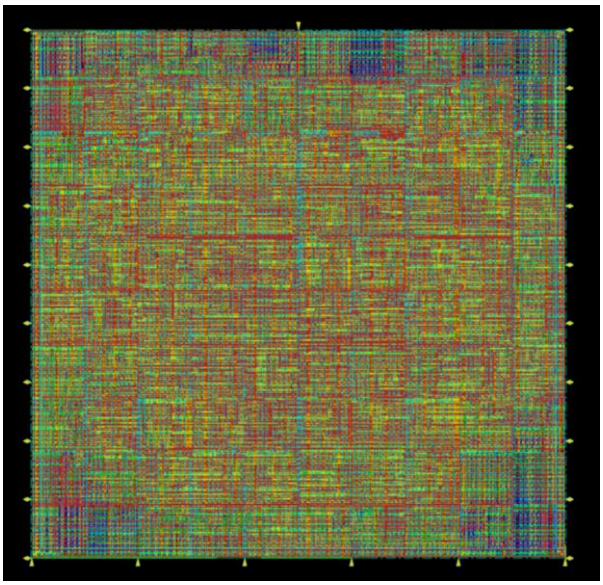

Fig. 17. Metal Filler Added

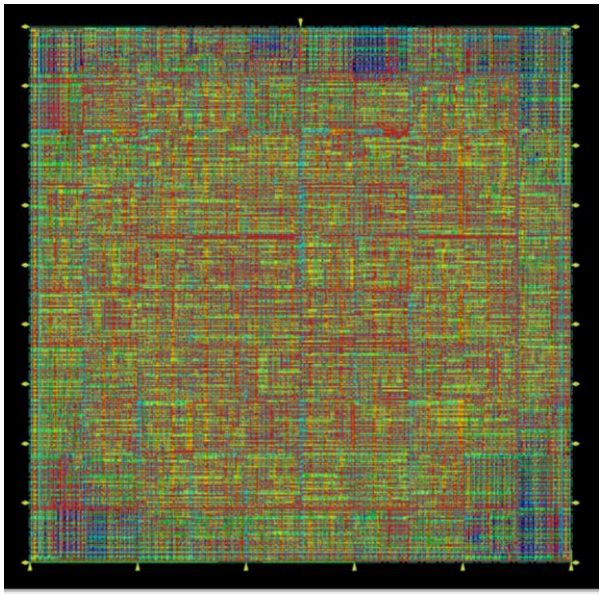

Fig. 18. Final Design after Static Timing Analysis, Physical Verification and Power Analysis

timeDesign Summary

Setup mode	all	reg2reg	default
WNS (ns):	0.000	N/A	0.000
TNS (ns):	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	0	N/A	0

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	2 (2)	-8.287	2 (2)
max_tran	24 (160)	-1.124	44 (476)
max_fanout	2 (2)	-10030	2 (2)
max_length	0 (0)	0	0 (0)

Density: 51.149%

Fig. 19. Pre-CTS Time Design Summary (DRV and setup violations)

Total 26 DRV violations are visible here. 2 of them is max_cap indicating that for 2 nets the maximum capacitance value excided. 24 violations of max_tran indicates that maximum transition of 3 ns is violated for 24 nets. And max_fanout violation indicates that for 2 nets the value of fanout excided 18.

optDesign Final Summary

Setup mode	all	reg2reg	default
WNS (ns):	0.000	N/A	0.000
TNS (ns):	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	0	N/A	0

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	20 (143)
max_fanout	37 (37)	-57	37 (37)
max_length	0 (0)	0	0 (0)

Density: 52.100%

Fig. 20. Pre-CTS Time Design Summary After Optimization (DRV and setup violations)

After optimization operation there is no max_cap and max_tran violation. But 37 violations are present as max_fanout. This max_fanout violations indicates that for 37 nets the value of fanout excided 18. To resolve this violation, we have let the design undergo another iteration consisting of maximum fanout value 60. But, after running static timing analysis we still got violations.

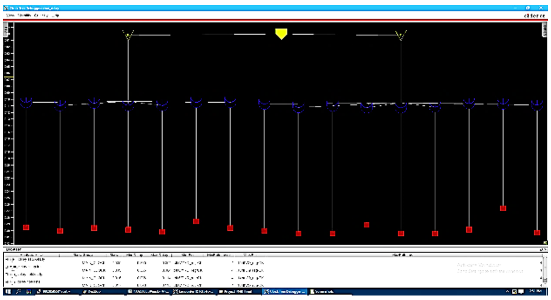

Fig. 21. Clock Tree Diagram

timeDesign Summary

Setup mode	all	reg2reg	default
WNS (ns):	0.000	N/A	0.000
TNS (ns):	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	0	N/A	0

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	19 (141)
max_fanout	37 (37)	-57	37 (37)
max_length	0 (0)	0	0 (0)

Density: 52.106%

Fig. 22. Post-route Time Design Summary (DRV and setup violations)

Total 37 violations are visible here. All of them are generated for maximum fanout error. These violations are generated from the previous analysis before clock tree synthesis

optDesign Final SI Timing Summary

Setup mode	all	reg2reg	default
WNS (ns):	0.000	N/A	0.000
TNS (ns):	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	0	N/A	0

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	19 (141)
max_fanout	37 (37)	-57	37 (37)
max_length	0 (0)	0	0 (0)

Density: 52.107%

Fig. 23. Post-route Time Design Summary After Optimization (DRV and setup violations)

After optimization operation we still got 37 violations as max_fanout.

timeDesign Summary

Hold mode	all	reg2reg	default
WNS (ns):	0.000	N/A	0.000
TNS (ns):	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	0	N/A	0

Density: 52.106%

Fig. 24. Post-route Time Design Summary (Hold violations)

There is no hold violation on post route time design Summary

```
encounter 6> verify_drc
 *** Starting Verify DRC (MEM: 882.6) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area : 1 of 16
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 2 of 16
  VERIFY DRC ..... Sub-Area : 2 complete 10 Viols.
  VERIFY DRC ..... Sub-Area : 3 of 16
  VERIFY DRC ..... Sub-Area : 3 complete 6 Viols.
  VERIFY DRC ..... Sub-Area : 4 of 16
  VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
  VERIFY DRC ..... Sub-Area : 5 of 16
  VERIFY DRC ..... Sub-Area : 5 complete 13 Viols.
  VERIFY DRC ..... Sub-Area : 6 of 16
  VERIFY DRC ..... Sub-Area : 6 complete 10 Viols.
  VERIFY DRC ..... Sub-Area : 7 of 16
  VERIFY DRC ..... Sub-Area : 7 complete 32 Viols.
  VERIFY DRC ..... Sub-Area : 8 of 16
  VERIFY DRC ..... Sub-Area : 8 complete 9 Viols.
  VERIFY DRC ..... Sub-Area : 9 of 16
  VERIFY DRC ..... Sub-Area : 9 complete 10 Viols.
  VERIFY DRC ..... Sub-Area : 10 of 16
  VERIFY DRC ..... Sub-Area : 10 complete 10 Viols.
  VERIFY DRC ..... Sub-Area : 11 of 16
  VERIFY DRC ..... Sub-Area : 11 complete 14 Viols.
  VERIFY DRC ..... Sub-Area : 12 of 16
  VERIFY DRC ..... Sub-Area : 12 complete 7 Viols.
  VERIFY DRC ..... Sub-Area : 13 of 16
  VERIFY DRC ..... Sub-Area : 13 complete 4 Viols.
  VERIFY DRC ..... Sub-Area : 14 of 16
  VERIFY DRC ..... Sub-Area : 14 complete 5 Viols.
  VERIFY DRC ..... Sub-Area : 15 of 16
  VERIFY DRC ..... Sub-Area : 15 complete 2 Viols.
  VERIFY DRC ..... Sub-Area : 16 of 16
  VERIFY DRC ..... Sub-Area : 16 complete 4 Viols.

  Verification Complete : 136 Viols.

 *** End Verify DRC (CPU: 0:00:11.9  ELAPSED TIME: 12.00  MEM: 222.0M) ***
```

Fig. 25. DRC Verification

```
  VERIFY GEOMETRY ..... Antenna         :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 21 complete 0 Viols. 0 Wrngs.
  VERIFY GEOMETRY ..... SubArea : 22 of 25
  VERIFY GEOMETRY ..... Cells           :  0 Viols.
  VERIFY GEOMETRY ..... SameNet         :  0 Viols.
  VERIFY GEOMETRY ..... Wiring          :  0 Viols.
  VERIFY GEOMETRY ..... Antenna         :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 22 complete 0 Viols. 0 Wrngs.
  VERIFY GEOMETRY ..... SubArea : 23 of 25
  VERIFY GEOMETRY ..... Cells           :  0 Viols.
  VERIFY GEOMETRY ..... SameNet         :  0 Viols.
  VERIFY GEOMETRY ..... Wiring          :  0 Viols.
  VERIFY GEOMETRY ..... Antenna         :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 23 complete 0 Viols. 0 Wrngs.
  VERIFY GEOMETRY ..... SubArea : 24 of 25
  VERIFY GEOMETRY ..... Cells           :  0 Viols.
  VERIFY GEOMETRY ..... SameNet         :  0 Viols.
  VERIFY GEOMETRY ..... Wiring          :  0 Viols.
  VERIFY GEOMETRY ..... Antenna         :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 24 complete 0 Viols. 0 Wrngs.
  VERIFY GEOMETRY ..... SubArea : 25 of 25
  VERIFY GEOMETRY ..... Cells           :  0 Viols.
  VERIFY GEOMETRY ..... SameNet         :  0 Viols.
  VERIFY GEOMETRY ..... Wiring          :  0 Viols.
  VERIFY GEOMETRY ..... Antenna         :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 25 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 27.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:26.9  MEM: 93.5M)
```

Fig. 25. Geometry Verification

```
encounter 8> verify_connectivity
VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Wed Feb  8 15:46:00 2023

Design Name: FPGA
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (599.5750, 593.1600)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 15:46:00 **** Processed 5000 nets.
**** 15:46:01 **** Processed 10000 nets.
**** 15:46:01 **** Processed 15000 nets.
**** 15:46:01 **** Processed 20000 nets.
**** 15:46:01 **** Processed 25000 nets.
**** 15:46:02 **** Processed 30000 nets.
**** 15:46:02 **** Processed 35000 nets.
**** 15:46:02 **** Processed 40000 nets.
**** 15:46:02 **** Processed 45000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Feb  8 15:46:03 2023
Time Elapsed: 0:00:03.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:03.2  MEM: -0.641M)
```

Fig. 25. Connectivity Verification

```
encounter 10> verifyProcessAntenna

******* START VERIFY ANTENNA ********
Report File: FPGA.antenna.rpt
LEF Macro File: FPGA.antenna.lef
5000 nets processed: 0 violations
10000 nets processed: 0 violations
15000 nets processed: 0 violations
20000 nets processed: 0 violations
25000 nets processed: 0 violations
30000 nets processed: 0 violations
35000 nets processed: 0 violations
40000 nets processed: 0 violations
45000 nets processed: 0 violations
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
(CPU Time: 0:00:04.2  MEM: 0.000M)
```

Fig. 25. Antenna Verification

```
  VERIFY PG SHORT ...... SubArea : 20 of 25
  VERIFY PG SHORT ...... Short:  0 Viols.
  VERIFY PG SHORT ...... SubArea : 21 of 25
  VERIFY PG SHORT ...... Short:  0 Viols.
  VERIFY PG SHORT ...... SubArea : 22 of 25
  VERIFY PG SHORT ...... Short:  0 Viols.
  VERIFY PG SHORT ...... SubArea : 23 of 25
  VERIFY PG SHORT ...... Short:  0 Viols.
  VERIFY PG SHORT ...... SubArea : 24 of 25
  VERIFY PG SHORT ...... Short:  0 Viols.
  VERIFY PG SHORT ...... SubArea : 25 of 25
  VERIFY PG SHORT ...... Short:  0 Viols.
  Verification Complete : 0 Short Viols.

**********End: VERIFY PG SHORT**********
 *** verify PG short (CPU: 0:00:12.6  MEM: 0.0M)
```

Fig. 25. PG Short Verification

```
*** CDM Built up (cpu=0:00:31.7  real=0:00:32.0  mem= 1175.8M) *
Timing Analysis Mode: CTE
Irms Scale Factor: 1
Verifying all signal nets.
5000 nets processed: 0 violations
10000 nets processed: 0 violations
15000 nets processed: 0 violations
20000 nets processed: 0 violations
25000 nets processed: 0 violations
30000 nets processed: 0 violations
35000 nets processed: 0 violations
40000 nets processed: 0 violations
45000 nets processed: 0 violations

Num Violations: 0

End Time: Wed Feb  8 15:52:54 2023
******** End: verifyACLimit ********
  (CPU Time: 0:00:45.7  MEM: -10.121M)
```

Fig. 25. AC Limit Verification

```
encounter 12> verify_power_via

******** Start: VERIFY POWER VIA ********
Start Time: Wed Feb  8 15:49:59 2023

Check all 2 Power/Ground nets
*** Checking Net VDD
*** Checking Net VSS
Actually Checked 2 Power/Ground nets with physical connectivity

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Feb  8 15:49:59 2023
******** End: VERIFY POWER VIA ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.004M)
```

Fig. 25. Power Via Verification

```
encounter 13> verify_power_via -stacked_via

******** Start: VERIFY POWER VIA ********
Start Time: Wed Feb  8 15:51:12 2023

Check all 2 Power/Ground nets
*** Checking Net VDD
*** Checking Net VSS
Actually Checked 2 Power/Ground nets with physical connectivity

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Feb  8 15:51:12 2023
******** End: VERIFY POWER VIA ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.004M)
```

Fig. 25. Stacked Power Via Verification