Pipelines Temperature Controller

Specifications:

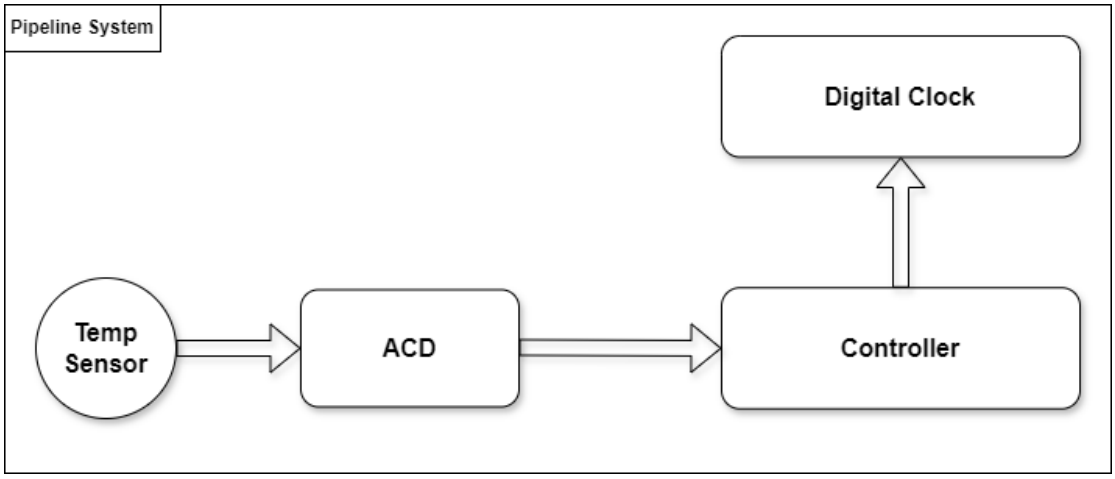
1- Temperature range from 100 C to 300 C

2- ADC 8 bits used to digitalize the signal from temperature sensor

3- Alarm at 250 C, shut down at 300 C

4- System should have reset

System Design:



This diagram created by draw.io: For best view please follow link https://shorturl.at/bxyX7

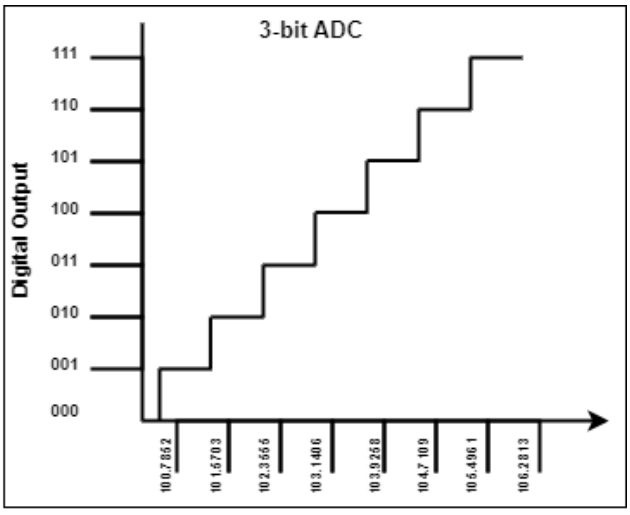
Temp Sensor: analog device used to sense the temperature of pipes and send it in analog signal to the ADC.

ADC: abbreviation to "analog to digital converter" which is a device used to digitalize the analog signal can process it easily in thee digital domain.

We have 8 bits ADC, so we have 2^8 or 256 level to represent the range from 100 to 300 C.

201(from 100 to 300) value need to digitize it in 256 level so the level will equal 201/256 = 0.78515625

So, 0.785 C is the least value can the ADC sense and that called code width which represent the **resolution of the converter** and the analog reference voltage (VREF)



ACD output table:

Degree in analog	ADC output
100 C	8'h00
100.7852 C	8'h01
101.5703 C	8'h02
. .	. .
300 C	8'hff

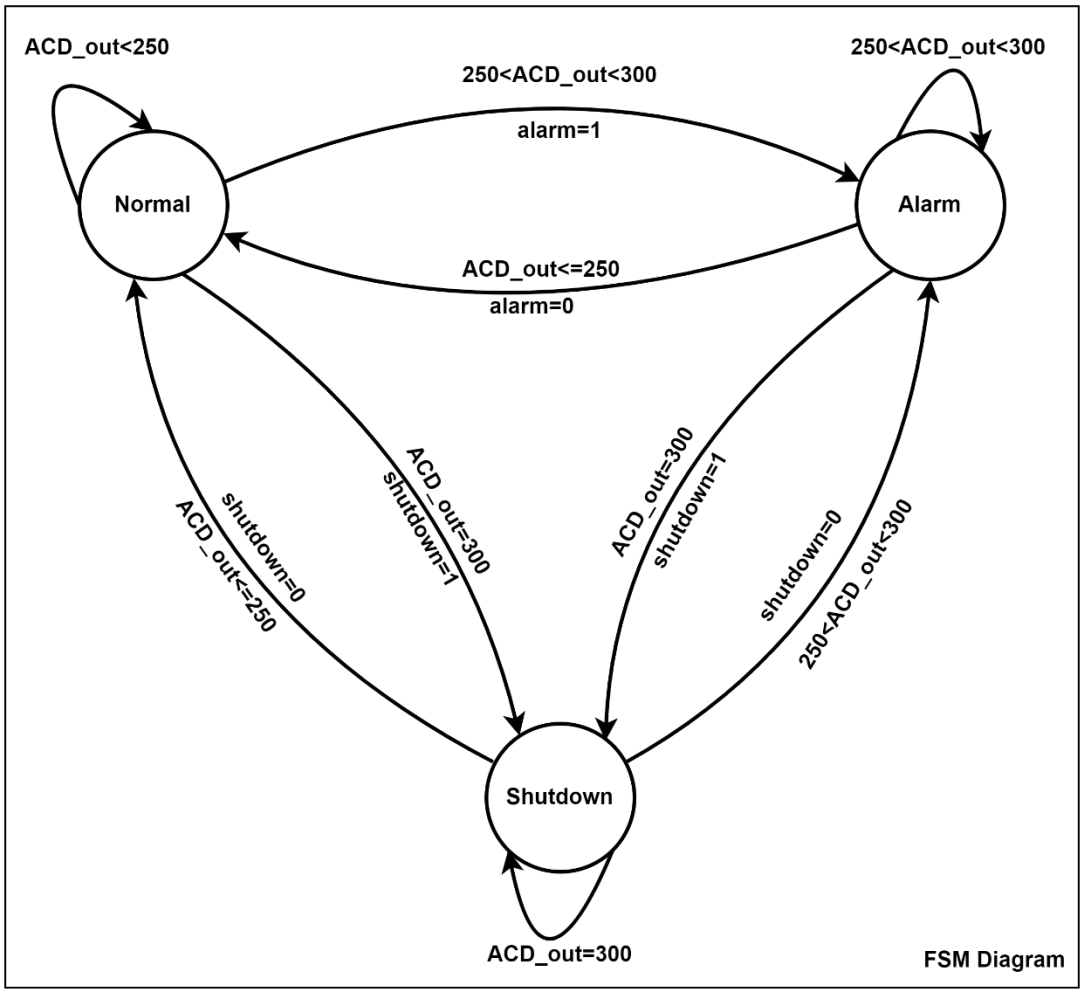
Controller: it will be FSM has 3 states:

Normal state: alarm and shut down flags = 0 and it's the state when temperature less than or equals 250 C

Alarm state: alarm flag =1 and shut down flag = 0 and it's the state when temperature less than 300 C and greater than 250 C

Shut down state: alarm flag =0 and shut down flag = 1 and it's the state when temperature equals 300 C

FSM Diagram:



Digital clock: it will used to display the temperature of pipes in hexadecimal format so it will be 3 pieces of 7segment display to can represent the range from 100 to 300.

We will take the value coming from ADC and add to it 100 then display it in the 7segments.

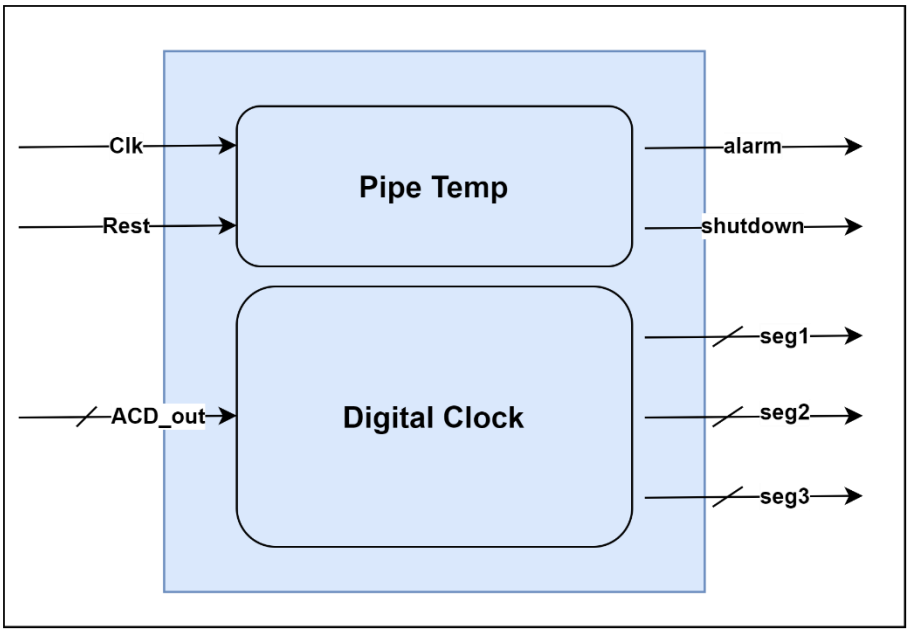
Why we add 100 to the output of ADC?

as we said before to maximize the usage of ADC we divide the levels (256) to the range of degrees (100-300) to have resolution of 0.78515625 C and that is the minimum amount of temperature can the ADC sense and 0 in ADC represent 100C in the pipes so we add 100 to the ADC output to display the correct temperature in the pipes.

A-table show input and output

Type	Port	Description	Possible Values
Inputs	clk	Clock signal for synchronous operation.	Low (0) High (1)
	reset	Asynchronous active-low reset signal.	reset (0) not reset (1)
	adc_out	8-bit input representing the output from an ADC (Analog-to-Digital Converter), which likely measures the temperature.	From 0 to 255 to represent the range from 100 to 300 in temperature 0 → 100C 255 → 300C
Outputs	alarm	Indicates whether the temperature is in an alarming state (1) or not (0).	1 → temperature between 250 and 300
	Shout down	Indicates whether the system should shut down (1) or not (0).	1 → temperature equals 300

B-Pipe system icon design:



C- Do you suggest a certain sensor?

The accuracy of the system depends on the accuracy of the ADC and temperature sensor. An 8-bit ADC can represent 2^8 or 256 level to represent the range from 100 to 300 C.

201(from 100 to 300) value need to digitize it in 256 level so the level will equal 201/256 = 0.78515625 C and that is the resolution of the system, and the minimum temperature can ADC sense.

The choice of temperature sensor depends on factors like accuracy, resolution, response time, and cost. Without knowing these specifics, it's hard to recommend a particular sensor. However, for higher accuracy, you might consider using a higher-resolution ADC and a temperature sensor with better accuracy and resolution.

Limitation of temperature sensor may be:

Accuracy

Resolution

Response Time

D- Deliver the Verilog models for your design. I made the files of:

FSM (pipe temp).v

Digital clock.v

Testbench.v

E-Provide the test vectors and test plan for your implementation.

Current state	Next state	Test vector	Expected output	State
Normal state	Normal state	Adc_out= 100	Alarm =0 Shut down = 0	succeeded
	Alarm state	Adc_out= 200	Alarm =1 Shut down = 0	succeeded
	Shut down state	Adc_out= 255	Alarm =0 Shut down = 1	succeeded
Alarm state	Normal state	Adc_out= 0	Alarm =0 Shut down = 0	succeeded
	Alarm state	Adc_out= 200	Alarm =1 Shut down = 0	succeeded
	Shut down state	Adc_out= 255	Alarm =0 Shut down = 1	succeeded
Shut down state	Normal state	Adc_out= 0	Alarm =0 Shut down = 0	succeeded
	Alarm state	Adc_out= 200	Alarm =1 Shut down = 0	succeeded
	Shut down state	Adc_out= 255	Alarm =0 Shut down = 1	succeeded

Simulation result:

```
# ******************** test the normal operation ****************************
# testcase passed
# testcase passed
# testcase passed
# ******************** finishing test the normal operation ****************************
# ******************** test the alarm operation ****************************
# testcase passed
# testcase passed
# testcase passed
# ******************** finishing test the normal operation ****************************
# ******************** test the alarm operation ****************************
# testcase passed
# testcase passed
# testcase passed
# ******************** finishing test the normal operation ****************************
# ** Note: $stop    : D:/verilog/free/Temp. Sensor/testbench.v(114)
#    Time: 150009 ps  Iteration: 0  Instance: /tb
# Break in Module tb at D:/verilog/free/Temp. Sensor/testbench.v line 114
```

Bonus

F-Synthesize the PipeTemp architecture:

Flow Summary

<<Filter>>

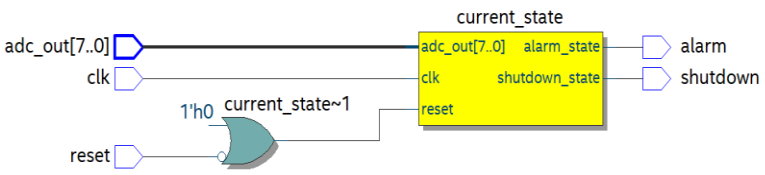
Flow Status	Successful - Mon Apr 29 19:15:24 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	PipeTemp
Top-level Entity Name	PipeTemp
Family	Cyclone IV E
Total logic elements	5 / 6,272 (< 1 %)
Total registers	2
Total pins	12 / 92 (13 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6E22C6
Timing Models	Final

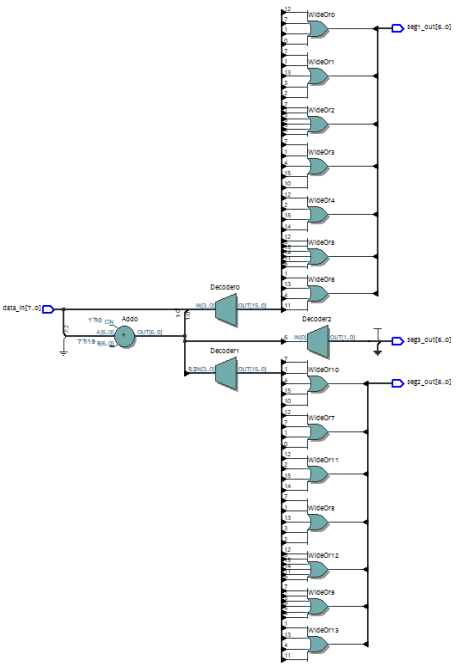
Flow Summary

<<Filter>>

Flow Status	Successful - Mon Apr 29 19:11:20 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	PipeTemp
Top-level Entity Name	SevenSegmentDisplay
Family	Cyclone IV E
Total logic elements	20 / 6,272 (< 1 %)
Total registers	0
Total pins	29 / 92 (32 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6E22C6
Timing Models	Final

G- Include a diagram of the synthesized output with your submission. [Use Quartus to get the diagram]





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