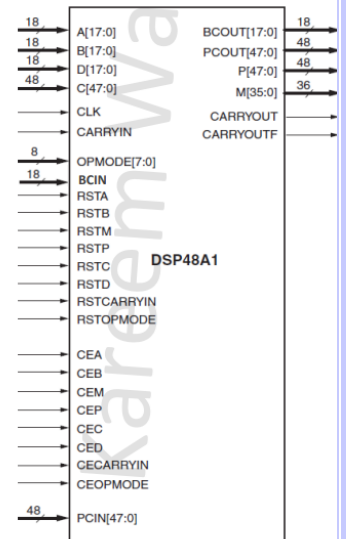


**Name Shams Khaled Ezzat****RTL CODE:**

```

module project_DSP#(
    parameter A0REG = 0, //
    parameter A1REG = 1, //
    parameter B0REG = 0, //
    parameter B1REG = 1,
    parameter CREG = 1, //
    parameter DREG = 1, //
    parameter MREG = 1, //
    parameter PREG = 1, //
    parameter CARRYINREG = 1, //
    parameter CARRYOUTREG = 1, //
    parameter OPMODEREG = 1,
    parameter CARRYINSEL = "OPMODE5", // CARRYIN ... OPMODE[5] ,
    parameter B_INPUT = "DIRECT", // .. CASCADE , ELSE ==0
    parameter RSTTYPE = "SYNC")(
    input [17:0] A, B, D, BCIN, // input ports
    input [47:0] C, PCIN, //
    input CARRYIN,
    input RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE,
    input CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE,
    input clk, // control input ports
    input [7:0] OPMODE,
    output reg [17:0] BCOUT, // output ports .... Cascade Ports
    output reg [47:0] PCOUT, // Cascade Ports
    output [47:0] P,
    output reg [35:0] M,
    output reg CARRYOUT,
    output reg CARRYOUTF);

```



```

30 reg cyi_in;
31 reg [17:0] out_b, in_b1_reg, add_sub, outZ;
32 reg [47:0] in_m_reg, inx3, in_p, outX;
33
34 wire [47:0] out_muxCY0, out_regCY0, out_muxp, out_p, out_muxM, out_regM, out_muxC, out_regC;
35 wire [7:0] out_reg_opmode, OPMODE_m;
36 wire [17:0] out_muxA1, out_regA1, out_regB1, out_muxB1, out_regD, out_muxD, out_regB, out_muxB, out_regA, out_muxA;
37 wire out_regCYI, out_muxCYI;
38
39 //1
40 reg_to_mux #(.sel_reg(OPMODEREG), .size(8), .RSTTYPE("SYNC")) OPMODE_REG(OPMODE, CEOPMODE, clk, RSTOPMODE, out_reg_opmode, OPMODE_m);
41 reg_to_mux #(.sel_reg(DREG), .size(18), .RSTTYPE("SYNC")) D_REG(D, CED, clk, RSTD, out_regD, out_muxD);
42 reg_to_mux #(.sel_reg(B0REG), .size(18), .RSTTYPE("SYNC")) B0_REG(out_b, CEB, clk, RSTB, out_regB, out_muxB);
43 reg_to_mux #(.sel_reg(A0REG), .size(18), .RSTTYPE("SYNC")) A0_REG(A, CEA, clk, RSTA, out_regA, out_muxA);
44 reg_to_mux #(.sel_reg(CREG), .size(48), .RSTTYPE("SYNC")) C_REG(C, CEC, clk, RSTC, out_regC, out_muxC);
45 reg_to_mux #(.sel_reg(B1REG), .size(18), .RSTTYPE("SYNC")) B1_REG(in_b1_reg, CEB, clk, RSTB, out_muxB1, out_regB1);
46 reg_to_mux #(.sel_reg(A1REG), .size(18), .RSTTYPE("SYNC")) A1_REG(out_muxA, CEA, clk, RSTA, out_muxA1, out_regA1);
47 reg_to_mux #(.sel_reg(MREG), .size(48), .RSTTYPE("SYNC")) M_REG(in_m_reg, CEM, clk, RSTM, out_muxM, out_regM);
48 reg_to_mux #(.sel_reg(CARRYINREG), .size(1), .RSTTYPE("SYNC")) CYI(cyi_in, CECARRYIN, clk, RSTCARRYIN, out_muxCYI, out_regCYI);
49 reg_to_mux #(.sel_reg(CARRYOUTREG), .size(48), .RSTTYPE("SYNC")) CYO(in_p, CEOPMODE, clk, RSTCARRYIN, out_muxCYO, out_regCYO);
50 reg_to_mux #(.sel_reg(PREG), .size(48), .RSTTYPE("SYNC")) P_REG(in_p, CEP, clk, RSTP, P, out_p);

```



```

52  always @(*) out_b = (B_INPUT=="DIRECT")?B:(B_INPUT=="CASCADE"?BCIN:0;
53  ▼ always @(*) begin
54  ▼      if(OPMODE_m[6])
55          add_sub = out_muxD - out_muxB;
56  ▼      else
57          add_sub = out_muxD + out_muxB;
58  end
59  always @(*) in_b1_reg =(OPMODE_m[4])?add_sub:out_muxB;
60  //2
61  always @(*) BCOUT=out_muxB1;
62  always @(*) in_m_reg = out_regA1 * out_regB1;
63  //3
64  always @(*) M = out_muxM;//36 bit
65  ▼ always @(*) begin
66  ▼      if(CARRYINSEL == "OPMODE5")
67          cyi_in = OPMODE_m[5];
68  ▼      else if(CARRYINSEL == "CARRYIN")
69          cyi_in = CARRYIN;
70          else cyi_in = 0;
71  end
72  //4
73  //.....X PIPELINING.....//
74  ▼ always @(*) begin
75  ▼      case (OPMODE_m[1:0])
76          0: outX = 0;
77          1: outX = out_muxM;
78          2: outX = PCOUT;
79          3: outX = inx3;//con
80      endcase
81  end
82  //.....Z PIPELINING.....//
83  ▼ always @(*) begin
84  ▼      case (OPMODE_m[3:2])
85          0: outZ = 0;
86          1: outZ = PCIN;
87          2: outZ = PCOUT;//pcout
88          3: outZ = out_muxC;//out reg c
89      endcase
90  end
91  ▼ always @(*) begin
92  ▼      if(OPMODE_m[7])
93          in_p = outZ-(outX+out_muxCYI);
94          else in_p = outZ+(outX+out_muxCYI);
95  end

```

```

99  always @(*) inx3= {D[11:0],A[17:0],B[17:0]};/////48 bit
100
101  always @(*) CARRYOUT = out_muxCYO;
102  always @(*) CARRYOUTF = out_muxCYO;
103  always @(*) PCOUT = P;
104
105
106
107
108  endmodule

```



## INSTANTIATED MODULE:

```
1  module reg_to_mux#(parameter sel_reg = 1,parameter size = 18,parameter RSTTYPE = "SYNC")(
2      input [size-1:0]in,
3      input clk_en,clk,rst,
4      output reg [size-1:0]out_reg,
5      output reg [size-1:0]out_mux
6  );
7  generate
8      if (RSTTYPE=="SYNC")begin
9          always @(posedge clk ) begin
10              if(rst) begin
11                  out_reg <= 0;
12              end else if(clk_en) begin
13                  out_reg <=in ;
14              end
15          end
16      end
17      else if (RSTTYPE=="ASYNC") begin
18          always @(posedge clk or posedge rst) begin
19              if(rst) begin
20                  out_reg <= 0;
21              end else if(clk_en) begin
22                  out_reg <=in ;
23              end
24          end
25      end
26  endgenerate
27
28  always @(*) out_mux=(sel_reg)?out_reg:in;
29
30  endmodule
```

## DO FILE

```
1  vlib work
2  vlog project_DSP.v reg_to_mux.v project_DSP_tb.v
3  vsim -voptargs=+acc work.project_DSP_tb
4  add wave *
5  run -all
6  #quit -sim
```



## TEST BENCH:

```

1  module project_DSP_tb#(
2      parameter A0REG = 0,//
3      parameter A1REG = 1,//
4      parameter B0REG = 0,//
5      parameter B1REG = 1,
6      parameter CREG = 1,//
7      parameter DREG = 1,//
8      parameter MREG = 1,//
9      parameter PREG = 1,//
10     parameter CARRYINREG = 1,//
11     parameter CARRYOUTREG = 1,//
12     //.....
13     parameter OPMODEREG = 1,//
14     parameter CARRYINSEL = "OPMODE5",//CARRYIN ...OPMODE[5] ,ELSE ==0
15     parameter B_INPUT="DIRECT",// ..CASCADE ,ELSE ==0
16     parameter RSTTYPE="SYNC"// ASYNC
17 );
18     reg [17:0]A;           //INPUT ports
19     reg [17:0]B;
20     reg [17:0]D;
21     reg [47:0]C;//
22     reg CARRYIN;
23     reg [17:0]BCIN;
24     reg RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE; //Reset INPUT Ports:
25     reg CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;//clk enable ports
26     reg [47:0]PCIN;//Cascade Ports
27     reg clk;              // control INPUT ports
28     reg [7:0]OPMODE;
29
30     wire [17:0]BCOUT;     //output ports ....Cascade Ports
31     wire [47:0]PCOUT; //Cascade Ports
32     wire [47:0]P;
33     wire [35:0]M;
34     wire CARRYOUT;
35     wire CARRYOUTF;
36
37
38
39 project_DSP DUT(A,B,D,BCIN,C,PCIN,CARRYIN,
40               RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,
41               CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,
42               clk,OPMODE,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
43
44 initial begin
45     clk =1;
46     forever #10 clk =~clk;//wait 10nsec for freq 100MHz
47 end
48
49 initial begin
50     A = 0;
51     B = 0;
52     C = 0;
53     D = 0;
54     OPMODE = 0;
55     CARRYIN = 0;
56     BCIN = 0;
57     PCIN = 0;
58     CEA = 0;CEB = 0;CEC = 0;CED = 0;CEM = 0;CEP = 0;CEOPMODE = 0;CECARRYIN = 0;
59     RSTP = 1;RSTA = 1;RSTB = 1;RSTM = 1;RSTP = 1;RSTC = 1;RSTD = 1;RSTCARRYIN = 1;RSTOPMODE = 1;
60     repeat(4) @(negedge clk) if( P!=0)begin
61         $display("error");
62         $stop;
63     end

```



```

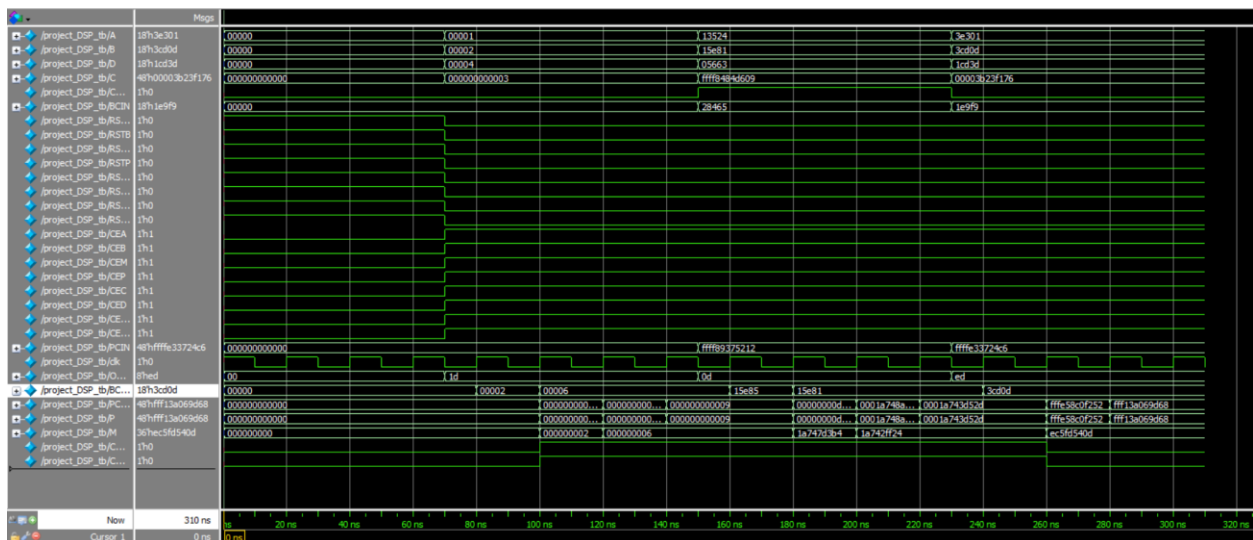
64  RSTP = 0; RSTA = 0; RSTB = 0; RSTM = 0; RSTP = 0; RSTC = 0; RSTD = 0; RSTCARRYIN = 0; RSTOPMODE = 0;
65  CEA = 1; CEB = 1; CEC = 1; CED = 1; CEM = 1; CEP = 1; CEOPMODE = 1; CECARRYIN = 1;
66  A = 1;
67  B = 2;
68  C = 3;
69  D = 4;
70  OPMODE = 8'b0001_1101;
71  CARRYIN = 0;
72  BCIN = 0;
73  PCIN = 0;
74  repeat(4) @(negedge clk);
75  A = $random;
76  B = $random;
77  C = $random;
78  D = $random;
79  OPMODE = $random;
80  CARRYIN = $random;
81  BCIN = $random;
82  PCIN = $random;
83  repeat(4) @(negedge clk);
84
85  A = $random;
86  B = $random;
87  C = $random;
88  D = $random;
89  OPMODE = $random;
90  CARRYIN = $random;
91  BCIN = $random;
92  PCIN = $random;
93  repeat(4) @(negedge clk);
94  $stop;
95  end
96  initial begin
97  $monitor("PCOUT=%d, P=%d, CARRYOUT=%d , CARRYOUTF=%d ,M=%d", PCOUT, P, CARRYOUT, CARRYOUTF , M);
98  end
99  endmodule

```

```

# Loading work.reg_to_mux(fast_3)
# Loading work.reg_to_mux(fast_4)
# PCOUT=      0, P=      0, CARRYOUT=0 , CARRYOUTF=0 ,M=      0
# PCOUT=      3, P=      3, CARRYOUT=1 , CARRYOUTF=1 ,M=      2
# PCOUT=      5, P=      5, CARRYOUT=1 , CARRYOUTF=1 ,M=      6
# PCOUT=      9, P=      9, CARRYOUT=1 , CARRYOUTF=1 ,M=      6
# PCOUT=    54799, P=    54799, CARRYOUT=1 , CARRYOUTF=1 ,M= 7101469620
# PCOUT= 7101524413, P= 7101524413, CARRYOUT=1 , CARRYOUTF=1 ,M= 7101153060
# PCOUT= 7101207853, P= 7101207853, CARRYOUT=1 , CARRYOUTF=1 ,M= 7101153060
# PCOUT=281467875816018, P=281467875816018, CARRYOUT=0 , CARRYOUTF=0 ,M=63451255821
# PCOUT=281411525713256, P=281411525713256, CARRYOUT=0 , CARRYOUTF=0 ,M=63451255821
# ** Note: $stop : project_DSP_tb.v(94)
# Time: 310 ns Iteration: 1 Instance: /project_DSP_tb
# Break in Module project_DSP tb at project_DSP tb.v line 94

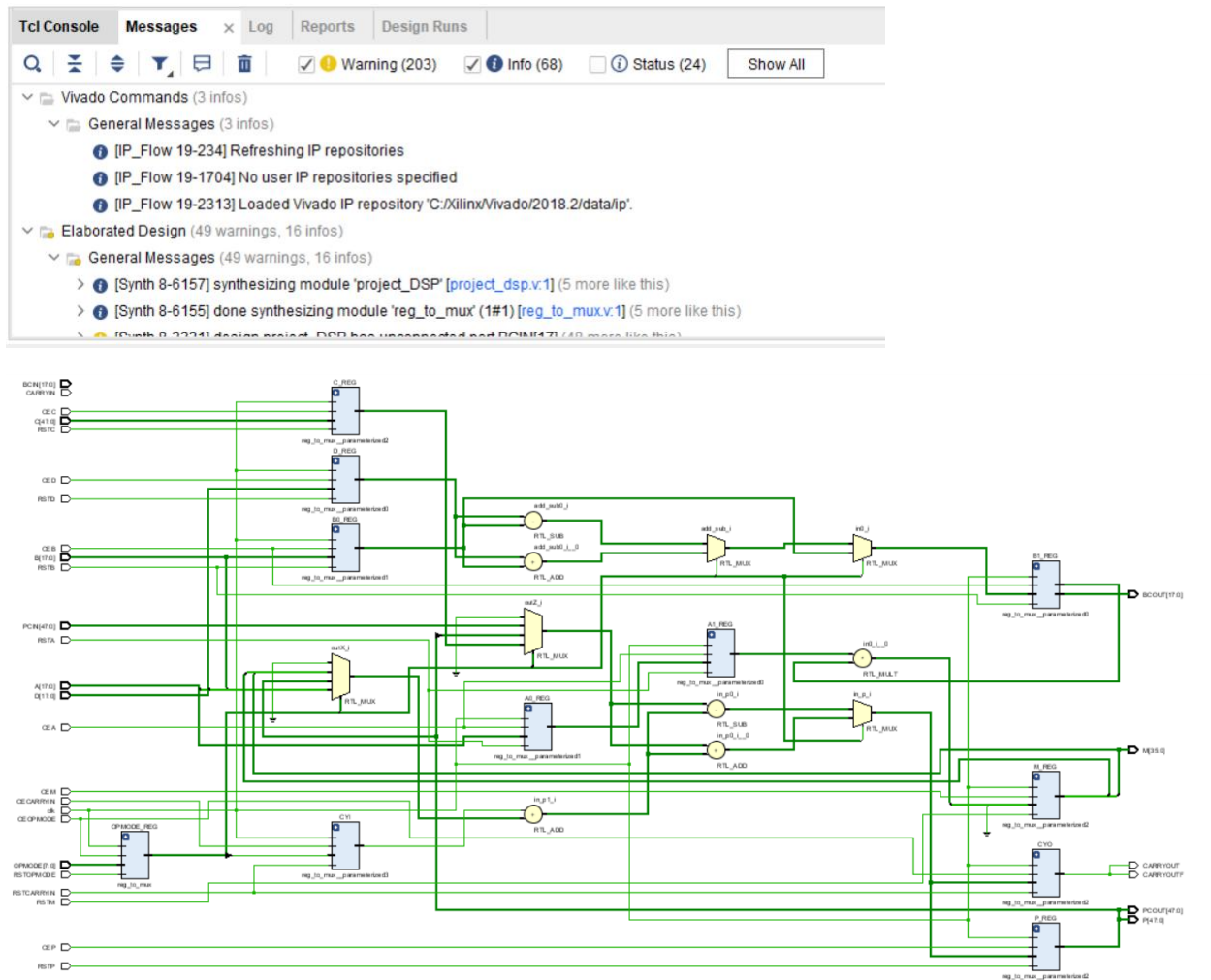
```





VIVADO:

ELABORATION:





## SYNTHESIS:

Name	Slice LUTs (134600)	Slice Registers (269200)	DSP s (740 )	Bonded IOB (500)	BUFGCTRL (32)
▼ <b>N</b> project_DSP	151	112	1	267	1
B1_REG (reg_to_mux_...	1	18	0	0	0
C_REG (reg_to_mux_...	0	18	0	0	0
CYI (reg_to_mux_par...	1	1	0	0	0
CYO (reg_to_mux_pa...	0	1	0	0	0
D_REG (reg_to_mux_...	16	18	0	0	0
M_REG (reg_to_mux_...	1	0	1	0	0
OPMODE_REG (reg_t...	132	8	0	0	0
P_REG (reg_to_mux_...	0	48	0	0	0

Tcl Console Messages Log Reports Design Runs Timing x Debug

Design Timing Summary

General Information  
Timer Settings  
Design Timing Summary  
Clock Summary (1)  
Check Timing (266)  
Intra-Clock Paths  
Inter-Clock Paths  
Other Path Groups  
Timing Summary - timing\_1

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.836 ns	Worst Hold Slack (WHS): 0.182 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 87	Total Number of Endpoints: 87	Total Number of Endpoints: 114

All user specified timing constraints are met.

Tcl Console Messages x Log Reports Design Runs Debug

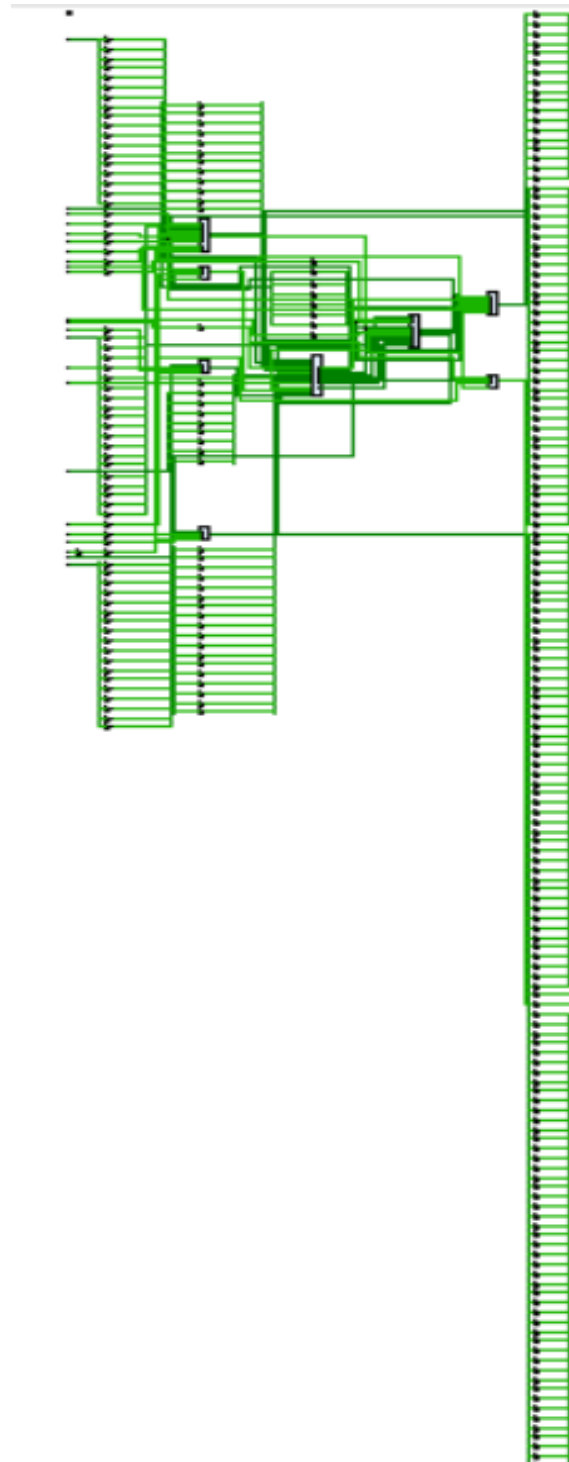
☒ Critical warning (1)
 ☒ Warning (178)
 ☐ Info (39)
 ☐ Status (21)
 Show All

▼ Synthesis (178 warnings)

- > [Synth 8-3331] design project\_DSP has unconnected port BCIN[17] (97 more like this)
- > [Synth 8-6014] Unused sequential element B0\_REG/out\_reg\_reg was removed. [reg\_to\_mux.v:11] (1 more like this)
- > [Synth 8-3332] Sequential element (C\_REG/out\_reg\_reg[47]) is unused and will be removed from module project\_DSP. (76 more like this)
- > [Constraints 18-5210] No constraint will be written out.

▼ Synthesized Design (1 critical warning)

- ▼ General Messages (1 critical warning)
  - [Vivado 12-1411] Cannot set LOC property of ports, Cannot place regular IO on system monitor or XADC site [Constraints\_basys3.xdc:67]







## Implementation:

**Tcl Console** Messages x Log Reports Design Runs Power DRC Methodology Timing

🔍 ⚙️ 📄 🗑️ ☒ Critical warning (22) ☒ Warning (180) ☐ Info (244) ☐ Status (471) **Show All**

- ▼ **Synthesis** (178 warnings)
  - > [Synth 8-3331] design project\_DSP has unconnected port BCIN[17] (97 more like this)
  - > [Synth 8-6014] Unused sequential element B0\_REG/out\_reg\_reg was removed. [reg\_to\_mux.v:11] (1 more like this)
  - > [Synth 8-3332] Sequential element (C\_REG/out\_reg\_reg[47]) is unused and will be removed from module project\_DSP. (76 more like this)
  - [Constraints 18-5210] No constraint will be written out.
- ▼ **Implementation** (11 critical warnings, 1 warning)
  - ▼ **Design Initialization** (1 critical warning)
    - ⚠️ [Vivado 12-1411] Cannot set LOC property of ports, Cannot place regular IO on system monitor or XADC site [Constraints\_basys3.xdc:67]

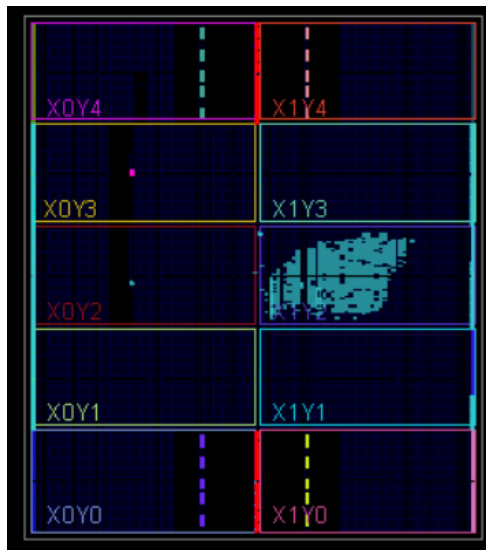
## Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 28.610 ns	Worst Hold Slack (WHS): 0.083 ns	Worst Pulse Width Slack (WPWS): 15.450 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 1036	Total Number of Endpoints: 1028	Total Number of Endpoints: 483

All user specified timing constraints are met.

🔍 ⚙️ 📄 🗑️ **hierarchy** 📄

Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSP s (740)	Bo
▼ <b>project_DSP</b>	2557	3936	69	3	1276	2137	420	1555	6.5	1	
B1_REG (reg_to_mux_...)	1	18	0	0	7	1	0	1	0	0	
C_REG (reg_to_mux_...)	0	18	0	0	6	0	0	0	0	0	
CYI (reg_to_mux_par...)	1	1	0	0	1	1	0	1	0	0	
CYO (reg_to_mux_pa...)	0	1	0	0	1	0	0	0	0	0	
D_REG (reg_to_mux_...)	16	18	0	0	12	16	0	0	0	0	
> dbg_hub (dbg_hub)	475	727	0	0	241	451	24	311	0	0	
M_REG (reg_to_mux_...)	0	0	0	0	0	0	0	0	0	1	
OPMODE_REG (reg_t...)	132	8	0	0	40	132	0	0	0	0	
P_REG (reg_to_mux_...)	0	48	0	0	12	0	0	0	0	0	
> u_ila_0 (u_ila_0)	1932	3097	69	3	997	1536	396	1186	6.5	0	





## Constraint File:

```

5
6  ## Clock signal
7  set_property -dict { PACKAGE_PIN W5      IOSTANDARD LVCMOS33 } [get_ports clk]
8  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
10
##Buttons
set_property -dict { PACKAGE_PIN U18      IOSTANDARD LVCMOS33 } [get_ports RSTP]
#set_property -dict { PACKAGE_PIN T18      IOSTANDARD LVCMOS33 } [get_ports btnU]

161 create_debug_core u_ila_0 ila
162 set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
163 set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
164 set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
165 set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
166 set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
167 set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
168 set_property C_TRIGGER_EN false [get_debug_cores u_ila_0]
169 set_property C_TRIGGER_OUT_EN false [get_debug_cores u_ila_0]
170 set_property port_width 1 [get_debug_ports u_ila_0/clk]
171 connect_debug_port u_ila_0/clk [get_nets [list clk IBUF BUF]]
172 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
173 set_property port_width 8 [get_debug_ports u_ila_0/probe0]
174 connect_debug_port u_ila_0/probe0 [get_nets [list OPMODE_IBUF[0] OPMODE_IBUF[1] OPMODE_IBUF[2] OPMODE_IBUF[3] OPMODE_IBUF[4] OPMODE_IBUF[5] OPMODE_IBUF[6] OPMODE_IBUF[7]
175 create_debug_port u_ila_0 probe
176 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
177 set_property port_width 18 [get_debug_ports u_ila_0/probe1]
178 connect_debug_port u_ila_0/probe1 [get_nets [list C_IBUF[0] C_IBUF[1] C_IBUF[2] C_IBUF[3] C_IBUF[4] C_IBUF[5] C_IBUF[6] C_IBUF[7] C_IBUF[8] C_IBUF[9] C_IBUF[10]
179 create_debug_port u_ila_0 probe
180 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
181 set_property port_width 18 [get_debug_ports u_ila_0/probe2]
182 connect_debug_port u_ila_0/probe2 [get_nets [list PCIN_IBUF[0] PCIN_IBUF[1] PCIN_IBUF[2] PCIN_IBUF[3] PCIN_IBUF[4] PCIN_IBUF[5] PCIN_IBUF[6] PCIN_IBUF[7] PCIN_IBUF[8]
183 create_debug_port u_ila_0 probe
184 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
185 set_property port_width 18 [get_debug_ports u_ila_0/probe3]
186 connect_debug_port u_ila_0/probe3 [get_nets [list A_IBUF[0] A_IBUF[1] A_IBUF[2] A_IBUF[3] A_IBUF[4] A_IBUF[5] A_IBUF[6] A_IBUF[7] A_IBUF[8] A_IBUF[9] A_IBUF[10]
187 create_debug_port u_ila_0 probe
188 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
189 set_property port_width 18 [get_debug_ports u_ila_0/probe4]
190 connect_debug_port u_ila_0/probe4 [get_nets [list D_IBUF[0] D_IBUF[1] D_IBUF[2] D_IBUF[3] D_IBUF[4] D_IBUF[5] D_IBUF[6] D_IBUF[7] D_IBUF[8] D_IBUF[9] D_IBUF[10]
191 create_debug_port u_ila_0 probe
192 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
193 set_property port_width 18 [get_debug_ports u_ila_0/probe5]
194 connect_debug_port u_ila_0/probe5 [get_nets [list B_IBUF[0] B_IBUF[1] B_IBUF[2] B_IBUF[3] B_IBUF[4] B_IBUF[5] B_IBUF[6] B_IBUF[7] B_IBUF[8] B_IBUF[9] B_IBUF[10]
195 create_debug_port u_ila_0 probe
196 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
197 set_property port_width 18 [get_debug_ports u_ila_0/probe6]
198 connect_debug_port u_ila_0/probe6 [get_nets [list BCOUT_OBUF[0] BCOUT_OBUF[1] BCOUT_OBUF[2] BCOUT_OBUF[3] BCOUT_OBUF[4] BCOUT_OBUF[5] BCOUT_OBUF[6] BCOUT_OBUF[7] BCOUT
199 create_debug_port u_ila_0 probe
200 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe7]
201 set_property port_width 36 [get_debug_ports u_ila_0/probe7]
202 connect_debug_port u_ila_0/probe7 [get_nets [list M_OBUF[0] M_OBUF[1] M_OBUF[2] M_OBUF[3] M_OBUF[4] M_OBUF[5] M_OBUF[6] M_OBUF[7] M_OBUF[8] M_OBUF[9] M_OBUF[10]
203 create_debug_port u_ila_0 probe
204 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe8]
205 set_property port_width 48 [get_debug_ports u_ila_0/probe8]

208 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
209 set_property port_width 1 [get_debug_ports u_ila_0/probe9]
210 connect_debug_port u_ila_0/probe9 [get_nets [list CARRYOUTF_OBUF]]
211 create_debug_port u_ila_0 probe
212 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe10]
213 set_property port_width 1 [get_debug_ports u_ila_0/probe10]
214 connect_debug_port u_ila_0/probe10 [get_nets [list CEA_IBUF]]
215 create_debug_port u_ila_0 probe
216 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
217 set_property port_width 1 [get_debug_ports u_ila_0/probe11]
218 connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
219 create_debug_port u_ila_0 probe
220 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
221 set_property port_width 1 [get_debug_ports u_ila_0/probe12]
222 connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
223 create_debug_port u_ila_0 probe
224 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
225 set_property port_width 1 [get_debug_ports u_ila_0/probe13]
226 connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
227 create_debug_port u_ila_0 probe
228 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
229 set_property port_width 1 [get_debug_ports u_ila_0/probe14]
230 connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
231 create_debug_port u_ila_0 probe
232 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
233 set_property port_width 1 [get_debug_ports u_ila_0/probe15]
234 connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]

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