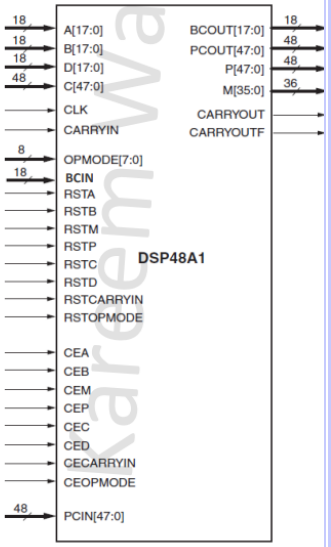
Spartan6 - DSP48A1

Name **Shams Khaled Ezzat**



RTL CODE:

```
module project_DSP#(
    parameter A0REG = 0,//
    parameter A1REG = 1,//
    parameter B0REG = 0,//
    parameter B1REG = 1,
    parameter CREG = 1,//
    parameter DREG = 1,//
    parameter MREG = 1,//
    parameter PREG = 1,//
    parameter CARRYINREG = 1,//
    parameter CARRYOUTREG = 1,//
    parameter OPMODEREG = 1,
    parameter CARRYINSEL = "OPMODE5",//CARRYIN ...OPMODE[5] ,
    parameter B_INPUT="DIRECT",// ..CASCADE ,ELSE ==0
    parameter RSTTYPE="SYNC")(
    input [17:0]A,B,D,BCIN,     //input ports
    input [47:0]C,PCIN,//
    input CARRYIN,
    input RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,
    input CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,
    input clk,          // control input ports
    input [7:0]OPMODE,
    output reg [17:0]BCOUT, //output ports ....Cascade Ports
    output reg [47:0]PCOUT, //Cascade Ports
    output  [47:0]P,
    output reg [35:0]M,
    output reg CARRYOUT,
    output reg CARRYOUTF);
```

```
30  reg cyi_in;
31  reg [17:0]out_b,in_b1_reg,add_sub,outZ;
32  reg [47:0]in_m_reg,inx3,in_p,outX;
33
34  wire [47:0]out_muxCYO,out_regCYO,out_muxp,out_p,out_muxM,out_regM,out_muxC,out_regC;
35  wire [7:0]out_reg_opmode,OPMODE_m;
36  wire [17:0]out_muxA1,out_regA1,out_regB1,out_muxB1,out_regD,out_muxD,out_regB,out_muxB,out_regA,out_muxA;
37  wire out_regCYI,out_muxCYI;
38
39  //1
40  reg_to_mux #(.sel_reg(OPMODEREG),.size(8),.RSTTYPE("SYNC")) OPMODE_REG(OPMODE,CEOPMODE,clk,RSTOPMODE,out_reg_opmode,OPMODE_m);
41  reg_to_mux  #(.sel_reg(DREG ),.size(18),.RSTTYPE("SYNC")) D_REG(D,CED,clk,RSTD,out_regD,out_muxD);
42  reg_to_mux  #(.sel_reg(B0REG),.size(18),.RSTTYPE("SYNC")) B0_REG(out_b,CEB,clk,RSTB,out_regB,out_muxB);
43  reg_to_mux  #(.sel_reg(A0REG),.size(18),.RSTTYPE("SYNC")) A0_REG(A,CEA,clk,RSTA,out_regA,out_muxA);
44  reg_to_mux #(.sel_reg(CREG ),.size(48),.RSTTYPE("SYNC")) C_REG(C,CEC,clk,RSTC,out_regC,out_muxC);
45  reg_to_mux  #(.sel_reg(B1REG),.size(18),.RSTTYPE("SYNC")) B1_REG(in_b1_reg,CEB,clk,RSTB,out_muxB1,out_regB1);
46  reg_to_mux  #(.sel_reg(A1REG),.size(18),.RSTTYPE("SYNC")) A1_REG(out_muxA ,CEA,clk,RSTA,out_muxA1,out_regA1);
47  reg_to_mux  #(.sel_reg(MREG),.size(48),.RSTTYPE("SYNC") ) M_REG(in_m_reg,CEM,clk,RSTM,out_muxM,out_regM);
48  reg_to_mux #(.sel_reg(CARRYINREG),.size(1),.RSTTYPE("SYNC")) CYI(cyi_in ,CECARRYIN,clk,RSTCARRYIN,out_muxCYI,out_regCYI);
49  reg_to_mux  #(.sel_reg(CARRYOUTREG),.size(48),.RSTTYPE("SYNC")) CYO(in_p ,CEOPMODE,clk,RSTCARRYIN,out_muxCYO,out_regCYO);
50  reg_to_mux  #(.sel_reg(PREG),.size(48),.RSTTYPE("SYNC")) P_REG(in_p ,CEP,clk,RSTP,P,out_p);
```

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```
52  always @(*) out_b = (B_INPUT=="DIRECT")?B:(B_INPUT=="CASCADE")?BCIN:0;
53  always @(*) begin
54              if(OPMODE_m[6])
55                  add_sub = out_muxD - out_muxB;
56              else
57                  add_sub = out_muxD + out_muxB;
58  end
59  always @(*) in_b1_reg =(OPMODE_m[4])?add_sub:out_muxB;
60  //2
61  always @(*) BCOUT=out_muxB1;
62  always @(*) in_m_reg = out_regA1 * out_regB1;
63  //3
64  always @(*) M = out_muxM;//36 bit
65  always @(*) begin
66              if(CARRYINSEL =="OPMODE5")
67                      cyi_in = OPMODE_m[5];
68              else if(CARRYINSEL =="CARRYIN")
69                      cyi_in =CARRYIN;
70              else cyi_in = 0;
71  end
72  //4
73  //..............X PIPELINING..............//
74  always @(*) begin
75              case (OPMODE_m[1:0])
76                  0: outX = 0;
77                  1: outX = out_muxM;
78                  2: outX = PCOUT;
79                  3: outX = inx3;//con
80              endcase
81  end
82  //..............Z PIPELINING..............//
83  always @(*) begin
84              case (OPMODE_m[3:2])
85                  0: outZ = 0;
86                  1: outZ = PCIN;
87                  2: outZ = PCOUT;//pcout
88                  3: outZ = out_muxC;//out reg c
89              endcase
90  end
91  always @(*) begin
92              if(OPMODE_m[7])
93                      in_p = outZ-(outX+out_muxCYI);
94                  else in_p = outZ+(outX+out_muxCYI);
95  end
```

```
 99    always @(*) inx3= {D[11:0],A[17:0],B[17:0]};////48 bit
100
101    always @(*) CARRYOUT = out_muxCYO;
102    always @(*) CARRYOUTF = out_muxCYO;
103    always @(*) PCOUT = P;
104
105
106
107
108    endmodule
```

INSTANTIATED MODULE:

```
module reg_to_mux#(parameter sel_reg = 1,parameter size = 18,parameter RSTTYPE = "SYNC")(
    input [size-1:0]in,
    input clk_en,clk,rst,
    output reg [size-1:0]out_reg,
    output reg [size-1:0]out_mux
);
generate
    if (RSTTYPE=="SYNC")begin
        always @(posedge clk ) begin
            if(rst) begin
                out_reg <= 0;
            end else if(clk_en) begin
                out_reg <=in ;
            end
        end
    end
    else if (RSTTYPE=="ASYNC") begin
        always @(posedge clk or posedge  rst) begin
            if(rst) begin
                out_reg <= 0;
            end else if(clk_en) begin
                out_reg <=in ;
            end
        end
    end
endgenerate

always @(*) out_mux=(sel_reg)?out_reg:in;

endmodule
```

DO FILE

```
vlib work
vlog project_DSP.v reg_to_mux.v project_DSP_tb.v
vsim -voptargs=+acc work.project_DSP_tb
add wave *
run -all
#quit -sim
```

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TEST BENCH:

```
module project_DSP_tb#(
    parameter A0REG = 0,//
    parameter A1REG = 1,//
    parameter B0REG = 0,//
    parameter B1REG = 1,
    parameter CREG = 1,//
    parameter DREG = 1,//
    parameter MREG = 1,//
    parameter PREG = 1,//
    parameter CARRYINREG = 1,//
    parameter CARRYOUTREG = 1,//
//.............
    parameter OPMODEREG = 1,//
    parameter CARRYINSEL = "OPMODE5",//CARRYIN ...OPMODE[5] ,ELSE ==0
    parameter B_INPUT="DIRECT",// ..CASCADE ,ELSE ==0
    parameter RSTTYPE="SYNC"//   ASYNC
);
    reg [17:0]A;        //INPUT ports
    reg [17:0]B;
    reg [17:0]D;
    reg [47:0]C;//
    reg CARRYIN;
    reg [17:0]BCIN;
    reg RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE; //Reset INPUT Ports:
    reg CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;//clk enable ports
    reg [47:0]PCIN;//Cascade Ports
    reg clk;            // control INPUT ports
    reg [7:0]OPMODE;

    wire [17:0]BCOUT;   //output ports ....Cascade Ports
    wire [47:0]PCOUT; //Cascade Ports
    wire [47:0]P;
    wire [35:0]M;
    wire CARRYOUT;
    wire CARRYOUTF;
```

```
project_DSP DUT(A,B,D,BCIN,C,PCIN,CARRYIN,
                RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,
                CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,
                clk,OPMODE,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);

initial begin
clk =1;
    forever #10 clk =~clk;//wait 10nsec for freq 100MHz
end

initial begin
    A = 0;
    B = 0;
    C = 0;
    D = 0;
    OPMODE = 0;
    CARRYIN = 0;
    BCIN = 0;
    PCIN = 0;
    CEA = 0;CEB = 0;CEC = 0;CED = 0;CEM = 0;CEP = 0;CEOPMODE = 0;CECARRYIN = 0;
    RSTP = 1;RSTA = 1;RSTB = 1;RSTM = 1;RSTP = 1;RSTC = 1;RSTD = 1;RSTCARRYIN = 1;RSTOPMODE = 1;
       repeat(4) @(negedge clk) if( P!=0)begin
            $display("error");
            $stop;
        end
```

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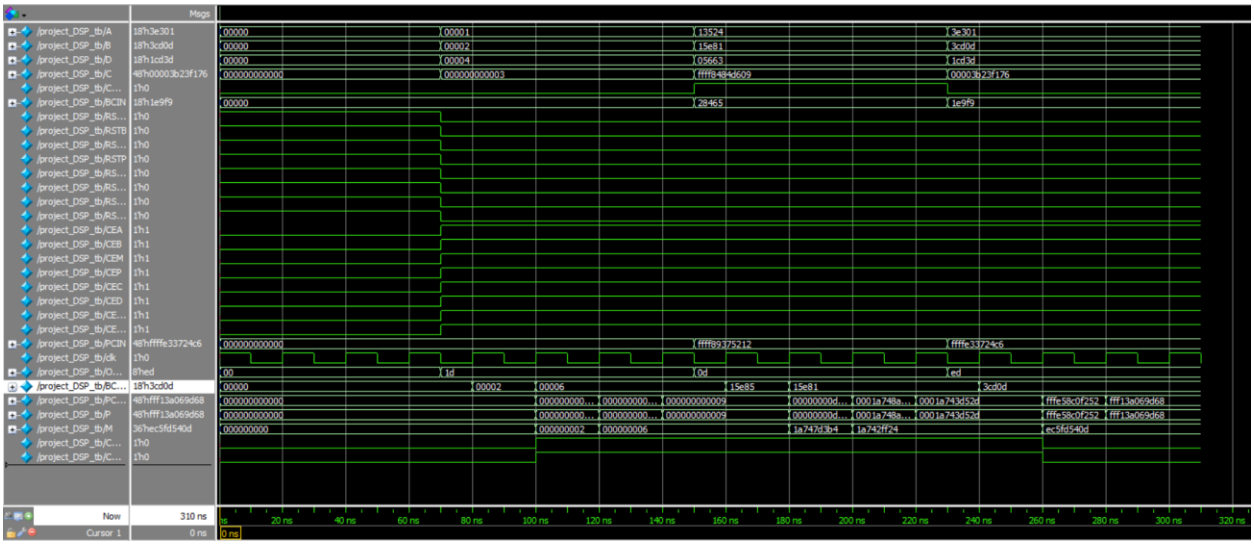
```
    RSTP = 0;RSTA = 0;RSTB = 0;RSTM = 0;RSTP = 0;RSTC = 0;RSTD = 0;RSTCARRYIN = 0;RSTOPMODE = 0;
    CEA = 1;CEB = 1;CEC = 1;CED = 1;CEM = 1;CEP = 1;CEOPMODE = 1;CECARRYIN = 1;
    A =1;
    B =2;
    C =3;
    D =4;
    OPMODE = 8'b0001_1101;
    CARRYIN =0;
    BCIN = 0;
    PCIN =0;
   repeat(4) @(negedge clk);
    A =$random;
    B =$random;
    C =$random;
    D =$random;
    OPMODE = $random;
    CARRYIN =$random;
    BCIN = $random;
    PCIN =$random;
   repeat(4) @(negedge clk);

    A =$random;
    B =$random;
    C =$random;
    D =$random;
    OPMODE = $random;
    CARRYIN =$random;
    BCIN = $random;
    PCIN =$random;
   repeat(4) @(negedge clk);
$stop;
end
initial begin
    $monitor("PCOUT=%d, P=%d, CARRYOUT=%d , CARRYOUTF=%d ,M=%d", PCOUT, P, CARRYOUT,CARRYOUTF , M);
end
endmodule
```

```
# Loading work.reg_to_mux(fast__3)
# Loading work.reg_to_mux(fast__4)
# PCOUT=                0, P=                0, CARRYOUT=0 , CARRYOUTF=0 ,M=           0
# PCOUT=                3, P=                3, CARRYOUT=1 , CARRYOUTF=1 ,M=           2
# PCOUT=                5, P=                5, CARRYOUT=1 , CARRYOUTF=1 ,M=           6
# PCOUT=                9, P=                9, CARRYOUT=1 , CARRYOUTF=1 ,M=           6
# PCOUT=            54799, P=            54799, CARRYOUT=1 , CARRYOUTF=1 ,M= 7101469620
# PCOUT=     7101524413, P=     7101524413, CARRYOUT=1 , CARRYOUTF=1 ,M= 7101153060
# PCOUT=     7101207853, P=     7101207853, CARRYOUT=1 , CARRYOUTF=1 ,M= 7101153060
# PCOUT=281467875816018, P=281467875816018, CARRYOUT=0 , CARRYOUTF=0 ,M=63451255821
# PCOUT=281411525713256, P=281411525713256, CARRYOUT=0 , CARRYOUTF=0 ,M=63451255821
# ** Note: $stop    : project_DSP_tb.v(94)
#    Time: 310 ns  Iteration: 1  Instance: /project_DSP_tb
# Break in Module project_DSP_tb at project_DSP_tb.v line 94
```



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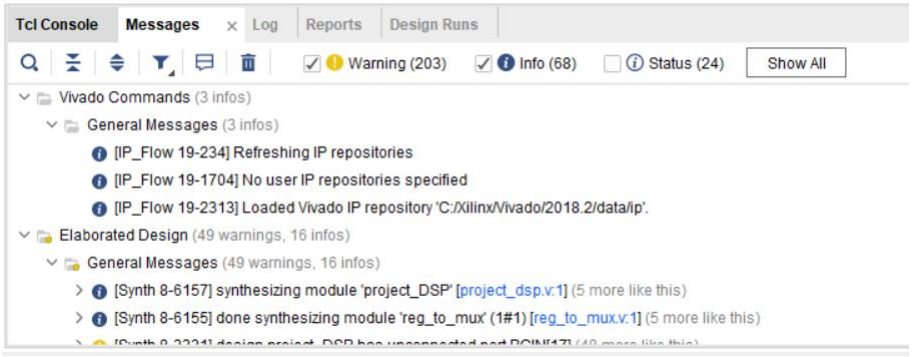
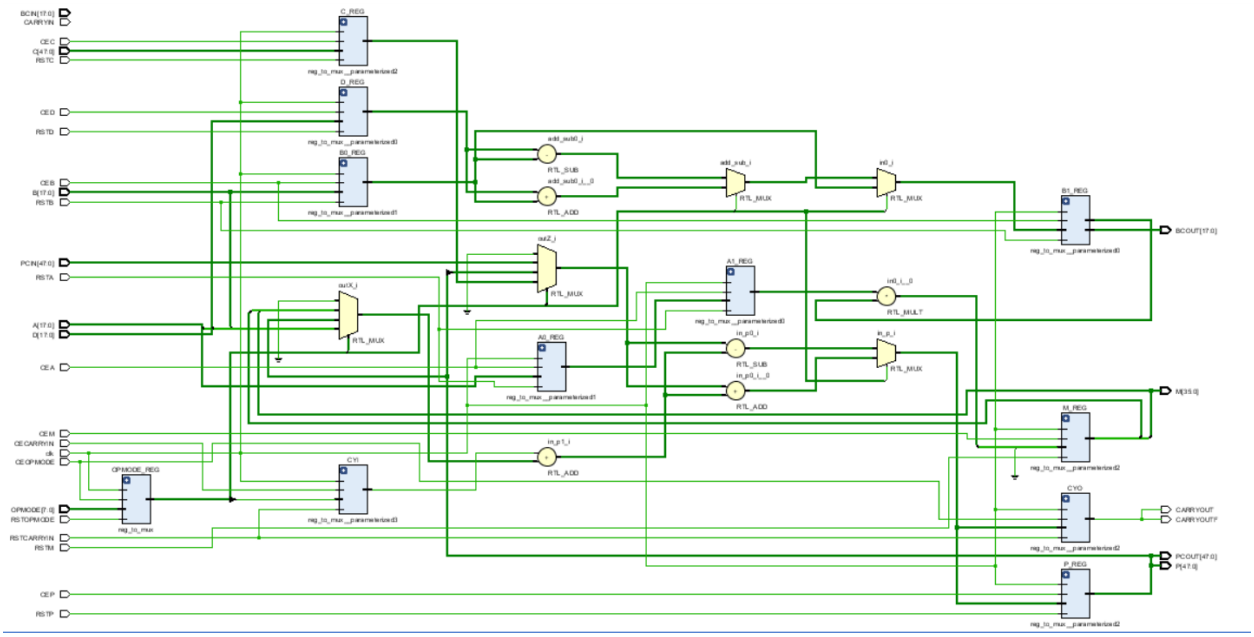
VIVADO:

ELABORATION:





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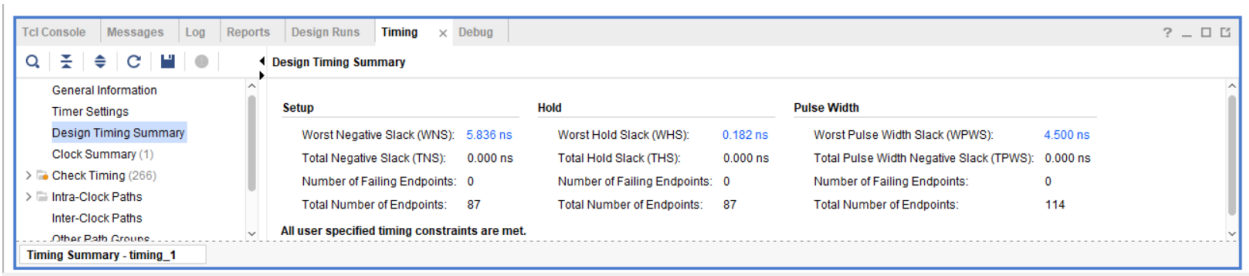
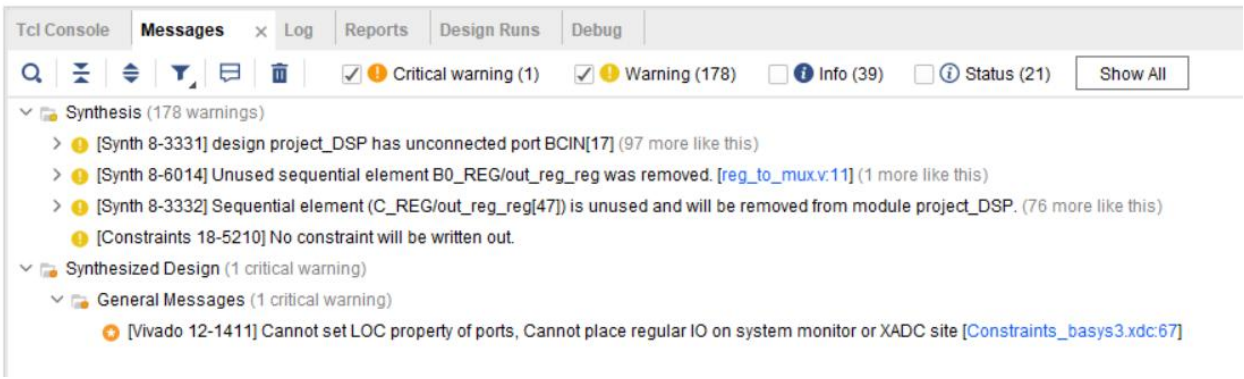
SYNTHESIS:

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
project_DSP	151	112	1	267	1
B1_REG (reg_to_mux...	1	18	0	0	0
C_REG (reg_to_mux_...	0	18	0	0	0
CYI (reg_to_mux__par...	1	1	0	0	0
CYO (reg_to_mux__pa...	0	1	0	0	0
D_REG (reg_to_mux_...	16	18	0	0	0
M_REG (reg_to_mux_...	1	0	1	0	0
OPMODE_REG (reg_t...	132	8	0	0	0
P_REG (reg_to_mux_...	0	48	0	0	0





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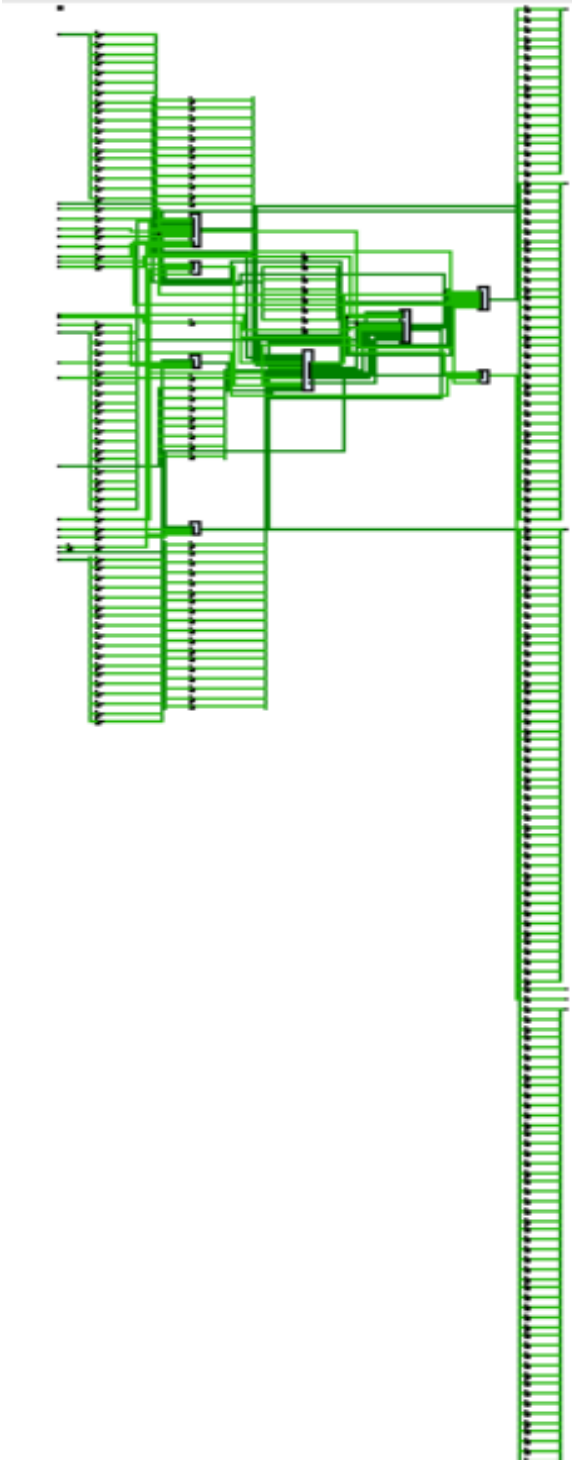

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Implementation:

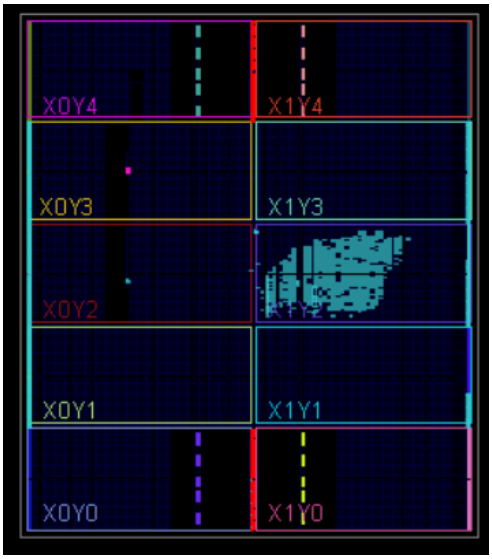
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	28.610 ns	Worst Hold Slack (WHS):	0.083 ns	Worst Pulse Width Slack (WPWS):	15.450 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1036	Total Number of Endpoints:	1028	Total Number of Endpoints:	483

All user specified timing constraints are met.

Hierarchy

Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSPs (740)	Bo
project_DSP	2557	3936	69	3	1276	2137	420	1555	6.5	1	
B1_REG (reg_to_mux...)	1	18	0	0	7	1	0	1	0	0	
C_REG (reg_to_mux_...)	0	18	0	0	6	0	0	0	0	0	
CYI (reg_to_mux__par...)	1	1	0	0	1	1	0	1	0	0	
CYO (reg_to_mux__pa...)	0	1	0	0	1	0	0	0	0	0	
D_REG (reg_to_mux_...)	16	18	0	0	12	16	0	0	0	0	
dbg_hub (dbg_hub)	475	727	0	0	241	451	24	311	0	0	
M_REG (reg_to_mux_...)	0	0	0	0	0	0	0	0	0	1	
OPMODE_REG (reg_t...)	132	8	0	0	40	132	0	0	0	0	
P_REG (reg_to_mux_...)	0	48	0	0	12	0	0	0	0	0	
u_ila_0 (u_ila_0)	1932	3097	69	3	997	1536	396	1186	6.5	0	



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Constraint File:

```
## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]


##Buttons
set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports RSTP]
#set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports btnU]
```

```
create_debug_core u_ila_0 ila
set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
set_property port_width 1 [get_debug_ports u_ila_0/clk]
connect_debug_port u_ila_0/clk [get_nets [list clk_IBUF_BUFG]]
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
set_property port_width 8 [get_debug_ports u_ila_0/probe0]
connect_debug_port u_ila_0/probe0 [get_nets [list {OPMODE_IBUF[0]} {OPMODE_IBUF[1]} {OPMODE_IBUF[2]} {OPMODE_IBUF[3]} {OPMODE_IBUF[4]} {OPMODE_IBUF[5]} {OPMODE_IBUF[6]} {OPMODE_IBUF[7
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
set_property port_width 18 [get_debug_ports u_ila_0/probe1]
connect_debug_port u_ila_0/probe1 [get_nets [list {C_IBUF[0]} {C_IBUF[1]} {C_IBUF[2]} {C_IBUF[3]} {C_IBUF[4]} {C_IBUF[5]} {C_IBUF[6]} {C_IBUF[7]} {C_IBUF[8]} {C_IBUF[9]} {C_IBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
set_property port_width 18 [get_debug_ports u_ila_0/probe2]
connect_debug_port u_ila_0/probe2 [get_nets [list {PCIN_IBUF[0]} {PCIN_IBUF[1]} {PCIN_IBUF[2]} {PCIN_IBUF[3]} {PCIN_IBUF[4]} {PCIN_IBUF[5]} {PCIN_IBUF[6]} {PCIN_IBUF[7]} {PCIN_IBUF[8]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
set_property port_width 18 [get_debug_ports u_ila_0/probe3]
connect_debug_port u_ila_0/probe3 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]} {A_IBUF[3]} {A_IBUF[4]} {A_IBUF[5]} {A_IBUF[6]} {A_IBUF[7]} {A_IBUF[8]} {A_IBUF[9]} {A_IBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 18 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list {D_IBUF[0]} {D_IBUF[1]} {D_IBUF[2]} {D_IBUF[3]} {D_IBUF[4]} {D_IBUF[5]} {D_IBUF[6]} {D_IBUF[7]} {D_IBUF[8]} {D_IBUF[9]} {D_IBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
set_property port_width 18 [get_debug_ports u_ila_0/probe5]
connect_debug_port u_ila_0/probe5 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]} {B_IBUF[3]} {B_IBUF[4]} {B_IBUF[5]} {B_IBUF[6]} {B_IBUF[7]} {B_IBUF[8]} {B_IBUF[9]} {B_IBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
set_property port_width 18 [get_debug_ports u_ila_0/probe6]
connect_debug_port u_ila_0/probe6 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]} {BCOUT_OBUF[2]} {BCOUT_OBUF[3]} {BCOUT_OBUF[4]} {BCOUT_OBUF[5]} {BCOUT_OBUF[6]} {BCOUT_OBUF[7]} {BCOU
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe7]
set_property port_width 36 [get_debug_ports u_ila_0/probe7]
connect_debug_port u_ila_0/probe7 [get_nets [list {M_OBUF[0]} {M_OBUF[1]} {M_OBUF[2]} {M_OBUF[3]} {M_OBUF[4]} {M_OBUF[5]} {M_OBUF[6]} {M_OBUF[7]} {M_OBUF[8]} {M_OBUF[9]} {M_OBUF[10]}
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe8]
set_property port_width 48 [get_debug_ports u_ila_0/probe8]
```

```
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
set_property port_width 1 [get_debug_ports u_ila_0/probe9]
connect_debug_port u_ila_0/probe9 [get_nets [list CARRYOUTF_OBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe10]
set_property port_width 1 [get_debug_ports u_ila_0/probe10]
connect_debug_port u_ila_0/probe10 [get_nets [list CEA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
set_property port_width 1 [get_debug_ports u_ila_0/probe11]
connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
set_property port_width 1 [get_debug_ports u_ila_0/probe12]
connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
set_property port_width 1 [get_debug_ports u_ila_0/probe13]
connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
set_property port_width 1 [get_debug_ports u_ila_0/probe14]
connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
set_property port_width 1 [get_debug_ports u_ila_0/probe15]
connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
```