Molla Shanawaz Baig

Roll No.:252VL022
Electronics and Communication Engineering
VLSI Design
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Education

•Master of Technology, VLSI Design *2027*
National Institute Of Technology, Karnataka (NITK)

•Bachelor of Technology, Electronics and Communication Engineering *2024*
Sri Venkateswara University College of Engineering, Tirupati CGPA: 6.87

•Intermediate (MPC) *2020*
Narayana Junior College, Kurnool CGPA: 9.75

Projects

•Asynchronous FIFO Design (Verilog HDL) *Hardware Design Project | FPGA and VLSI Design*

- Designed and implemented an **asynchronous FIFO** using Verilog HDL to enable reliable data transfer between two clock domains.
- Utilized **Gray-coded pointers** and **two-flip-flop synchronizers** for metastability mitigation and accurate full/empty flag detection.
- Developed separate modules for *write*, *read*, *synchronization*, and *dual-port memory* blocks.
- Verified functionality through simulation in **ModelSim** and synthesized using **Intel Quartus Prime** targeting the **DE10 FPGA board**.
- Gained in-depth understanding of **clock domain crossing (CDC)**, **FIFO architecture**, and **low-level hardware synchronization**.

•Motion Estimation of Multiple Vehicles Using Machine Learning
B.Tech Final Year Project on real-time vehicle tracking using YOLOv8 and Deep SORT.

- Developed a real-time vehicle detection and tracking system using YOLOv8 and Deep SORT.
- Implemented speed estimation using OpenCV, Python, and NumPy.
- Addressed occlusion, lighting variations, and multiple vehicle types.
- Showcased applications in smart traffic monitoring and accident prevention.

•College Web App
Full Stack web application for college built using React and Firebase.

- Built a responsive college web app using React and Firebase.
- Enhanced UI using Bootstrap and Materialize CSS.
- Managed backend data flow via Firebase.
- **Repo:** GitHub Link

Technical Skills

Languages:

- Verilog
- Javascript
- Python
- C

SKills and Tools :

- RTL Design
- Static Timing Analysis
- Cadence Virtuoso , LTspice
- Quartus Prime, Xilinx Vivado
- VS code,Git

ACHIEVEMENTS AND EXTRA-CURRICULAR

- Currently serving as the Internship Coordinator for MTech VLSI
- Achieved **first place** in a college-level hackathon competition.
- Leaded Technical Operations team in College Technical fest