ECE3002 (VLSI SYSTEM DESIGN)

LAB TASK 2 – FULL ADDER

AIM

Simulate the full adder carry and sum using CMOS logic and find the rise time and fall time of the respective outputs using Cadence.

THEORY

The truth table of full adder is as given below

A	B	Cin	Cout	(Cout)'	Sum
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	1	0	1

From the above truth table, we obtain:

$$C_{out} = A.B + (A + B).C$$

$$Sum = (C_{out})'.(A + B + C) + A.B.C$$

Now we first simulate the Carry (C_{out}) and then we use that to obtain the Sum.

Circuit Design

The given width ratio of PMOS to NMOS is 3:1. Based on given specifications, we proceed with the transistor designing.

1. Cout

PMOS: => R = 3 (R / K) x 2

- ⇨ K = 6
- ⇨ **$W_p = 6\ W_n$**

Also, for (A + B).C:

- ⇨ W_p (C) = 6 W_n (C)
- ⇨ K (A or B) = 2 x 6 = 12
- ⇨ **$W_p = 12\ W_n$**

NMOS: => R = (R / K) x 2

- ⇨ K = 2
- ⇨ **$W_p = 2\ W_n$**

2. Sum

PMOS: => R = (3 R / K) x 2

- ⇨ K = 6
- ⇨ **$W_p = 6\ W_n$ (When the path ABC is considered in pull-up network)**

Also, for (A+B+C)

- ⇨ K = 3 x 6 = 18
- ⇨ W_p = 18 W_n
- ⇨ **Wp (C_{out}') = 6 W_n (C_{out}')**

NMOS: => For C_{out}' R = 2 (R/ K)

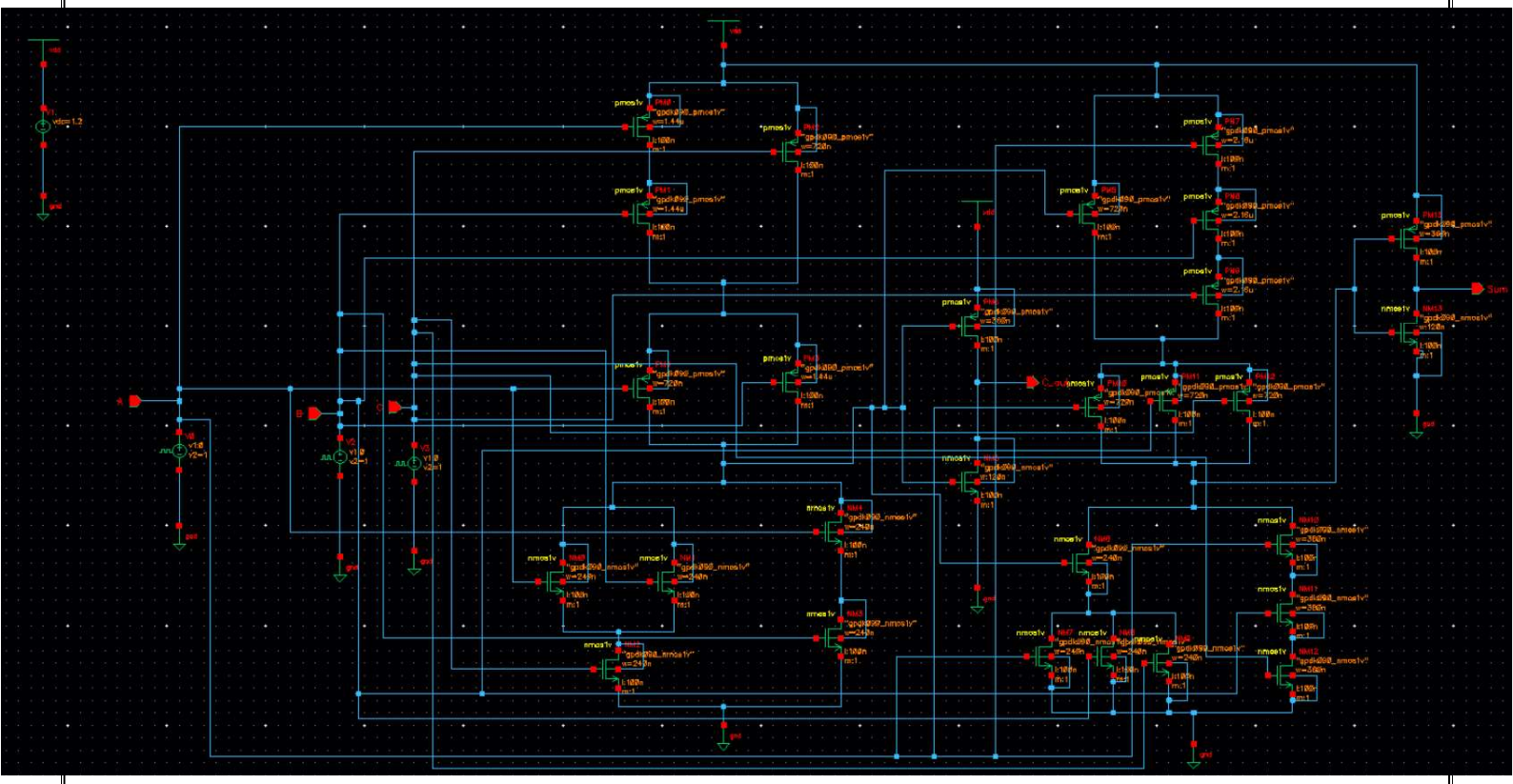
- ⇨ W_p = 2 W_n

Also, for ABC => R = 3 (R / K)

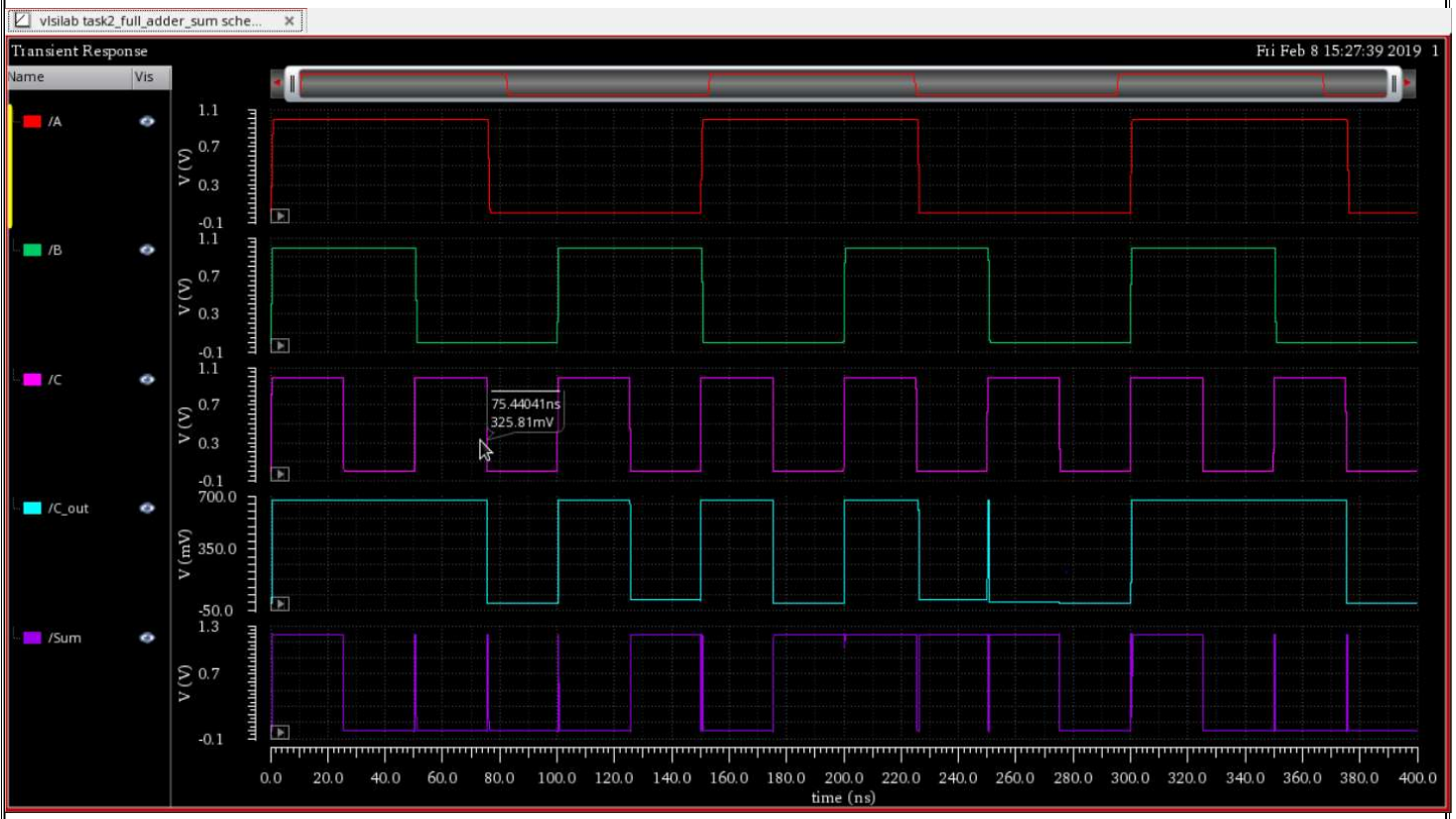
- ⇨ **$W_p = 3\ W_n$**

First, we simulate the C_{out} and then we use the output from C_{out} to compute the final sum. We give the time period for the inputs A, B and C as 150 ns, 100 ns, and 50 ns.

Simulating both in Cadence we obtain the following circuits:



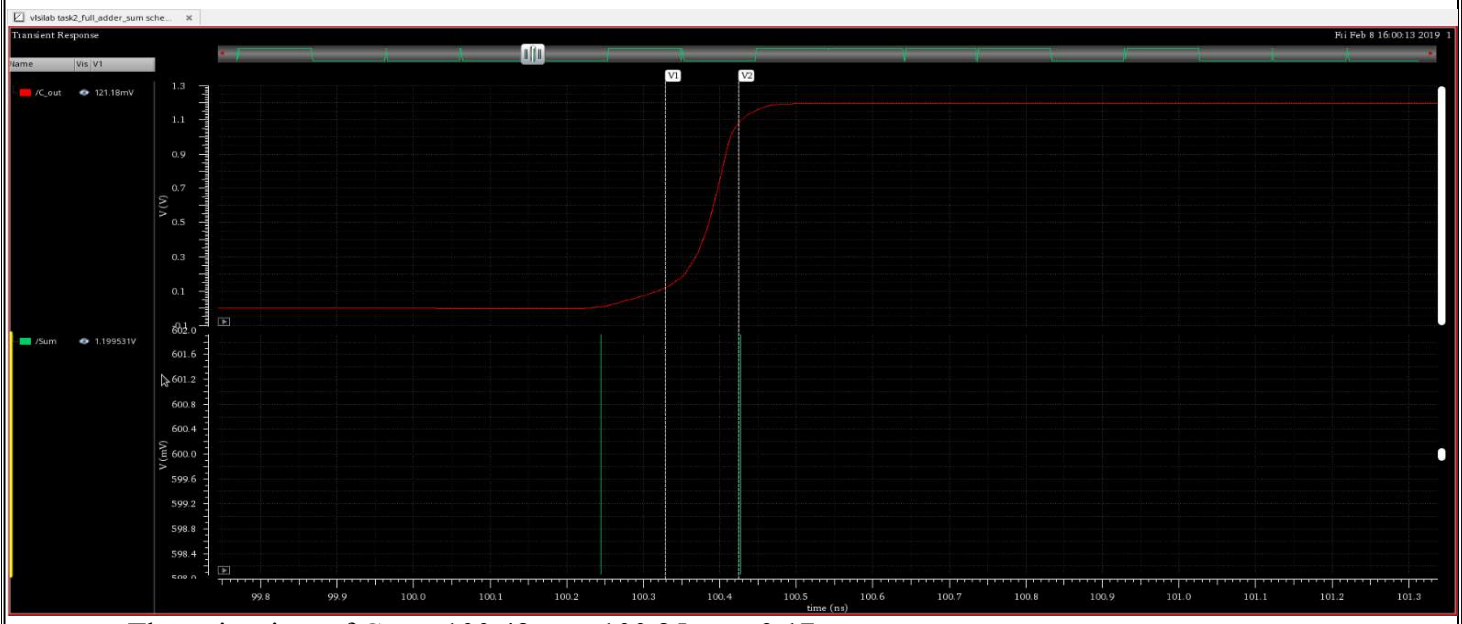
This yields the following outputs as shown in the next page.



Rise Time and Fall Time

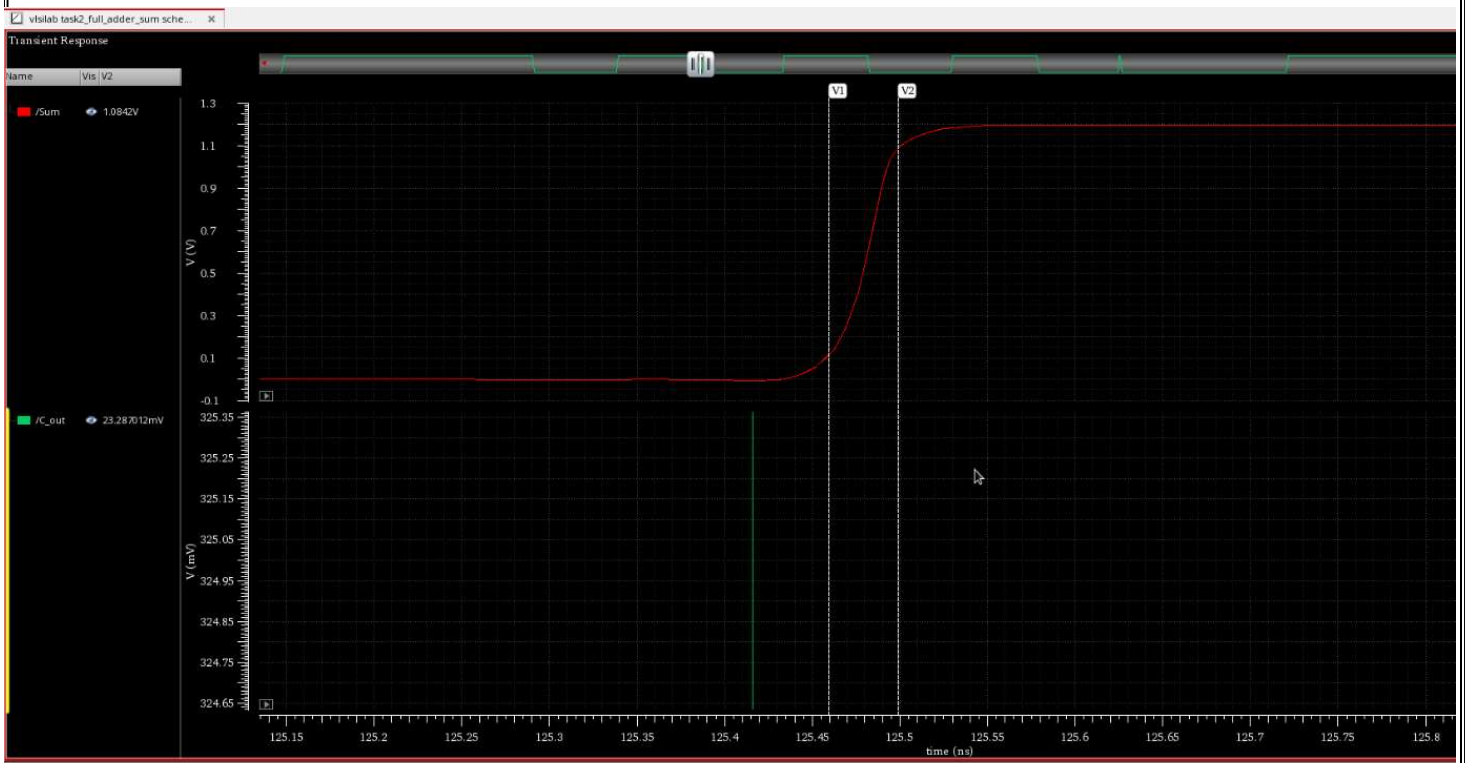
The peak value of output voltages is 1.2V and the minimum voltages is 0V.

90 % of peak = 1.08 V
10 % of peak = 0.12 V



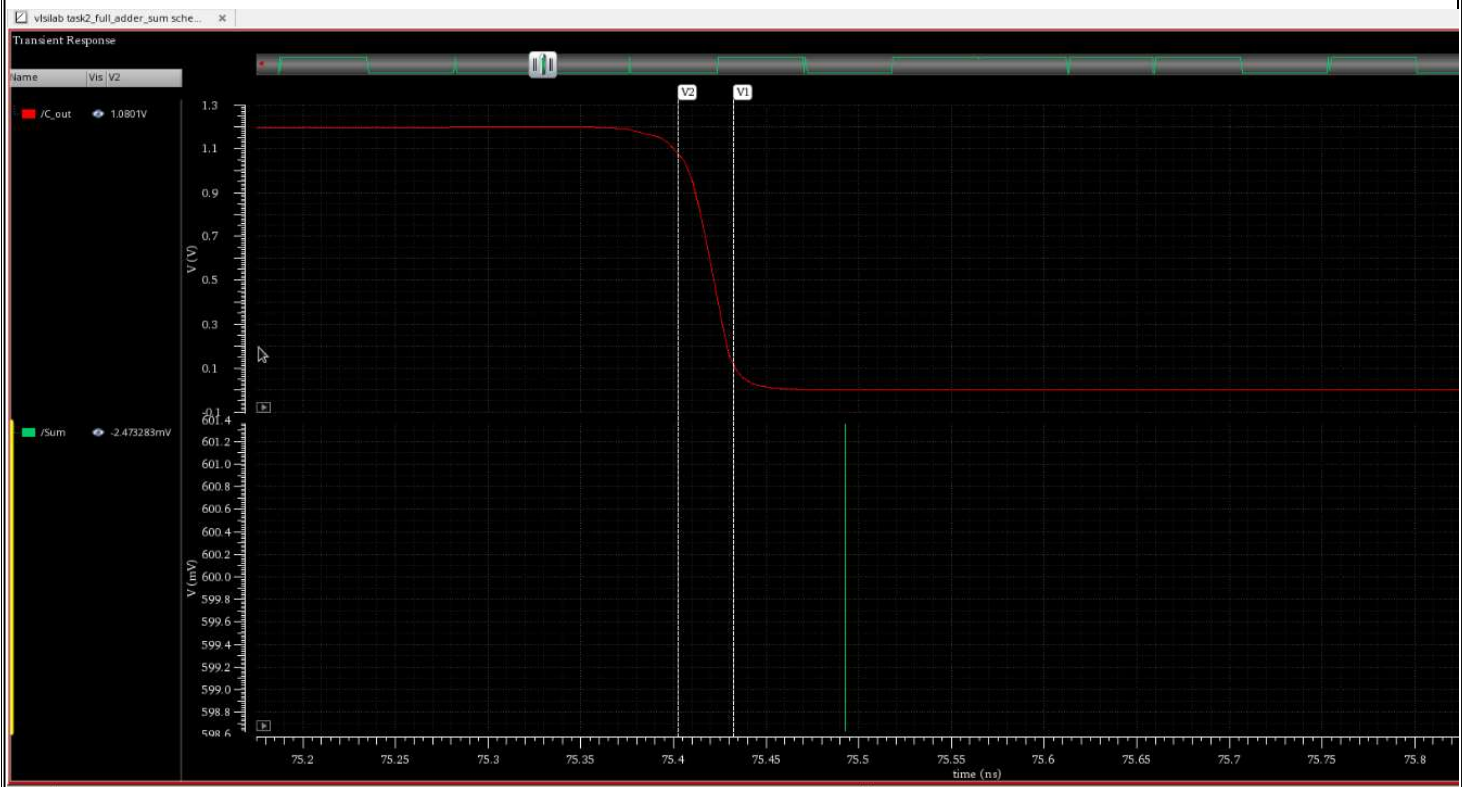
Thus, rise time of C_{out} = 100.42 ns – 100.25 ns = **0.17 ns**

Similarly, the rise time of Sum is calculated from the graph of sum output given below.



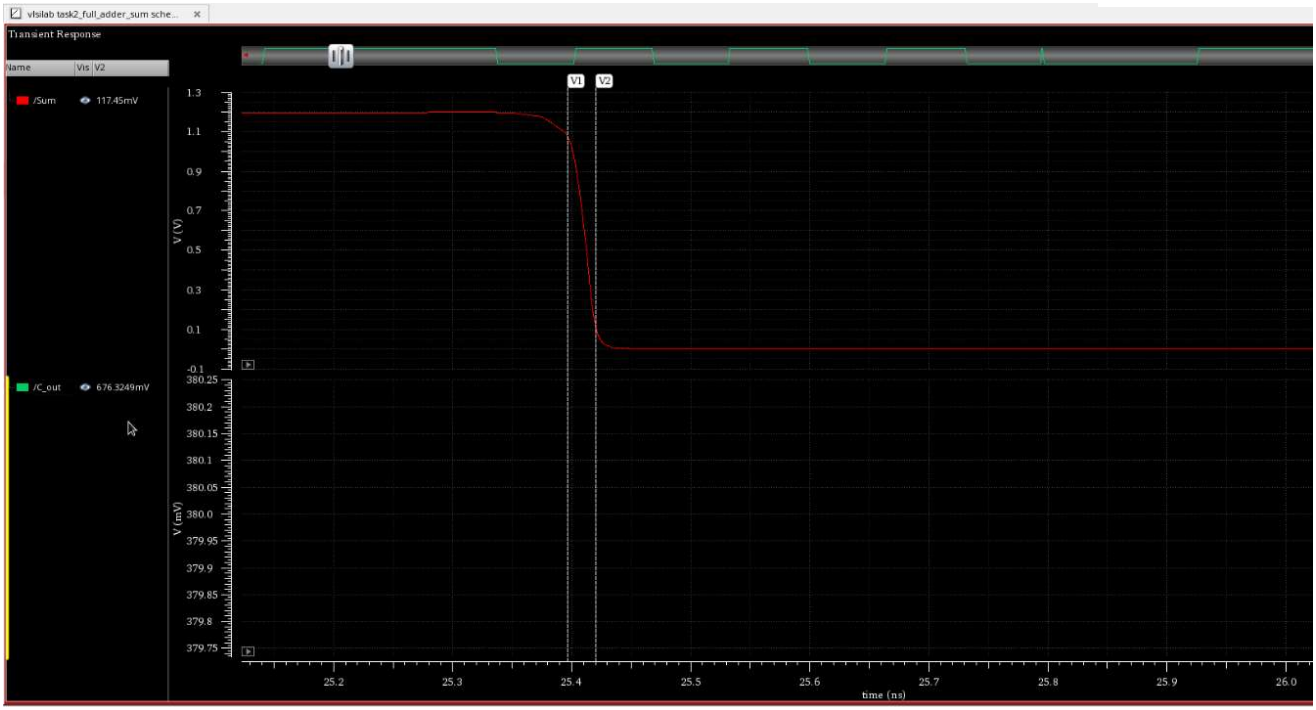
Rise time of sum = 125.5 ns – 125.452 ns = **0.048 ns**

Fall time of C_{out}:



Fall time = 75.46 ns – 75.41 ns = **0.05 ns**

Fall time of Sum = 25.41 ns – 25. 39 ns = **0.02 ns**



RESULT:

The required Full Adder has been designed using CMOS logic.

a) C_{out}:
   (i) Rise time = 0.048 ns
   (ii) Fall time = 0.05 ns

b) Sum:
   (i) Rise time = 0.017 ns
   (ii) Fall time = 0.02 ns