VLSI SYSTEM DESIGN (ECE3002)

LAB TASK 3

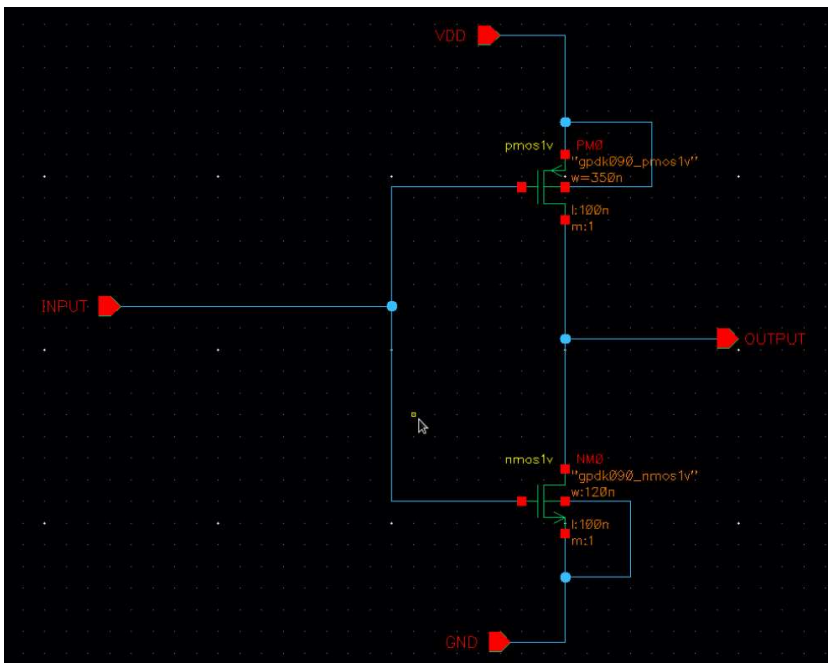
Question:

Create the Symbol and simulate the following circuits

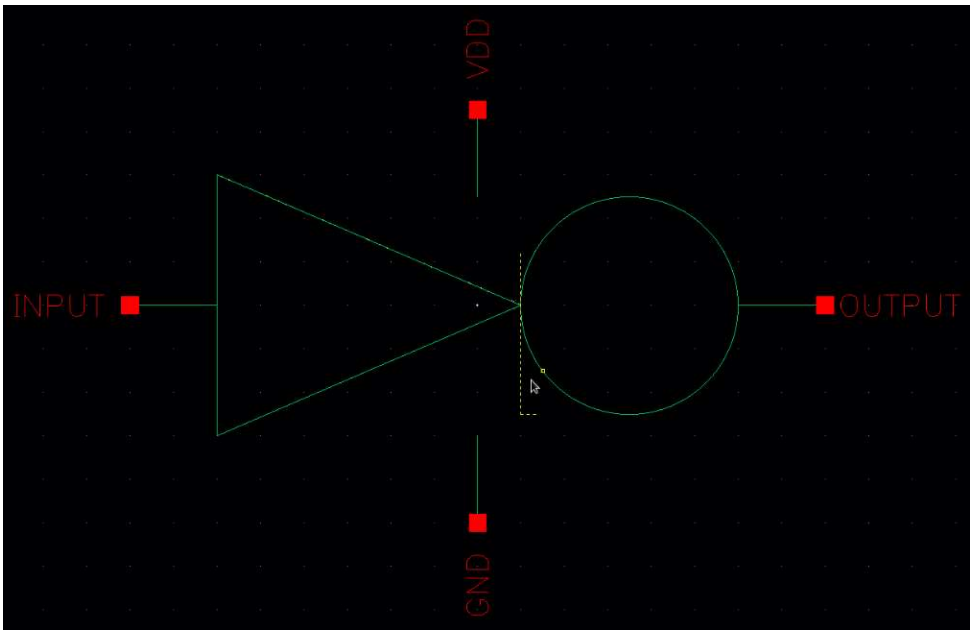
1. **Inverter**

For any given logical circuit, the steps to follow are as follows:

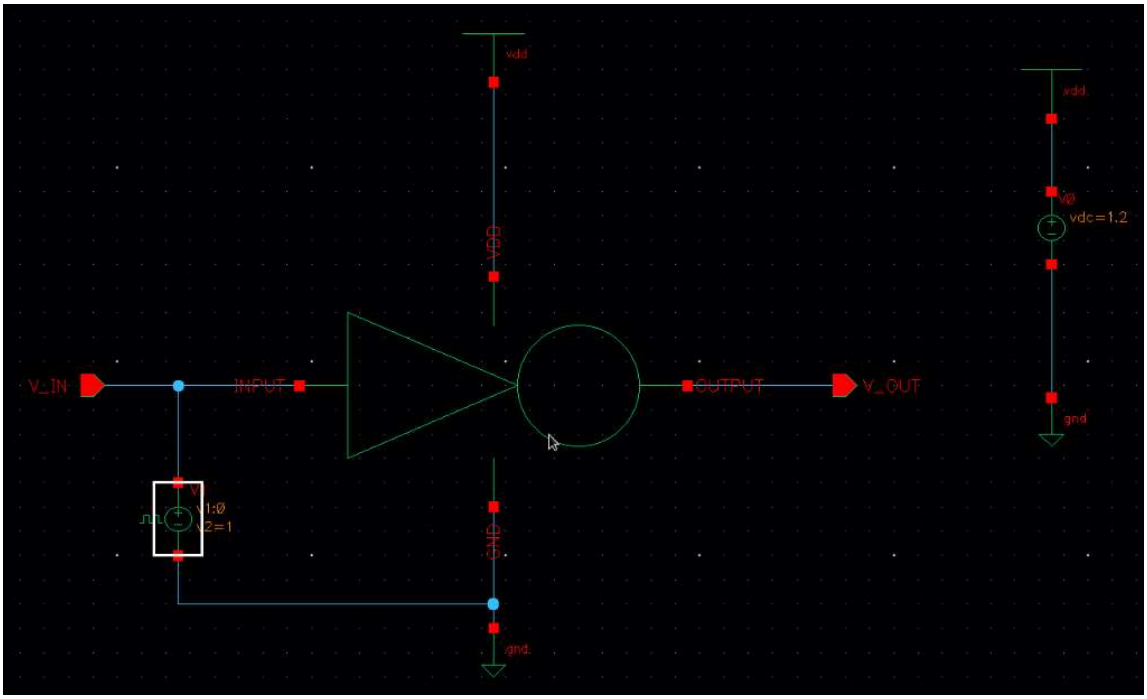
a) Create the Schematic of the logical circuit, without the sources (Like V_{dd}, DC Source, Ground, Pulse Input), and mark the points of connection of V_{dd}, ground and input(s), with their respective pins.



b) Now go to Create -> Cell view -> From Cell View. Inside the dialog box that pops up, give the required details of pin locations on the symbol being created.



c) Verify the symbol by simulating it in a new cell view with the required source symbols and ground symbol and observe the output plotted graphically using Transient Analysis.



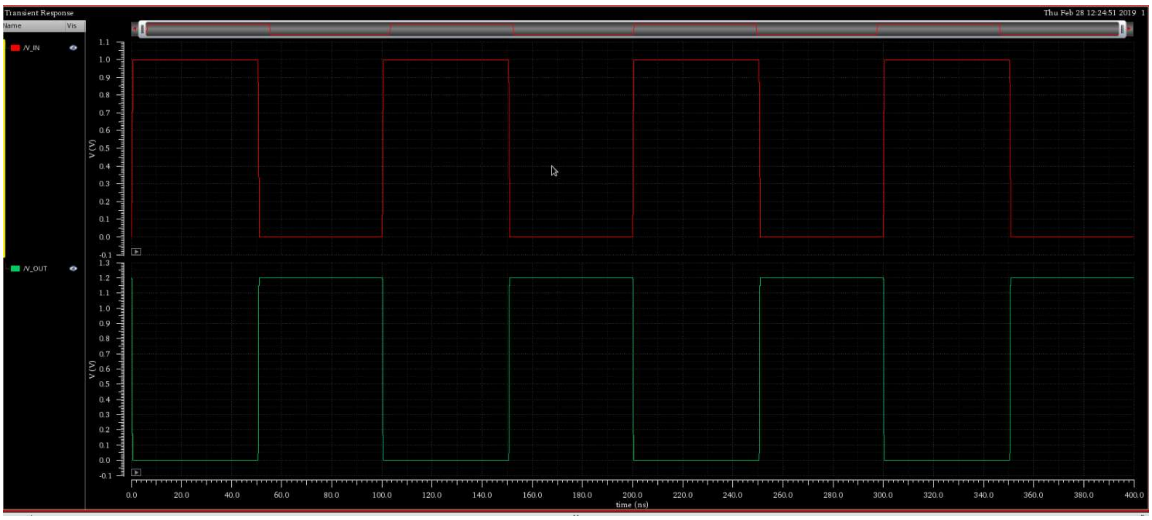


Fig.: Output of symbol verification (Red=input;Green=output)

2. NAND and NOR (2 inputs)

a) NAND

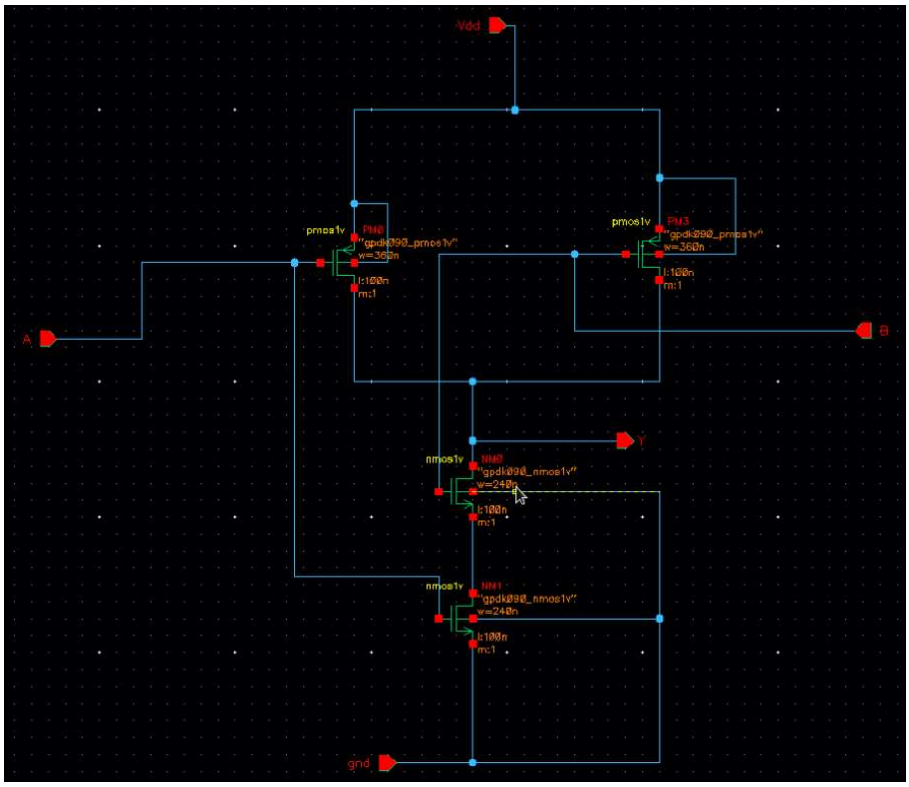
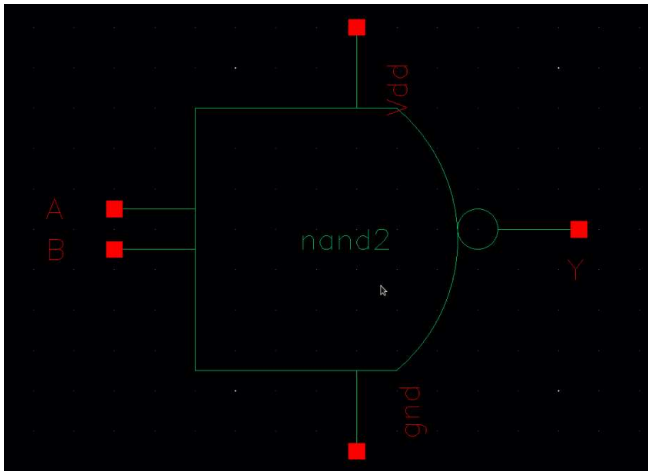
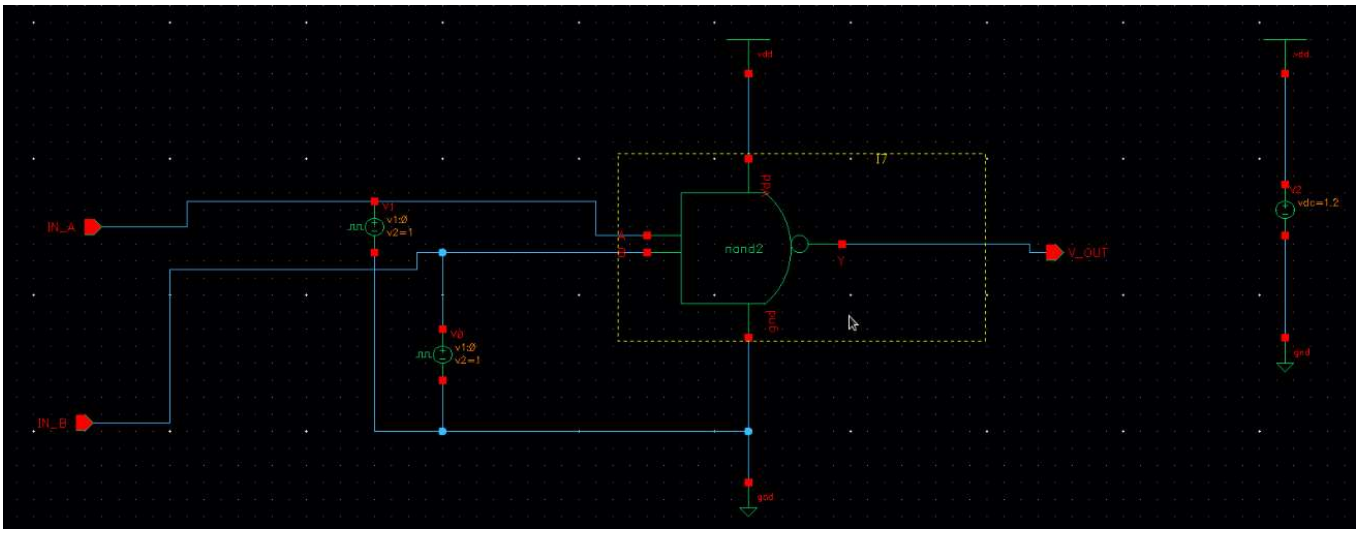


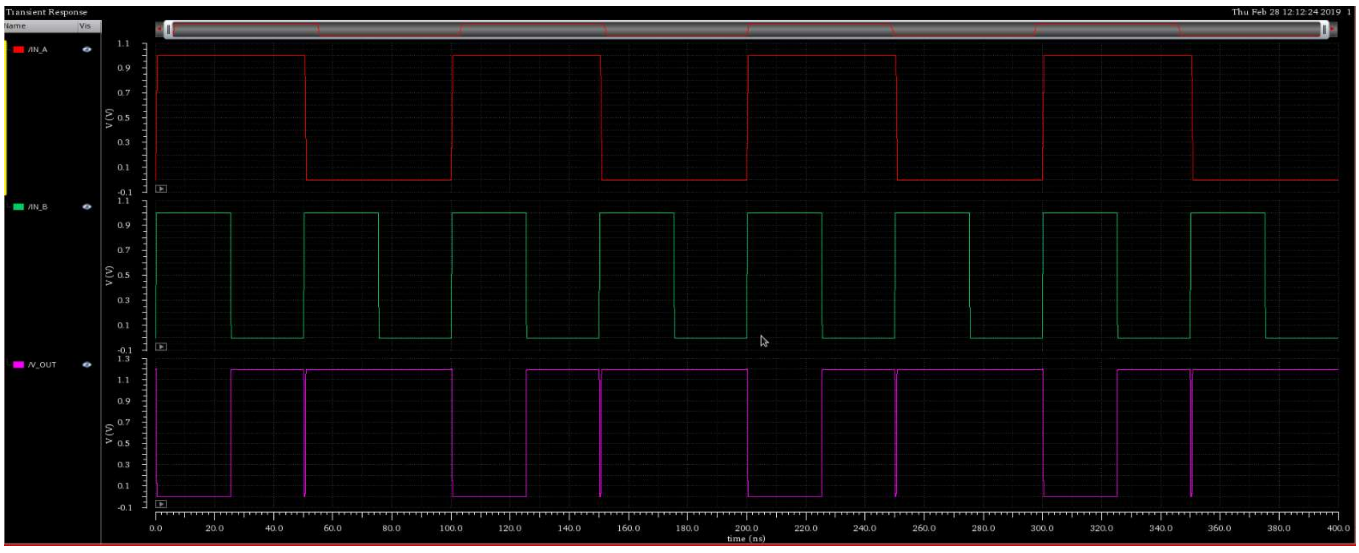
Fig.: NAND Schematic with no sources

The resultant symbol obtained through the schematic is:



The test cellview of the NAND symbol and the obtained output are shown below. In the output, RED and GREEN are INPUTS, and VIOLET is OUTPUT.





Hence the truth table of NAND is verified as:

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

b) NOR

The procedure to construct the symbol for NOR (2 inputs) remains the same.

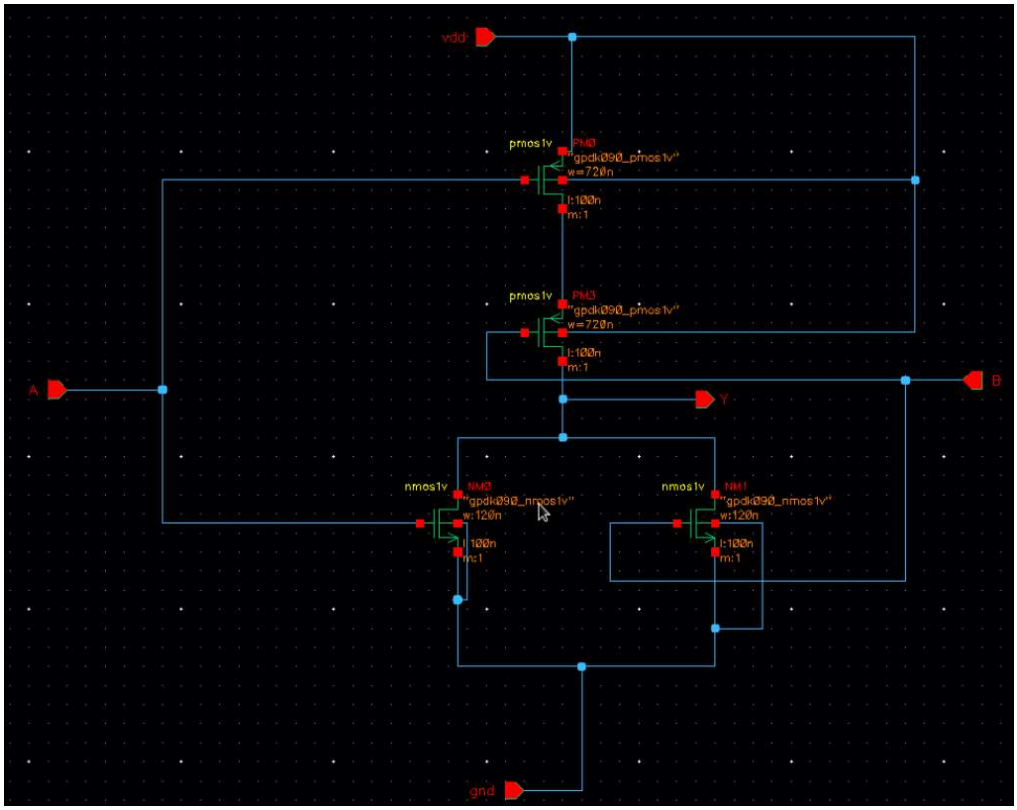


Fig.: NOR Schematic with no sources

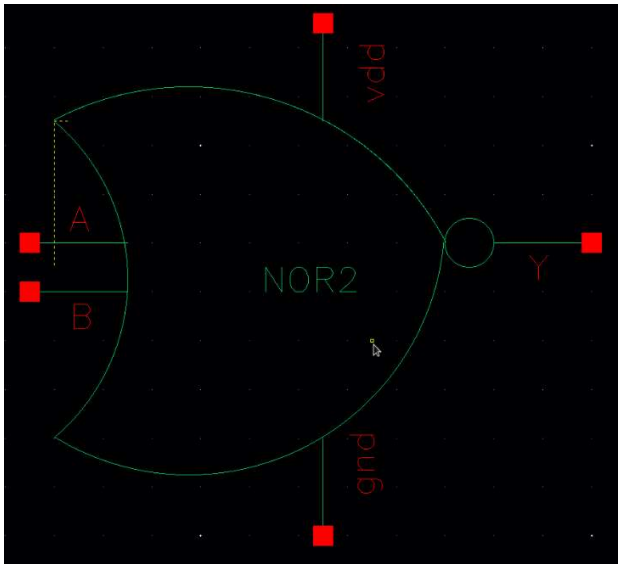


Fig.: NOR Symbol

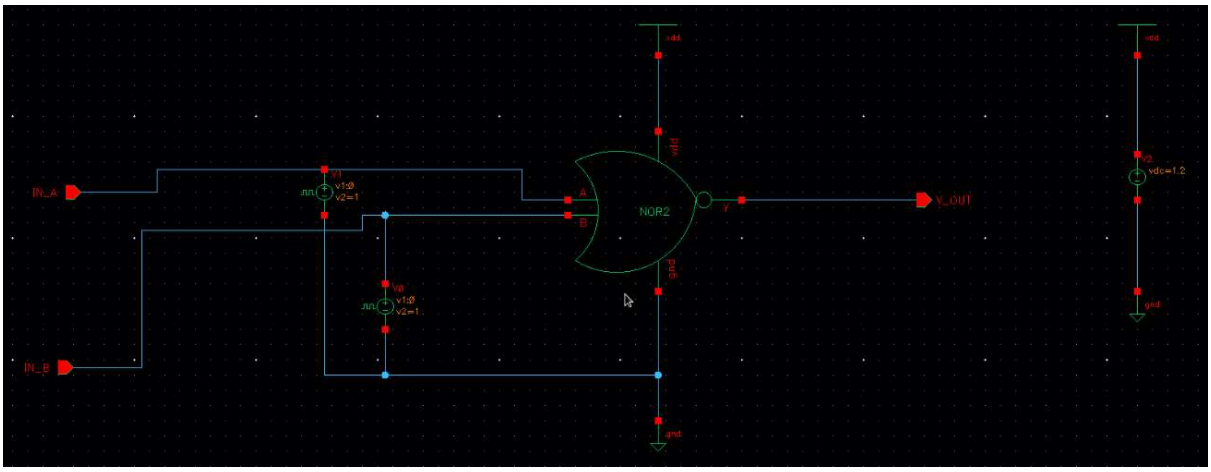


Fig.: NOR symbol testing cellview

Fig.: Output of the test cellview
(RED,GREEN=INPUT;VIOLET=OUTPUT)

The truth table for above circuit is verified as:

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

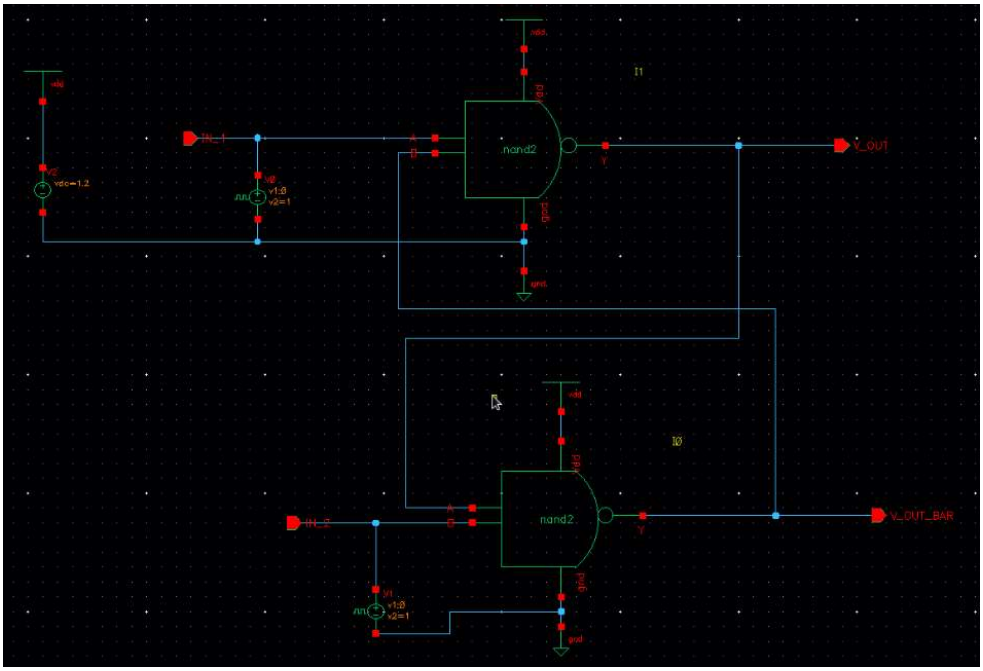
3. RS Latch using designed NAND and NOR

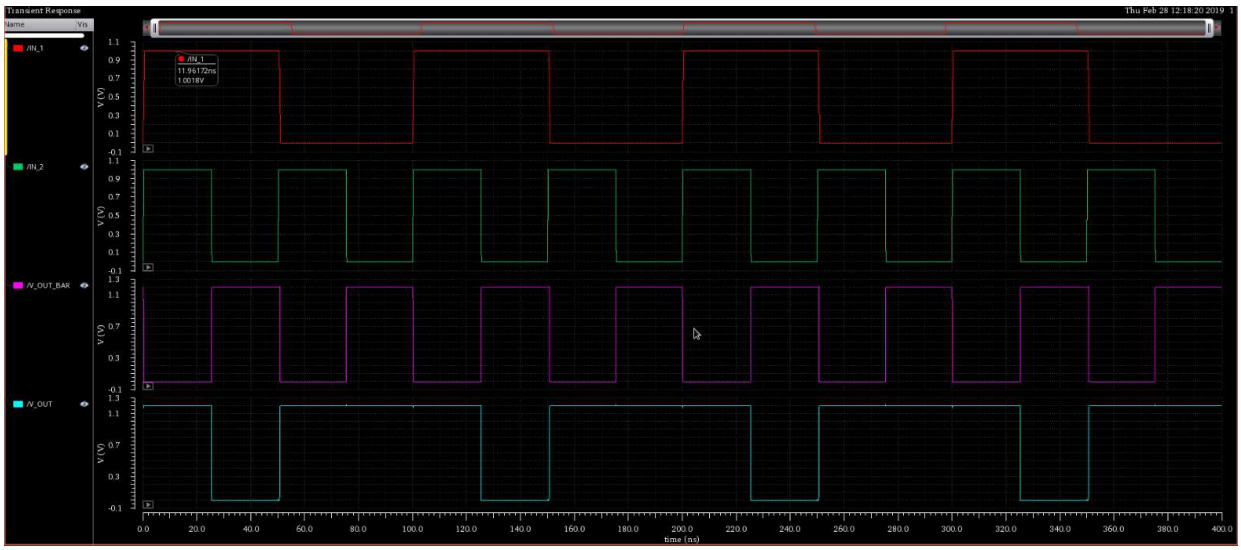
a) Using NAND:

RS Latch is built using NAND gates with the input S' and R' where S stands for SET, and R stands for RESET. The truth table for the RS Latch is as given below.

S	R	S'	R	Q	Q'
0	0	1	1	1	0
0	1	1	0	0	1
1	0	0	1	1	0
1	1	0	0	1	1

Using the predesigned NAND symbols, the testing cellview for the RS Latch is built as shown below. Here, IN_A is S', IN_B is R', V_OUT is Q and V_OUT_BAR is Q'.



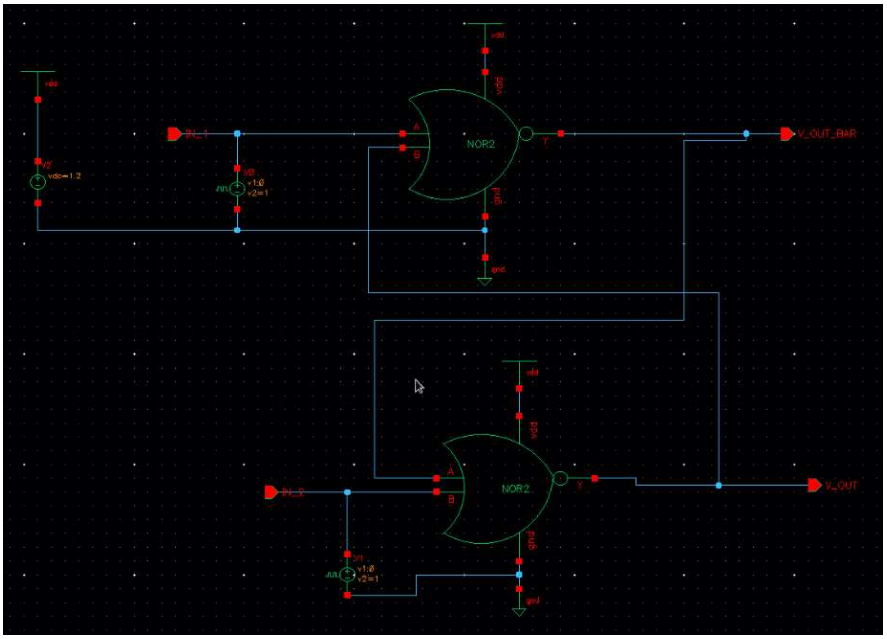


From above table and graphical output, we can see that when the inputs (S', R') are 11 the output remains the previous state. This is because the output of NAND i9s dependant on 0. If there is at least 1 0 as input the NAND then the output will be 1.
Hence, when R' is 0, Q' becomes 1 which is the reset state (as R is 1, S=0).
Also, when S' is 0, Q becomes 1 which is the set state (as S=1, R=0)
But when input is S'=0 and R'=0, both the outputs become 1, which is the unstable state as the outputs are complementary.

Hence, since all cases are correct the circuit is verified.

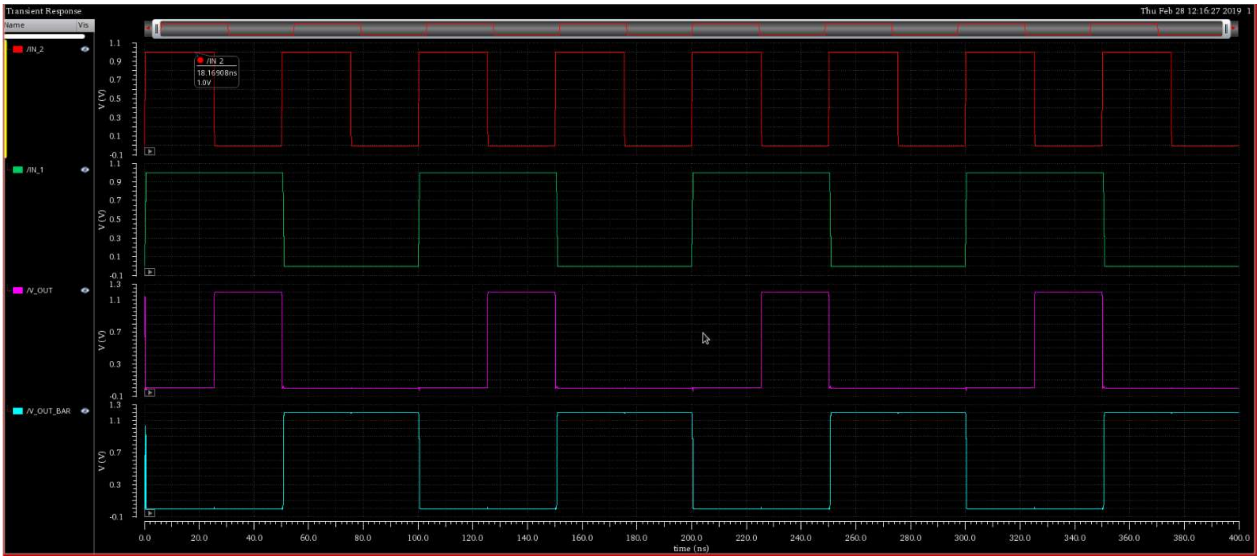
b) Using NOR

Using NOR, the circuit is built as shown below.



Here, IN_A is S, IN_B is R, V_OUT_BAR is Q, and V_OUT is Q'.

The graphical output of the transient analysis is:



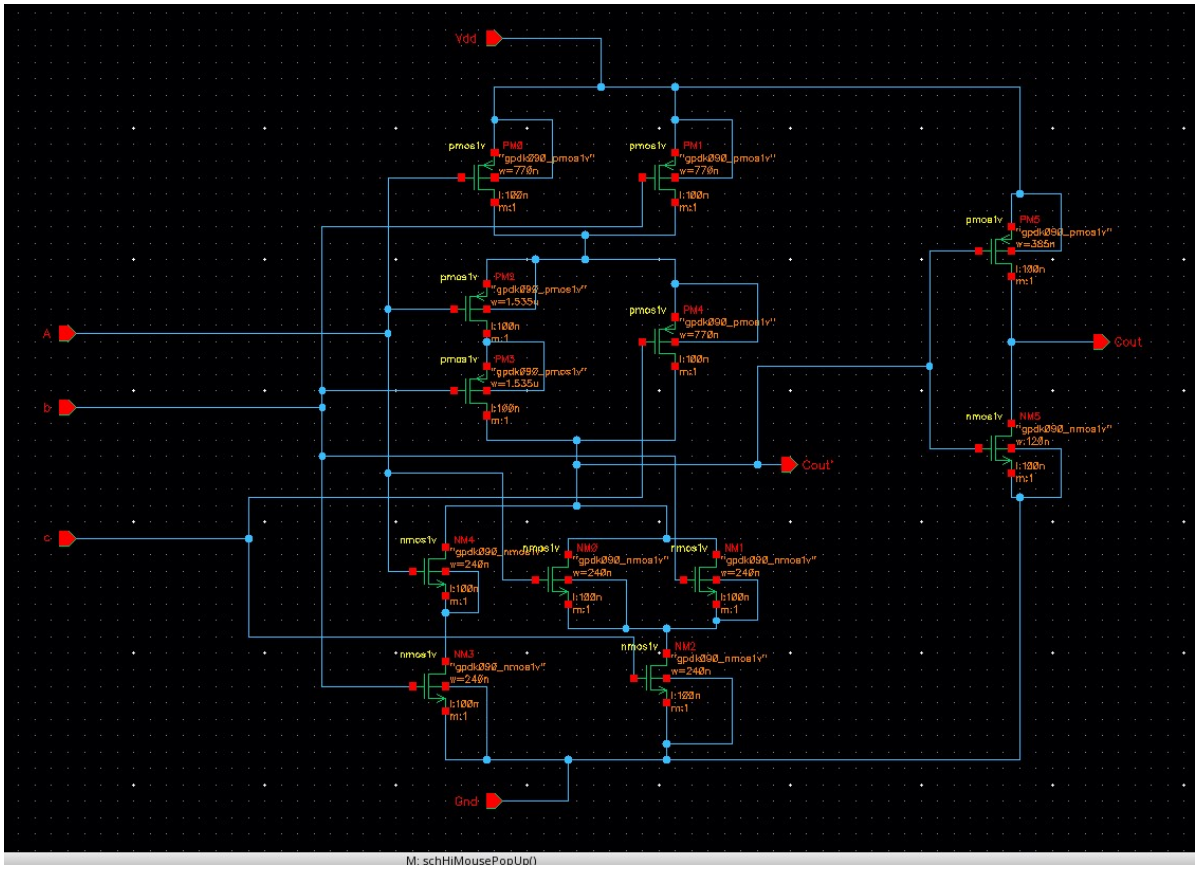
Comparing the truth table and the transient analysis output, we can conclude that the circuit's functionality has been verified.

S	R	Q	Q'
0	0	1	0
0	1	1	0
1	0	0	1
1	1	0	0

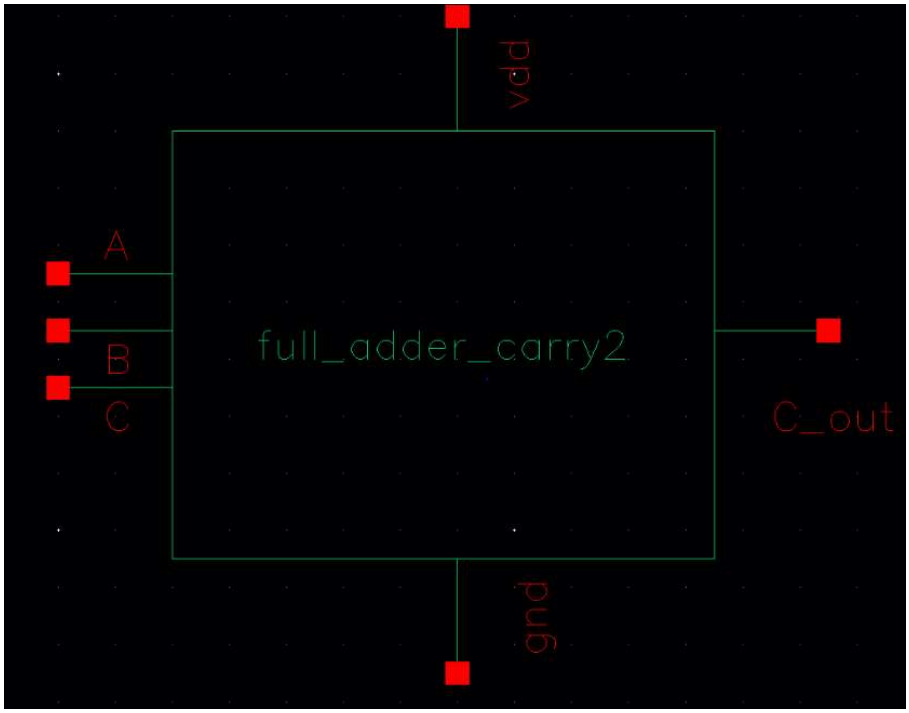
4. Full adder Carry circuit

Here, we create the schematic of Full adder carry.
$C_{out} = (A + B) \times C_{in} + A\,B$

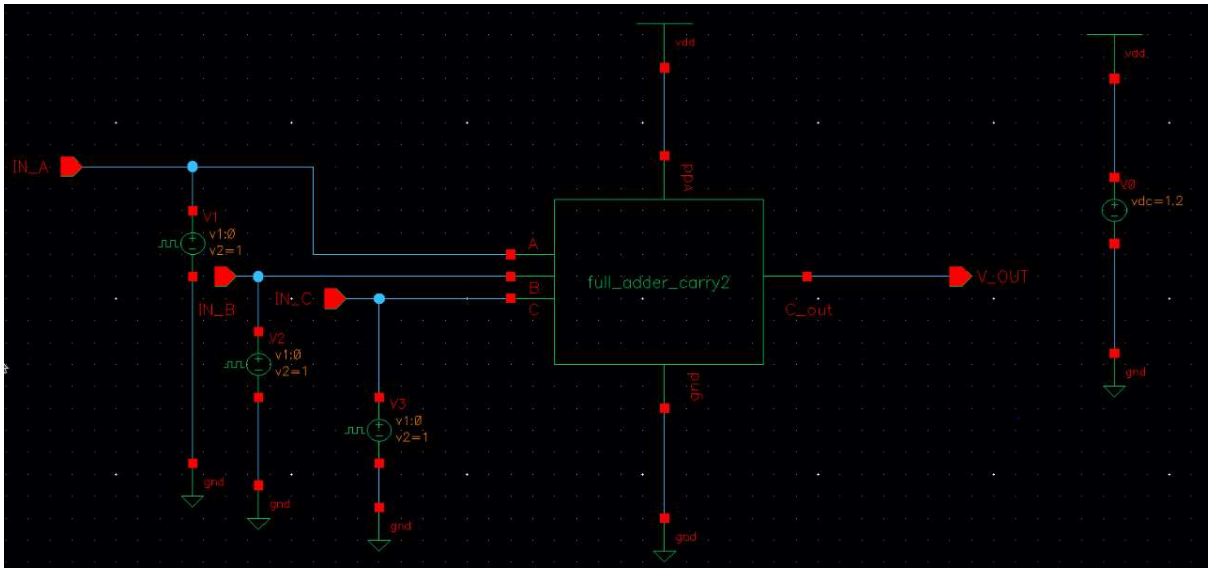
Making the circuit and then removing sources and replacing then with appropriate pins gives us the following circuit.



Now the created symbol is as given below.

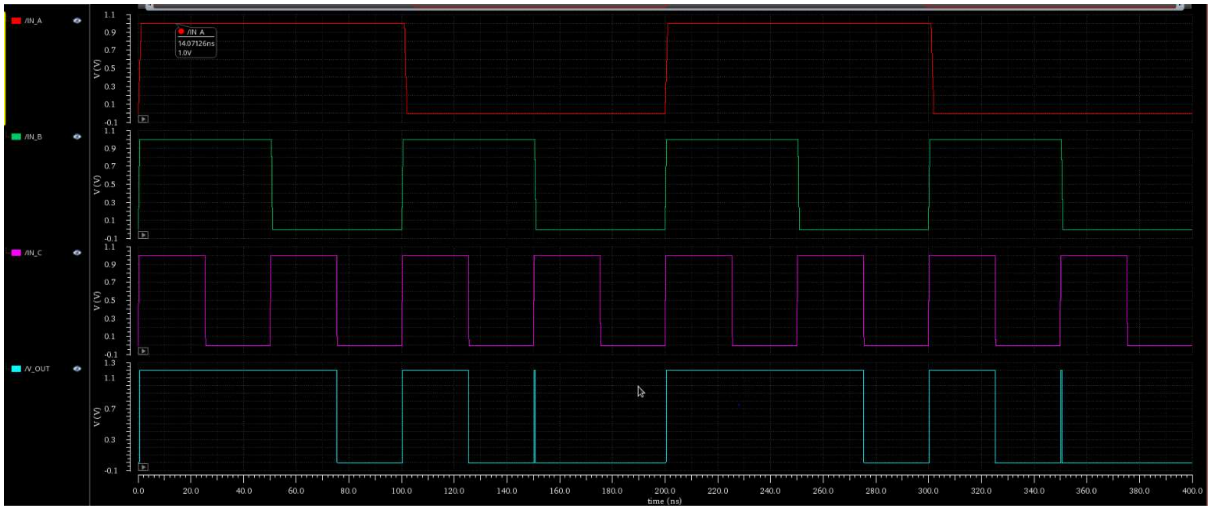


The symbol is tested using the following circuit.



Then output is C_{out}, while the inputs are A, B and C.

Simulating this gives the following output:



Truth Table:

A	B	C	C_{out}
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

This is the same as that of Full Adder carry. Hence, the circuit is verified.