VLSI SYSTEM DESIGN (ECE3002)

LAB TASK – I

PMOS DC AND PARAMETRIC ANALYSIS

Question:

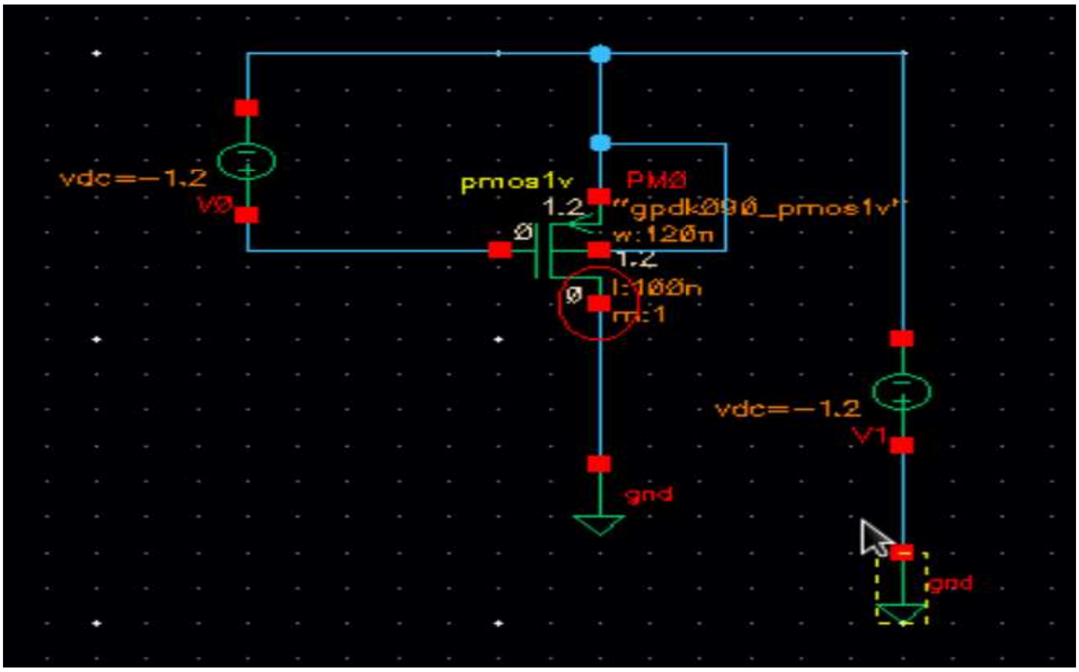
1. Verify the PMOS Characteristics using Cadence Virtuoso

2. Verify the Body effect and Channel length Modulation.

AIM

a) Verify PMOS Characteristics using Cadence Virtuoso and show the graphical output
b) Verify the Body Effect and Channel Length Modulation

CIRCUIT DIAGRAM



THEORY

PMOS DC Characteristics

PMOS DC characteristics are similar to that of the NMOS characteristics. The PMOS characteristics are 180^{O} rotated version of the NMOS. In swapping n-channel for p-channel, we've reversed the direction of current flows and the required supply voltage becomes negative for a p-MOSFET. The p-channels are designed for negative power supplies and out-flowing (negative) drain currents - the opposite of n-channels. The behavior of p-MOS is largely controlled by the voltage at the gate (usually a *negative* voltage). For the usual drain-source voltage drops (i.e., the saturation region: negative voltages from a few volts down to some breakdown voltage) the drain current (I_D) is nearly independent of the drain-source voltage (VDS), and instead depends on the gate voltage (V_G).

In the curve of I_D vs V_{DS}, with constant V_{GS}, we see that the 3 regions of operations (cutoff, linear, and saturation) have similar characteristics as that of n-MOSFET.

The circuit diagram shown above is modified so that one simulation considers V_{GS} to vary from -1.2V to 0V (Output Characteristics – I_D vs V_{DS}) and the other simulation considers V_{DS} to vary from -1.2V to 0V (Input Characteristics – I_D vs V_{GS}).

Body Effect and Channel Length Modulation

Body effect is observed when the source voltage and body voltage are different values. Body effect alters the threshold voltage of the MOSFET, where the threshold voltage increases with the increase in the difference between source and body voltage. Essentially, this change in channel strength by application of reverse bias is called the 'body effect'. The body effect upon the channel can be described using a modification of the threshold voltage, approximated by the following equation:

$$V_{\mathrm{TB}} = V_{T0} + \gamma \left(\sqrt{V_{\mathrm{SB}} + 2\varphi_B} - \sqrt{2\varphi_B} \right)$$

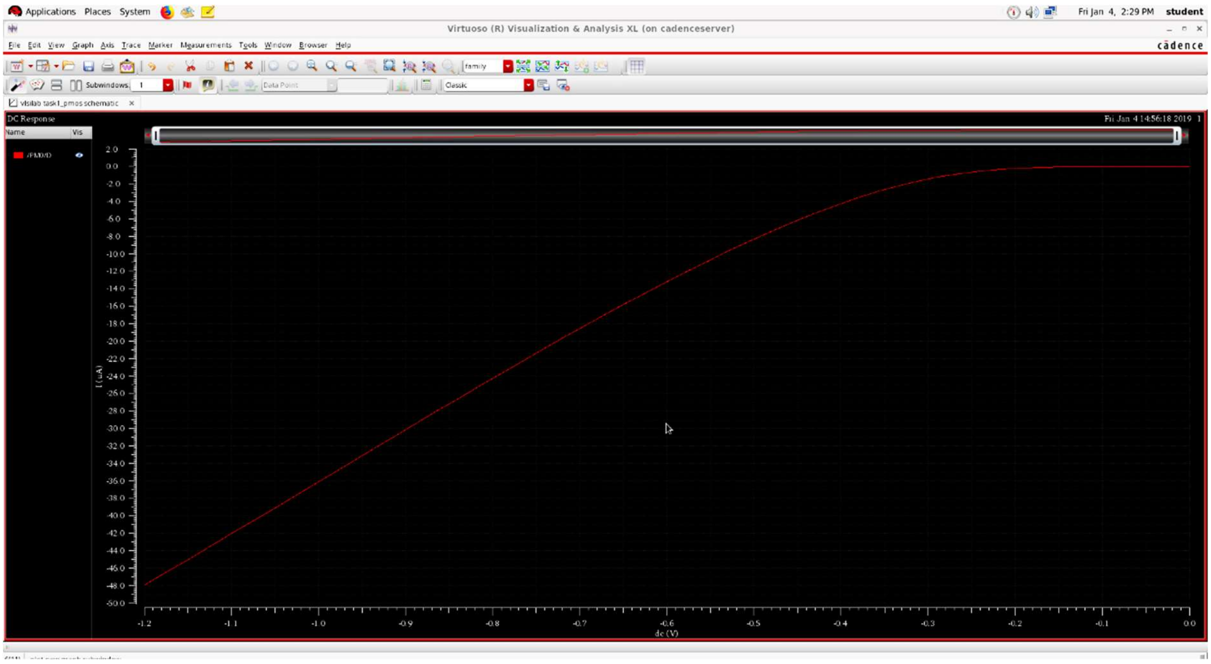
Channel length modulation is observed in the saturation region operation of the p-MOSFET, when the value of V_{DS} keeps increasing. Channel length modulation is a shortening of the length of the inverted channel region towards the drain terminal with increase in drain bias for large drain biases. The result of channel modulation is an increase in current with drain bias and a reduction of output resistance.

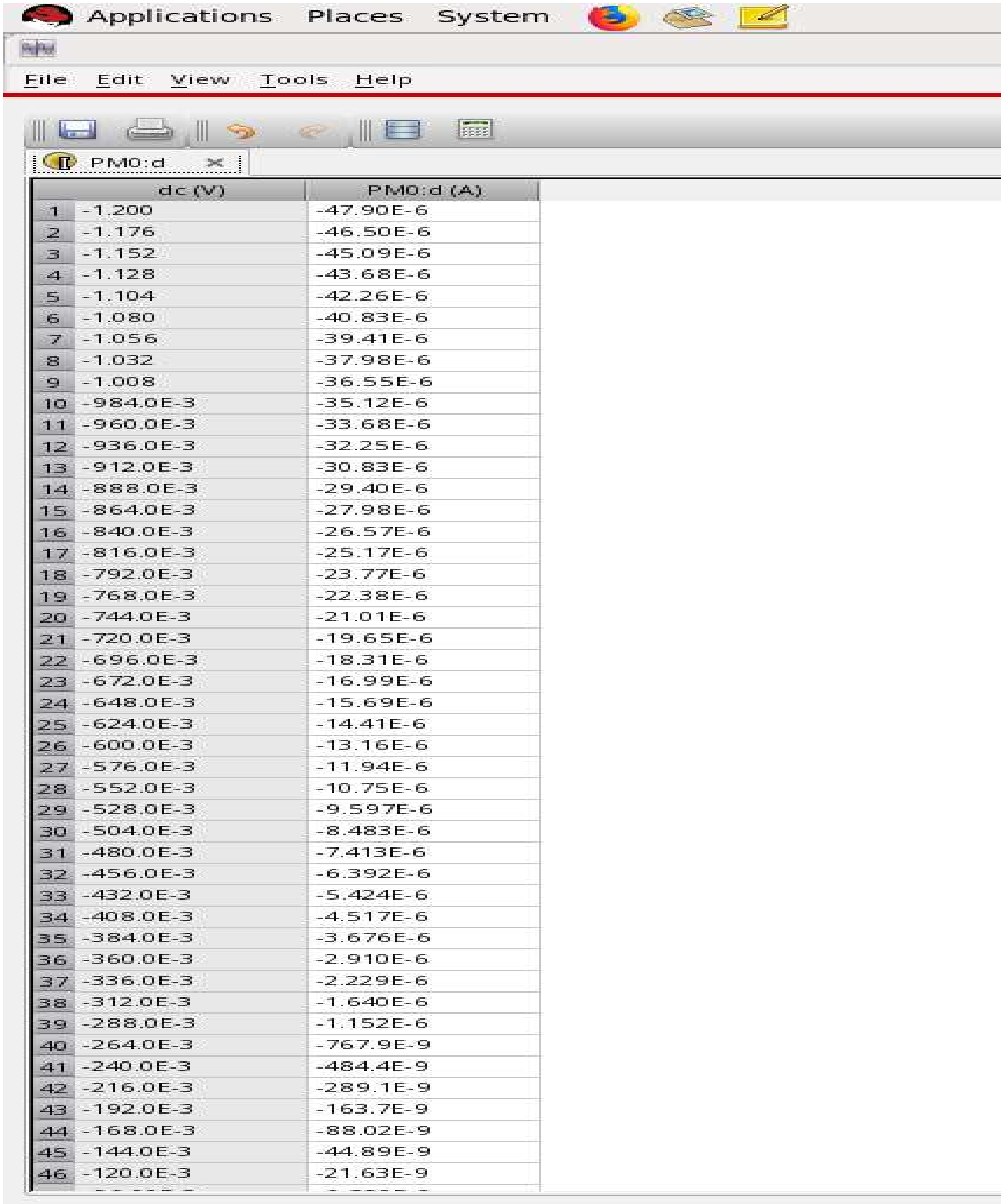
In order to simulate body effect, a dc source of -1.2V is connected to the body instead of connecting the body to the source as usual. Channel length modulation is observed straight from the input characteristics where I_D vs V_{GS} is observed for varying values of V_{DS}.

OBSERVATION GRAPHS

1. DC Characteristics

Transfer characteristics (input) of PMOS

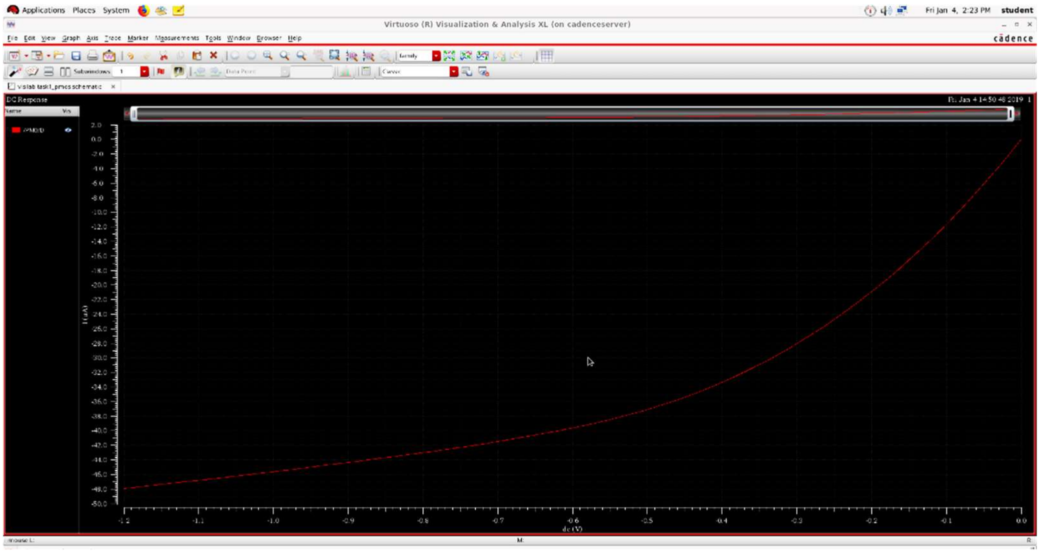




	dc (V)	PM0:d (A)
1	-1.200	-47.90E-6
2	-1.176	-46.50E-6
3	-1.152	-45.09E-6
4	-1.128	-43.68E-6
5	-1.104	-42.26E-6
6	-1.080	-40.83E-6
7	-1.056	-39.41E-6
8	-1.032	-37.98E-6
9	-1.008	-36.55E-6
10	-984.0E-3	-35.12E-6
11	-960.0E-3	-33.68E-6
12	-936.0E-3	-32.25E-6
13	-912.0E-3	-30.83E-6
14	-888.0E-3	-29.40E-6
15	-864.0E-3	-27.98E-6
16	-840.0E-3	-26.57E-6
17	-816.0E-3	-25.17E-6
18	-792.0E-3	-23.77E-6
19	-768.0E-3	-22.38E-6
20	-744.0E-3	-21.01E-6
21	-720.0E-3	-19.65E-6
22	-696.0E-3	-18.31E-6
23	-672.0E-3	-16.99E-6
24	-648.0E-3	-15.69E-6
25	-624.0E-3	-14.41E-6
26	-600.0E-3	-13.16E-6
27	-576.0E-3	-11.94E-6
28	-552.0E-3	-10.75E-6
29	-528.0E-3	-9.597E-6
30	-504.0E-3	-8.483E-6
31	-480.0E-3	-7.413E-6
32	-456.0E-3	-6.392E-6
33	-432.0E-3	-5.424E-6
34	-408.0E-3	-4.517E-6
35	-384.0E-3	-3.676E-6
36	-360.0E-3	-2.910E-6
37	-336.0E-3	-2.229E-6
38	-312.0E-3	-1.640E-6
39	-288.0E-3	-1.152E-6
40	-264.0E-3	-767.9E-9
41	-240.0E-3	-484.4E-9
42	-216.0E-3	-289.1E-9
43	-192.0E-3	-163.7E-9
44	-168.0E-3	-88.02E-9
45	-144.0E-3	-44.89E-9
46	-120.0E-3	-21.63E-9

From the image, and from the table created by it, we observe that the **threshold voltage of the device is -0.288 V.** This is obtained as the point where the voltage change becomes sharp. (from E-9 to E-6).

Drain characteristics (Output) of PMOS



	dc (V)	PM0:d (A)
1	-1.200	-47.90E-6
2	-1.176	-47.63E-6
3	-1.152	-47.36E-6
4	-1.128	-47.08E-6
5	-1.104	-46.80E-6
6	-1.080	-46.52E-6
7	-1.056	-46.24E-6
8	-1.032	-45.95E-6
9	-1.008	-45.66E-6
10	-984.0E-3	-45.37E-6
11	-960.0E-3	-45.07E-6
12	-936.0E-3	-44.77E-6
13	-912.0E-3	-44.47E-6
14	-888.0E-3	-44.16E-6
15	-864.0E-3	-43.84E-6
16	-840.0E-3	-43.52E-6
17	-816.0E-3	-43.19E-6
18	-792.0E-3	-42.85E-6
19	-768.0E-3	-42.50E-6
20	-744.0E-3	-42.14E-6
21	-720.0E-3	-41.77E-6
22	-696.0E-3	-41.37E-6
23	-672.0E-3	-40.96E-6
24	-648.0E-3	-40.53E-6
25	-624.0E-3	-40.07E-6
26	-600.0E-3	-39.58E-6
27	-576.0E-3	-39.06E-6
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29	-528.0E-3	-37.86E-6
30	-504.0E-3	-37.17E-6
31	-480.0E-3	-36.41E-6
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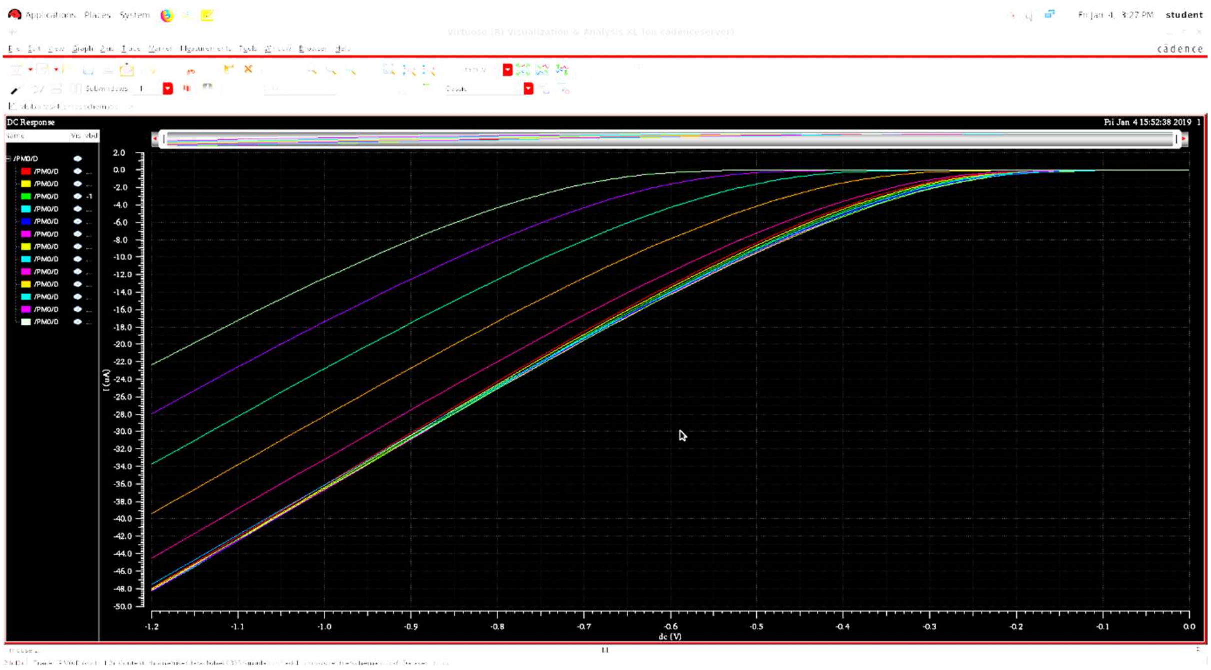
33	-432.0E-3	-34.67E-6
34	-408.0E-3	-33.67E-6
35	-384.0E-3	-32.59E-6
36	-360.0E-3	-31.41E-6
37	-336.0E-3	-30.13E-6
38	-312.0E-3	-28.75E-6
39	-288.0E-3	-27.27E-6
40	-264.0E-3	-25.68E-6
41	-240.0E-3	-23.98E-6
42	-216.0E-3	-22.16E-6
43	-192.0E-3	-20.23E-6
44	-168.0E-3	-18.17E-6
45	-144.0E-3	-15.99E-6
46	-120.0E-3	-13.68E-6

From the image, and from the table created by it, we observe that the **<u>pinch-off voltage (saturation) of the device is -1.128 V</u>.** This is obtained as the point where the voltage becomes constant, i.e. it achieves saturation.

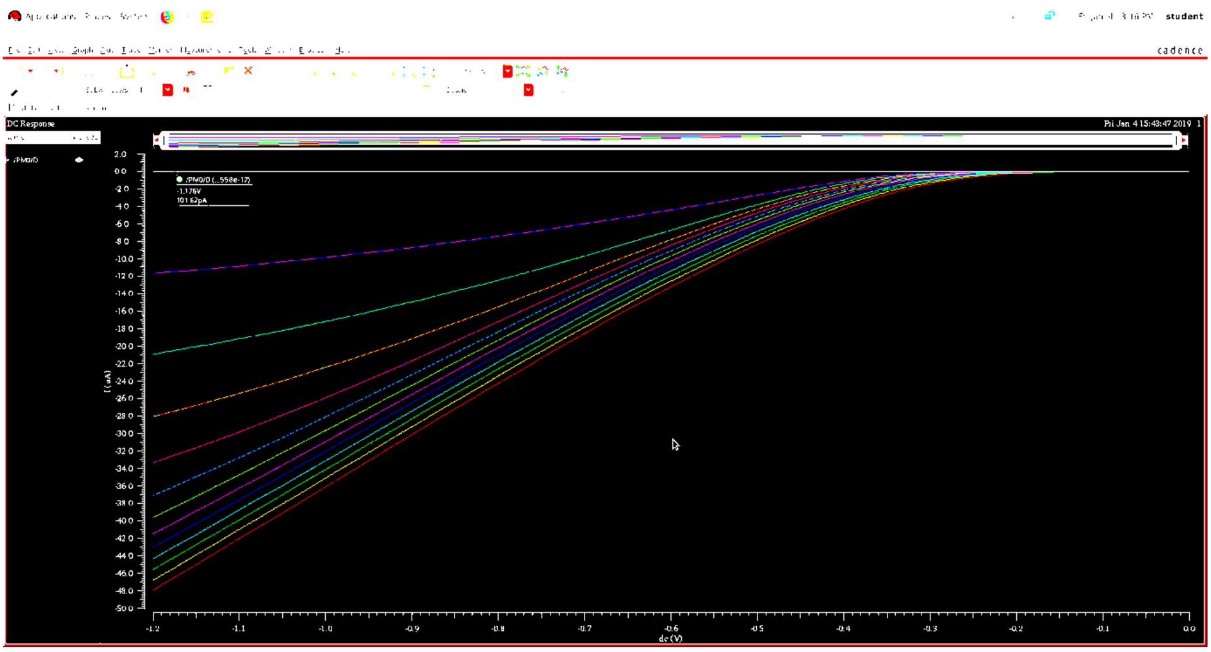
2. Transient Characteristics

Body effect



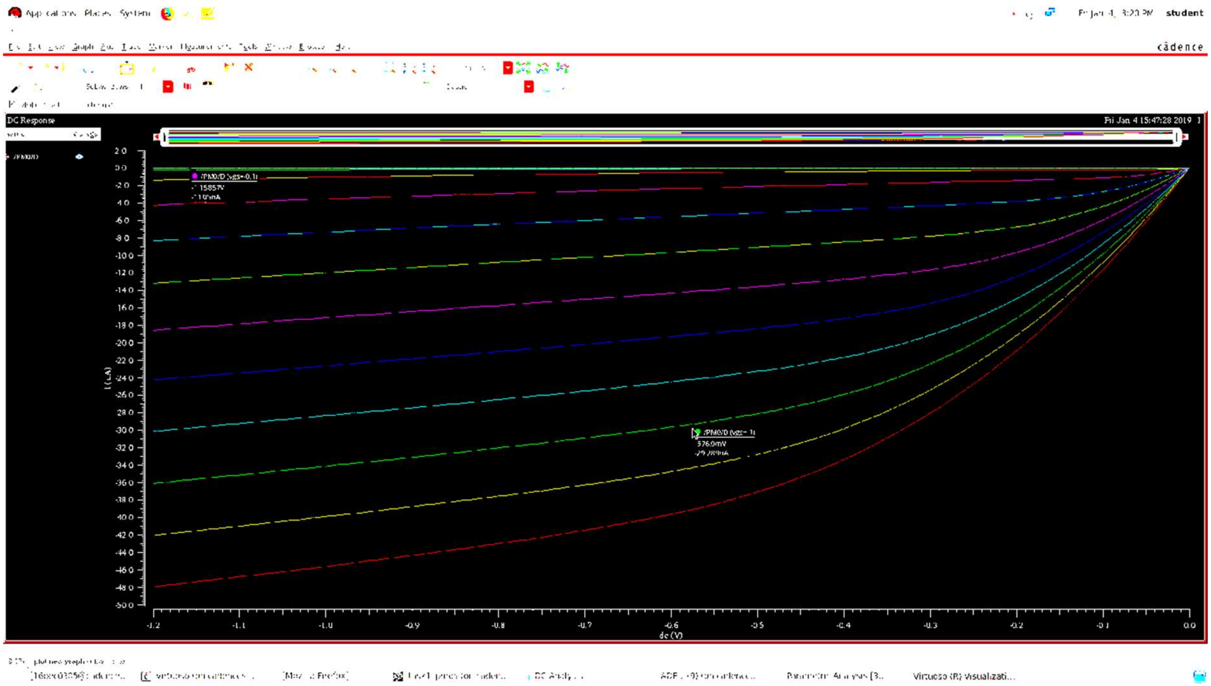
The figure above shows that **with increase in V_{BS}, the threshold voltage of curve increases.**

Input Characteristics



From the figure above, it is clear that **with increase in V_{DS} (negative increase), the I_D increases as well.**

Output Characteristics



From the figure above, it is clear that **with increase in V_{GS} (negative increase), the saturation current of I_D increases as well.**

INFERENCE

1. DC characteristics

Transfer characteristics

There needs to be a minimum voltage applied to drain so that the current starts to flow in the channel. This produces a V_{DS}, which plays an important role to create the movement of electrons in the channel and thereby flow of current. That voltage is called **threshold voltage**.

Drain characteristics

As the gate voltage increase, the width of the decreases at the drain and after a point it reaches a stagnant situation. Thus, anymore increase in V_{GS} will not increase the drain current. This phenomenon is called **saturation.**

2. Transient characteristics

Body effect

As explained in the theory, the body-source voltage difference causes the change in the width of depletion region, and thus increase the threshold voltage.

Input characteristics

There needs to be a minimum V_{DS} (negative) for there to be an I_D (negative). Also, with the increase in V_{DS}, I_D also increases. This is because with increase in V_{DS}, the electrons flow more freely in the channel.

Output Characteristics

The increase in V_{GS} (negative) the channel width increases. This allows more flow of electron and thus pushes the pinch off region even further. This increases the maximum saturation current possible.