PixArt Imaging Inc.
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PS5420
DATA SHEET

1/2.9” 4MP HDR CMOS IMAGE SENSOR

Aug. 2023

Version 1.25

PS5420 4MP CMOS IMAGE SENSOR

General Description

The **PS5420** is a highly integrated CMOS image sensor that output of **1944x1944 (4MP)** pixels with rolling shutter readout. It embedded the new FinePixel™ and HDR sensor technology to perform excellent image quality and single-shot high dynamic range synthesized image output. **PS5420** can outputs linear 14-bit or local tone mapped 12-bit or 10-bit raw data through MIPI CSI-2 interface with very low power consumption.

The **PS5420** can be programmed to set the exposure time and analog gain for different luminance condition via I^2C serial control bus. Embedded HDR image synthesis with local tone mapping to deliver high performance, cost effective and time to market for high resolution HDR application.

Features

- **1960 x 1960 active pixels with Bayer-RGB color filter array and micro-lens**
- **Output format:**
  - 10-bit Linear RAW RGB
  - 14-bit Linear HDR-RAW RGB
  - 12-bit/10bit LTM HDR-RAW RGB
- **Output interface**
  - 4 lane MIPI output, up to 900Mbps
- **On-chip column A/D converter**
- **On-chip manual analog gain control**
- **Continuous variable frame time & exposure time**
- **I^2C Interface**
- **Automatic black-level calibration**
- **Black sun cancellation**
- **Programmable fast-switch configuration**
- **Support on-chip HDR combination**
- **Support LTM (local tone mapping) function**
- **Support multi-sensor frame synchronization**
- **Support WOI and subsampling**
- **Support dummy line & pixel timing**
- **Support output Hsync at Vsync**
- **Support 1.7V~3.3V I/O**
- **On-chip PLL**
  (input_clock / PLL_m >= 1MHz)

Specifications

Parameter	Typical Value
Resolution	1944(H) x 1944(V)
Pixel size	2.20um (H) x 2.20um (V)
Shutter type	Electronic rolling shutter (ERS)
Optical format	1/2.9-inch (1:1)
Max. chief ray angle	10.9 degree
ADC	10-bit
Sensitivity@530nm	2400 mV/Lux-sec
SNRmax	39 dB
Dynamic range	74 dB (Linear) 85 dB (HDR)
Scan mode	Progressive scan
Input clock	Max 28MHz
Pixel clock	Max 165MHz
Max. frame rate	4MP: 1944x1944 HDR @ 30fps 1080p:1920x1080 HDR @ 45fps
Supply voltage	Analog: 3.3 V Digital: 1.2 V I/O: 1.8V to 3.3V
Power consumption	215mW @ HDR LTM 4Mp30
Operating temperature	-30 ºC to 85 ºC

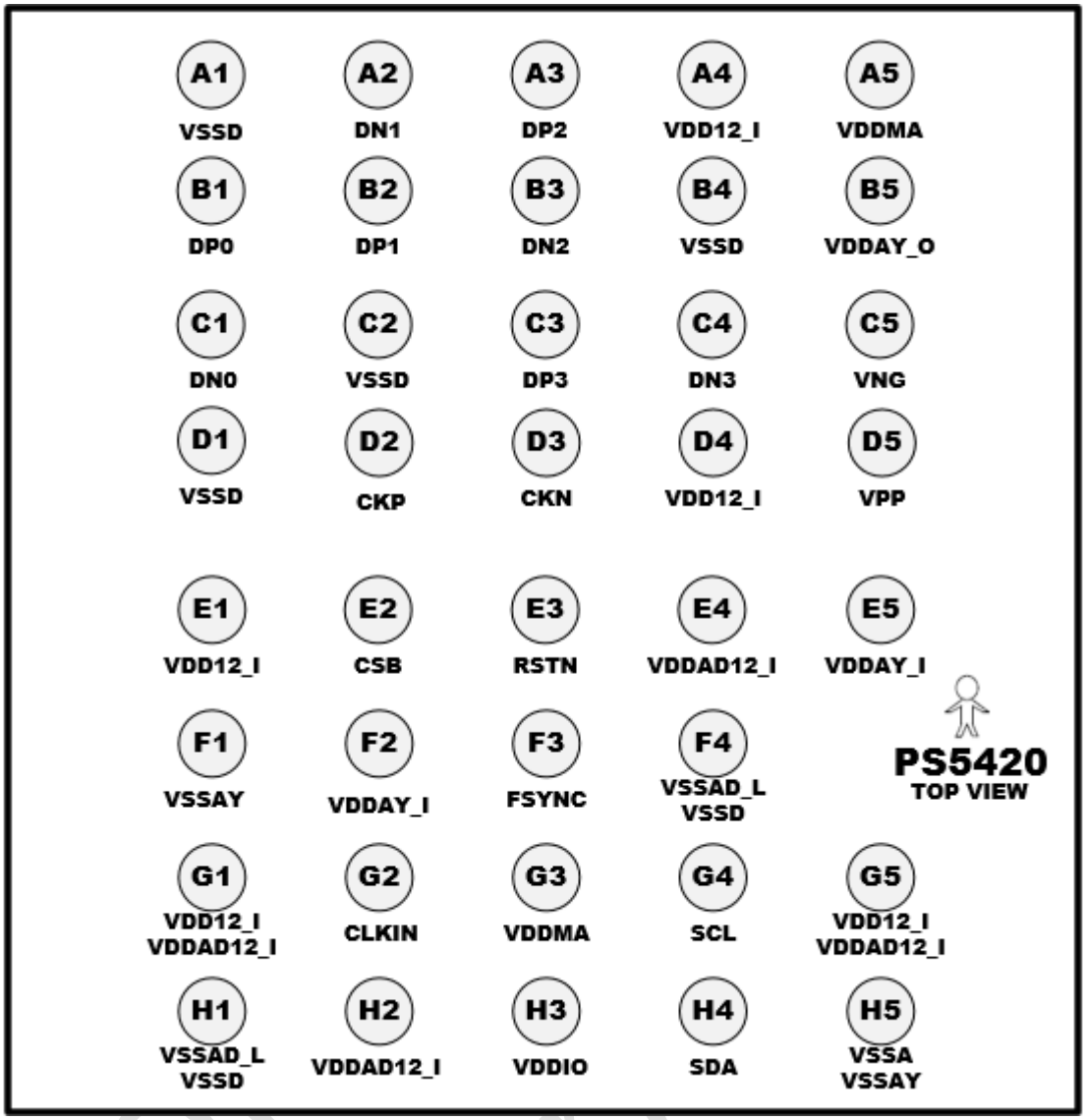
Applications

- **Video Doorbell Camera**
- **Fisheye Camera**
- **360 Panoramic Camera**
- **Sports DV Camera**

Ordering Information

Part Number	Description
PS5420LT-AA	39-Ball CSP

1. Pin Assignment



Pin No.	Name	Type	Description
A1	**VSSD**	GND	GND
A2	**DN1**	Output	MIPI digital data output_1 negative terminal
A3	**DP2**	Output	MIPI digital data output_2 positive terminal
A4	**VDD12_I**	Power	Digital power: 1.2V
A5	**VDDMA**	Power	Analog power: 3.3V
B1	**DP0**	Output	MIPI digital data output_0 positive terminal
B2	**DP1**	Output	MIPI digital data output_1 positive terminal
B3	**DN2**	Output	MIPI digital data output_2 negative terminal
B4	**VSSD**	GND	GND
B5	**VDDAY_O**	Power	VDDAY LDO output voltage (2.7 to 3.0V)

C1	**DN0**	Output	MIPI digital data output_0 negative terminal
C2	**VSSD**	GND	GND
C3	**DP3**	Output	MIPI digital data output_3 positive terminal
C4	**DN3**	Output	MIPI digital data output_3 negative terminal
C5	**VNG**	Power	Reference voltage
D1	**VSSD**	GND	GND
D2	**CKP**	Output	MIPI output clock positive terminal
D3	**CKN**	Output	MIPI output clock negative terminal
D4	**VDD12_I**	Power	Digital power: 1.2V
D5	**VPP**	Power	External voltage for OTP device
E1	**VDD12_I**	Power	Digital power: 1.2V
E2	**CSB**	Input	Suspend control, "1": suspend mode, "0": normal mode
E3	**RSTN**	Input	Reset signal, active low, internal pull high
E4	**VDDAD12_I**	Power	Analog power input voltage(1.2V)
E5	**VDDAY_I**	Power	Sensor power input
F1	**VSSAY**	GND	GND
F2	**VDDAY_I**	Power	Sensor power input
F3	**FSYNC**	Input	Frame sync signal
F4	**VSSAD_L / VSSD**	GND	GND
G1	**VDD12_I / VDDAD12_I**	Power	Digital power: 1.2V
G2	**CLKIN**	Input	Master clock input
G3	**VDDMA**	Power	Analog power: 3.3V
G4	**SCL**	I/O	I2C clock, open drain type
G5	**VDD12_I / VDDAD12_I**	Power	Digital / Analog power: 1.2V
H1	**VSSAD_L / VSSD**	GND	GND
H2	**VDDAD12_I**	Power	Analog power input voltage(1.2V)
H3	**VDDIO**	Power	I/O power: 1.8V to 3.3V
H4	**SDA**	I/O	I2C data, open drain type
H5	**VSSA/VSSAY**	GND	GND

2. Specifications

Absolute Maximum Ratings †		
Operating Temperature ††		-30 ºC to 85 ºC
Ambient Storage Temperature		-40ºC to 125ºC
Supply Voltage (with respect to ground)	V_{DDA}	4.5V
	V_{DDD}	3.0V
	V_{DDIO}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to V_{DDIO} + 0.3V
Lead-free temperature, Surface-mount process		245ºC
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃) †††					
Symbol	Parameter	Min.	Typ.	Max.	Unit
Type: POWER					
V_{DDA}	DC supply voltage – Analog	3.14	3.3	3.47	V
V_{DDD}	DC supply voltage – Digital core	1.14	1.2	1.3	V
V_{DDIO}	DC supply voltage – I/O	1.71		3.47	V
I_{DDA}	Operating Current – Analog (2-lane MIPI)		16.7		mA
I_{DDD}	Operating Current – Digital (2-lane MIPI)		133.3		mA
I_{DDIO}	Operating Current – I/O (2-lane MIPI)		1		mA
Type: IN & I/O					
V_{IH}	Input Voltage HIGH	V_{DDIO} * 0.7			V
V_{IL}	Input Voltage LOW			V_{DDIO} * 0.3	V
Type: OUT & I/O					
V_{OH}	Output Voltage HIGH	V_{DDIO} * 0.9			V
V_{OL}	Output Voltage LOW			V_{DDIO} * 0.1	V

AC Operating Condition					
Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency	10	27	28	MHz
t_{sysclk_dc}	System clock duty cycle	45		55	%
	Clock input rise/fall time (20% ~ 80% VDDIO)			3	ns

Sensor Characteristics		
Parameter	Typ.	Unit
Sensitivity@530nm	2400	mV/Lux-Sec
Signal to Noise Ratio MAX	39	dB
Dynamic Range	85	dB

†: Absolute Maximum Ratings

1. **At ambient temperature = 25°C.**
2. **Maximum Ratings are the maximum parameter values that can damage the device when exceeding this limit.**
3. **Exposure to these conditions or conditions beyond those indicated may adversely affect device**

reliability. Functional operation under absolute-maximum-rated conditions is not recommended.

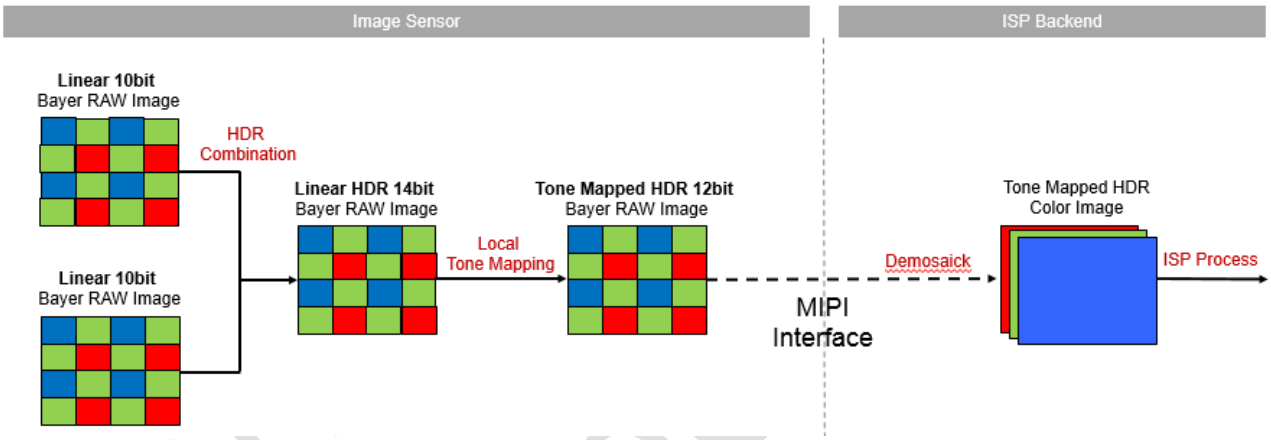
††: Sensor function works in the ambient operating temperature range. However, the image quality may change at high temperature condition.

†††:The power consumption is measured with 4X analog gain in HDR LTM 4MP 30fps at Tj = 25ºC.

3. HDR Data Format

The sensor performs single exposure with dual sensitivity image data and on-chip combine dual image data line-by-line as a linear high dynamic range 14bit data. Then sensor perform local tone mapping from higher data bits (14bits) to lower data bits (12bit) for suppressing data range and enhancing local contrast during the process.

Finally, the sensor output tone mapped RAW 12bit or 10bit data via MIPI interface. Backend chip received the tone mapped RAW data without complex HDR timing and combination while using staged HDR sensor.



PS5420 support linear or HDR output mode, the available output format summary as following table:

Output Format		Output I/F		Description
		DVP	MIPI	
Linear	RAW10	--	V	Linear 10bit RAW data
Linear HDR	RAW14	--	V	Linear DCG Combined HDR 14bit RAW data
Linear HDR	RAW12	--	V	Linear DCG Combined HDR 12bit RAW data
HDR + LTM	RAW12	--	V	12bit HDR+LTM RAW data
HDR + LTM	RAW10	--	V	10bit HDR+LTM RAW data

4. I²C Bus

PS5420 supports I²C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1001000" and supports receiving / transmitting speed as maximum 400 kHz.

I²C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 3.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 3.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

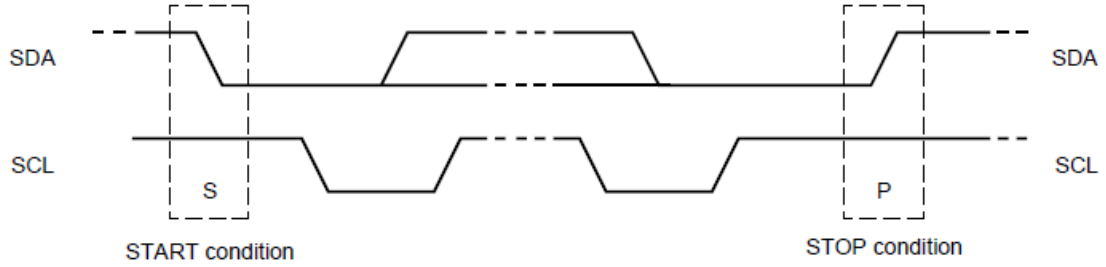


Fig.3.1 Start and Stop Condition

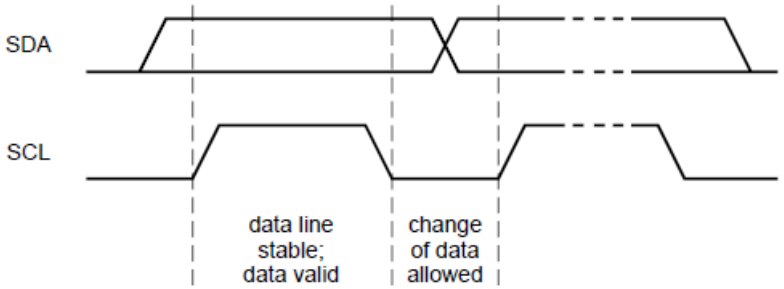


Fig.3.2 Valid Data

Data Transfer Format

Master transmits data to salve (write cycle)

- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 : Read cycle, RW = 0 : Write cycle.
- SUBADDRESS : The address values of **PS5420** internal control registers. (Please refer to **PS5420** register description)

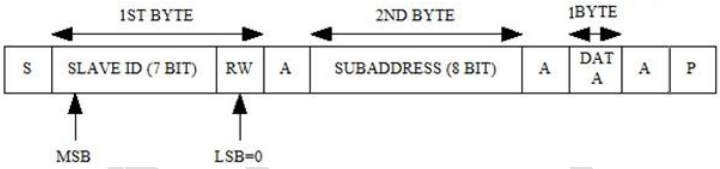


Fig.3.3 Master-transmitter transmits to slave-receiver

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (**PS5420**) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the **PS5420** acknowledgment, the master places the 8 bits data on SDA line and transmit to **PS5420** control register (address was assigned by 2nd byte). After **PS5420** issues acknowledgment, the master can generate a stop condition to end of this write cycle. Every control registers value inside **PS5420** can be programming via this way.

Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.

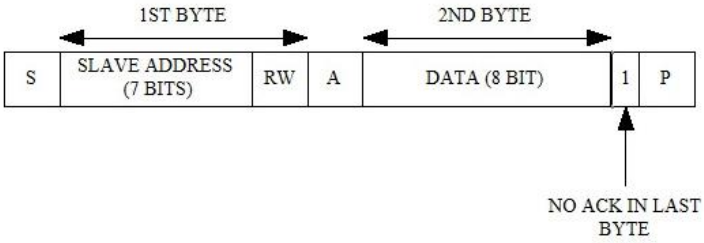


Fig.3.4 Slave-transmitter transmits to master-receiver

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by **PS5420**. The 8 bits data was read from **PS5420** internal control register that address was assigned by previous write cycle. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (**PS5420**) must releases SDA line to master to generate STOP condition.

I²C Bus Timing

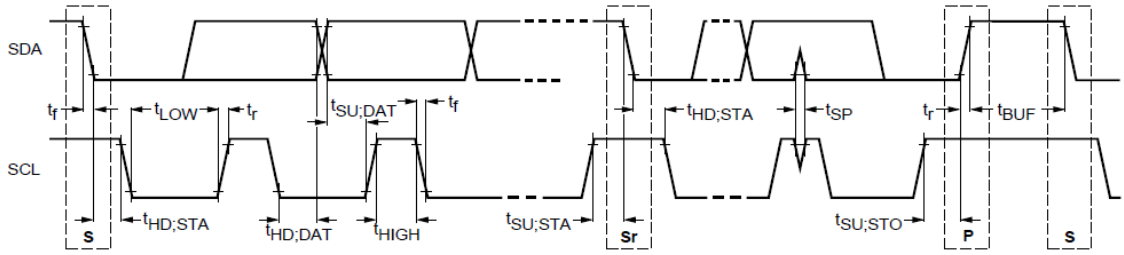


Fig.3.5 Definition of timing for F/S mode devices on the I2C-bus

I²C Bus Timing Specification						
Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency.	f_{scl}	10	100	0	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	0.6	-	µs
Low period of the SCL clock.	t_{LOW}	4.7	-	1.3	-	µs
High period of the SCL clock.	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data set-up time.	$t_{SU;DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals.	t_r	-	1000	-	300	ns (note l)
Fall time of both SDA and SCL signals.	t_f	-	300	-	300	ns (note l)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line.	C_b	-	400	-	400	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-		0.1 VDD	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-		0.2 VDD	V

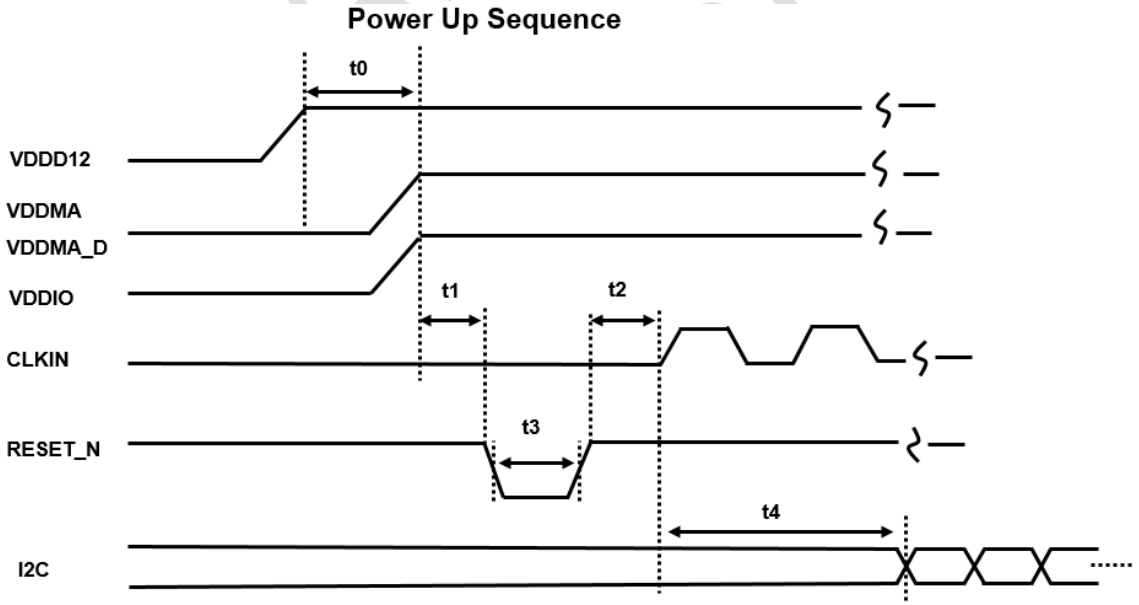
Note: It depends on the “high” period time of SCL.

5. Power Sequence

Power-Up Sequence

The recommended power-up sequence for the PS5420 is shown as the following figure. The available power supplies must have the separation specified below.

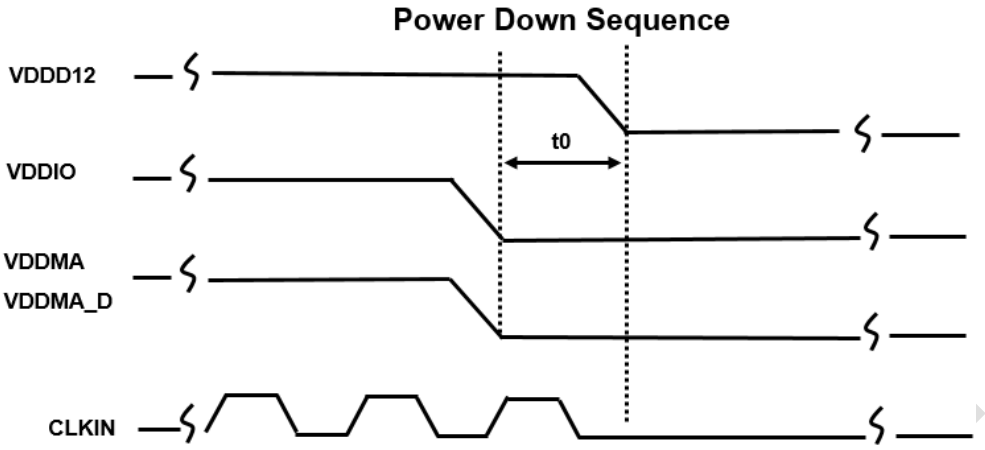
1. Turn on VDDD12 power supply.
2. After 100µs (t0), VDDMA, VDDMA_D and VDDIO power supply simultaneously.
3. After 100µs (t1), RESET_N must go low.
4. RESET_N active low for at least 1ms (t3).
5. After 100µs (t2), enable CLKIN.
6. Wait at least 61440*MCLK (t4), I2C starts to write commands.



Power-Down Sequence

The recommended power-down sequence for the PS5420 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn off VDDMA, VDDMA_D and VDDIO power supply simultaneously.
2. After 100µs (t0), turn off VDDD12 power supply.



Note: This Power-Down Sequence could be ignored if there is a RESET_N signal toggle in Power-Up Sequence (ie. RESET_N active low for at least 1ms (t3)).

CSB Suspend Sequence

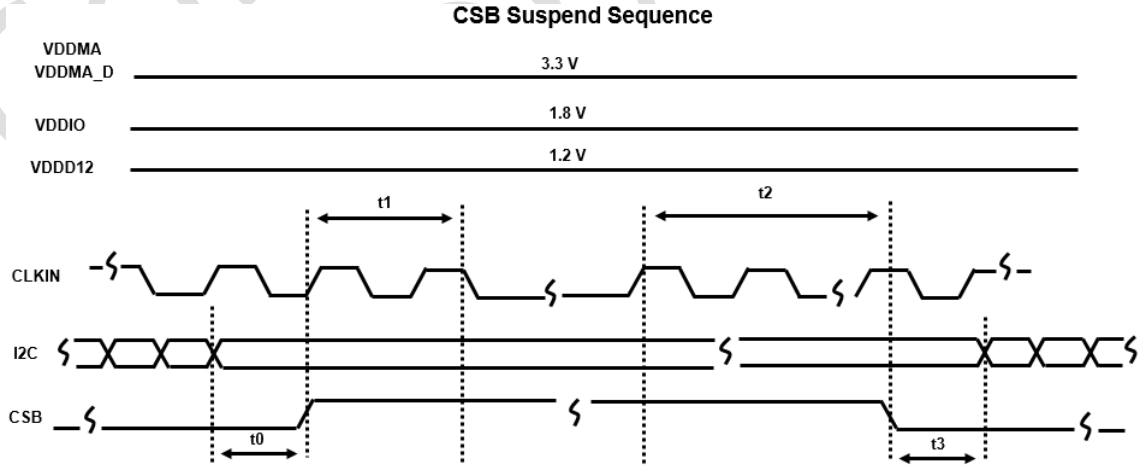
The recommended CSB Suspend sequence for the PS5420 is shown as the following figure. The available power supplies must have the separation specified below.

ON → OFF :

1. I2C must write commands to turn off internal clock for PS5420 .
2. After 100µs (t0), CSB must go high
3. After 100µs (t1), turn off CLKIN.

OFF → ON :

1. Turn on CLKIN.
2. After 100µs (t2), CSB must go low.
3. Wait at least 1ms (t3) for internal clock stable.
4. I2C starts to write commands.



6. Register Table

Bank	Address		Bit	Name	R/W	Description
	Hex	Dec				
0	00	00	[7:0]	PartID[15:8]	R	Sensor ID
0	01	01	[7:0]	PartID[7:0]	R	Sensor ID
0	02	02	[3:0]	VersionID[3:0]	R	Sensor ID
0	03	03	[3:0]	SubID[3:0]	R	Sensor ID
0	11	17	[7]	Cmd_GatedAllClk	R/W	Clock Gated Control (1: Gate Clock)
1	05	05	[3]	Cmd_10_TriState	R/W	TriState IO of PxData[1:0]
			[2]	Cmd_Sw_PwrDn	R/W	Power-Down Control
			[1]	Cmd_Sw_TriState	R/W	TriState IO of PxData, Hsync, Vsync, and Pxclk
1	09	09	[0]	UpdateFlag	R/W	Exposure & Gain Update Control (Write 0x01)
1	0A	10	[7:0]	Cmd_Lpf [15:8]	R/W	Line per frame = Cmd_Lpf+ 1
1	0B	11	[7:0]	Cmd_Lpf [7:0]	R/W	Line per frame = Cmd_Lpf+ 1
1	0C	12	[7:0]	Cmd_OffNy1[15:8]	R/W	Exposure Control
1	0D	13	[7:0]	Cmd_OffNy1[7:0]	R/W	Exposure Control
1	0E	14	[3:0]	Cmd_OffNe1[11:8]	R/W	Exposure Control
1	0F	15	[7:0]	Cmd_OffNe1[7:0]	R/W	Exposure Control
1	1B	27	[7]	Cmd_Hflip	R/W	Horizontal Flip
			[6:5]	Cmd_Askip_H[1:0]	R/W	Horizontal Skip
			[3:0]	Cmd_Hsize_e1[11:8]	R/W	Raw Image Horizontal Size
1	1C	28	[7:0]	Cmd_Hsize_e1[7:0]	R/W	Raw Image Horizontal Size
1	1D	29	[7]	Cmd_Vflip	R/W	Vertical Flip
			[6:5]	Cmd_Askip_V[1:0]	R/W	Vertical Skip
			[2:0]	Cmd_Vsize[10:8]	R/W	Raw Image Vertical Size
1	1E	30	[7:0]	Cmd_Vsize[7:0]	R/W	Raw Image Vertical Size
1	1F	31	[2:0]	Cmd_Vstart[10:8]	R/W	Raw Image Vertical Offset
1	20	32	[7:0]	Cmd_VStart[7:0]	R/W	Raw Image Vertical Offset
1	27	39	[4:0]	Cmd_LineTime [12:8]	R/W	Line Time = Cmd_LineTime* 0.5 clock cycles
1	28	40	[7:0]	Cmd_LineTime [7:0]	R/W	Line Time = Cmd_LineTime* 0.5 clock cycles
1	80	128	[7:0]	Cmd_DG_gain_idx[7:0]	R/W	Sensor Digital Gain index
1	83	131	[7:0]	Cmd_gain_idx[7:0]	R/W	Sensor Analog Gain index
1	8F	143	[2]	Cmd_ImgSyn_Mode	R/W	HDR Image Mode : 0: Analog nonHDR-mode

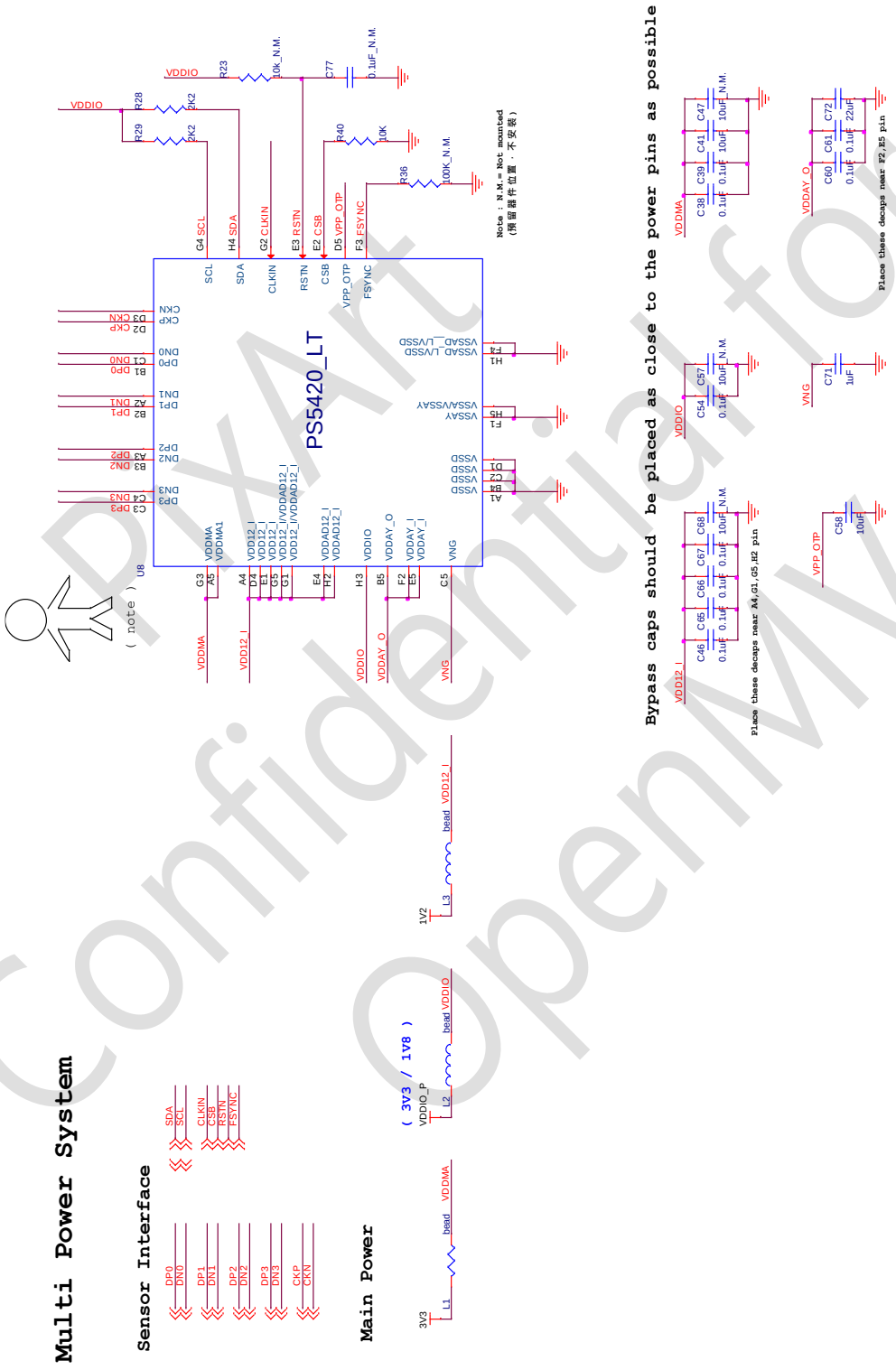
						1: Analog HDR-mode
			[0]	Cmd_ImgSyn_EnH	R/W	HDR Image Synthesis Enable
1	90	144	[0]	Cmd_Adc_sample_posedge	R/W	ADC sample timing control
1	92	146	[4:0]	R_ISP_TestMode[4:0]	R/W	Test Image Control
1	93	147	[7:0]	R_ISP_TestValueLo[7:0]	R/W	Test Image Control
1	94	148	[7:0]	R_ISP_TestValueHi[7:0]	R/W	Test Image Control
1	97	151	[0]	Cmd_Pga_D1frm	R/W	Pga Gain auto-delay one frame
1	A3	163	[4]	Cmd_WOI_VOffset_sign	R/W	Vertical offset of output image
			[2:0]	Cmd_WOI_VOffset[10:8]	R/W	Vertical offset of output image
1	A4	164	[7:0]	Cmd_WOI_VOffset[7:0]	R/W	Vertical offset of output image
1	A5	165	[2:0]	Cmd_WOI_VSize[10:8]	R/W	Vertical size of output image
1	A6	166	[7:0]	Cmd_WOI_VSize[7:0]	R/W	Vertical size of output image
1	A7	167	[4]	Cmd_WOI_HOffset_sign	R/W	Horizontal offset of output image
			[3:0]	Cmd_WOI_HOffset[11:8]	R/W	Horizontal offset of output image
1	A8	168	[7:0]	Cmd_WOI_HOffset[7:0]	R/W	Horizontal offset of output image
1	A9	169	[2:0]	Cmd_WOI_HSize[10:8]	R/W	Horizontal size of output image Note. Cmd_WOI_HSize <= 2047
1	AA	170	[7:0]	Cmd_WOI_HSize[7:0]	R/W	Horizontal size of output image Note. Cmd_WOI_HSize <= 2047
1	AB	171	[3:0]	Cmd_Np[3:0]	R/W	Frequency eliminate control
1	F1	241	[5:0]	T_spll_predivider[5:0]	R/W	PLL Control
1	F2	242	[5:0]	T_spll_postdivider [5:0]	R/W	PLL Control
1	F5	245	[4]	T_spll_enh	R/W	PLL Control
			[3]	T_spll_div2_enH	R/W	PLL Control
			[1:0]	T_spll_modedivider [1:0]	R/W	PLL Control
2	10	16	[1]	R_FrameSyncWait	R/W	0: Continue mode - Continuous output after one pulse trigger signal. 1: Single mode (Not support LTM function) - One frame output after one pulse trigger signal.
			[0]	R_FrameSyncMode	R/W	0: Normal Mode. 1: Frame Sync Mode.
2	2E	46	[4:0]	Cmd_ABC_LockRange2_UB[4:0]	R/W	If BLC diff value > Cmd_ABC_LockRange2_UB , then BLC update for HGain channel
2	33	51	[4:0]	Cmd_ABC_LockRange1_UB[4:0]	R/W	If BLC diff value > Cmd_ABC_LockRange1_UB, then BLC update for LGain channel
2	3A	58	[2]	Cmd_ABC_EnH	R/W	BLC function enable

2	46	70	[7]	Cmd_DigDac_B_Sign	R/W	Black Level Offset for B Channel
			[2:0]	Cmd_DigDac_B_Offset[10:8]	R/W	Black Level Offset for B Channel
2	47	71	[7:0]	Cmd_DigDac_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	48	72	[7]	Cmd_DigDac_Gb_Sign	R/W	Black Level Offset for Gb Channel
			[2:0]	Cmd_DigDac_Gb_Offset[10:8]	R/W	Black Level Offset for Gb Channel
2	49	73	[7:0]	Cmd_DigDac_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	4A	74	[7]	Cmd_DigDac_Gr_Sign	R/W	Black Level Offset for Gr Channel
			[2:0]	Cmd_DigDac_Gr_Offset[10:8]	R/W	Black Level Offset for Gr Channel
2	4B	75	[7:0]	Cmd_DigDac_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	4C	76	[7]	Cmd_DigDac_R_Sign	R/W	Black Level Offset for R Channel
			[2:0]	Cmd_DigDac_R_Offset[10:8]	R/W	Black Level Offset for R Channel
2	4D	77	[7:0]	Cmd_DigDac_R_Offset[7:0]	R/W	Black Level Offset for R Channel
2	A0	160	[7]	Cmd_DigDac2_B_Sign	R/W	Black Level Offset for B Channel
			[2:0]	Cmd_DigDac2_B_Offset[10:8]	R/W	Black Level Offset for B Channel
2	A1	161	[7:0]	Cmd_DigDac2_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	A2	162	[7]	Cmd_DigDac2_Gb_Sign	R/W	Black Level Offset for Gb Channel
			[2:0]	Cmd_DigDac2_Gb_Offset[10:8]	R/W	Black Level Offset for Gb Channel
2	A3	163	[7:0]	Cmd_DigDac2_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	A4	164	[7]	Cmd_DigDac2_Gr_Sign	R/W	Black Level Offset for Gr Channel
			[2:0]	Cmd_DigDac2_Gr_Offset[10:8]	R/W	Black Level Offset for Gr Channel
2	A5	165	[7:0]	Cmd_DigDac2_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	A6	166	[7]	Cmd_DigDac2_R_Sign	R/W	Black Level Offset for R Channel
			[2:0]	Cmd_DigDac2_R_Offset[10:8]	R/W	Black Level Offset for R Channel
2	A7	167	[7:0]	Cmd_DigDac2_R_Offset[7:0]	R/W	Black Level Offset for R Channel
2	ED	237	[0]	UpdateFlag	R/W	ABC Update Control (Write 0x01)
5	06	6	[2:0]	R_Data_Format[2:0]	R/W	Data Format type : - 3 for RAW8 - 4 for RAW10 - 5 for RAW12 - 6 for RAW14
5	0F	15	[0]	R_CSI2_Enable	R/W	0: Stop MIPI signal output 1: Start MIPI signal output
5	10	16	[2:0]	R_CsiTx_LaneN[2:0]	R/W	1 for 1_Lane application 2 for 2_Lane application 4 for 4_Lane application
5	40	64	[5:0]	T_pll_predivider[5:0]	R/W	MIPI pll clock divider
5	41	65	[5:0]	T_pll_postdivider[5:0]	R/W	MIPI pll clock scalar
5	43	67	[3]	T_pll_div2_EnH	R/W	MIPI pll clock divider2 selection

5	44	68	[0]	T_pll_enh	R/W	MIPI pll Control
5	B0	176	[0]	R_MIPI_Skip_Line_SP_EnH	R/W	MIPI data lane if skip LS/LE short packet
5	ED	237	[0]	UpdateFlag	R/W	MIPI Update Control (Write 0x01)
6	45	69	[6]	R_Temp_manual_En	R/W	Temp_save manual mode enable
			[2:0]	R_Temp_manual[10:8]	R/W	Temp_save manual value
6	46	70	[7:0]	R_Temp_manual[7:0]	R/W	Temp_save manual value
6	98	152	[0]	R_LTM_EnH	R/W	LTM function enable
6	99	153	[7:0]	Cmd_LTM_BackLight[7:0]	R/W	LTM BackLight strength
6	9A	154	[3:0]	Cmd_LTM_DeHaze[3:0]	R/W	LTM DeHaze strength
6	9A	154	[3:0]	Cmd_LTM_brighteness[3:0]	R/W	LTM brightness strength
6	9E	158	[4:0]	Cmd_LTM_limit[4:0]	R/W	LTM strength limitation
6	F1	241	[0]	UpdateFlag	R/W	LTM Update Control (Write 0x01)

7. Reference Circuit Schematic

➢ **reference circuit for multi power system**

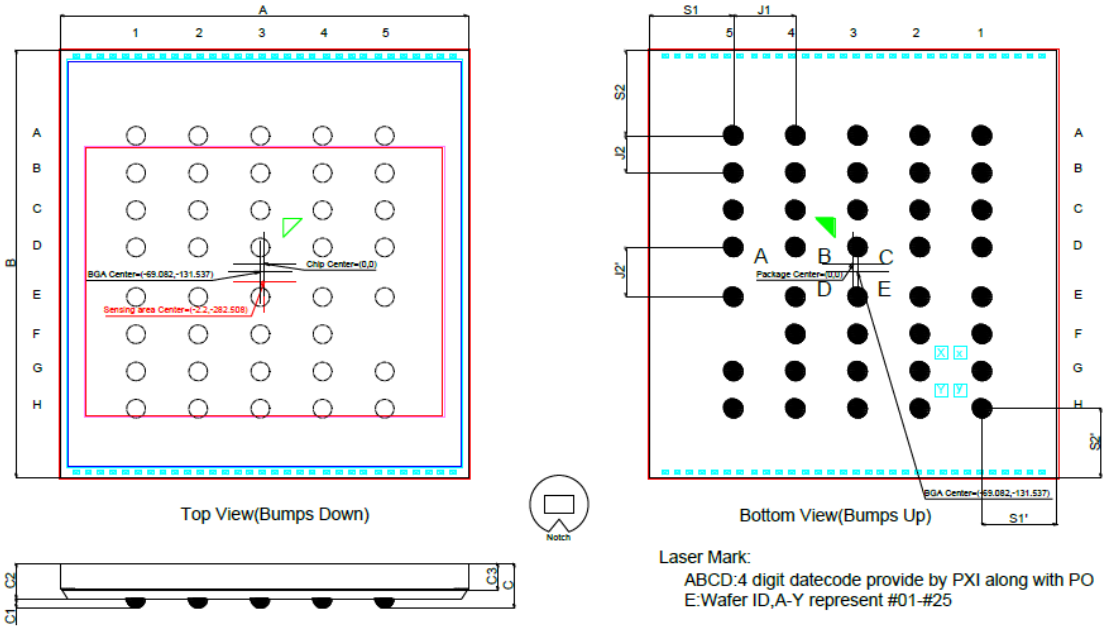


8. Package Information

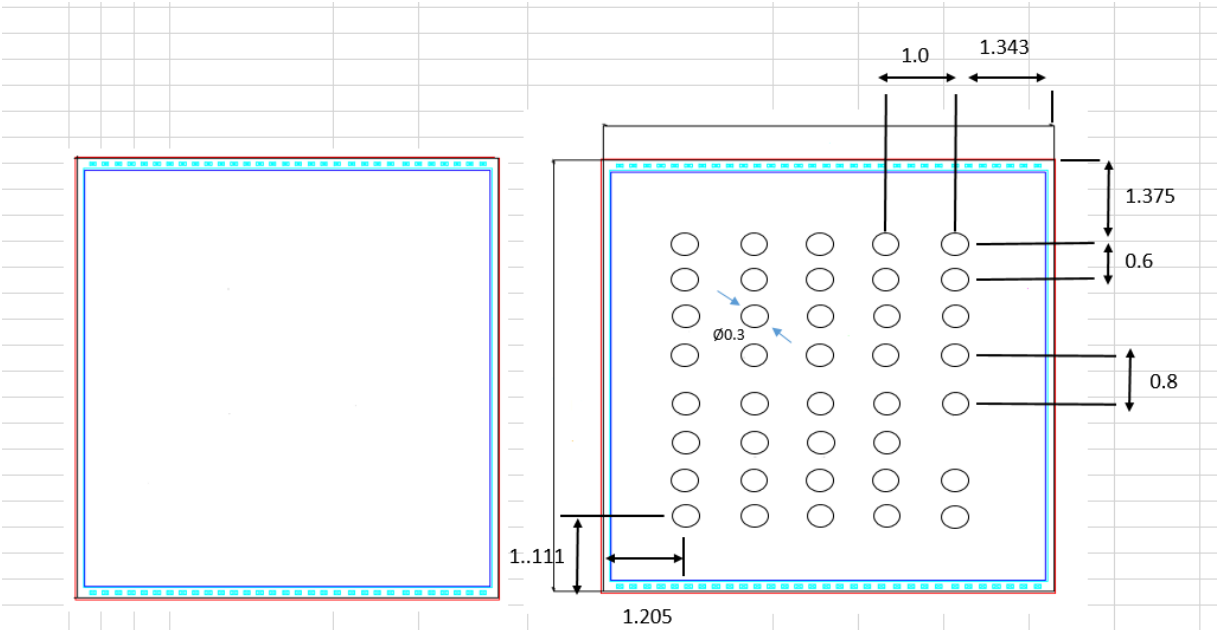
- **Package Outline Dimension**

	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	6.548	6.523	6.573	0.25780	0.25681	0.25878
Package Body Dimension Y	B	6.886	6.861	6.911	0.27110	0.27012	0.27209
Package Height	C	0.820	0.760	0.880	0.03228	0.02992	0.03465
Ball Height	C1	0.160	0.130	0.190	0.00630	0.00512	0.00748
Package Body Thickness	C2	0.660	0.625	0.695	0.02598	0.02461	0.02736
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465	0.01752	0.01673	0.01831
Ball Diameter	D	0.300	0.270	0.330	0.01181	0.01063	0.01299
Total Ball Count	N	39					
Pins pitch X axis	J1	1.000					
Pins pitch Y axis	J2	0.600					
Pins pitch Y' axis	J2'	0.800					
Edge to Pin Center Distance along X	S1	1.343082	1.313082	1.373082	0.052877	0.051696	0.054058
Edge to Pin Center Distance along Y	S2	1.374537	1.344537	1.404537	0.054116	0.052935	0.055297
Edge to Pin Center Distance along X'	S1'	1.204918	1.174918	1.234918	0.047438	0.046257	0.048619
Edge to Pin Center Distance along Y'	S2'	1.111463	1.081463	1.141463	0.043758	0.042577	0.044939

Mechanical Drawing



- **Recommended PCB Layout**



Note:
1. All diemension is millimeter
2. Top view

Rev.	Description	Date
A	New Issue	05/28/17

Title	PS5420LT PCB Layout		
Part Number	PS5420LT		
Package type	CSP 39B		
P number	N/A		
Drawn	YCWu	Scale	mm
Check		Chip Size	N/A
Approve		Rev.	A

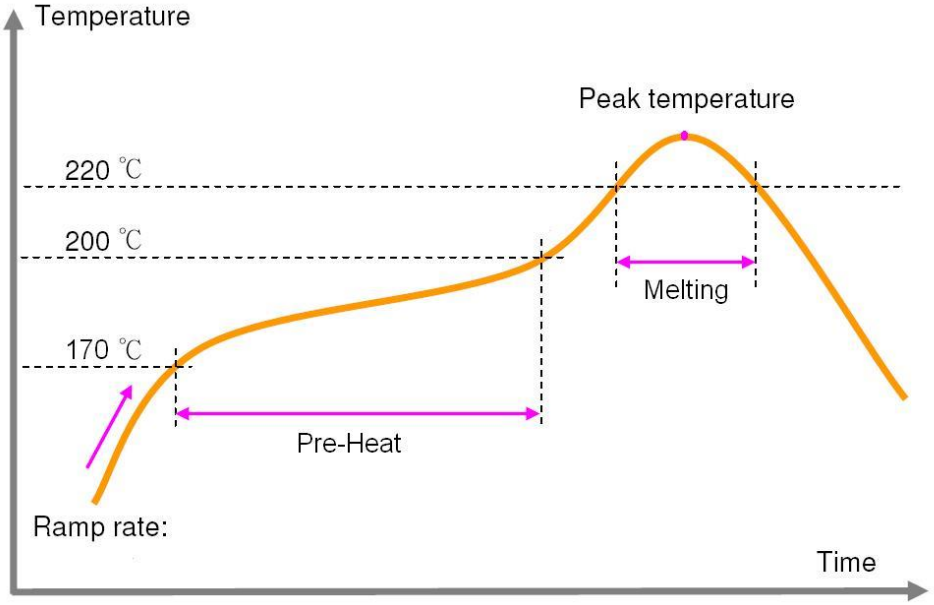
- If use FPC (Flex) board, need add stiffener onto the back-side to enhance the Flex strength.
- Recommended Stiffener type: FR4 or stainless steel or equivalent material.

- **Recommended Guideline for PCB Assembly**

I. Recommended vender and type for Pb-free solder paste
   1 Almit LFM-48W TM-HP
   2 Senju M705-GRN360-K

II. IR Reflow Soldering Profile:

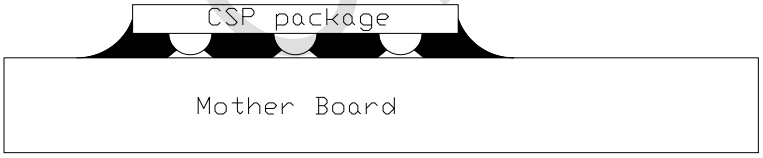
Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure below.



- **Reflow Profile**
  1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
  2. Preheat zone:
     2.1 Temp ramp from 170~ 200 degree C
     2.2 Exposure time: 90 +/- 30 sec
  3. Melting zone:
     3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
     3.2 Peak temperature: 245 degree C.

III. Others

- **Epoxy under-filled process is required post IC mounting process.**



- **Peek tweezers or plastic tweezers is required post IC manual handling for pick and place.**

9. Revision History

Revision	Description	Date
V1.0	First data sheet released	Jan. 18, 2019
V1.1	Update wait time for I2C starts to write in power-up sequence	Jul. 12, 2019
V1.2	Update register LTM_BackLight and LTM_DeHaze description	Sep. 09, 2019
V1.21	Add chapter3: HDR data format Update max. input clock spec. to 28MHz Update "I^2C Bus Timing Specification" - Data hold time. Update max. input clock rise/fall time spec. from 1ns to 3ns	May. 5, 2020
V1.22	Change Company Logo from PrimeSensor to PixArt	Aug, 3, 2021
V1.23	Update Cmd_WOI_HSize description in Chapter 6	Feb, 21, 2023
V1.25	1. Add Note for Absolute Maximum Ratings description in Chapter 2 2. Update R_FrameSyncWait description in Chapter 6 - Not support Frame Sync - Single mode when LTM is enable	Aug, 27, 2023