PS5520: PrimeSensor™ 1/2.5” 5MP HDR CMOS Image Sensor

General Description

The PS5520 is a highly integrated CMOS image sensor that output of 2592x1944 (5MP) pixels with rolling shutter readout. It embedded the new FinePixel™ and HDR sensor technology to perform excellent image quality and single-shot high dynamic range synthesized image output. PS5520 can outputs linear 14-bit or local tone mapped 12-bit or 10-bit raw data through MIPI CSI-2 interface with very low power consumption.

The PS5520 can be programmed to set the exposure time and analog gain for different luminance condition via I²C serial control bus. Embedded HDR image synthesis with local tone mapping to deliver high performance, cost effective and time to market for high resolution HDR application.

Key Features

- 2608 x 1960 active pixels with Bayer-RGB color filter & monochrome array and micro-lens
- Output format:
  - 10-bit Linear RAW
  - 14-bit Linear HDR-RAW
  - 12-bit/10bit LTM HDR-RAW
- Output interface: 4 lane MIPI output, up to 900Mbps
- On-chip column A/D converter
- On-chip manual analog gain control
- Continuous variable frame time & exposure time
- I²C Interface
- Automatic black-level calibration
- Black sun cancellation
- Programmable fast-switch configuration
- Support on-chip HDR combination
- Support LTM (local tone mapping) function
- Support 2x2 monochrome binning
- Support multi-sensor frame synchronization
- Support WOI and subsampling
- Support dummy line & pixel timing
- Support output Hsync at Vsync
- Support 1.7 to 3.3V I/O
- On-chip PLL (input_clock / PLL_m ≥ 1MHz)

Applications

- Surveillance HD-CCTV Camera
- Surveillance IP Camera
- 360 Panoramic Camera
- Sports DV Camera
- Car Video Recorder
- Video Door Phone

Key Parameters

Parameter	Value
Resolution	2592(H) x 1944(V)
Pixel size	2.20um (H) x 2.20um (V)
Color Filter Array	Bayer-RGB, Monochrome
Shutter type	Electronic rolling shutter (ERS)
Optical format	1/2.5-inch (5MP 4:3) 1/2.7-inch (4MP 16:9) 1/2.9-inch (2K2K 1:1)
Max. chief ray angle	12.6 degree
ADC	10-bit
Sensitivity@530nm	Bayer-RGB: 2400 mV/Lux-sec Monochrome:2800mV/Lux-sec
SNRmax	39 dB
Dynamic range	74 dB (Linear) 85 dB (HDR)
Scan mode	Progressive scan
Input clock	Max 28MHz
Pixel clock	Max 165MHz
Max. frame rate	5MP: 2592x1944 HDR @ 30fps 4MP: 2560x1440 HDR @ 30fps 2K2K:1944x1944 HDR @ 30fps 1080p:1920x1080 HDR @ 45fps
Supply voltage	Analog: 3.3 V Digital: 1.2 V I/O: 1.8V to 3.3V
Power consumption	142mw@5Mp30 217mW@ HDR LTM 5Mp30
Operating temperature	-30 °C to 85 °C

Ordering Information

Part Number	Description	Package Type	Packing Type	MOQ
PS5520LT-AA	Bayer-RGB 5MP CMOS Image Sensor	39-Ball CSP	Tray	3,000
PS5520LT-BA	Monochrome 5MP CMOS Image Sensor	39-Ball CSP	Tray	3,000

RoHS compliant

For any additional inquiries, please contact us at https://www.pixart.com

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1.1 Pin Assignment and Signal Description

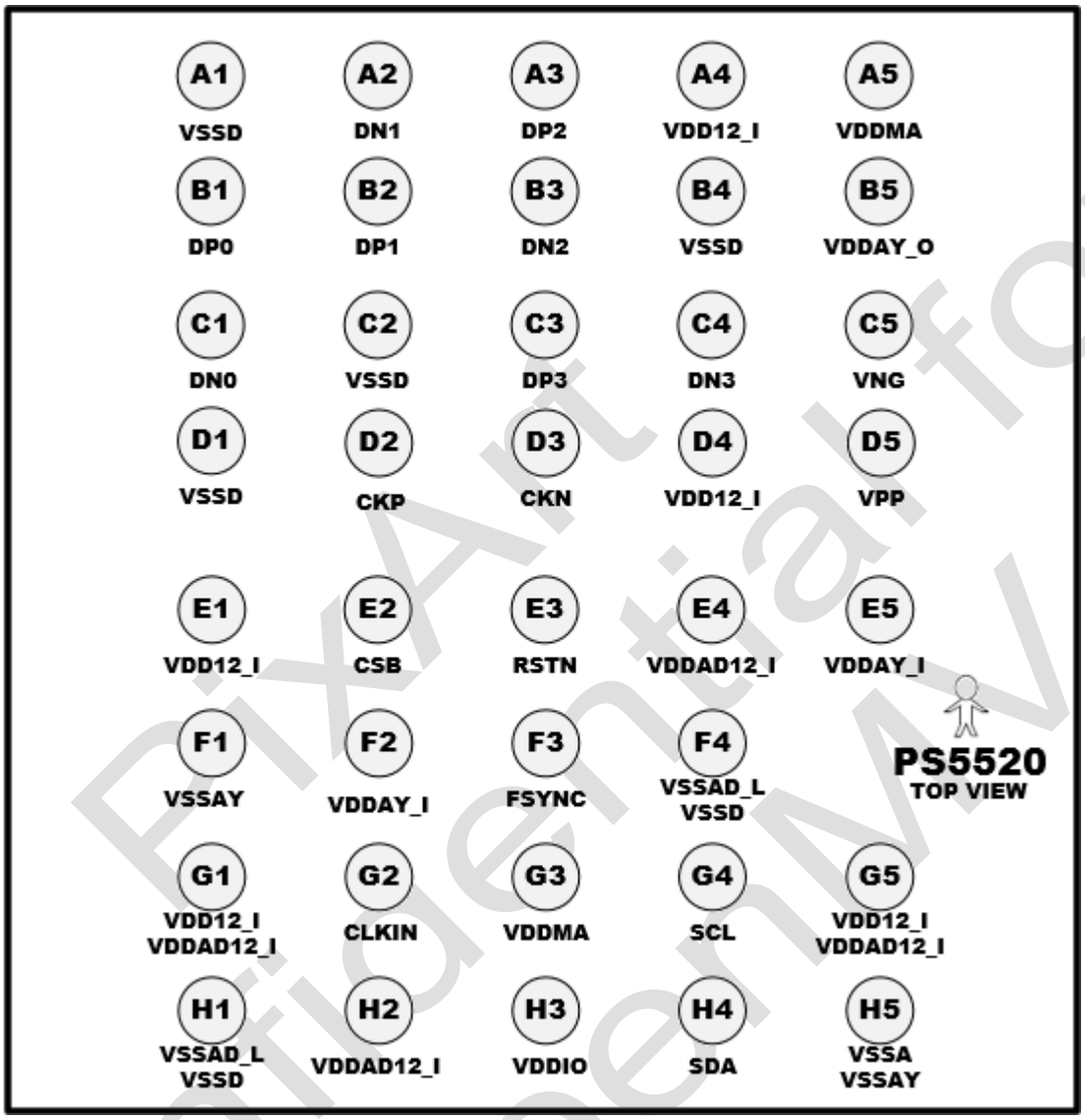


Figure 1. Pin Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
A1	VSSD	GND	GND
A2	DN1	Output	MIPI digital data output_1 negative terminal
A3	DP2	Output	MIPI digital data output_2 positive terminal
A4	VDD12_I	Power	Digital power : 1.2V
A5	VDDMA	Power	Analog power : 3.3V
B1	DP0	Output	MIPI digital data output_0 positive terminal
B2	DP1	Output	MIPI digital data output_1 positive terminal
B3	DN2	Output	MIPI digital data output_2 negative terminal
B4	VSSD	GND	GND
B5	VDDAY_O	Power	VDDAY reference output voltage (2.7 to 3.0V)
C1	DN0	Output	MIPI digital data output_0 negative terminal
C2	VSSD	GND	GND
C3	DP3	Output	MIPI digital data output_3 positive terminal
C4	DN3	Output	MIPI digital data output_3 negative terminal
C5	VNG	Power	Reference voltage
D1	VSSD	GND	GND
D2	CKP	Output	MIPI output clock positive terminal
D3	CKN	Output	MIPI output clock negative terminal
D4	VDD12_I	Power	Digital power : 1.2V
D5	VPP	Power	External voltage for OTP device
E1	VDD12_I	Power	Digital power : 1.2V
E2	CSB	Input	Suspend control, "1":suspend mode, "0": normal mode
E3	RSTN	Input	Reset signal, active low, internal pull high
E4	VDDAD12_I	Power	Analog power input voltage(1.2V)
E5	VDDAY_I	Power	Sensor power input
F1	VSSAY	GND	GND
F2	VDDAY_I	Power	Sensor power input
F3	FSYNC	Input	Frame sync signal
F4	VSSAD_L / VSSD	GND	GND
G1	VDD12_I / VDDAD12_I	Power	Digital power : 1.2V
G2	CLKIN	Input	Master clock input
G3	VDDMA	Power	Analog power : 3.3V
G4	SCL	I/O	I^2C clock, open drain type
G5	VDD12_I / VDDAD12_I	Power	Digital / Analog power : 1.2V
H1	VSSAD_L / VSSD	GND	GND
H2	VDDAD12_I	Power	Analog power input voltage(1.2V)
H3	VDDIO	Power	I/O power : 1.8V to 3.3V
H4	SDA	I/O	I^2C data, open drain type
H5	VSSA/VSSAY	GND	GND

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Operating Temperature	T_A	-30	85	°C	Sensor function works in the operating temperature range. However, the image quality may change at high temperature condition.
Ambient Storage Temperature	T_S	-40	125	°C	
Lead-free Solder Temperature	T_P		245	°C	Surface-mount process Refer to IR Reflow Solder Profile
Supply Voltage	V_{DDA}		4.5	V	
	V_{DDD}		3.0	V	
	V_{DDIO}		4.5	V	
All I/O Voltage	V_{IO}	-0.3	V_{DDIO} + 0.3	V	with respect to ground
ESD	ESDHBM		2	kV	Class 2 on all pins, as per human body model JESD22-A114E with 15 sec zap interval.

Notes:

1. At ambient temperature = 25°C.
2. Maximum Ratings are the maximum parameter values that can damage the device when exceeding this limit.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not recommended.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_J	0	-	70	°C	
Analog DC Supply Voltage	V_{DDA}	3.14	3.3	3.47	V	Includes ripples
Digital DC Supply Voltage	V_{DDD}	1.14	1.2	1.3	V	Includes ripples
I/O DC Supply Voltage	V_{DDIO}	1.71		3.47	V	Includes ripples

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

2.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Current – Analog	I_{DDA}		16.7		mA	4-lane MIPI
Operating Current – Digital	I_{DDD}		134		mA	4-lane MIPI
Operating Current – I/O	I_{DDIO}		1		mA	4-lane MIPI
I/O Input High Voltage	V_{IH}	0.7 x V_{DDIO}	-	-	V	
I/O Input Low Voltage	V_{IL}	-	-	0.3 x V_{DDIO}	V	
I/O Output High Voltage	V_{OH}	0.9 x V_{DDIO}	-	-	V	
I/O Output Low Voltage	V_{OL}	-	-	0.1 x V_{DDIO}	V	

Note: The power consumption is measured with 4X analog gain in HDR LTM 5MP 30fps at T_J = 25°C.

2.4 AC Characteristics

Table 5. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
System clock frequency	fsysclk	10	27	28	MHz	
System clock duty cycle	tsysclk_dc	45		55	%	
Clock Input Rise/Fall Time	-			3	ns	20% ~ 80% VDDIO

2.5 Sensor Characteristics

Table 6. Sensor Specifications

Description	Symbol	Min.	Typ.	Max.	Unit	Condition
Sensitivity@530nm	SEN		2400		mV/Lux-Sec	
MAX Signal to Noise Ratio	SNR		39		dB	
Dynamic Range	DR		85		dB	

3.0 Mechanical Specifications

3.1 Mechanical Dimension

Table 7. Package Outline Dimensions

Parameters	Symbol	Unit: mm			Unit: inches		
		Nominal	Min.	Max.	Nominal	Min.	Max.
Package Body Dimension X	A	6.548	6.523	6.573	0.25780	0.25661	0.25878
Package Body Dimension Y	B	6.886	6.861	6.911	0.27110	0.27012	0.27209
Package Height	C	0.820	0.760	0.880	0.03228	0.02992	0.03465
Ball Height	C1	0.160	0.130	0.190	0.00630	0.00512	0.00748
Package Body Thickness	C2	0.660	0.625	0.695	0.2598	0.02461	0.02736
Thickness of Glass surface to wafer	C3	0.445	0.425	0.465	0.01752	0.01673	0.01831
Ball Diameter	D	0.300	0.270	0.330	0.01181	0.01063	0.01299
Total Ball Count	N	39					
Pin Pitch X axis	J1	1.000					
Pin Pitch Y axis	J2	0.600					
Pin Pitch Y’ axis	J2’	0.800					
Edge to Pin Center Distance along X	S1	1.343082	1.313082	1.373082	0.052877	0.051696	0.054058
Edge to Pin Center Distance along Y	S2	1.374537	1.344537	1.404537	0.054116	0.052935	0.055297
Edge to Pin Center Distance along X’	S1’	1.204918	1.174918	1.234918	0.047438	0.046257	0.048619
Edge to Pin Center Distance along Y’	S2’	1.111463	1.081463	1.141463	0.043758	0.042577	0.044939

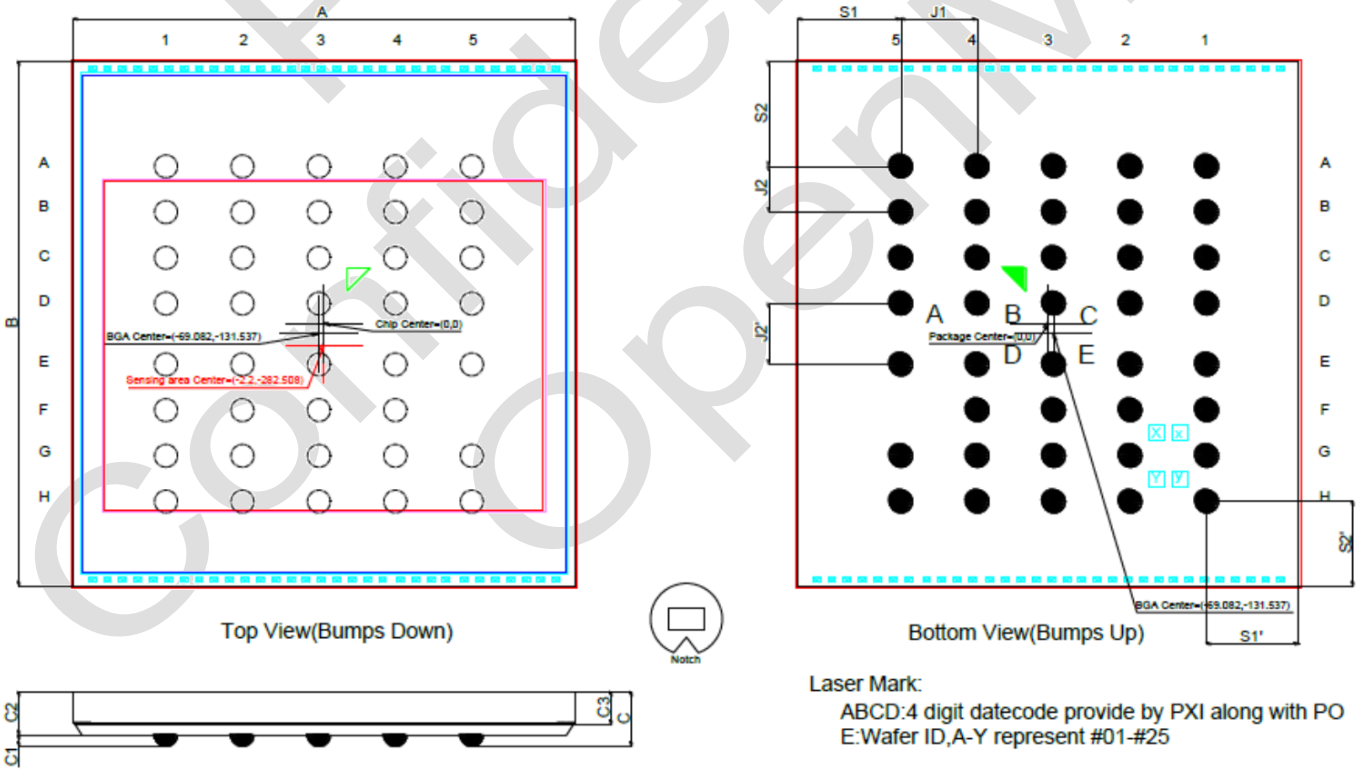


Figure 2. Package Outline Diagram

3.2 Package Marking Identification

Refer to Figure 2 above for the code marking location on the device package.

Table 8. Code Identification

Marking	Description
ABCD	4 digit Datecode
E	Wafer ID, A-Y represent #01 - #25

4.0 Design References

4.1 General Reference Schematic

Reference circuit for multi power system

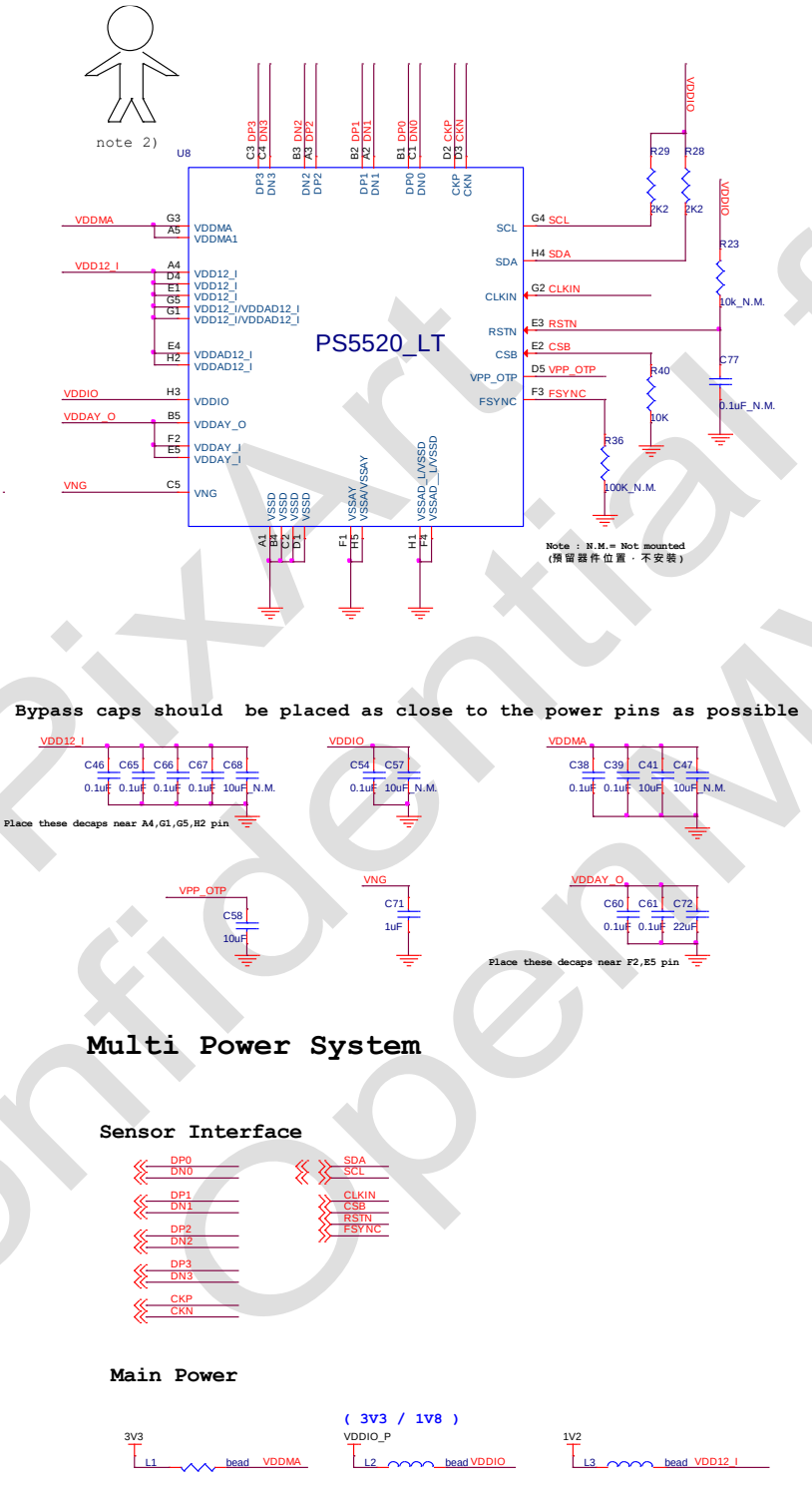


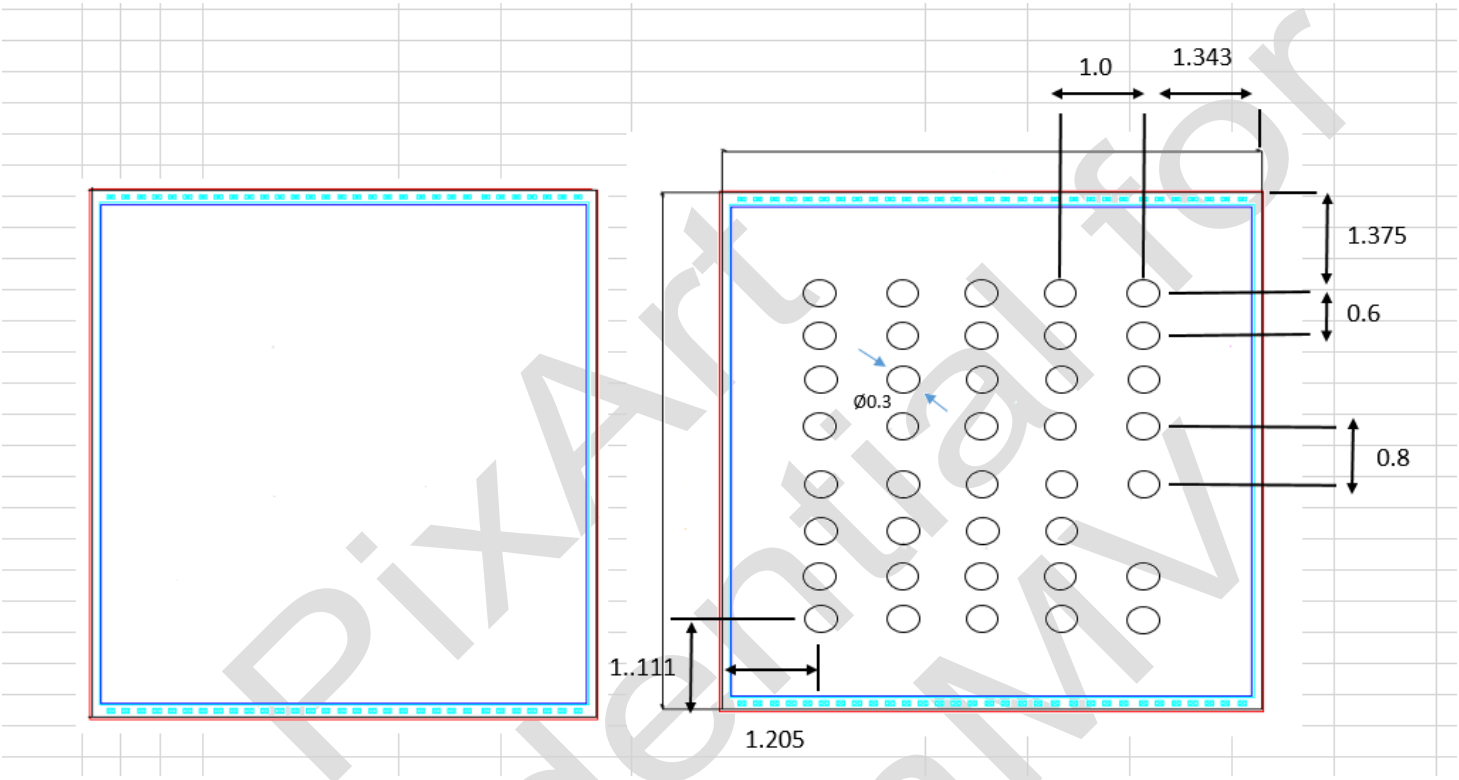
Figure 3. Reference Application Circuit for Power Configuration

4.2 PCB Layout Design Guide

4.2.1 Design Rules

- If use FPC (Flex) board, need add stiffener onto the back-side to enhance the Flex strength.
- Recommended Stiffener type: FR4 or stainless steel or equivalent material.

4.2.2 Recommended PCB Footprint



Note:
1. All diemension is millimeter
2. Top view

Rev.	Description	Date
A	New Issue	05/28/17

Title	PS5520LT PCB Layout		
Part Number	PS5520LT		
Package type	CSP 39B		
P number	N/A		
Drawn	YCWu	Scale	mm
Check		Chip Size	N/A
Approve		Rev.	A

Figure 4. Recommended Chip Orientation, Mechanical Cutouts and Spacing (Top View)

4.3 Assembly Guide

4.3.1 IR Reflow Solder Profile/Reflow Profile

Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is showed below

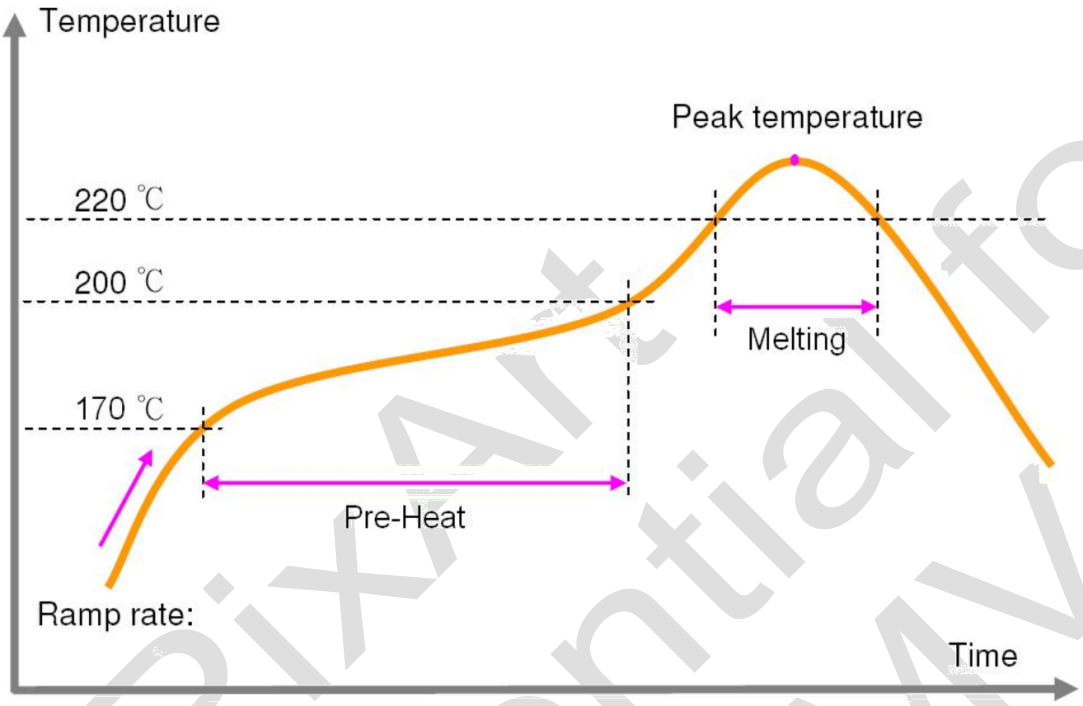


Figure 5. IR Reflow Solder Profile

Table 9. Reflow Profile

Parameter	Symbol	Min	Max	Unit	Notes
Average Ramp-up Rate	T_{RAMP}	1.5	2.5	°C/sec	From 30°C to preheat zone
Pre-Heat Zone Temperature	T_{PRE}	170	200	°C	
Pre-Heat Zone Exposure Time	t_S	60	120	sec	90±30 sec
Melting duration	t_{MELT}	30	50	sec	T_{MELT} ≥220 °C
Melting Temperature	T_{MELT}	220	245	°C	

Note: Almit LFM-48W TM-HP and Senju M705-GRN360-K are the recommended Pb-free Solder Paste.

4.3.2 Under-filled Process

The epoxy under-filled process is required post IC mounting process.

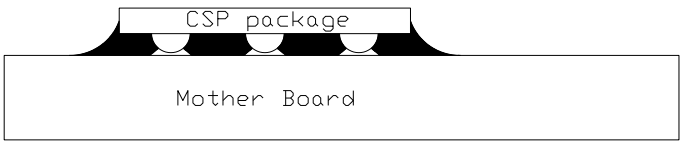


Figure 6. Under-Filled Process

4.3.3 Handling Precaution for the Prevention of ESD

Proper handling precaution procedures must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices. The following basic rules must be obeyed.

4.3.3.1 Working Environment

1. Equalize potentials of terminals when transporting or storing the devices
2. Equalize the potentials of electric device, work table and operator’s body that come in contact with the IC.
3. Prepare an environment that does not generate static electricity.

4.3.3.2 Operator

1. The operator should wear wrist straps and must maintain electric contact with bare skin.
2. Wear cotton or antistatic-treated materials clothes and gloves.
3. When a conductive floor mat is used, the operator must be worn conductive shoes.
4. Do not touch the IC’s leads at any time. Touch only the body of IC’s when holding it.

4.3.3.3 Equipment and Tools

1. Any electrical equipment and tools placed on top of the work table must be grounded and isolated from the surface of work table itself.
2. The surface of work table must be using conductive material or conductive mat.

4.3.3.4 Transporting, Storing and Packing

Use the original packing and conductive or shielding bag to store the package

4.3.3.5 Soldering Operation

1. Use a soldering iron with a grounding wire.
2. When performing manual soldering operation, the operator should wear wrist strap.
3. Do not use the de-soldering pump to remove the chip from the PCB board. Use a solder-wick or equivalent.

4.3.4 Others Handling

Peek tweezers or plastic tweezers is required post IC manual handling for pick and place.

Figure 7. Tweezers

5.0 Power Sequences

5.1 Power-Up Sequence

The recommended power-up sequence for the PS5520 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn on VDDD12 power supply.
2. After 100µs (t0), VDDMA, VDDMA_D and VDDIO power supply simultaneously.
3. After 100µs (t1), RESET_N must go low.
4. RESET_N active low for at least 1ms (t3).
5. After 100µs (t2), enable CLKIN.
6. Wait at least 61440*MCLK (t4), I^2C starts to write commands.

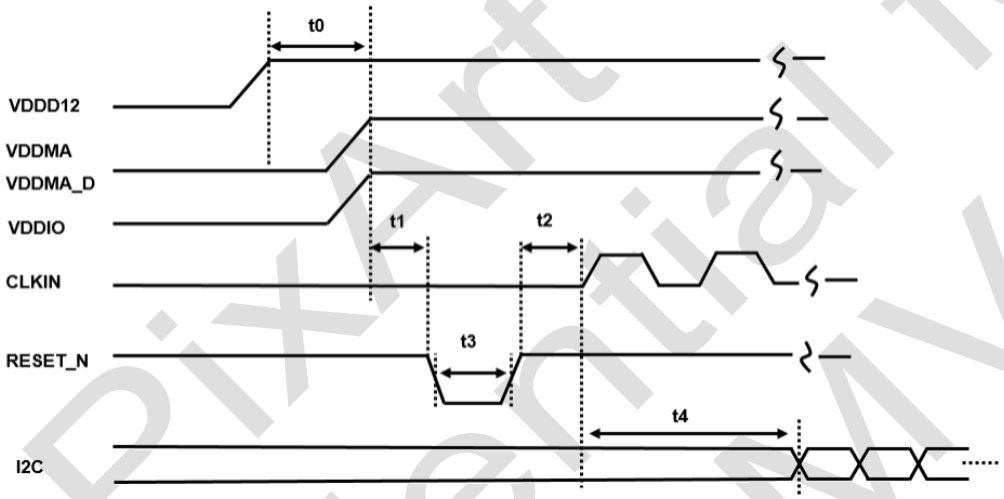


Figure 8. Power-Up Timing Diagram

5.2 Power-Down Sequence

The recommended power-down sequence for the PS5520 is shown as the following figure. The available power supplies must have the separation specified below.

1. Turn off VDDMA, VDDMA_D and VDDIO power supply simultaneously.
2. After 100µs (t0), turn off VDDD12 power supply.

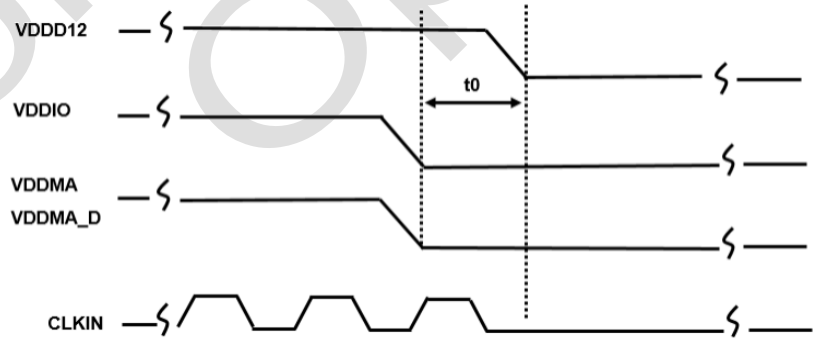


Figure 9. Power-Down Timing Diagram

Note: This Power-Down Sequence could be ignored if there is a RESET_N signal toggle in Power-Up Sequence (ie. RESET_N active low for at least 1ms (t3)).

5.3 CSB Suspend Sequence

The recommended CSB Suspend sequence for the PS5520 is shown as the following figure. The available power supplies must have the separation specified below.

ON → OFF :

1. I²C must write commands to turn off internal clock for PS5520 .
2. After 100µs (t0), CSB must go high
3. After 100µs (t1), turn off CLKIN.

OFF → ON :

1. Turn on CLKIN.
2. After 100µs (t2), CSB must go low.
3. Wait at least 1ms (t3) for internal clock stable.
4. I²C starts to write commands.

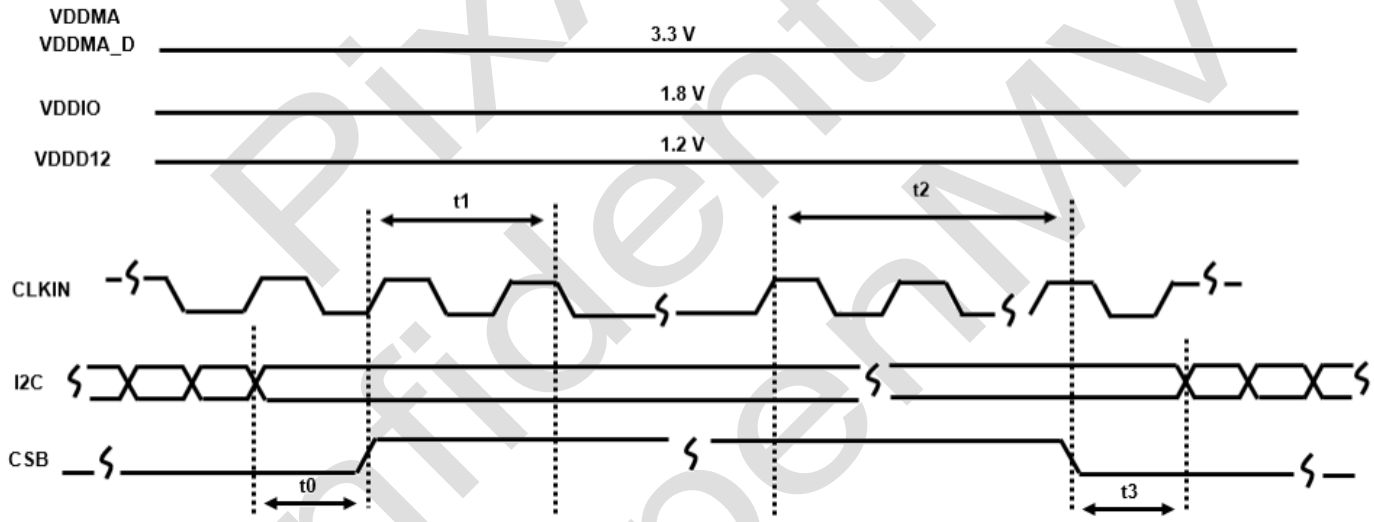


Figure 10. CSB Suspend Timing Diagram

6.0 I²C Bus

PS5520 supports I²C bus transfer protocol and acts as slave device. The 7-bits unique slave address is “1001000” and supports receiving / transmitting speed as maximum 400 kHz.

6.1 Signal Description

Only two wires, SCD and SCL carry information between the devices connected to the I²C bus. Normally both SDA and SCL lines are open collector structure

Table 10. I²C Signals Description

Signal Name	Label	Type	Reset Status	Description
Serial Clock	SCL	Input	Input (Floating)	The SCL is the I²C serial clock pin and driven by the host where is to synchronize the serial data transmission. An external pull-up resistor is required.
Serial Data	SDA	I/O	Input (Floating)	The SDA signal is data line to read from or write to the chip. An external pull-up resistor is required.

6.2 Operation Definition

6.2.1 START and STOP conditions

All transactions begin with a START (S) and are terminated by a STOP (P). START and STOP conditions are always generated by the host.

- START condition: A HIGH to LOW transition on the SDA line while SCL is HIGH.
- STOP condition: A LOW to HIGH transition on the SDA line while SCL is HIGH.

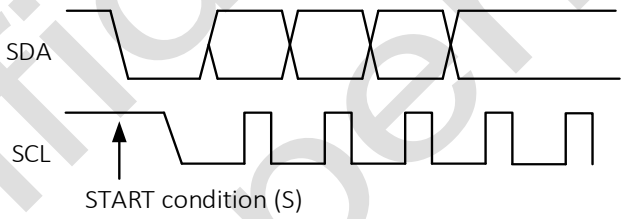


Figure 11. START Condition

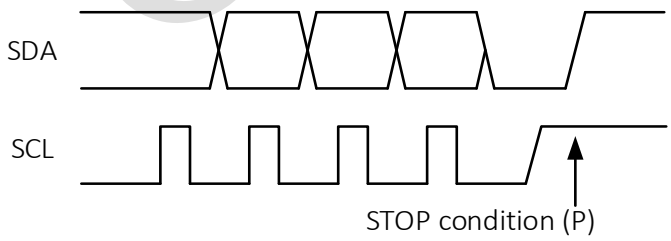


Figure 12. STOP Condition

6.2.2 Valid Data

The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte.

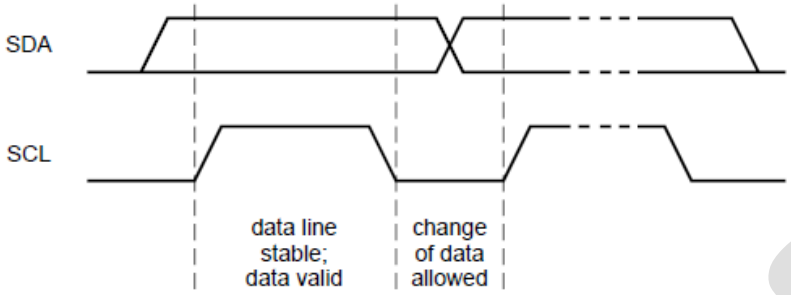


Figure 13. Valid Data

6.2.3 Acknowledge

Both the master and slave can transmit and receive data from the bus.

The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

6.3 Data Transfer Format

6.3.1 Master transmits data to salve in write cycle

- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 : Read cycle, RW = 0 : Write cycle.
- SUBADDRESS : The address values of PS5520 internal control registers. (Please refer to PS5520 register description)

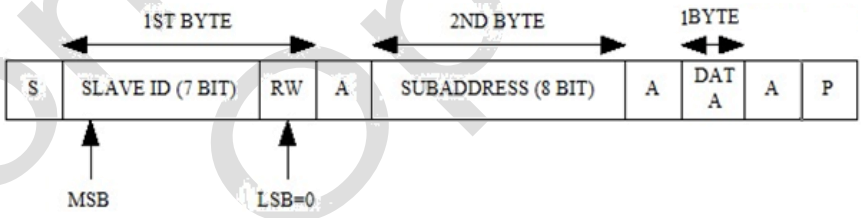


Figure 14. Master-transmitter transmits to slave-receiver

During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PS5520) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the PS5520 acknowledgment, the master places the 8 bits data on SDA line and transmit to PS5520 control register (address was assigned by 2nd byte). After PS5520 issues acknowledgment, the master can generate a stop condition to end of this write cycle. Every control registers value inside PS5520 can be programming via this way.

6.3.2 Slave transmits data to master in read cycle

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.

Note: There is no acknowledgment from master after last byte read.

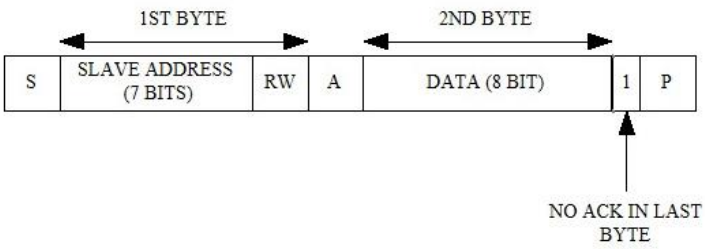


Figure 15. Slave-transmitter transmits to master-receiver

During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PS5520. The 8 bits data was read from PS5520 internal control register that address was assigned by previous write cycle. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PS5520) must releases SDA line to master to generate STOP condition.

6.3.3 I²C Timing Specification

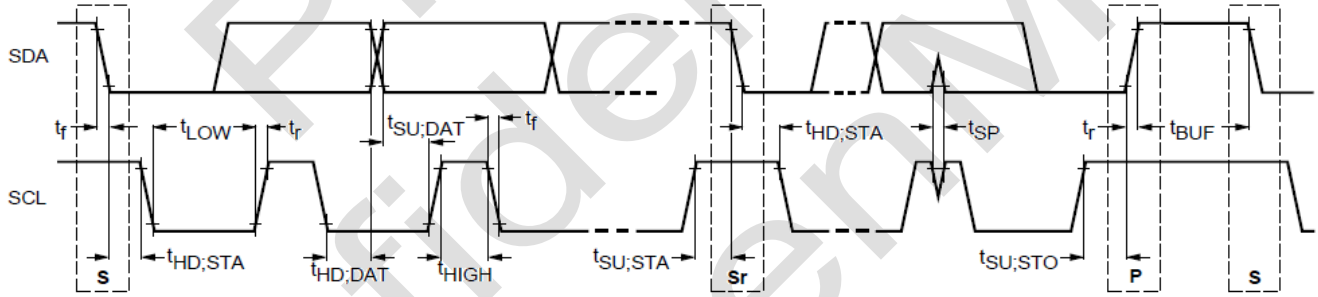


Figure 16. I²C Timing Diagram for F/S mode devices on the I²C-bus

Table 11. I²C Timing Specifications

Parameters	Symbol	Standard Mode		Fast Mode		Unit	Notes
		Min.	Max.	Min.	Max.		
SCL clock frequency	f_{scl}	10	100	0	400	KHz	
Hold time (repeated) Start condition. After this period, the first clock pulse is generated	$t_{HD:STA}$	4.0	-	0.6	-	µs	
Low period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs	
High period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs	
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs	
Data hold time. For I²C-bus device	$t_{HD;DAT}$	0	3.45	0	0.9	µs	
Data set-up time	$t_{SU;DAT}$	250	-	100	-	ns	
Rise time of both SDA and SCL signals	t_r	-	1000	-	300	ns	It depends on the “high” period time of SCL
Fall time of both SDA and SCL signals	t_f	-	300	-	300	ns	
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs	
Bus free time between a STOP and START	t_{BUF}	4.7	-	1.3	-	µs	
Capacitive load for each bus line	C_b	-	400	-	400	pF	
Noise margin at LOW level for each connected device	V_{nL}	0.1xVDD	-		0.1xVDD	V	Including hysteresis
Noise margin at HIGH level for each connected device	V_{nH}	0.2xVDD	-		0.2xVDD	V	Including hysteresis

7.0 HDR Data Format

The sensor perform single exposure with dual sensitivity image data and on-chip combine dual image data line-by-line as a linear high dynamic range 14bit data. Then sensor perform local tone mapping from higher data bits (14bits) to lower data bits (12bit) for suppressing data range and enhancing local contrast during the process.

Finally, the sensor output tone mapped RAW 12bit or 10bit data via MIPI interface. Backend chip received the tone mapped RAW data without complex HDR timing and combination while using staged HDR sensor.

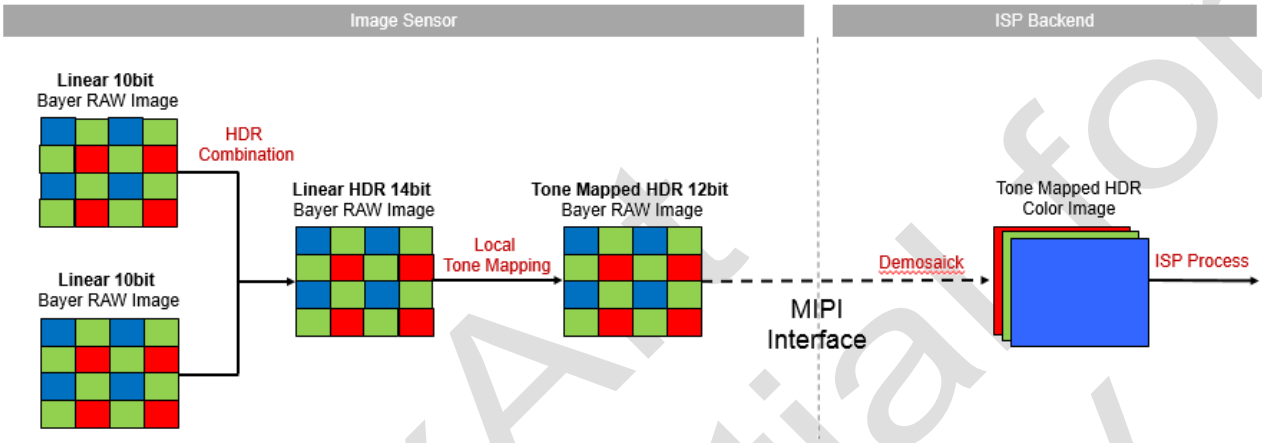


Figure 17. HDR Data

PS5520 support linear or HDR output mode, the available output format summary as following table:

Table 12. Output Formats

Output Format		Output I/F		Description
		DVP	MIPI	
Linear	RAW10	--	V	Linear 10bit RAW data
Linear HDR	RAW14	--	V	Linear DCG Combined HDR 14bit RAW data
Linear HDR	RAW12	--	V	Linear DCG Combined HDR 12bit RAW data
HDR + LTM	RAW12	--	V	12bit HDR+LTM RAW data
HDR + LTM	RAW10	--	V	10bit HDR+LTM RAW data

8.0 Registers

8.1 Register Map

Bank	Address		Bit	Name	Access	Description
	Hex	Dec				
0	00	00	[7:0]	PartID[15:8]	R	Sensor ID
0	01	01	[7:0]	PartID[7:0]	R	Sensor ID
0	02	02	[3:0]	VersionID[3:0]	R	Sensor ID
0	03	03	[3:0]	SubID[3:0]	R	Sensor ID
0	11	17	[7]	Cmd_GatedAllClk	R/W	Clock Gated Control (1: Gate Clock)
1	05	05	[3]	Cmd_10_TriState	R/W	TriState IO of PxData[1:0]
			[2]	Cmd_Sw_PwrDn	R/W	Power-Down Control
			[1]	Cmd_Sw_TriState	R/W	TriState IO of PxData, Hsync, Vsync, and Pxclk
1	09	09	[0]	UpdateFlag	R/W	Exposure & Gain Update Control (Write 0x01)
1	0A	10	[7:0]	Cmd_Lpf [15:8]	R/W	Line per frame = Cmd_Lpf+ 1
1	0B	11	[7:0]	Cmd_Lpf [7:0]	R/W	Line per frame = Cmd_Lpf+ 1
1	0C	12	[7:0]	Cmd_OffNy1[15:8]	R/W	Exposure Control
1	0D	13	[7:0]	Cmd_OffNy1[7:0]	R/W	Exposure Control
1	0E	14	[3:0]	Cmd_OffNe1[11:8]	R/W	Exposure Control
1	0F	15	[7:0]	Cmd_OffNe1[7:0]	R/W	Exposure Control
1	1B	27	[7]	Cmd_Hflip	R/W	Horizontal Flip
			[6:5]	Cmd_Askip_H[1:0]	R/W	Horizontal Skip
			[3:0]	Cmd_Hsize_e1[11:8]	R/W	Raw Image Horizontal Size
1	1C	28	[7:0]	Cmd_Hsize_e1[7:0]	R/W	Raw Image Horizontal Size
1	1D	29	[7]	Cmd_Vflip	R/W	Vertical Flip
			[6:5]	Cmd_Askip_V[1:0]	R/W	Vertical Skip
			[2:0]	Cmd_Vsize[10:8]	R/W	Raw Image Vertical Size
1	1E	30	[7:0]	Cmd_Vsize[7:0]	R/W	Raw Image Vertical Size
1	1F	31	[2:0]	Cmd_Vstart[10:8]	R/W	Raw Image Vertical Offset
1	20	32	[7:0]	Cmd_VStart[7:0]	R/W	Raw Image Vertical Offset
1	27	39	[4:0]	Cmd_LineTime [12:8]	R/W	Line Time = Cmd_LineTime* 0.5 clock cycles
1	28	40	[7:0]	Cmd_LineTime [7:0]	R/W	Line Time = Cmd_LineTime* 0.5 clock cycles
1	80	128	[7:0]	Cmd_DG_gain_idx[7:0]	R/W	Sensor Digital Gain index
1	83	131	[7:0]	Cmd_gain_idx[7:0]	R/W	Sensor Analog Gain index
1	8F	143	[2]	Cmd_ImgSyn_Mode	R/W	HDR Image Mode : 0: nonHDR-mode 1: HDR-mode
			[0]	Cmd_ImgSyn_EnH	R/W	HDR Image Synthesis Enable
1	90	144	[0]	Cmd_Adc_sample_posedge	R/W	ADC sample timing control
1	92	146	[4:0]	R_ISP_TestMode[4:0]	R/W	Test Image Control

Bank	Address		Bit	Name	Access	Description
	Hex	Dec				
1	93	147	[7:0]	R_ISP_TestValueLo[7:0]	R/W	Test Image Control
1	94	148	[7:0]	R_ISP_TestValueHi[7:0]	R/W	Test Image Control
1	97	151	[0]	Cmd_Pga_D1frm	R/W	PGA Gain auto-delay one frame
1	A3	163	[4]	Cmd_WOI_VOffset_sign	R/W	Vertical offset of output image
			[2:0]	Cmd_WOI_VOffset[10:8]	R/W	Vertical offset of output image
1	A4	164	[7:0]	Cmd_WOI_VOffset[7:0]	R/W	Vertical offset of output image
1	A5	165	[2:0]	Cmd_WOI_VSize[10:8]	R/W	Vertical size of output image
1	A6	166	[7:0]	Cmd_WOI_VSize[7:0]	R/W	Vertical size of output image
1	A7	167	[4]	Cmd_WOI_HOffset_sign	R/W	Horizontal offset of output image
			[3:0]	Cmd_WOI_HOffset[11:8]	R/W	Horizontal offset of output image
1	A8	168	[7:0]	Cmd_WOI_HOffset[7:0]	R/W	Horizontal offset of output image
1	A9	169	[3:0]	Cmd_WOI_HSize[11:8]	R/W	Horizontal size of output image
1	AA	170	[7:0]	Cmd_WOI_HSize[7:0]	R/W	Horizontal size of output image
1	AB	171	[3:0]	Cmd_Np[3:0]	R/W	Frequency eliminate control
1	F1	241	[5:0]	T_spll_predivider[5:0]	R/W	PLL Control
1	F2	242	[5:0]	T_spll_postdivider [5:0]	R/W	PLL Control
1	F5	245	[4]	T_spll_enh	R/W	PLL Control
			[3]	T_spll_div2_enH	R/W	PLL Control
			[1:0]	T_spll_modedivider [1:0]	R/W	PLL Control
2	10	16	[1]	R_FrameSyncWait	R/W	0: Continue mode - Continuous output after one pulse trigger signal. 1: Single mode (Not support LTM function) - One frame output after one pulse trigger signal.
			[0]	R_FrameSyncMode	R/W	0: Normal Mode. 1: Frame Sync Mode.
2	2E	46	[4:0]	Cmd_ABC_LockRange2_UB[4:0]	R/W	If BLC diff value > Cmd_ABC_LockRange2_UB , then BLC update for HGain channel
2	33	51	[4:0]	Cmd_ABC_LockRange1_UB[4:0]	R/W	If BLC diff value > Cmd_ABC_LockRange1_UB, then BLC update for LGain channel
2	3A	58	[2]	Cmd_ABC_EnH	R/W	BLC function enable
2	46	70	[7]	Cmd_DigDac_B_Sign	R/W	Black Level Offset for B Channel
			[2:0]	Cmd_DigDac_B_Offset[10:8]	R/W	Black Level Offset for B Channel
2	47	71	[7:0]	Cmd_DigDac_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	48	72	[7]	Cmd_DigDac_Gb_Sign	R/W	Black Level Offset for Gb Channel
			[2:0]	Cmd_DigDac_Gb_Offset[10:8]	R/W	Black Level Offset for Gb Channel
2	49	73	[7:0]	Cmd_DigDac_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	4A	74	[7]	Cmd_DigDac_Gr_Sign	R/W	Black Level Offset for Gr Channel

Bank	Address		Bit	Name	Access	Description
	Hex	Dec				
			[2:0]	Cmd_DigDac_Gr_Offset[10:8]	R/W	Black Level Offset for Gr Channel
2	4B	75	[7:0]	Cmd_DigDac_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	4C	76	[7]	Cmd_DigDac_R_Sign	R/W	Black Level Offset for R Channel
			[2:0]	Cmd_DigDac_R_Offset[10:8]	R/W	Black Level Offset for R Channel
2	4D	77	[7:0]	Cmd_DigDac_R_Offset[7:0]	R/W	Black Level Offset for R Channel
2	A0	160	[7]	Cmd_DigDac2_B_Sign	R/W	Black Level Offset for B Channel
			[2:0]	Cmd_DigDac2_B_Offset[10:8]	R/W	Black Level Offset for B Channel
2	A1	161	[7:0]	Cmd_DigDac2_B_Offset[7:0]	R/W	Black Level Offset for B Channel
2	A2	162	[7]	Cmd_DigDac2_Gb_Sign	R/W	Black Level Offset for Gb Channel
			[2:0]	Cmd_DigDac2_Gb_Offset[10:8]	R/W	Black Level Offset for Gb Channel
2	A3	163	[7:0]	Cmd_DigDac2_Gb_Offset[7:0]	R/W	Black Level Offset for Gb Channel
2	A4	164	[7]	Cmd_DigDac2_Gr_Sign	R/W	Black Level Offset for Gr Channel
			[2:0]	Cmd_DigDac2_Gr_Offset[10:8]	R/W	Black Level Offset for Gr Channel
2	A5	165	[7:0]	Cmd_DigDac2_Gr_Offset[7:0]	R/W	Black Level Offset for Gr Channel
2	A6	166	[7]	Cmd_DigDac2_R_Sign	R/W	Black Level Offset for R Channel
			[2:0]	Cmd_DigDac2_R_Offset[10:8]	R/W	Black Level Offset for R Channel
2	A7	167	[7:0]	Cmd_DigDac2_R_Offset[7:0]	R/W	Black Level Offset for R Channel
2	ED	237	[0]	UpdateFlag	R/W	ABC Update Control (Write 0x01)
5	06	6	[2:0]	R_Data_Format[2:0]	R/W	Data Format type : 3 for RAW8 4 for RAW10 5 for RAW12 6 for RAW14
5	0F	15	[0]	R_CSI2_Enable	R/W	0: Stop MIPI signal output 1: Start MIPI signal output
5	10	16	[2:0]	R_CsiTx_LaneN[2:0]	R/W	1 for 1_Lane application 2 for 2_Lane application 4 for 4_Lane application
5	40	64	[5:0]	T_pll_predivider[5:0]	R/W	MIPI pll clock divider
5	41	65	[5:0]	T_pll_postdivider[5:0]	R/W	MIPI pll clock scalar
5	43	67	[3]	T_pll_div2_EnH	R/W	MIPI pll clock divider2 selection
5	44	68	[0]	T_pll_enh	R/W	MIPI pll Control
5	B0	176	[0]	R_MIPI_Skip_Line_SP_EnH	R/W	MIPI data lane if skip LS/LE short packet
5	ED	237	[0]	UpdateFlag	R/W	MIPI Update Control (Write 0x01)
6	45	69	[6]	R_Temp_manual_En	R/W	Temp_save manual mode enable
			[2:0]	R_Temp_manual[10:8]	R/W	Temp_save manual value
6	46	70	[7:0]	R_Temp_manual[7:0]	R/W	Temp_save manual value
6	98	152	[0]	R_LTM_EnH	R/W	LTM function enable
6	99	153	[7:0]	Cmd_LTM_inverse[7:0]	R/W	LTM inverse value base on ISP Gamma curve (AE function)
6	9A	154	[3:0]	Cmd_LTM_contrast[3:0]	R/W	LTM contrast strength

Bank	Address		Bit	Name	Access	Description
	Hex	Dec				
6	9A	154	[3:0]	Cmd_LTM_brighteness[3:0]	R/W	LTM brightness strength
6	9E	158	[4:0]	Cmd_LTM_limit[4:0]	R/W	LTM strength limitation
6	F1	241	[0]	UpdateFlag	R/W	LTM Update Control (Write 0x01)

Document Revision History

Revision Number	Date	Description
V1.0	Nov. 29, 2018	Formal data sheet released
V1.1	May 02, 2019	Update ordering information: PS5520LT-AA Update wait time for I^2C starts to write in power-up sequence
V1.11	May 5, 2020	Add chapter3: HDR data format Update max. input clock spec. to 28MHz Update “I^2C Bus Timing Specification” - Data hold time. Update max. input clock rise/fall time spec. from 1ns to 3ns
V1.12	Oct 23, 2020	Change to PixArt datasheet
V1.13	Feb 22, 2021	Input clock MAX 28MHz
V1.2	Dec 13, 2022	Add “Part Number - PS5520LT-BA” for monochrome sample
V1.21	Jan 4, 2023	Update “DC Electrical Specifications” test condition in Table 4
V1.22	Mar 8, 2023	Update I2C word
V1.25	Aug, 27, 2023	1. Update Note for “Absolute Maximum Ratings” in Table 2 2. Update R_FrameSyncWait description in Chapter 8 - Not support Frame Sync - Single mode when LTM is enable