life.augmented

# STM32N657xx

## Arm® Cortex®-M55, ST Neural-ART Accelerator,H264 encoder, Neo-Chrom 2.5D GPU, 4.2 Mbyte-contiguous SRAM

**Preliminary Data brief**

## Features

- Includes ST state-of-the-art patented technology

### Core

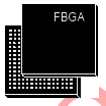
- Arm® 32-bit Cortex®-M55, 3360 CoreMark®, frequency up to 800 MHz, 1280 DMIPS, 32-Kbyte ICACHE, 32-Kbyte DCACHE
- Arm® MVE (M-Profile vector extension)
- Arm® Helium™ technology
- Arm® TrustZone® MPU, NVIC
- Single and half-precision floating point unit

### Neural processing unit

- ST Neural-ART Accelerator, frequency up to 1 GHz, 600 Gops, 288 MAC/cycle
- Specialized hardware units for DNN (deep-neural network) inference functions
- Flexible dedicated stream processing engine
- Real-time encryption/decryption
- On-the-fly weight decompression

### Memories

- 4.2-Mbyte contiguous SRAM
- 64-Kbyte TCM (tightly-coupled memory) RAM with ECC for critical real-time data + 128-Kbyte instruction TCM RAM with ECC for critical real-time routines
- 8-Kbyte backup SRAM active in $V_{BAT}$ mode
- Flexible external memory controller with cypher engine supporting up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- XSPIM 8-bit configuration with cypher engine: up to 400 Mbit/s at 200 MHz
- XSPIM 16-bit configuration with cypher engine: up to 800 Mbit/s at 200 MHz




VFBGA142 (8 x 8 mm) pitch 0.5 mm
VFBGA169 (6 x 6 mm) pitch 0.4 mm
VFBGA178 (12 x 12 mm) pitch 0.8 mm
VFBGA198 (10 x 10 mm) pitch 0.65 mm
VFBGA223 (10 x 10 mm) pitch 0.5 mm
VFBGA264 (14 x 14 mm) pitch 0.8 mm

### Graphics

- Neo-Chrom 2.5D GPU: scaling, rotation, alpha blending, texture mapping, perspective transformation
- Chrom-ART Accelerator (DMA2D)
- Hardware JPEG codec with MJPEG
- LCD-TFT controller up to XGA resolution

### Video

- Parallel and 2-lane CSI-2 camera interfaces
- ISP (image signal processor) with three parallel pipes on same input stream: bad pixel, decimation, black level, exposure, de-mosaic, column conversion, contrast, crop, downsize, ROI, gamma, YUV convention, pixel packer
- H264 video encoding acceleration: baseline profile, main profile, high profile level 1 to level 5.2, 1080p30 and 720p60

### Security and cryptography

- Arm® TrustZone® and securable I/Os memories and peripherals
- SESIP Level 3 (security evaluation standard for IoT platforms), Arm® PSA (platform security architecture) certified
- Flexible life-cycle scheme with RDP and password-protected debug
- Secure provisioning of customer keys in OTP (one-time programmable) fuses
- Secure bootcode in ROM, decrypting and authenticating customer uRoT (updatable root-of-trust)
- Secure data storage with hardware-unique key (HUK)

- Secure firmware upgrade support with TF-M (trusted firmware-M)
- Two AES coprocessors, including one with DPA (differential power analysis) resistance
- Public key accelerator (PKA), DPA resistant
- On-the-fly encryption/decryption of external memories
- HASH hardware accelerator
- True random number generator (RNG), NIST SP800-90B compliant
- 96-bit unique ID
- 1.5-Kbyte OTP fuses
- Active tampers

### Communication peripherals

- 1x USB 2.0 high-speed/full-speed device/host/ OTG controller
- 1x USB 2.0 high-speed/full-speed device/host/ OTG controller, with UCPD (USB Type-C® Power Delivery)
- 10-, 100-Mbit, and 1-Gbit Ethernet with TSN (time-sensitive networking)
- 4x I2C Fm+ interfaces (SMBus/PMBus®) + 2x I3C
- 6x SPI, of which four I2S-capable
- 2x SAI, with four DMIC support
- 5x USART, 5x UART (ISO78916 interface, LIN, IrDA, up to 12.5 Mbit/s) + 1x LPUART
- 2x SDMMC: MMC version 4.0, CE-ATA version 1.0, and SD version 1.0.1
- 3x FDCAN with TTCAN capability

### Low power

- Sleep, Stop and Standby modes
- $V_{BAT}$ supply for RTC, 32x 32-bit backup registers + 8 Kbyte backup SRAM

### Timers and watchdogs

- 1x high-resolution timer
- 4x 32-bit timers with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input (up to 240 MHz)
- 2x 16-bit advanced motor control timers (up to 240 MHz)
- 12x 16-bit general-purpose and 5x 16-bit low-power timers (up to 240 MHz)
- 2x watchdogs (independent and window)
- 1x SysTick timer
- RTC with subsecond accuracy and hardware calendar

### Debug

- Development support: serial-wire debug (SWD), JTAG
- Embedded Trace Macrocell™ (ETM)

### General-purpose I/Os

- Up to 164 pins

### Analog peripherals

- 1x temperature sensor
- 2x ADCs with 12-bit maximum resolution (up to 5 MSPS)
- 1x ADF filter with SAD
- 1x MDF (six filters)

### Reset and power management

- POR, PDR, PBVD, and BOR
- Embedded SMPS step-down converter providing $V_{DDCORE}$
- 1.7 to 3.6 V application supply and I/Os
- Dedicated power for USB and XSPI I/Os
- Backup regulator (~0.9 V)
- Voltage reference for analog peripheral ($V_{REF+}$)

### Clock management

- Internal oscillators: 64 MHz HSI, 4 MHz MSI, 32 kHz LSI
- External oscillators: 16 to 48 MHz HSE, 32.768 kHz LSE
- 4× PLL (one for the system clock, one for the ST Neural-ART Accelerator, two for kernel clocks) with fractional mode

### ECOPACK2 compliant packages

**Table 1. Device summary**

| Reference | Part numbers |
|---|---|
| STM32N657xx | STM32N657X0, STM32N657L0, STM32N657B0, STM32N657I0, STM32N657Z0, STM32N657A0 |

# Contents

# List of tables

# List of figures

# 1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32N657xx microcontrollers.

For information on the Arm®(a) Cortex®-M55 core, refer to the Cortex®-M55 Technical Reference Manual, available from the www.arm.com website.



a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

# 2 Description

The STM32N657xx devices are based on the high-performance Arm® Cortex®-M55, operating at a frequency up to 800 MHz.

The Cortex®-M55 core features the Arm® Helium™ vector processing technology. On top of standard microcontroller tasks, this core enables energy-efficient digital signal processing. The Cortex®-M55 is equipped with a floating-point unit (FPU) that supports single- and half-precision (IEEE 754 compliant) data-processing. The Cortex®-M55 includes a 32-Kbyte ICACHE, a 32-Kbyte DCACHE, as well as 64-Kbyte TCM RAM and 128-Kbyte instruction TCM RAM with ECC for critical real-time routines.

The devices have TrustZone®-aware support and a memory protection unit (MPU) for enhanced application security. A secure boot ROM ensures secure booting from external interfaces.

These devices embed a 4.2-Mbyte contiguous SRAM organized in several banks, an 8-Kbyte backup SRAM active in $V_{BAT}$ mode, and a flexible external memory controller (FMC) for static memories, XSPI 8-/16-bit configurations.

The ST Neural-ART accelerator, running at up to 1 GHz and providing 600 Gops using optimized hardware units for DNN (deep-neural network) inference functions. optimizes power efficiency. Dedicated streaming engines are integrated into it to optimize data flow and minimize internal buffer usage and power. The accelerator supports on-the-fly weight decompression and real-time data encryption and decryption.

The Neo-Chrom graphic accelerator ensures efficient 2.5D graphic processing, by providing hardware acceleration for functions like scaling, using high-quality interpolation, free rotation, alpha blending, texture mapping, and perspective transformation.

For camera applications, a parallel and CSI interface together with an integrated hardware ISP is foreseen. The ISP provides processing of three parallel pipes on the same input stream. Supported algorithms are bad pixel, decimation, black-level tuning, exposure control, de-mosaicking, column conversion, contrast, cropping, downsizing, ROI isolation, gamma correction, YUV conversion, and pixel packer. The ISP output can be directly fed via a DMA to the NPU.

Optionally, the devices embed a hardware H264 encoding block supporting baseline profile, main profile and high profile level 1 to level 5.2, supporting frame rates of up to 30 frames per second for 1080p resolution.

A dedicated hardware accelerator ensures fast and simple JPEG and motion JPEG compression and decompression.

The devices offer an extensive range of enhanced I/Os and peripherals, and operate in the -40 to +125 °C temperature range, from 1.7 to 3.6 V power supply. A comprehensive set of low-power modes (Sleep, Stop, and Standby) allows the design of low-power applications.

The STM32N657 devices are offered in six VFBGA packages, ranging from 142 to 264 pins.

**Table 2. STM32N657xx features and peripheral counts**

| Feature / Peripheral | | STM32 N657X0 | STM32 N657L0 | STM32 N657B0 | STM32 N657I0 | STM32 N657A0 | STM32 N657Z0 |
|---|---|---|---|---|---|---|---|
| SRAM | System (Mbytes) | 4.2 | | | | | |
| | Backup (Kbytes) | 8 | | | | | |
| XSPI | 16 bits | 1 | | | 0 | | |
| | 8 bits | 1 | | | | | |
| Timers | Advanced control | 2 | 1 | | | | 0 |
| | General purpose | 10 | | | | 7 | |
| | Basic | 3 | | | | 2 | 1 |
| | Low-power | 5 | 4 | | 2 | 1 | |
| Communication interfaces | I2S | 3 | | | | 1 | 0 |
| | SPI | 6 | | | | | 5 |
| | I2C | 4 | | | | 3 | |
| | I3C | 2 | | | | | |
| | USART | 5 | | 4 | | 3 | 2 |
| | UART | 5 | | | 4 | 3 | |
| | LPUART | 1 | | | | | |
| | SAI | 2 | | | | | |
| | FDCAN | 3 | | | | | |
| | OTG HS | 2 | | | | | |
| | UCPD | Yes | | | | | |
| | SDMMC | 2 | | 1 | | 0 | |
| | CSI | Yes | | | | | |
| | PSSI | Yes | | | | | |
| | LTDC | Yes | | | | | |
| | ETH RGMIi/MIII | Yes | | | No | | |
| | ETH RMII | Yes | | | | | No |
| Multi-function digital filter (MDF) | | 6 filters | | | | | 2 filters |
| Audio digital filter (ADF) | | Yes | | | | | |
| Real time clock (RTC) | | Yes | | | | | |
| RNG | | Yes | | | | | |
| ADC (12 bits) | | 2 | | | | | |
| Internal voltage reference buffer | | Yes | | | | | |
| Digital temperature sensor (DTS) | | Yes | | | | | |
| Maximum CPU frequency | | 600 MHz, 800 MHz (overdrive mode) | | | | | |
| Operating voltage | | 1.71 to 3.6 V | | | | | |

**Table 2. STM32N657xx features and peripheral counts (continued)**

| Feature / Peripheral | | STM32 N657X0 | STM32 N657L0 | STM32 N657B0 | STM32 N657I0 | STM32 N657A0 | STM32 N657Z0 |
|---|---|---|---|---|---|---|---|
| Operating temperature | Ambient | – 40 to 85 °C /– 40 to 125 °C | | | | | |
| | Junction | – 40 to 105 °C / – 40 to 130 °C | | | | | |
| Package | | VFBGA264 | VFBGA223 | VFBGA198 | VFBGA178 | VFBGA169 | VFBGA142 |
| | Size | 14 x 14 mm | 10 x 10 mm | 10 x 10 mm | 12 x 12 mm | 6 x 6 mm | 8 x 8 mm |
| | Pitch | 0.8 mm | 0.5 mm | 0.65 mm | 0.8 mm | 0.4 mm | 0.5 mm |

# 3 Functional overview

## 3.1 Arm Cortex-M55 core with TrustZone, FPU, NVIC

The device architecture relies on an Arm Cortex-M55 core optimized for execution:

- Main masters:
  - Cortex-M55 with Arm TrustZone mainline, with two master ports
    - M-AXI: provides access to the memory and to the peripherals
    - P-AHB: provides access to the peripherals
  - NPU (neural processor unit), including two master AXI ports
- Memories:
  - AHB and APB peripherals
  - 4.2 Mbytes of SRAM
  - 64-Kbyte TCM RAM with ECC for critical real-time data, and 128 Kbytes of instruction TCM RAM with ECC for critical real-time routines (TCMs case not extended)
  - 8 Kbytes of backup SRAM (BKPSRAM) active in VBAT mode
  - 2 x 16-Kbyte AHB RAMs
  - Flexible external memory controller (FLEXMEM) with cypher engine supporting up to 32-bit data bus: SRAM, PSRAM, SDRAM, LPSDR SDRAM, NOR/NAND memories
  - XSPI 8-bit configuration with cypher engine
  - XSPI 16-bit configuration with cypher engine (only on STM32N657X0H3Q, STM32N657L0H3Q, and STM32N657B0H3Q)

## 3.2 SRAM configuration

AHBSRAM1/2, AXISRAM1 to 6, BKPSRAM, FLEXRAM, and VENCRAM, with the following features:

- Error code correction (ECC):
  - Single-error detection and correction with interrupt generation
  - Double-error detection with interrupt generation
  - Status with failing address
- Hardware erase: on reset or dedicated event, the RAM content is automatically erased (written as 0)
- Software erase: the software can trigger an SRAM erase through RAMCFG registers

## 3.3 AXI cache configuration

The AXI cache (CACHEAXI) is introduced on AXI interconnect driven by an AXI master peripheral to improve the performance of data traffic to/from main memories. Main features:

- Bus interface
- Optionally, the CACHEAXI can be configured to behave as an SRAM

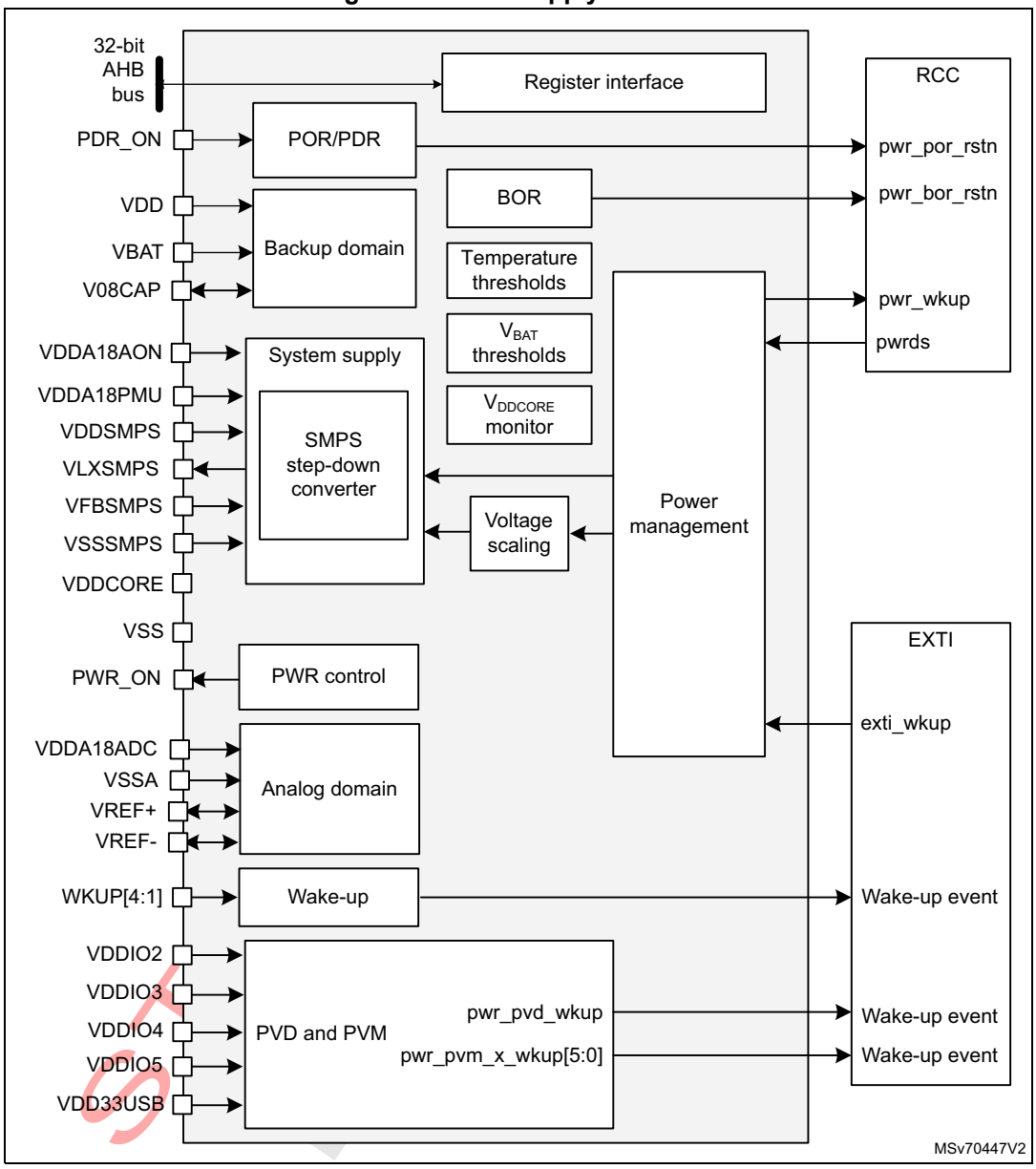
- Cache access
- Replacement and refill
- System compartments support:
- TrustZone security support
- Maintenance operations
- Performance counters
- Error management

## 3.4 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domain ($V_{CORE}$ = $V_{DDCORE}$)
  - $V_{DD}$ domain ($V_{RET}$)
  - Backup domain ($V_{SW}$, $V_{BAT}$)
  - Analog domain ($V_{DDA18ADC}$)
- System supply voltage regulation
  - Efficient SMPS step down converter
- Power supply supervision
  - POR/PDR monitor
  - BOR monitor
  - $V_{DDA18PMU}$ monitor
  - PVD monitor
  - PVM monitor ($V_{DDA}$, $V_{DDUSB}$, $V_{DDIO2}$, $V_{DDIO3}$, $V_{DDIO4}$, $V_{DDIO5}$, $V_{DD33USB}$, $V_{DDA18ADC}$)
  - $V_{BAT}$ thresholds
  - Temperature thresholds
  - $V_{DDCORE}$ monitor
  - PVD monitor
  - PVM monitor ($V_{DDA}$, $V_{DDUSB}$, $V_{DDIO2}$)
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes

**Figure 1. Power supply overview**




### 3.4.1 Voltage scaling

The $V_{CORE}$ domain is supplied from a single voltage regulator that supports voltage scaling with the following features:

- Run mode voltage scaling
  - VOS low
  - VOS high
- Stop mode voltage scaling
  - SVOS low
  - SVOS high

### 3.4.2 Power supply schemes

### 3.4.3 Core domain

The core domain supply can be provided by the SMPS step-down converter, or by an external supply (VDDCORE). $V_{CORE}$ supplies all the digital circuitries, except for the backup domain, and the retention domain in Standby mode. When a system reset occurs, the SMPS step-down converter is enabled to deliver 0.8 V, hence the system can start up in any supply configuration.

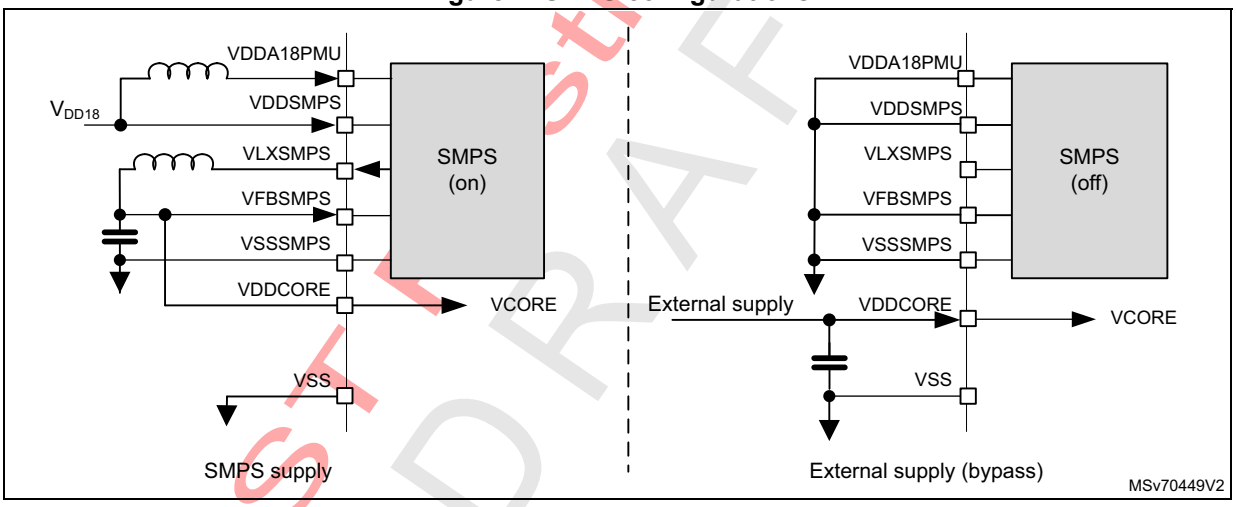
The system startup sequence from power-on in different supply configurations is controlled through power management.

### 3.4.4 SMPS usage

The devices embed an SMPS to provide the $V_{CORE}$ supply. The SMPS generates this voltage on VLXSMPS, with a total external capacitor of 88 (4x 22) µF (typical). The SMPS requires an external coil of 1 µH (typical).

Two configurations exist, namely SMPS step-down converter supply on and off (bypass mode). In the latter the step-down converter supply is disabled.

**Figure 2. SMPS configurations**




### 3.4.5 Backup domain

To retain the content of the backup domain (RTC, backup registers, and backup RAM) when $V_{DD}$ is turned off, the VBAT pin can be connected to an optional voltage supplied from a battery or another source. The switching to $V_{BAT}$ is controlled by the power-down reset (PDR) embedded in the block that monitors the $V_{DD}$ supply.

### 3.4.6 Analog supply

The analog supply domain is powered by dedicated VDDA18ADC and VSSA pins, which allow the supply to be filtered and shielded from noise on the PCB, thus improving ADC conversion accuracy.

The analog supply voltage input is available on a separate VDDA18ADC pin, and an isolated supply ground connection is provided on VSSA pin.

### 3.4.7 System supply startup

The system startup sequence from power-on has different supply configurations (see *Figure 3* and *Figure 4*), according to the usage of the SMPS.

**Figure 3. Device startup with $V_{CORE}$ supplied directly from an external SMPS**

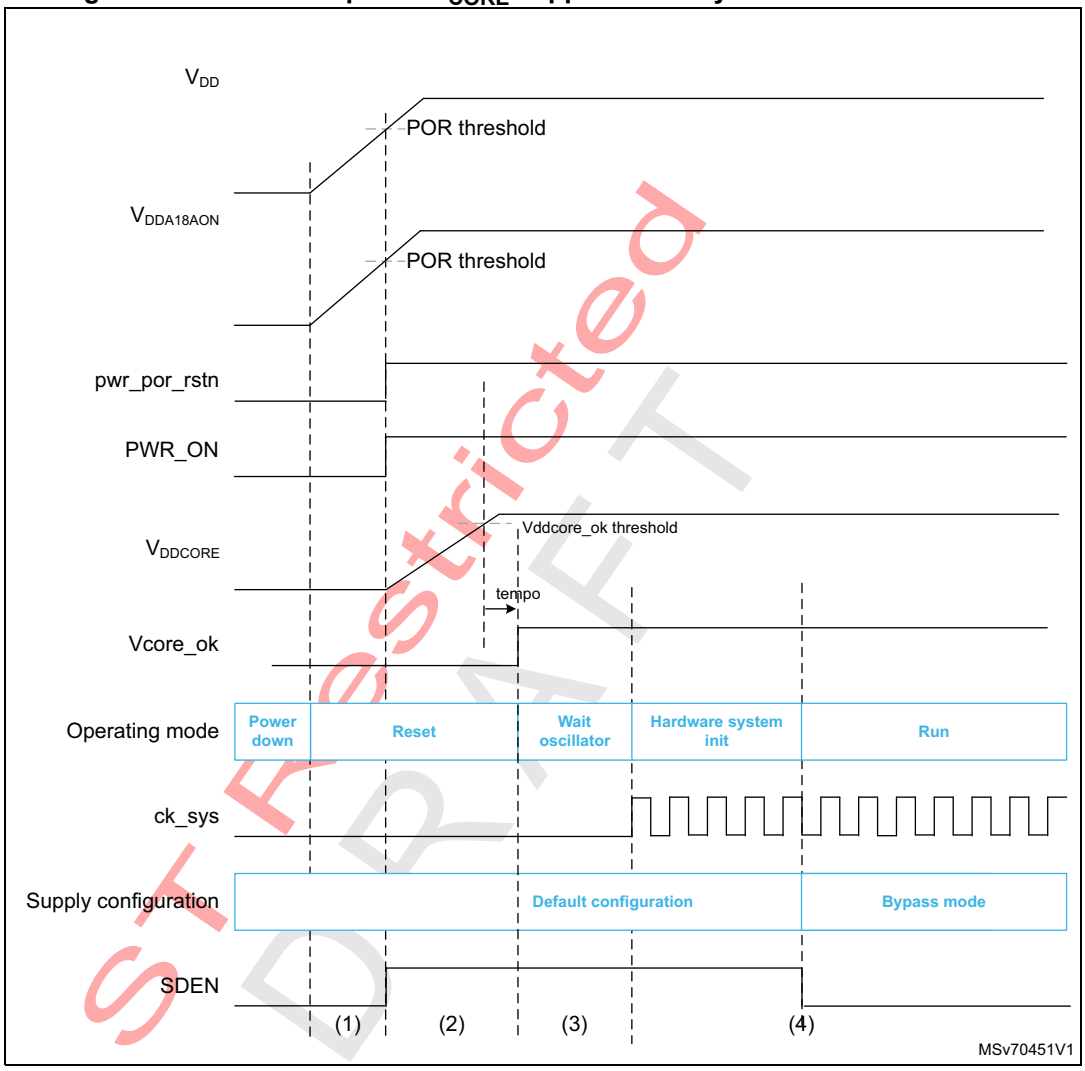
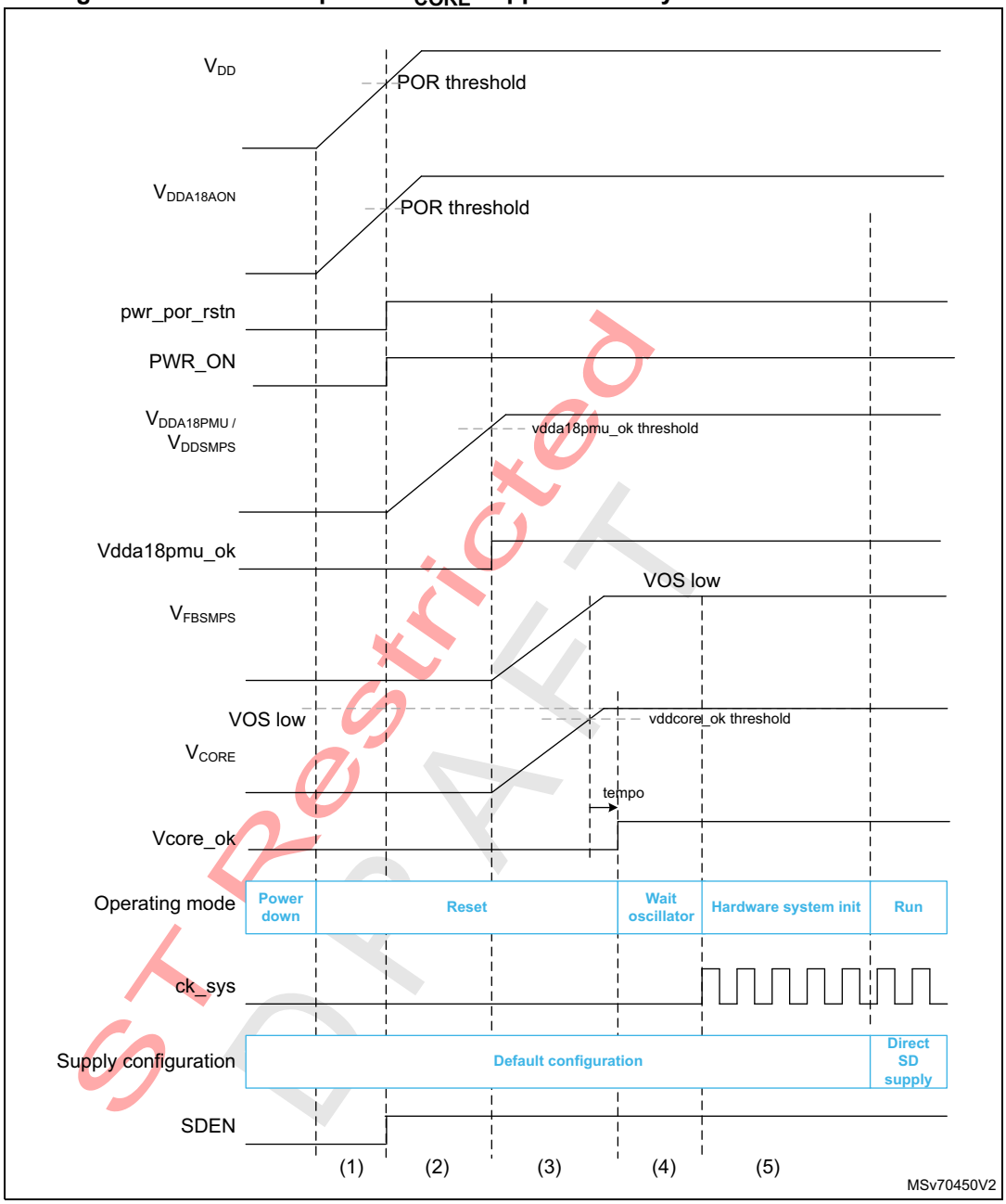


**Figure 4. Device startup with $V_{CORE}$ supplied directly from the internal SMPS**






## 3.4.8 Operation modes

Several system operating modes are available to tune the system according to the required performance. The user can select the operating mode that gives the best compromise between power consumption, start-up time, and available wake-up sources.

**Table 3. Operating mode summary**

| System | Entry | Wake-up | System oscillator | System clock | Peripheral clock | CPU clock | Voltage regulator | PWR_ON |
|---|---|---|---|---|---|---|---|---|
| Run | - | - | ON | ON | ON | ON[1] | ON (VOS low/high) | 1 |
| Sleep | WFI or return from ISR or WFE[2] | See *Table 4* | | | ON/OFF[3] | | | |
| Stop SVOS high | SVOS + SLEEPDEEP + WFI or return from ISR, WFE, or wake-up source cleared[4] | | ON/OFF[5] | OFF | | OFF | ON (SVOS high) | |
| Stop SVOS low | SLEEPDEEP + WFI or return from ISR, WFE, or wake-up source cleared[3] | | OFF | | OFF | | ON (SVOS low) | |
| Standby | PDDS + SLEEPDEEP + WFI or return from ISR, WFE, or wake-up source cleared[3] | WKUP pins rising or falling edge, RTC alarm (alarm A or alarm B), RTC wake-up event, RTC tamper events, RTC timestamp event, external reset in NRST pin, IWDG reset | OFF | OFF | OFF | OFF | OFF | 0[6] |

1. The clock is gated in the core in Sleep mode.
2. WFI = wait for interrupt, ISR = interrupt service routine, WFE = wait for event.
3. The CPU subsystem peripherals that have a PERxLPEN bit, operate accordingly.
4. When the CPU is in Stop mode, the last EXTI wake-up source must be cleared by software.
5. When HSI or MSI is used, the state is controlled by HSISTOPEN and MSISTOPEN, otherwise the system oscillator is off.
6. A guaranteed minimum PWR_ON pulse low time can be defined by POPL bits in PWR_CR1.

**Table 4. Functionalities depending on system operating mode**

| Peripheral[1] | Run mode | Stop mode SVOS high | | Stop mode SVOS low | | Standby mode | | $V_{BAT}$ mode |
|---|---|---|---|---|---|---|---|---|
| | | - | Wake-up capability | - | Wake-up capability | - | Wake-up capability | |
| CPU | Y | R | - | R | - | - | - | - |
| NPU | O | O | - | R | - | - | - | - |
| Debug | O | O | O | R | - | - | - | - |
| ROM | Y | R | - | R | - | - | - | - |

**Table 4. Functionalities depending on system operating mode (continued)**

| Peripheral[1] | Run mode | Stop mode SVOS high | | Stop mode SVOS low | | Standby mode | | $V_{BAT}$ mode |
|---|---|---|---|---|---|---|---|---|
| | | - | Wake-up capability | - | Wake-up capability | - | Wake-up capability | |
| RAMCFG | O | R | - | R | - | - | - | - |
| I-TCM | O | R | - | R | - | R | - | - |
| I-TCM FLEXMEM | O | R | - | R | - | R | - | - |
| D-TCM | O | R | - | R | - | R | - | - |
| AXISRAM1 | O | R | - | R | - | R[2] | - | - |
| AXISRAMx (x = 2, 3, 4) | O | O | - | R | - | - | - | - |
| I-TCM FLEXMEM extension | O | O | - | R | - | R[3] | - | - |
| D-TCM FLEXMEM extension | O | O | - | R | - | - | - | - |
| CACHEAXI1 | O | O | - | R | - | - | - | - |
| VENCRAM | O | O | - | R | - | - | - | - |
| GPU RAM | O | O | - | R | - | - | - | - |
| BKPSRAM | O | R | - | R | - | O | - | O |
| AHBSRAMx (x = 1, 2) | O | O | - | R | - | - | - | - |
| XSPIx (x = 1, 2, 3) | O | R | - | R | - | - | - | - |
| XSPIM | O | R | - | R | - | - | - | - |
| MCEx (x = 1, 2, 3, 4) | O | R | - | R | - | - | - | - |
| FMC | O | R | - | R | - | - | - | - |
| Backup registers | Y | R | - | R | - | R | - | R |
| Brownout reset (BOR) | Y | Y | Y | Y | Y | Y | Y | - |
| Programmable voltage detector (PVD) | O | O | O | O | O | - | - | - |
| Peripheral voltage monitor (PVM) | O | O | O | O | O | - | - | - |
| VBATH/VBATL monitoring | O | O | O | O | O | O | O | O |
| TEMPH/TEMPL monitoring | O | O | O | O | O | O | O | O |
| GPDMA1 | O | R | - | R | - | - | - | - |
| HPDMA1 | O | R | - | R | - | - | - | - |
| High speed internal (HSI) | O | O | - | - | - | - | - | - |
| High speed external (HSE) | O | - | - | - | - | - | - | - |
| Low speed internal (LSI) | O | O | - | O | - | O | - | - |
| Low speed external (LSE) | O | O | - | O | - | O | - | O |
| Multi speed internal (MSI) | O | O | - | - | - | - | - | - |
| HSE CSS (clock security system) | O | - | - | - | - | - | - | - |
| LSE CSS | O | O | O | O | O | O | O | O |

**Table 4. Functionalities depending on system operating mode (continued)**

| Peripheral[1] | Run mode | Stop mode SVOS high | | Stop mode SVOS low | | Standby mode | | $V_{BAT}$ mode |
|---|---|---|---|---|---|---|---|---|
| | | - | Wake-up capability | - | Wake-up capability | - | Wake-up capability | |
| RTC/auto wake-up | O | O | O | O | O | O | O | O |
| TAMP, number of tamper pins | 7 | 7 | O | 4 | O | 4 | O | 4 |
| OTG1 HS | O | R | O | R | - | - | - | - |
| OTG2 HS | O | R | O | R | - | - | - | - |
| UCPD1 | O | R | O | R | - | - | - | - |
| SDMMCx (x = 1, 2) | O | R | - | R | - | - | - | - |
| FDCAN | O | R | - | R | - | - | - | - |
| MDIOS | O | R | O | R | - | - | - | - |
| ETH1 | O | R | O | R | - | - | - | - |
| LPUART1 | O | O | O | R | - | - | - | - |
| U(S)ARTx (x = 1 to 10) | O | O | O | R | - | - | - | - |
| I2Cx (x = 1, 2, 3, 4) | O | O | O | R | - | - | - | - |
| I3Cx (x = 1, 2) | O | O | O | R | - | - | - | - |
| SPIx (x = 1 to 6) | O | O | O | R | - | - | - | - |
| SAIx (x = 1, 2) | O | R | - | R | - | - | - | - |
| ADF1 | O | O | O | R | - | - | - | - |
| MDF1 | O | O | O | R | - | - | - | - |
| DCMI | O | R | - | R | - | - | - | - |
| PSSI | O | R | - | R | - | - | - | - |
| DCMIPP | O | R | - | R | - | - | - | - |
| GPU | O | R | - | R | - | - | - | - |
| DMA2D | O | R | - | R | - | - | - | - |
| GFXTIM | O | R | - | R | - | - | - | - |
| GFXMMU | O | R | - | R | - | - | - | - |
| JPEG | O | R | - | R | - | - | - | - |
| VENC | O | R | - | R | - | - | - | - |
| LTDC | O | R | - | R | - | - | - | - |
| ADCx (x = 1, 2) | O | R | - | R | - | - | - | - |
| VREFBUF | O | R | - | R | - | - | - | - |
| DTS | O | R | O | R | - | - | - | - |
| TIMx (x = 1 to 18) | O | R | - | R | - | - | - | - |
| LPTIMx (x = 1 to 5) | O | O | O | R | - | - | - | - |

**Table 4. Functionalities depending on system operating mode (continued)**

| Peripheral[1] | Run mode | Stop mode SVOS high | | Stop mode SVOS low | | Standby mode | | $V_{BAT}$ mode |
|---|---|---|---|---|---|---|---|---|
| | | - | Wake-up capability | - | Wake-up capability | - | Wake-up capability | |
| IWDG | O | O | O | O | O | O | O | - |
| WWDG | O | R | - | R | - | - | - | - |
| RNG | O | R | - | R | - | - | - | - |
| SAES | O | R | - | R | - | - | - | - |
| CRYP | O | R | - | R | - | - | - | - |
| HASH | O | R | - | R | - | - | - | - |
| CRC | O | R | - | R | - | - | - | - |
| GPIOs | O | O | O | O | O<br>4 pins | O | O<br>4 pins | - |

1. Legend: Y = Yes (enable). O = Optional (disable by default. Can be enabled by software). R = data/state retained. -= not available.
2. Only the first 80 Kbytes can optionally be retained (see the dedicated section of RM0486 for details).
3. Only the first 64 Kbytes can optionally be retained (see the dedicated section of RM0486 for details).

### 3.4.9 Low-power modes

Several low-power modes are available to save power when the CPU does not need to execute code (when waiting for an external event). The user must select the mode that gives the best compromise between low-power consumption, short start-up time, and available wake-up sources:

- Low-power modes
  - Sleep (CPU clock stopped and still in Run mode)
  - Stop (system clock stopped)
  - Standby (system powered down)
- Reset mode
  - To improve the consumption under reset, the I/O state under and after reset is “analog state” (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

## 3.5 Convolution neural network accelerator (NPU)

The neural processing unit (NPU) core is the design time parametric and runtime reconfigurable neural network inference engine. It can accelerate a wide range of neural network architectures in hardware.

The host configures the NPU subsystem through an AHB/AXI lite slave port, connected to one of the ports of the system bus matrix/interconnect. The two master ports of NPU are 64-bit wide master AXI-4 interfaces that connect to the system bus matrix/Interconnect. The system memory is shared between the host subsystem and the NPU subsystem.

## 3.6 Boot modes

The BootROM is the first code executed after any system reset. The boot mode is determined by BOOT0 and BOOT1 pins, one OTP word (flash source selection), and one TAMP backup register.

- BOOT0 is a dedicated pin latched upon reset release
- BOOT1 is a non-dedicated boot pin. The BOOT1 value comes from BOOT1 pin (default pin), or any other pin defined by system

Depending the configuration of these signals, there are two boot modes, namely serial boot, and external flash boot.

### 3.6.1 External flash boot

The firmware is loaded from an external flash memory. The BootROM code supports following types of boot memory devices:

- XSPI serial NOR (in SPI mode, single)
- XSPI HyperFlash™ (8-bit)
- e.MMC™ SDMMC1 or e.MMC™ SDMMC2 (up to JEDEC v5.1)
- SD-Card SDMMC1 or SD-Card SDMMC2 (up to SD standard v6.0)

### 3.6.2 Serial boot

The image is loaded from a serial interface. The BootROM code supports following types of serial boot interfaces:

- USB boot
- UART boot

## 3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked, if needed, following a specific sequence, to avoid spurious writing to the I/Os registers.

## 3.8 System configuration controller (SYSCFG)

The devices feature a set of configuration registers. The SYSCFG manages:

- Cortex-M55 internal settings (such as TCM, CACHE, or vectors)
- interconnect, security, and memory settings
- compensation cells

## 3.9 General purpose direct memory access controller (GPDMA)

The GPDMA controller is a bus master and system peripheral, used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

The GPDMA main features are:

- Dual bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during low-power modes
- Transfer arbitration based on a 4-grade programmed priority at channel level:
  - One high priority traffic class, for time-sensitive channels (queue 3)
  - Three low priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)
- Per channel event generation, on any of the following events: transfer complete, half transfer complete, data transfer error, user setting error, link transfer error, completed suspension, and trigger overrun
- Per channel interrupt generation, with separately programmed interrupt enable per event
- 16 concurrent GPDMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intra-channel GPDMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode.
  - Intra-channel and inter-channel GPDMA transfers chaining via programmable GPDMA input triggers connection to GPDMA task completion events
- Per linked-list item within a channel:
- Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive burst transfers
  - 2D source and destination addressing: programmable signed address offsets between successive burst transfers (non-contiguous addressing within a block, combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level, for a reduced set of channels
  - Support for scatter-gather (multi-buffer transfers), data interleaving and deinterleaving via 2D addressing
  - Programmable GPDMA request and trigger selection
  - Programmable GPDMA half transfer and transfer complete events generation

  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the GPDMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting, including FIFO level, and event flags
- TrustZone support:
  - Support for secure and non-secure GPDMA transfers, independently at a first channel level, and independently at a source/destination and link sublevels.
  - Secure and non-secure interrupts reporting, resulting from any of the respectively secure and non-secure channels.
  - TrustZone-aware AHB slave port, protecting any GPDMA secure resource (register, register field) from a non-secure access.
- Privileged/unprivileged support:
  - Support for privileged and unprivileged GPDMA transfers, independently at a channel level
  - Privileged-aware AHB slave port

**Table 5. GPDMA1 channel implementation**

| Channel x | Hardware parameters | | Features | Comment |
|---|---|---|---|---|
| | dma_fifo_size[x] | dma_addressing[x] | | |
| 0 to 11 | 2 | 0 | – 8 bytes, 2 words FIFO<br>– Fixed/contiguously incremented addressing | Typically allocated for GPDMA transfers between an APB/AHB peripheral and SRAM. |
| 12 to 15 | 4 | 1 | – 32 bytes, 8 words FIFO<br>– 2D addressing | Can be used for GPDMA transfers, between a demanding AHB peripheral and SRAM, or for transfers from/to external memories. |

## 3.10 High performance direct memory access controller (HPDMA)

The HPDMA is used to perform programmable data transfers between memory-mapped peripherals, and/or memories via linked-lists, upon the control of an off-loaded CPU.

Main features:

- Single bidirectional AXI master and single bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during low-power modes. Transfer arbitration based on a 4-grade programmed priority at channel level:
  - One high priority traffic class, for time-sensitive channels (queue 3)
  - Three low priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)

- Per channel event generation, on any of the following events:
  - transfer complete, half transfer complete
  - data transfer error, user setting error, link transfer error
  - completed suspension
  - trigger overrun
- Per channel interrupt generation, with separately programmed interrupt enable per event
- 16 concurrent HPDMA channels:
  - Per channel FIFO for queuing source and destination transfers
  - Intra-channel HPDMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode.
  - Intra-channel and inter-channel HPDMA transfers chaining via programmable HPDMA input triggers connection to HPDMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing, or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing either fixed or contiguously incremented addressing, programmed at block level, between successive burst transfers
  - 2D source and destination addressing programmable signed address offsets between successive burst transfers (non-contiguous addressing within a block, combined with programmable signed address offsets between successive blocks, at a second 2D/repeated block level, for a reduced set of channels
  - Support for scatter-gather (multi-buffer transfers), data interleaving and deinterleaving via 2D addressing
  - Selection of programmable HPDMA request and trigger
  - Generation of programmable HPDMA half-transfer and transfer-complete event
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the HPDMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting, including FIFO level, and event flags
- TrustZone support:
  - Support for secure and non-secure HPDMA transfers, independently at a first channel level, and independently at a source/destination and link sublevels
  - Secure and non-secure interrupts reporting, resulting from any of the respectively secure and non-secure channels
  - TrustZone-aware AHB slave port, protecting any HPDMA secure resource (register, bitfield) from a non-secure access
- Privileged/unprivileged support:
  - Support for privileged and unprivileged HPDMA transfers, independently at channel level

  - Privileged-aware AHB slave port
- Channel isolation support:
  - Support for compartmented DMA transfers, independently at channel level, via compartment IDs (named CIDs)
  - CID-aware interrupts reporting
  - CID-aware AHB slave port, with integrated semaphores for a concurrent control from any of the CPUs

**Table 6. Implementation of HPDMA1 channels**

| Channel x | Hardware parameters | | Features |
|---|---|---|---|
| | dma_fifo_size[x] | dma_addressing[x] | |
| x = 0 to 11 | 3 | 0 | Channel x (x = 0 to 11) is implemented with:<br>– a FIFO of 16 bytes, 4 words, 2 double-words<br>– fixed/contiguously incremented addressing<br>These channels can be used for HPDMA transfers between an APB or AHB peripheral, an AHB/AXI SRAM, or CPU TCM. |
| x = 12 to 15 | 5 | 1 | Channel x (x = 12 to 15) is implemented with:<br>– a FIFO of 64 bytes, 8 double-words<br>– 2D addressing<br>These channels can be also used for HPDMA transfers, including AXI external memories. |

**Table 7. HPDMA1 in low-power modes**

| Feature | Low-power modes |
|---|---|
| Wake-up | HPDMA1 in Sleep mode |

## 3.11 Chrom-ART Accelerator controller (DMA2D)

The Chrom-ART Accelerator (DMA2D) is a specialized DMA dedicated to image manipulation. It can perform the following operations:

- Fill a part or the whole of a destination image with a specific color
- Copy a part or the whole of a source image into a part or the whole of a destination image
- Copy a part or the whole of a source image into a part or the whole of a destination image with a pixel format conversion
- Blend a part and/or two complete source images with different pixel format and copy the result into a part or the whole of a destination image with a different color format

All the classical color coding schemes are supported, from 4- up to 32-bit per pixel with indexed or direct color mode, including block based YCbCr to handle JPEG decoder output.

The DMA2D has its own dedicated memories for CLUTs (color look-up tables).

The main DMA2D features are:

- Single AXI master bus architecture
- AHB slave programming interface supporting 8-,16-,32-bit accesses (except for CLUT accesses which are 32-bit)
- User-programmable working area size
- User-programmable offset for sources and destination areas expressed in pixels or bytes
- User-programmable sources and destination addresses on the whole memory space
- Up to two sources with blending operation
- Alpha value that can be modified (source value, fixed value, or modulated value)
- User programmable source and destination color format
- Up to 12 color formats supported from 4-bit up to 32-bit per pixel with indirect or direct color coding
- Block based (8x8) YCbCr support with 4:4:4, 4:2:2 and 4:2:0 chroma sub-sampling factors
- Two internal memories for CLUT storage in indirect color mode
- Automatic CLUT loading or CLUT programming via the CPU
- User programmable CLUT size
- Internal timer to control AXI bandwidth
- Operating modes:
  - register-to-memory
  - memory-to-memory
  - memory-to-memory with pixel format conversion
  - memory-to-memory with pixel format conversion and blending
  - memory-to memory with pixel format conversion, blending, and fixed color foreground
- Area filling with a fixed color
- Copy from an area to another
- Copy with pixel format conversion between source and destination images
- Copy from two sources with independent color format and blending
- Output buffer byte swapping to support refresh of displays through parallel interface
- Abort and suspend of DMA2D operations
- Watermark interrupt on a user programmable destination line
- Interrupt generation on bus error or access conflict
- Interrupt generation on process completion

## 3.12 Chrom-GRC (GFXMMU)

The Chrom-GRC (GFXMMU) is a graphical oriented memory management unit aimed to optimize memory usage according to the display shape. Main features are:

- Fully programmable display shape to physically store only the visible pixel
- Up to four virtual buffers
- Each virtual buffer has 3072 or 4096 bytes per line and 1024 lines

- Each virtual buffer can be physically mapped to any system memory
- Packing and unpacking operation to store 32-bit pixel data into 24-bit packed
- Interrupt in case of buffer overflow (one per buffer)
- Interrupt in case of memory transfer error

## 3.13 Graphic timer (GFXTIM)

The graphic timer (GFXTIM) is a graphic oriented timer for smart management of graphical events for frame or line counting. Its main features are:

- Integrated frame and line clock generation
- One absolute frame counter with one compare channel
- Two auto-reload relative frame counters
- One line timer with two compare channels
- External tearing-effect line management and synchronization
- Four programmable event generators with external trigger generation
- One watchdog counter

## 3.14 Interrupts and events

### 3.14.1 Nested vectored interrupt controller (NVIC)

The NVIC includes the following features:

- Up to 195 maskable interrupt channels (not including the Cortex-M55 interrupt lines)
- 16 programmable priority levels (using four bits of interrupt priority)
- Low latency exception and interrupt handling
- Power management control
- Implementation of system control registers

The NVIC and the processor core interface are closely coupled, which enables low latency interrupt processing and efficient processing of late arriving interrupts. All interrupts, including the core exceptions, are managed by the NVIC.

### 3.14.2 Extended interrupt/event controller (EXTI)

The EXTI manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control, and generates interrupt requests to the CPU NVIC and events to the CPU event input. For the CPU an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run modes. The EXTI also includes the EXTI multiplexer I/O port selection.

The EXTI main features are the following:

- All event inputs allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Selectable active trigger edge

  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt and event generation
  - Software trigger possibility
- TrustZone secure events: the access to control and configuration bits of secure input events can be made secure
- EXTI I/O port selection

## 3.15 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from 8-, 16- or 32-bit data word and a generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

## 3.16 Flexible memory controller (FMC)

The FMC includes three memory controllers, namely the NOR/PSRAM, the NAND, and the synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller. Its main features are:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (four memory subregions)
  - Ferroelectric RAM
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- Burst mode support for faster access to synchronous devices such as NOR flash memory, PSRAM and SDRAM)
- Programmable continuous clock output for asynchronous and synchronous accesses
- 8-,16- or 32-bit wide data bus
- Independent chip-select control for each memory region
- Independent configuration for each memory region
- Write enable and byte lane select outputs for use with PSRAM, SRAM and SDRAM devices
- External asynchronous wait control

At startup the FMC pins must be configured by the user application. The FMC input/output pins not used by the application can be used for other purposes.

## 3.17 XSPI interface

### 3.17.1 Extended-SPI interface (XSPI)

The XSPI supports most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, HyperRAM™ and HyperFlash™ memories, with the following functional modes:

- Indirect: all the operations are performed using the XSPI registers to preset commands, addresses, data and transfer parameters.
- Automatic status-polling: the external memory status register is periodically read and an interrupt can be generated in case of flag setting.
- Memory-mapped: the external memory is memory mapped and it is seen by the system as if it was an internal memory, supporting both read and write operations.

The XSPI supports the following protocols with associated frame formats:

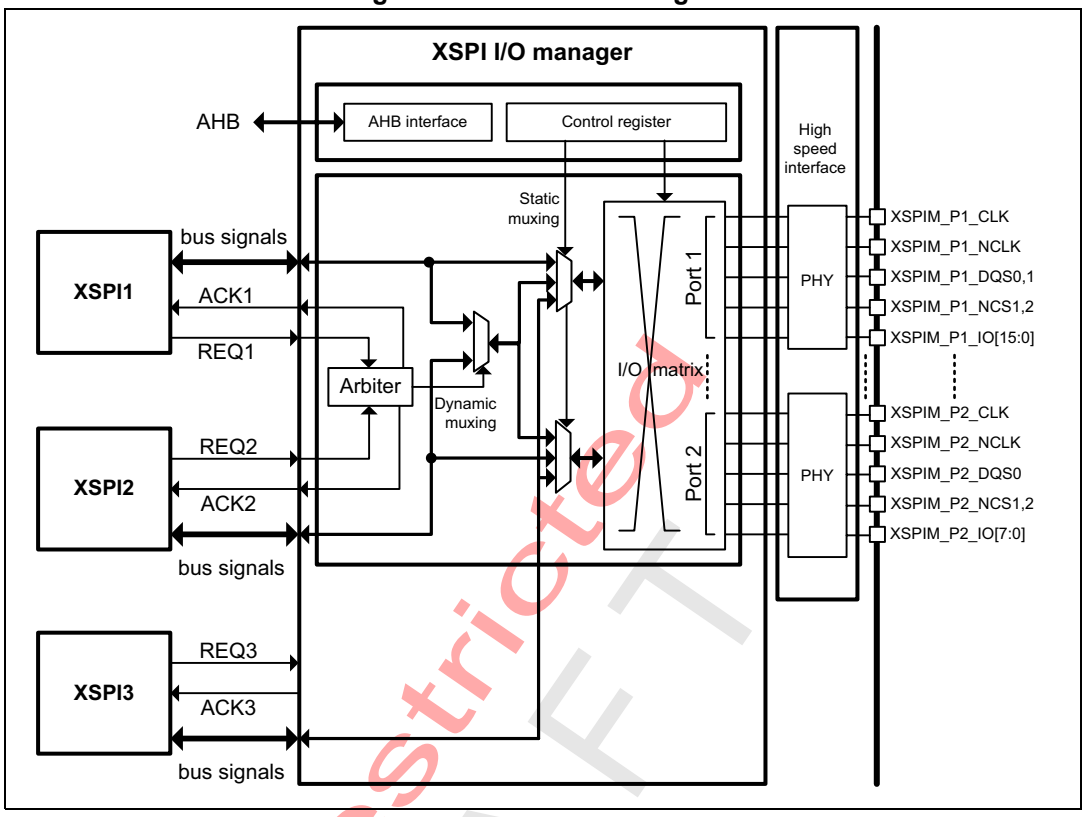
- regular-command frame format with the command, address, alternate byte, dummy cycles and data phase
- HyperBus™ frame format

The devices feature three XSPIs connected to the I/O ports through the XSPIM I/O manager.

### 3.17.2 XSPI I/O manager (XSPIM)

The XSPI I/O manager is a low level interface, enabling efficient XSPI pin assignment with a full I/O matrix (before alternate function map), and multiplex of single/dual/quad/octal/16-bit SPI interfaces over the same bus. In the STM32N6xx configuration, the XSPIM supports two XSPI interfaces (16 bits and octal on two ports, assigned to XSPIM_P1/ XSPIM_P2).

Figure 5. XSPIM block diagram




## 3.18 Secure digital input/output MultiMediaCard interface (SDMMC)

The SD/SDIO, embedded MultiMediaCard (e•MMC) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and eMMC devices.

The MultiMediaCard system specifications are available through the MultiMediaCard Association website at www.jedec.org, published by the MMCA technical committee.

SD memory card and SD I/O card system specifications are available through the SD card Association website at www.sdcard.org.

The SDMMC features include the following:

- Compliance with Embedded MultiMediaCard System Specification Version 5.1. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit. (HS200 SDMMC_CK speed limited to maximum allowed I/O speed) (HS400 is not supported).
- Full compatibility with previous versions of MultiMediaCards (backward compatibility).
- Full compliance with SD memory card specifications version 6.0. (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Full compliance with SDIO card specification version 4.0. Card support for two different databus modes: 1-bit (default) and 4-bit. (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).

- Data transfer up to 208 Mbyte/s for the 8-bit mode. (depending maximum allowed I/O speed).
- Data and command output enable signals to control external bidirectional drivers.
- IDMA linked list support

The MultiMediaCard/SD bus connects cards to the host.

The current version of the SDMMC supports only one SD/SDIO/e•MMC card at any one time and a stack of eMMC

## 3.19 SDMMC delay block (DLYB)

This block is used to generate two output clocks dephased from two input clocks. The phase of each output clock must be programmed by the user application. The output clocks are then used to clock the data transmitted/received by another peripheral such as an SDMMC.

## 3.20 Analog-to-digital converters (ADC)

The devices embed two ADCs (ADC1, ADC2) tightly coupled, which can operate in Dual mode (ADC1 is master).

Each ADC consists of one 12-bit successive approximation analog-to-digital converter, and has up to 20 multiplexed channels. The conversions can be performed in Single, Continuous, Scan, or Discontinuous mode. The result is stored in a left- or right-aligned (default configuration) 32-bit data register. The ADCs are mapped on the AHB bus for fast data handling.

The analog watchdog features allow the application to detect if the input voltage goes outside the user-defined high or low thresholds.

A built-in hardware oversampler improves analog performance, while off-loading the related computational burden from the CPU.

An efficient low-power mode is implemented for very low consumption at low frequencies.

The ADCx main features are:

- High-performance features
  - 12-, 10-, 8- or 6-bit configurable resolution
  - Conversion time independent from the AHB bus clock frequency
  - Faster conversion time by lowering resolution
  - Management of single-ended or differential inputs (programmable per channels)
  - AHB slave bus interface to allow fast data handling
  - Offset calibration support
  - Channel-wise programmable sampling time
  - Flexible sampling time control
  - Up to four injected channels (analog inputs assignment to regular or injected channels is fully configurable)
  - Data alignment with in-built data coherency
  - Data can be managed by DMA for regular channel conversions
  - Data can be routed to MDF for post processing

  - Four dedicated data registers for the injected channels
- Low-power features
  - Speed adaptive low-power mode to reduce ADC consumption when operating at low frequency
  - Allows slow bus frequency application while keeping optimum ADC performance
  - Provides automatic control to avoid ADC overrun in low AHB bus clock frequency application (Auto-delay mode)
- Oversampler
  - 32-bit data register
  - Oversampling ratio adjustable from 2 to 1024
  - Programmable data right shift
- Data preconditioning
  - Gain compensation
  - Offset compensation
- Analog input channels
  - External analog inputs (per ADC): up to 17 GPIO pads
  - One channel for the internal reference voltage (VREFINT)
  - One channel for monitoring the external VBAT power supply pin
  - One channel connected to the analog positive reference voltage VREF+
  - One channel for monitoring $V_{DDCORE}$ internal voltage
- Start-of-conversion can be initiated:
  - By software for both regular and injected conversions
  - By hardware triggers with configurable polarity (internal timers events or GPIO input events) for both regular and injected conversions
- Conversion modes
  - Each ADC can convert a single channel or can scan a sequence of channels
  - Single mode converts selected inputs once per trigger
  - Continuous mode converts selected inputs continuously
  - Discontinuous mode
- Interrupt generation at ADC ready, the end of sampling, the end of conversion (regular or injected), end of sequence conversion (regular or injected), analog watchdog 1, 2 or three or overrun events
- Three analog watchdogs per ADC
- Input range: $V_{SSA} \leq V_{IN} \leq V_{REF+}$

## 3.21 Digital temperature sensor (DTS)

The DTS is a high precision low-power junction temperature sensor (TS), composed of a configurable controller plus two embedded temperature sensors (TS0 and TS1). The controller features a generic interface that enables the DTS to be accessed in read and write modes, through the APB bus.

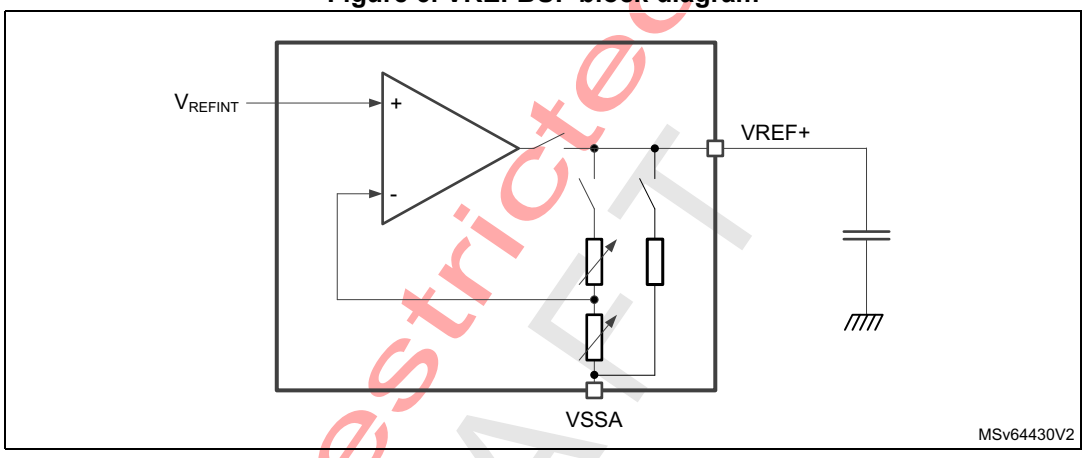
The main features are:

- For each temperature sensor, two programmable (rise or fall) hardware alarms incorporating hysteresis and status registers recording the minimum and maximum data values received
- A power-up timer with IRQ to support manual operation

## 3.22 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer supporting 1.21 and 1.5 V, which can be used as reference for ADCs and for external components through the VREF+ pin.

**Figure 6. VREFBUF block diagram**




## 3.23 Multi-function digital filter (MDF)

The multi-function digital filter (MDF) is a high performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators, mainly for audio capture signals, motor control, and metering.

The MDF features six digital serial interfaces (SITFx) and digital filters (DFLTx) with flexible digital processing options to offer up to 24-bit final resolution.

The DFLTx of the MDF also include the filters of the audio digital filter (ADF).

The MDF can receive, via its serial interfaces, streams coming from various digital sensors. It supports SPI, Manchester coded 1-wire, and PDM interface standards.

## 3.24 Audio digital filter (ADF)

The audio digital filter (ADF) is a high performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators, mainly for audio capture signals and metering.

The ADF features one digital serial interface (SITF0) and one digital filter (DFLT0) with flexible digital processing options in order to offer up to 24-bit final resolution.

The ADF serial interface supports SPI, Manchester coded 1-wire, and PDM interface standards.

## 3.25 Camera subsystem

The camera subsystem is built around a double path:

- a low resolution path, with the DCMI and a low-frequency parallel interface, supporting sensors up to 24 Mpixel/s.
- a high resolution path, with the DCMIPP and a high frequency parallel interface or serial CSI-2 interface (RGB or rawBayer), targeting sensors up to 5 Mpixels at 30 fps.

For the connection of a camera sensor, it is recommended to use the DCMIPP. The DCMI is recommended only in two noticeable cases:

- to get backward compatibility with former platforms that embed also the DCMI
- to input the pixels from a second camera sensor

*Note: The DCMIPP inputs pixels from one sensor via the CSI-2 interface, while the DCMI gets pixels from the second sensor via the parallel interface.*

The DCMI path offers the following summarized maximum features:

- Target sensor: 24 Mpixel/s 16 bpp (limited by the DMA)
- Parallel input: 80 MHz on 14-bit input capability
- Central DMA to extract and dump its pixels
- Software extraction of its pixel data

The DCMIPP path offers the following summarized maximum features:

- Target sensors: 5 Mpixel at 30 fps max
- Parallel input: 120 MHz on 16-bit input capability
- Serial input: CSI-2 @2.5 Gbps/lane on two data lanes
- ISP (image signal processor): demosaicing, exposure, white-balance, contrast, bad-pixel
- Application pipes: two pipes with crop, downsize, gamma, YUV conversion, YUV420

Some over-target use cases are possible, but with specific constraints:

- sensors with resolution above 5 Mpixels
- sensors with pixel rate above 150 Mpixel/s
- double sensors in parallel

### 3.25.1 Digital camera interface (DCMI)

The digital camera is a synchronous parallel interface able to receive a high speed data flow from an external 8-, 10-, 12- or 14-bit CMOS camera module. It supports different data formats: YCbCr4:2:2/RGB565 progressive video and compressed data (JPEG).

DCMI main features are:

- 8-, 10-, 12- or 14-bit parallel interface
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature
- Supports the following data formats:
  - 8/10/12/14-bit progressive video: either monochrome or raw Bayer
  - YCbCr 4:2:2 progressive video

- RGB 565 progressive video
- Compressed data: JPEG

### 3.25.2 Digital camera interface pixel pipeline (DCMIPP)

The DCMIPP is the pixel pipeline section of a highresolution camera subsystem: it gets pixels from a parallel or a CSI interface, and after some processing (such as decimation, cropping, downsize, color conversion, gamma correction, auto-exposure) dumps them to the memory.

DCMIPP supports multiple types of external sensors, among others:

- dumb sensors (without internal ISP), which output raw Bayer pixels
- smart sensors (with an internal ISP), which usually output RGB or YUV pixels
- smart sensors with internal compression, which output a bit-stream (such as JPEG or H264)
- sensors with interlaced video, which output their odd and even fields sequentially

The DCMIPP input interface integrates a parallel interface (up to 16 bits at 120 MHz, with internal/external synchronization), and makes it possible to abut an external CSI-2 host (one to two data lanes, up to 2.5 Gbps/lane).

A first common part of the DCMIPP selects the input exclusively from the parallel or the CSI interfaces. Data go to dedicated pipeline(s) before they are sent to memory for further processing or display purposes.

## 3.26 CSI-2 Host (CSI)

The camera serial interface 2 (CSI-2) is a part of a group of communication protocols defined by the MIPI® Alliance. The MIPI CSI-2 Host controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification. It provides an interface between the system and the MIPI D-PHY, allowing communication with a CSI-2 compliant camera.

Standard and references:

- MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2) v1.3 - 29 May 2014
- MIPI Alliance Specification for D-PHY v1.2 - 01 August 2014

## 3.27 Parallel synchronous slave interface (PSSI)

The PSSI and the DCMI use the same circuitry. As a result, these two peripherals cannot be used at the same time: when using the PSSI, the DCMI registers cannot be accessed, and vice versa. In addition, the PSSI and the DCMI share the same alternate functions and the same interrupt vector.

The PSSI is a generic synchronous 8-/16-bit parallel data input/output slave interface. It enables the transmitter to send a data valid signal that indicates when the data is valid, and the receiver to output a flow control signal that indicates when it is ready to sample the data.

The PSSI peripheral main features are the following:

- Slave mode operation
- 8- or 16-bit parallel data input or output

- 4-word (16-byte) FIFO
- Data enable (PSSI_DE) alternate function input and ready (PSSI_RDY) alternate function output

When selected, these inputs can either enable the transmitter to indicate when the data is valid, or allow the receiver to indicate when it is ready to sample the data, or both.

## 3.28 Display subsystem

The display subsystem is targeted to drive up to 1080p60 display panels, through a parallel interface. It supports some on-the-fly compositions to offload the GPU and optimize the use of the system bandwidth: up to two layers, color conversion, blend, mirror, and a final YUV conversion.

The display subsystem can display a secure layer with data that cannot be read by nonsecure application, and with the display guaranteed stable.

The display subsystem is built around LTDC:

- LTDC: handles display composition and rotation
  - Composition: 2 layers
  - Input pixel format: flexible format, including YUV420 full-planar on layer L1
  - Secure layer: protected access to buffer and configuration registers.
  - Mirror: horizontal and vertical
  - Miscellaneous: color lookup-table, color keying, Gamma
  - 1080p60 max performance
- LTDC parallel interface (integrated inside the LTDC):
  - Standard: 24 bpp + Hs, Vs, De (DataEnable) synchronization signals with ReTime
  - Output rate: 150 Mpixel/s
  - Resolution: 1920x1080 at 60 fps max, with HDMI blankings
  - Pixel formats: RGB888, 666, 565, YUV422-16 bits/BT601/709

## 3.29 LCD-TFT display controller (LTDC)

The LTDC (liquid crystal display - thin film transistor) display controller provides a parallel digital RGB (Red, Green, Blue) and signals for horizontal, vertical synchronization, pixel clock and data enable as output to interface directly to a variety of LCD-TFT panels.

LTDC main features are:

- Two input layers blended together to compose the display
- Cropping of layers from any input size and location
- Multiple input pixel formats:
  - Predefined ARGB, with 7 formats: ARGB8888, ABGR8888, RGBA8888, BGRA8888, RGB565, BGR565, RGB888packed
  - Flexible ARGB, allowing any width and location for A,R,G,B components
  - Predefined YUV, with 3 formats: YUV422-1L (FourCC: YUYV, Interleaved), YUV420-2L (FourCC: NV12, semi planar), YUV420-3L (FourCC: Yxx I420, full planar) with some flexibility on the sequence of the component

- Color look-up table (CLUT) up to 256 colors (256x24 bits) per layer
- Color transparency keying
- Composition with flexible window position and size versus output display
- Blending with flexible layer order and alpha value (per pixel or constant)
- Background underlying color
- Gamma with non-linear configurable table
- Dithering for output with less bits per component (pseudo-random on 2 bits)
- Polarity inversion for HSync, VSync, and DataEnable outputs
- Output as RGB888 24 bpp or YUV422 16 bpp
- Secure layer (using layer2) capability, with grouped regs and additional interrupt set
- Interrupts based on seven different events
- AXI master interface with long efficient bursts (64 or 128 bytes)

## 3.30 Neo-Chrom graphic processor (GPU2D)

The GPU2D is a dedicated graphics processing unit accelerating numerous 2.5D graphics applications such as graphical user interface (GUI), menu display or animations. The GPU2D works together with an optimized software stack designed for state of the art graphic rendering.

- GPU2D main features
  - Multi-threaded fragment (pixel) processing core with a VLIW (very-long instruction word) instruction set.
  - Fixed point functional units
  - Command list based DMAs to minimize CPU overhead
  - Two 64-bit AXI master interfaces for texture and framebuffer access
  - Dedicated 64-bit AXI master interface for command list
  - 32-bit AHB slave interface for register bank access
  - Up to four general-purpose flags for system-level synchronization
  - Texture decompression unit with TSC™4 and TSC™6/TSC™6a support
- 2D drawing features
  - Pixel/line drawing
  - Filled rectangles
  - Triangles, quadrilateral drawing
  - Anti-aliasing 8xMSAA (multi-sample anti-aliasing)
- Image transformations
  - 3D perspective correct projections
  - Texture mapping with bilinear filtering or point sampling
- Blit support
  - Rotation, mirroring, stretching (independently on x and y axis)
  - Source and/or destination color keying
  - Pixel format conversions
- Text rendering support
  - A1, A2, A4, and A8 bitmap anti-aliased

  - Subsampled anti-aliased
- Color formats
  - ABGR8888, ARGB8888, BGRA8888, RGBA8888
  - xBGR8888, xRGB8888, BGRx8888, RGBx8888, RGB888, BGR888
  - BGR565, RGB565
  - RGB322, BGR322
  - TSC4, TSC6, TSC6A
  - L1, L2, L4, L8 (gray scale)
  - A1, A2, A4, A8
- Full alpha blending with hardware blender
  - Programmable blending modes
  - Source/destination color keying

## 3.31 Video encoder (VENC)

The video encoder (VENC) provides a hardware acceleration to encode a 1080p30 video stream in H264 (= MPEG4_Part10/AVC). The VENC also provides hardware acceleration to encode still images (JPEG) of up to 300 Mpixel/s. The VENC implementation embeds a large 128-Kbyte video RAM (VENCRAM). When the VENC is disabled, the VENCRAM is unused for video purposes, and is accessible by the system as a contiguous extension of the system SRAM.

The VENC supports the following features:

- Video encode:
  - codecs: H264 (MPEG4_Part10/AVC, baseline/Main/High up to 5.2)
  - performance: 1080p30 for H264
- Still-image encode:
  - codecs: JPEG (baseline interleaved)
  - performance: 300 Mpixel/s for JPEG
- VENCRAM:
  - size: 128 Kbytes
  - access: can be statically assigned to the system by SYSCFG settings
- Security via RIF:
  - the VENC is protected by a default slave and master control (RISUP and RIMU)
  - by default, the VENC works in non-protected mode
  - the VENC can be set in protected mode, for instance to handle DRM tasks with a secure datapath. In such cases, the drivers must run in a protected process.
- Synchronization from an upstream peripheral: pixels can be streamed from an upstream peripheral (such as the camera) directly to the VENC, without writing to a full frame buffer, nor requiring external bandwidth.
- Encode with multiple codecs on a same system: the VENC hardware processes the encode tasks sequentially, interleaved at frame level. Performance is shared across all the tasks.

## 3.32 JPEG codec (JPEG)

The hardware 8-bit JPEG codec encodes uncompressed image data stream or decodes JPEG-compressed image data stream. It also fully manages JPEG headers.

JPEG codec main features are:

- High-speed fully-synchronous operation
- Configurable as encoder or decoder
- Single-clock-per-pixel encode/decode
- RGB, YCbCr, YCMK and BW (grayscale) image color space support
- 8-bit depth per image component at encode/decode
- JPEG header generator/parser with enable/disable
- Four programmable quantization tables
- Single-clock Huffman coding and decoding
- Fully-programmable Huffman tables (two AC and two DC)
- Fully-programmable minimum coded unit (MCU)
- Concurrent input and output data stream interfaces

## 3.33 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a nondeterministic random bit generator (NDRBG).

The RNG true random number generator has been precertified NIST SP800-90B. It has also been tested using the German BSI statistical tests of AIS-31 (T0 to T8).

RNG main features are:

- Delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage.
- Entropy source to construct a nondeterministic random bit generator (NDRBG).
- In the NIST configuration, produces four 32-bit random samples every 824 AHB clock cycles if fAHB < fthreshold (512 RNG clock cycles otherwise).
- Embeds startup and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- Can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration).
- AMBA® AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored).

## 3.34 Secure AES coprocessor (SAES)

The SAES encrypts or decrypts data in compliance with the advanced encryption standard (AES) defined by NIST. It incorporates a protection against side-channel attacks (SCA),

including differential power analysis (DPA), certified SESIP and PSA security assurance level 3.

SAES supports ECB, CBC, CTR, GCM, GMAC, and CCM chaining modes for key sizes of 128 or 256 bits, and special modes such as hardware secret key encryption/decryption (Wrapped-key mode) and key sharing with faster CRYP peripheral (Shared-key mode).

SAES has the possibility to load STM32 hardware secret master keys (boot hardware key BHK and derived hardware unique key DHUK), usable but not readable by application.

The peripheral supports DMA single transfers for incoming and outgoing data (two DMA channels are required). It is hardware-linked with the true random number generator (TRNG) and with the CRYP peripheral.

SAES main features:

- Compliant with NIST FIPS publication 197 “Advanced encryption standard (AES)” (November 2001)
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- Protection against side-channel attacks (SCA), incl. differential power analysis (DPA), certified SESIP and PSA security assurance level 3
- 128-bit data block processing, supporting cipher key lengths of 128-bit and 256-bit
- 480 or 680 clock cycle latency in ECB mode for processing one 128-bit block with, respectively, 128-bit or 256-bit key
- Hardware secret key encryption/ decryption (Wrapped-key mode)
- Using dedicated key bus, optional key sharing with faster CRYP peripheral (Sharedkey mode), controlled by SAES
- Integrated key scheduler to compute the last round key for ECB/CBC decryption
- 256-bit of write-only registers for storing cryptographic keys (eight 32-bit registers)
- Optional 128-bit or 256-bit hardware loading of two hardware secret keys (BHK, DHUK) that can be XOR-ed together
- Security context enforcement for keys
- 128-bit of registers for storing initialization vectors (four 32-bit registers)
- 32-bit buffer for data input and output
- Automatic data flow control supporting two direct memory access (DMA) channels, one for incoming data, one for processed data. Only single transfers are supported.
- Data-swapping logic to support 1-, 8-, 16-, or 32-bit data
- AMBA AHB slave peripheral, accessible through 32-bit word single accesses only. Other access types generate an AHB error, and other than 32-bit writes may corrupt the register content.
- Possibility for software to suspend a message if SAES needs to process another message with a higher priority, then resume the original message

## 3.35 Cryptographic processor (CRYP)

The cryptographic processor (CRYP) encrypts or decrypts data in compliance with the advanced encryption standard (AES) defined by NIST.

CRYP supports ECB, CBC, CTR, GCM, GMAC, and CCM chaining modes for key sizes of 128, 192, or 256 bits. CRYP has the possibility to load by hardware the key stored in SAES peripheral, under SAES control.

The peripheral supports both single and fixed DMA burst transfers for incoming and outgoing data (two DMA channels are required). CRYP also includes input and output FIFOs for better performance.

CRYP main features are:

- Compliant with NIST FIPS publication 197 “Advanced encryption standard (AES)” (November 2001)
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- 16-byte data block processing, supporting cipher key lengths of 128, 192 and 256 bits
- 14 or 18 clock cycle latency in ECB mode for processing one 16-byte block with 128-bit or 256-bit key, respectively
- Using dedicated key bus, optional key sharing with side-channel resistant SAES peripheral (shared-key mode), controlled by SAES
- Integrated key scheduler to compute the last round key for ECB/CBC decryption
- 256-bit of write-only registers for storing the cryptographic keys (eight 32-bit registers)
- 128-bit of registers for storing initialization vectors (four 32-bit registers)
- 32-bit input buffer associated with an internal input FIFO of eight 32-bit words, corresponding to two AES blocks
- 32-bit output buffer associated with an internal output FIFO of eight 32-bit words, corresponding to two AES blocks
- Automatic data flow control supporting two direct memory access (DMA) channels, one for incoming data, one for processed data. The output FIFO supports both single and burst transfers, while the input FIFO supports only burst transfers.
- Data swapping logic to support 1-, 8-, 16- or 32-bit data
- AMBA AHB slave peripheral, accessible through 32-bit word single accesses only. Other access types generates an AHB error, and write accesses are ignored.
- Possibility for software to suspend a message if CRYP needs to process another message with a higher priority, then resume the original message

## 3.36 Hash processor (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-2 family) and the HMAC (keyed-hash message authentication code) algorithm. HMAC is suitable for applications requiring message authentication.

The hash processor computes FIPS (Federal Information Processing Standards) approved digests of length of 160, 224, 256 bits, for messages of any length less than 264 bits (for SHA-1, SHA-224 and SHA-256) or less than 2128 bits (for SHA-384, SHA-512).

HASH main features are:

- Suitable for data authentication applications, compliant with:
  - Federal Information Processing Standards Publication FIPS PUB 180-4, Secure Hash Standard (SHA-1 and SHA-2 family)
  - Federal Information Processing Standards Publication FIPS PUB 186-4, Digital Signature Standard (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, HMAC: Keyed-Hashing for Message Authentication and Federal Information Processing Standards Publication FIPS PUB 198-1, The Keyed-Hash Message Authentication Code (HMAC)
- Fast computation of SHA-1, SHA2-224, SHA2-256, SHA2-384, and SHA2-512
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
  - 98 clock cycles for processing one 1024-bit block of data using either SHA2-384 or SHA2-512 algorithm
  - Support for SHA-2 truncated outputs (SHA2-512/224, SHA2-512/256)
  - Support for HMAC mode with all supported algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit-string
  - Supported word swapping format: bits, bytes, half-words and 32-bit words
- Single 32-bit, write-only, input register associated to an internal input FIFO, corresponding to a 64-byte block size (16 x 32 bits)
- Automatic padding to complete the input bit string to fit digest minimum block size
- AHB slave peripheral, accessible by 32-bit words only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H15) for output message digest
- Automatic data flow control supporting direct memory access (DMA) using one channel.
- Support for both single and fixed DMA burst transfers of four words.
- Interruptible message digest computation, on a per-block basis
  - Re-loadable digest registers
  - Hashing computation suspend/resume mechanism, including DMA

## 3.37 Memory cipher engine (MCE)

Memory cipher engine (MCE) defines, in a given address space, multiple regions with specific security setup (encryption). All system bus traffic going through an encrypted region is managed on-the-fly by the MCE, automatically decrypting reads and encrypting writes if authorized.

Multiple ciphering option (stream, block, fast block) are available to offer the best security versus performance trade-off.

MCE main features are:

- System bus in-line encryption (for writes) and decryption (for reads), based on embedded firewall programming
  - Four encryption modes per region (maximum 4 regions available): no encryption (bypass mode), stream cipher, block cipher and fast block cipher modes
  - Start and end of regions defined with 4-Kbytes granularity
  - Default filtering (region 0): any access granted
  - Regions 1 to 4 access filtering criteria: none
- Supported block ciphers: AES-128, AES-256 or Noekeon (12 round version), selected at boot
- Supported chaining modes: block and stream
  - Block mode with AES cipher is compatible with ECB mode specified in NIST FIPS publication 197 Advanced encryption standard (AES) (normal or fast).
  - Stream mode with AES cipher is compliant with CTR mode specified in NIST SP800-38A Recommendation for Block Cipher Modes of Operation.
  - Includes a leakage resilient mode of operation as defense against side channel attacks (SCA).
- One set of write-only and lockable 256-bit master key registers per block cipher (normal, fast)
- Two sets of lockable cipher contexts (128-bit key, IV), usable for stream and block ciphers
- Optimization for XSPI data pre-fetching mechanism (stream cipher only)
- Read-write arbitration scheme, for better read performances
- AHB configuration port
- AXI system bus master/slave interfaces (64-bit)
  - Support for any AXI-64bit read transactions
  - When encryption is enabled, support for AXI-64bit INCRx (x = 1 to 8) and WRAPx (x = 4) write transactions

## 3.38 Public key accelerator (PKA)

PKA (public key accelerator) is intended for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann or ECC (elliptic curve cryptography) over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

For a given operation, all needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

When manipulating secrets, the PKA incorporates a protection against side-channel attacks (SCA), including differential power analysis (DPA), certified SESIP and PSA security assurance level 3.

PKA main features are:

- Acceleration of RSA, DH and ECC over GF(p) operations, based on the Montgomery method for fast modular multiplications:
  - RSA modular exponentiation, RSA chinese remainder theorem (CRT) exponentiation
  - ECC scalar multiplication, point on curve check, complete addition, double base ladder, projective to affine
  - ECDSA signature generation and verification
- Capability to handle operands up to 4160 bits for RSA/DH and 640 bits for ECC
- When manipulating secrets: protection against side-channel attacks (SCA), including differential power analysis (DPA), certified SESIP and PSA security assurance level 3
- Applicable to modular exponentiation, ECC scalar multiplication and ECDSA signature generation
- Arithmetic and modular operations such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication
- Built-in Montgomery domain inward and outward transformations
- AMBA AHB slave peripheral, accessible through 32-bit word single accesses only (otherwise an AHB bus error is generated, and write accesses are ignored)

## 3.39 Timers (TIMx)

The devices contain 18 timers and 5 low-power timers.

### 3.39.1 Advanced control timers (TIM1/TIM8)

The devices embed two advanced control timers (TIM1/TIM8) that consist of a 16-bit auto-reload counter driven by a programmable prescaler.

These timers can be used for a variety of purposes, such as measuring the pulse length of input signals (input capture) or generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

The advanced control (TIM1/TIM8) and general purpose (TIMy) timers are completely independent, and do not share any resources. They can be synchronized together

Advanced control timers main features are:

- 16-bit up, down, up/down auto-reload counter.
- 16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536.
- Up to six independent channels for:
  - Input capture (except channels 5 and 6)
  - Output compares
  - PWM generation (Edge- and Center-aligned mode)

  - One-pulse mode output
- Complementary outputs with programmable dead-time
- Synchronization circuit to control the timer with external signals and to interconnect several timers together.
- Repetition counter to update the timer registers only after a given number of cycles of the counter.
- Two break inputs to put the timer's output signals in a safe user selectable configuration.
- Interrupt/DMA generation on the following events:
  - Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output compare
- Support of incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes
- Trigger input for external clock or cycle-by-cycle current management
- ADC synchronization for jitter-free sampling points

### 3.39.2 General purpose timers (TIM2/TIM3/TIM4/TIM5)

The four general purpose timers (TIM2/TIM3/TIM4/TIM5) consist of a 16- or 32-bit auto-reload counter driven by a programmable prescaler.

These timers can be used for a variety of purposes, such as measuring the pulse length of input signals (input capture), or generating output waveforms (output compare and PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

The timers are completely independent, and do not share any resources. They can be synchronized together.

Main features:

- 16- or 32-bit up, down, up/down auto-reload counter.
- 16-bit programmable prescaler used to divide (also "on the fly") the counter clock frequency by any factor between 1 and 65535.
- Up to four independent channels for:
  - Input capture
  - Output compare
  - PWM generation (Edge- and Center-aligned modes)
  - One-pulse mode output
- Synchronization circuit to control the timer with external signals and to interconnect several timers.
- Interrupt/DMA generation on the following events:
  - Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or count by internal/external trigger)
  - Input capture

  - Output compare
- Support of incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes
- Trigger input for external clock or cycle-by-cycle current management
- ADC synchronization for jitter-free sampling points

### 3.39.3 Basic timers (TIM6/TIM7/TIM18)

There are three basic timers that consist in a 16-bit auto-reload counter driven by a programmable prescaler.

They may be used as generic timers for time-base generation. The timers are completely independent, and do not share any resources.

Main features:

- 16-bit auto-reload upcounter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- Interrupt/DMA generation on the update event: counter overflow
- ADC synchronization for jitter-free sampling points

### 3.39.4 General purpose timers (TIM9/TIM10/TIM11/TIM12/TIM13/TIM14)

The six general purpose timers consist in a 16-bit auto-reload counter driven by a programmable prescaler.

They may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

The timers are completely independent, and do not share any resources. They can be synchronized together.

Main features:

- 16-bit auto-reload upcounter
- 16-bit programmable prescaler used to divide the counter clock frequency by any factor between 1 and 65536 (can be changed “on the fly”)
- Up to two independent channels for:
  - Input capture
  - Output compare
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Interrupt generation on the following events:
  - Update: counter overflow, counter initialization (by software or internal trigger)
  - Trigger event (counter start, stop, initialization or count by internal trigger)
  - Input capture
  - Output compare

- ADC synchronization for jitter-free sampling points

### 3.39.5 General purpose timers (TIM15/TIM16/TIM17)

These three timers consist of a 16-bit auto-reload counter driven by a programmable prescaler.

They may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

The timers are completely independent, and do not share any resources.

TIM15 can be synchronized. It includes the following features:

- 16-bit auto-reload upcounter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- Up to two independent channels for:
  - Input capture
  - Output compare
  - PWM generation (edge mode)
  - One-pulse mode output
- Complementary outputs with programmable dead-time (for channel 1 only)
- Synchronization circuit to control the timer with external signals and to interconnect several timers together
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Break input to put the timer’s output signals in the reset state or a known state
- Interrupt/DMA generation on the following events:
  - Update: counter overflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output compares
  - Break input (interrupt request)
- ADC synchronization for jitter-free sampling points

The TIM16/TIM17 timers include the following features:

- 16-bit auto-reload upcounter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
- One channel for:
  - Input capture
  - Output compare
  - PWM generation (edge-aligned mode)
  - One-pulse mode output

- Complementary outputs with programmable dead-time
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Break input to put the timer's output signals in the reset state or a known state
- Interrupt/DMA generation on the following events:
  - Update: counter overflow
  - Input capture
  - Output compare
  - Break input

### 3.39.6 Low-power timer (LPTIM)

The LPTIM is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. Thanks to the diversity of its clock sources, the LPTIM is able to keep running in all power modes except for Standby mode. Given its capability to run even with no internal clock source, the LPTIM can be used as a pulse counter. The capability to wake up the system from low-power modes makes it suitable for timeout functions with extremely low consumption.

The LPTIM introduces a flexible clock scheme that provides the needed functionalities and performance, while minimizing the power consumption. Its main features are:

- 16 bit upcounter
- 3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, and 128)
- Selectable clock
  - Internal clock sources: configurable internal clock source (see RCC section)
  - External clock source over LPTIM input (working with no LP oscillator running, used by pulse counter application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
  - Update event
  - Input capture

## 3.40 Independent watchdog (IWDG)

This peripheral offers a high safety level, thanks to its capability to detect malfunctions due to software or hardware failures. The IWDG is clocked by an independent clock, and stays active even if the main clock fails. In addition, the watchdog function is performed in the $V_{DD}$ voltage domain, allowing the IWDG to remain functional even in low-power modes. Refer to the dedicated section of the reference manual to check its capabilities in this product.

The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, making it very reliable to detect any unexpected behavior. Its main features are:

- 12-bit down-counter
- Dual voltage domain, enabling operation in low-power modes
- Independent clock
- Early wake-up interrupt generation
- Reset generation in case of timeout and of refresh outside the expected window

## 3.41 System window watchdog (WWDG)

The WWDG is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence.

The watchdog circuit generates a reset on expiry of a programmed time period, unless the program refreshes the contents of the down-counter before bit T6 is cleared. A reset is also generated if the 7-bit down-counter value (in the control register) is refreshed before the down-counter reaches the window register value. This implies that the counter must be refreshed in a limited window.

The WWDG clock is prescaled from the APB clock, and has a configurable time-window that can be programmed to detect abnormally late or early application behavior.

The WWDG is best suited for applications requiring the watchdog to react within an accurate timing window. The WWDG main features are:

- Programmable free-running down-counter
- Conditional reset (if watchdog activated)
  - When the down-counter value becomes lower than 0x40
  - If the down-counter is reloaded outside the window
- Early wake-up interrupt (EWI): triggered (if enabled and the watchdog activated) when the down-counter is equal to 0x40

## 3.42 Real-time clock (RTC)

The RTC is an independent BCD timer/counter that provides an automatic wake-up to manage all low-power modes.

The RTC provides a time of- day clock/calendar with programmable alarm interrupts. As long as the supply voltage remains in the operating range, it never stops, regardless of the device status (Run mode, low-power mode or under reset). The RTC is functional in VBAT mode.

Its main features are:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Binary mode with 32-bit free-running counter.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. (can be used to synchronize it with a master clock).
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Timestamp, which can be used to save the calendar content: can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period.
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up Timer and timestamp individual secure or non-secure configuration
- Alarm A, alarm B, wake-up Timer and timestamp individual privilege protection
- The RTC is supplied through a switch that takes power either from the $V_{DD}$ supply when present, or from the VBAT pin.
- The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE.
- All RTC events (Alarm, wake-up Timer, Timestamp) can generate an interrupt and wake up the device from the low-power modes.

## 3.43 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks.

32-bit backup registers are retained in all low-power modes and in VBAT mode. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with eight tamper pins and ten internal tampers. The external tamper pins can be configured for edge or level detection with or without filtering, or active tamper, which increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features are:

- A tamper detection can erase the backup registers, backup SRAM, SRAM2, cryptographic peripherals.
- 32 32-bit backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the backup domain that remains powered-on by VBAT when the VDD power is switched off.
- Eight tamper pins for eight external tamper detection event:

  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks.
  - Flexible active tamper I/O management: from 4 meshes (each input associated to its own exclusive output) to 7 meshes (single output shared for up to 7 tamper inputs)
  - Passive tampers: ultralow-power edge or level detection with internal pull-up hardware management.
  - Configurable digital filter.
- Ten internal tamper events to protect against transient or environmental perturbation attacks
- Each tamper can be configured in two modes:
  - Confirmed mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Potential mode: most of the secrets erase following a tamper detection are launched by software
- Any tamper detection can generate a RTC timestamp event.
- TrustZone support:
  - Tamper secure or non-secure configuration.
  - Backup registers configuration in 3 configurable-size areas:
- One read/write secure area.
- One write secure/read non-secure area.
- One read/write non-secure area.
  - Boot hardware key for secure AES, stored in backup registers, protected against read and write access.
- Tamper configuration and backup registers privilege protection
- Monotonic counter.

## 3.44 Inter-integrated circuit (I2C) interface

The devices contain four Inter integrated circuit (I2C1 to I2C4)

The I2C (inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I2C bus. It provides multimaster capability, and controls all I2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode Plus (Fm+). It is also SMBus (system management bus) and PMBus® (power management bus) compatible.

DMA can be used to reduce CPU overload.

I2C main features are:

- I2C bus specification rev03 compatibility:
  - Slave and master modes
  - Multimaster capability
  - Standard-mode (up to 100 kHz)
  - Fast-mode (up to 400 kHz)
  - Fast-mode Plus (up to 1 MHz)
  - 7- and 10-bit addressing mode

  - Multiple 7-bit slave addresses (two addresses, one with configurable mask)
  - All 7-bit addresses acknowledge mode
  - General call
  - Programmable setup and hold times
  - Easy to use event management
  - Optional clock stretching
  - Software reset
- 1-byte buffer with DMA capability
- Programmable analog and digital noise filters

The following additional features are also available, depending on the product implementation

- SMBus specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Command and data acknowledge control
  - Address resolution protocol (ARP) support
  - Host and device support
  - SMBus alert
  - Timeouts and idle condition detection
- PMBus rev 1.3 standard compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the i2c_pclk reprogramming
- Wake-up from Stop mode on address match



**Table 8. I2C implementation**

| I2C features(1) | I2C1 | I2C2 | I2C3 | I2C4 |
|---|---|---|---|---|
| 7-bit addressing mode | X | X | X | X |
| 10-bit addressing mode | X | X | X | X |
| Standard-mode (up to 100 kbit/s) | X | X | X | X |
| Fast-mode (up to 400 kbit/s) | X | X | X | X |
| Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s) | X | X | X | X |
| Independent clock | X | X | X | X |
| Wake-up from stop mode | X(2) | X(2) | X(2) | X(2) |
| SMBus/PMBus | X | X | X | X |

1. X = supported.
2. Supported only from Stop SVOS high.

## 3.45 Improved inter-integrated circuit (I3C)

The I3C interface handles communication between this device and others, such as sensors and host processor, connected on an I3C bus. An I3C bus is a two-wire, serial single-ended, multidrop bus, intended to improve a legacy I2C bus.

The I3C SDR-only peripheral implements all the features required by the MIPI® I3C specification v1.1. It can control all I3C bus-specific sequencing, protocol, arbitration, and timing, and can act as controller (formerly known as master), or as target (formerly known as slave).

When acting as controller, the I3C peripheral improves the features of the I2C interface preserving some backward compatibility: it allows an I2C target to operate on an I3C bus in legacy I2C fast-mode (Fm) or legacy I2C fast-mode plus (Fm+), provided that the latter does not perform clock stretching.

The I3C peripheral can be used with DMA, to off-load the CPU. Its main features are:

- MIPI® I3C specification v1.1, as:
  - I3C SDR-only primary controller
  - I3C SDR-only secondary controller
  - I3C SDR-only target
- I3C SCL bus clock frequency up to 12.5 MHz
- Registers configuration from the host application via the APB slave port
- Queued data transfers:
  - Transmit FIFO (TX-FIFO) for data bytes/words to be transmitted on the I3C bus
  - Receive FIFO (RX-FIFO) for received data bytes/words on the I3C bus
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Queued control/status transfers, when controller:
  - Control FIFO (C-FIFO) for control words to be sent on the I3C bus
  - Optional status FIFO (S-FIFO) for status words as received on the I3C bus
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Messages:
  - Legacy I2C read/write messages to legacy I2C targets in Fm/Fm+
  - I3C SDR read/write private messages
  - I3C SDR broadcast CCC messages
  - I3C SDR read/write direct CCC messages
- Frame-level management, when controller:
  - Optional C-FIFO and TX-FIFO preload
  - Multiple messages encapsulation
  - Optional arbitrable header generation on the I3C bus
  - HDR exit pattern generation on the I3C bus for error recovery
- Programmable bus timing, when controller:
  - SCL high and low period
  - SDA hold time
  - Bus free (minimum) time
  - Bus available/idle condition time
  - Clock stall time
- Target-initiated requests management:
  - Simultaneous support up to four targets, when controller
  - In-band interrupts, with programmable IBI payload (up to four bytes), with pending read notification support

  - Bus control request, with recovery flow support and hand-off delay
  - Hot-join mechanism
- HDR exit pattern detection when target
- Bus error management:
  - CEx with x = 0, 1, 2, 3 when controller
  - TEx with x = 0, 1, ..., 6 when target
  - Bus control switch error and recovery
  - Target reset
- Individual programmable event-based management:
  - Per-event identification with flag reporting and clear control
  - Host application notification via flag polling, and/or via interrupt with a per-event programmable enable
  - Error type identification
- Wake-up from low-power mode(s)
  - Acknowledged target request completion, when controller
  - Missed start detection, when target
  - Reset pattern detection, when target
- Multiclock domain management:
  - Separate APB clock and kernel clock, driven from independently programmed clock sources via the RCC, in addition to SCL clock
  - Minimum operating frequency for the kernel clock and the APB clock vs. the application-driven SCL clock

## 3.46 Universal synchronous/asynchronous receiver transmitter (USART/UART/LPUART)

USART offers a flexible way to perform Full-duplex data exchange with external equipments requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

### 3.46.1 USART/UART

The USART supports both synchronous one-way and Half-duplex Single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and Modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications are possible by using the DMA (direct memory access) for multibuffer configuration.

USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems

- Two internal FIFOs for transmit and receive data Each FIFO can be enabled/disabled by software and come with a status flag.
- A common programmable transmit and receive baud rate
- Dual clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection
- Programmable data word length (7, 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous Master/Slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire Half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA.
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop mode

USART extended features are:

- LIN master synchronous break send capability and LIN slave break detection capability
- 13-bit break generation and 10/11 bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16 bit duration for Normal mode
- Smartcard mode
- Support of T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
- 0.5 and 1.5 stop bits for Smartcard operation

- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

### 3.46.2 LPUART

The LPUART is an UART that enables bidirectional UART communications with a limited power consumption.

Only 32.768 kHz LSE clock is required to enable UART communications up to 9600 bauds. Higher baud rates can be reached when the LPUART is clocked by other clock sources.

Even when the microcontroller is in low-power mode, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption.

The LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption. It supports Half-duplex, Single-wire communications, and modem operations (CTS/RTS). It also supports multiprocessor communications. DMA can be used for data transmission/reception

LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 to 9600 bauds using a 32.768 kHz clock source.
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data. Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual clock domain with dedicated kernel clock for peripherals independent from PCLK.
- Programmable data word length (7, 8, or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (one or two stop bits)
- Single-wire Half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA.
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wake up from Mute mode by idle line detection or address mark detection
- Wake-up from Stop mode

**Table 9. Instance implementation**

| Instance | STM32N6xx |
|---|---|
| USART1 | Full |
| USART2 | Full |
| USART3 | Full |
| USART6 | Full |
| USART10 | Full |
| UART4 | Basic |
| UART5 | Basic |
| UART7 | Basic |
| UART8 | Basic |
| UART9 | Basic |
| LPUART1 | Low-power |

**Table 10. USART/LPUART features**

| Mode or feature(1) | Full feature | Basic feature | Low-power feature |
|---|---|---|---|
| Hardware flow control for modem | X | X | X |
| Continuous communication using DMA | X | X | X |
| Multiprocessor communication | X | X | X |
| Synchronous mode (master/slave) | X | - | - |
| Smartcard mode | X | - | - |
| Single-wire half-duplex communication | X | X | X |
| IrDA SIR ENDEC block | X | X | - |
| LIN mode | X | X | - |
| Dual-clock domain | X | X | X |
| Receiver timeout interrupt | X | X | - |
| Modbus communication | X | X | - |
| Auto baud rate detection | X | X | - |
| Driver enable | X | X | X |
| USART data length | 7, 8 and 9 bits | | |
| Tx/Rx FIFO | X | X | X |
| Tx/Rx FIFO size (bytes) | 16 | | |
| Wake-up from low-power mode | X(2) | X(2) | X(2) |

1. X = supported.
2. Wake-up supported from Stop mode.

## 3.47 Serial peripheral interface (SPI)

The devices embed three serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to setup communication with concrete slave and to assure it handles the data flow properly. The Motorola® data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4- to 32-bit data size selection or fixed to 8- and 16-bit only
- Multi master or multi slave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency divided by two, or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO x MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- Support of SPI Motorola® and Texas Instruments® formats
- Hardware CRC feature can secure communication at the end of transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 16x or 8x 8-bit embedded Rx and TxFIFOs with DMA capability
- Programmable number of data in transaction
- Configurable FIFO thresholds (data packing)
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Autonomous functionality in Stop modes (handling of the transaction flow and required clock distribution) with wakeup from stop capability
- Optional status pin RDY signalizing the slave device ready to handle the data flow.

**Table 11. SPI features**

| Feature | SPI1, SPI2, SPI3, SPI6 | SPI4, SPI5 |
|---|---|---|
| Data and CRC size | Configurable from 4 to 32 bits | Configurable from 4 to 16 bits |
| CRC computation | CRC polynomial length, configurable from 5 to 33 bits | CRC polynomial length, configurable from 9 to 17 bits |
| Size of FIFOs | 16x8 bits | 8x8 bits |
| Number of data control (TSIZE) | Up to 65536 | |
| I2S feature | Yes | No |
| Autonomous in Stop modes with wake-up capability | No | |
| Autonomous in Standby mode | No | |

## 3.48 Serial audio interface (SAI)

The SAI offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications can be targeted. I2S standards, LSB or MSB-justified, PCM/DSP, TDM, and AC'97 protocols can be addressed. SPDIF output is offered when the audio block is configured as a transmitter.

The SAI contains two independent audio sub-blocks, each has its own clock generator and I/O line controller.

The SAI works in master or slave configuration. The audio sub-blocks act as receiver or transmitter, and work synchronously or not (with respect to the other one).

The SAI can be connected with other SAIs, to work synchronously.

SAI main features are:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Possible synchronization between multiple SAIs.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97
- PDM interface, supporting up to four microphone pairs
- SPDIF output available if required.
- Up to 16 slots available with configurable size.
- Number of bits by frame can be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.

- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection,
  - Anticipated frame synchronization signal detection in slave mode,
  - Late frame synchronization signal detection in slave mode,
  - Codec not ready for the AC’97 mode in reception.
- Interrupt sources when enabled:
  - Errors
  - FIFO requests.
- 2-channel DMA interface.

**Table 12. SAI features(1)**

| Feature | SAI1 | SAI2 |
|---|---|---|
| I2S, LSB- or MSB-justified, PCM/DSP, TDM, AC’97 | X | X |
| FIFO size | 8 words | |
| SPDIF | X | X |
| PDM | X(2) | - |

1. ‘X’ = supported, ‘-’ = not supported.
2. Only signals D[3:1] and CK[2:1] are available.

## 3.49 SPDIF receiver interface (SPDIFRX)

The SPDIFRX interface handles S/PDIF audio protocol. Its main features are:

- Up to four inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 8 to 192 kHz supported
- Supports audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

## 3.50 Management data input/output (MDIOS)

An MDIO bus can be useful in systems where a master chip needs to manage (configure and get status data from) one or multiple slave chips.

The bus protocol uses only two signals:

1. MDC: the management data clock
2. MDIO: the data line carrying the opcode (write or read), the slave (port) address, the MDIOS register address, and the data

In each transaction, the master either reads the contents of an MDIOS register in one of itsslaves, or it writes data to an MDIOS register in one of its slaves.

The MDIOS peripheral serves as a slave interface to a MDIO bus. A MDIO master can use the MDC/MDIO lines to write and read 32 16-bit MDIOS registers, which are held in the MDIOS. These MDIOS registers are managed by the firmware. This allows the MDIO master to configure the application running on the STM32 and get status information from it.

The MDIOS can operate in Stop mode, optionally waking up the device if the MDIO master performs a read or a write to one of its MDIOS registers.

The MDIOS includes the following features:

- 32 MDIOS register addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIOS read-only output data registers
  - 32 x 16-bit firmware read-only, MDIOS write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIOS register write
  - MDIOS register read
  - MDIOS protocol error
- Able to operate in and wake up from Stop mode

## 3.51 Controller area network with flexible data rate (FDCAN)

The controller area network (CAN) subsystem consists of three CAN modules, a shared message RAM and a clock calibration unit. Refer to the product memory organization for the base address of each of them.

FDCAN modules are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

In addition, the first CAN module FDCAN1 supports time triggered CAN (TTCAN), specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10 Kbyte message RAM implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TTCAN). This message RAM is shared between the FDCAN modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for each FDCAN from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

## 3.52 USB on-the-go highspeed (OTG)

Reference is made to the following documents:

- USB On-The-Go Supplement, Revision 2.0
- Universal Serial Bus Revision 2.0 Specification
- USB 2.0 Link Power Management Addendum Engineering Change Notice to the USB 2.0 specification, July 16, 2007
- Errata for USB 2.0 ECN: Link Power Management (LPM) - 7/2007
- Battery Charging Specification, Revision 1.2

The USB OTG is a dual-role device (DRD) controller that supports both device and host functions and is fully compliant with the On-The-Go Supplement to the USB 2.0 Specification. It can also be configured as a host-only or device-only controller, fully compliant with the USB 2.0 Specification. OTG supports the speeds defined in *Table 13*.

**Table 13. Supported OTG speeds**

| Mode | HS (480 Mbit/s) | FS (12 Mbit/s) | LS (1.5 Mbit/s) |
|---|---|---|---|
| Host mode | X | X | X |
| Device mode | X | X | - |

## 3.53 USB HS PHY controller (USBPHYC)

There are two near-identical instances, namely USBPHYC1 (associated with OTG1), and USBPHYC2 (associated with OTG2).

For a more complete system view of the USB controllers and PHYs, refer to the block diagram of the main OTG controller. This controller handles general and miscellaneous control of the OTG PHYs.

The main features are:

- PLL configuration
- Trimming of the electrical parameters (should this be required)

## 3.54 USB Type-C / USB Power Delivery controller (UCPD)

The device embeds one controller (UCPD) compliant with USB Type-C Cable and Connector Specification release 2.0 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB power delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- “Dead battery” support
- USB power delivery message transmission and reception
- FRS (fast role swap) support

The digital controller handles:

- USB Type-C level detection with debounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB power delivery payload, generating interrupts (DMA compatible)
- USB power delivery timing dividers (including a clock prescaler)
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB power delivery messages and FRS signaling.

## 3.55 Ethernet (ETH): gigabit media access control (GMAC) with DMA controller



The Ethernet peripheral enables to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2015 standard.

The peripheral is configurable to meet the needs of a large variety of consumer and industrial applications, including AV nodes and TSN (time sensitive networking) nodes.

The Ethernet peripheral embeds a dedicated DMA for direct memory interface, a media access controller (MAC) and a PHY interface block supporting several formats.

The Ethernet peripheral is compliant with the following standards:

- IEEE 802.3-2015 for Ethernet MAC and media independent interface (MII)
- IEEE 1588-2008 for precision networked clock synchronization (PTP)
- IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic
- IEEE 802.3az-2010 for Energy Efficient Ethernet (EEE)
- AMBA 2.0 for AHB slave port
- AMBA4 for AXI master port
- RGMII specification version 2.6 from HP/Marvell
- RMII specification version 1.2 from RMII consortium

**Caution:** The gigabit media independent interface (GMII) is only available internally to supply the RGMII adapter. No GMII signals are available off-chip

## 3.56 Development support

### 3.56.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### 3.56.2 Embedded Trace Macrocell

The Arm Embedded Trace Macrocell (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

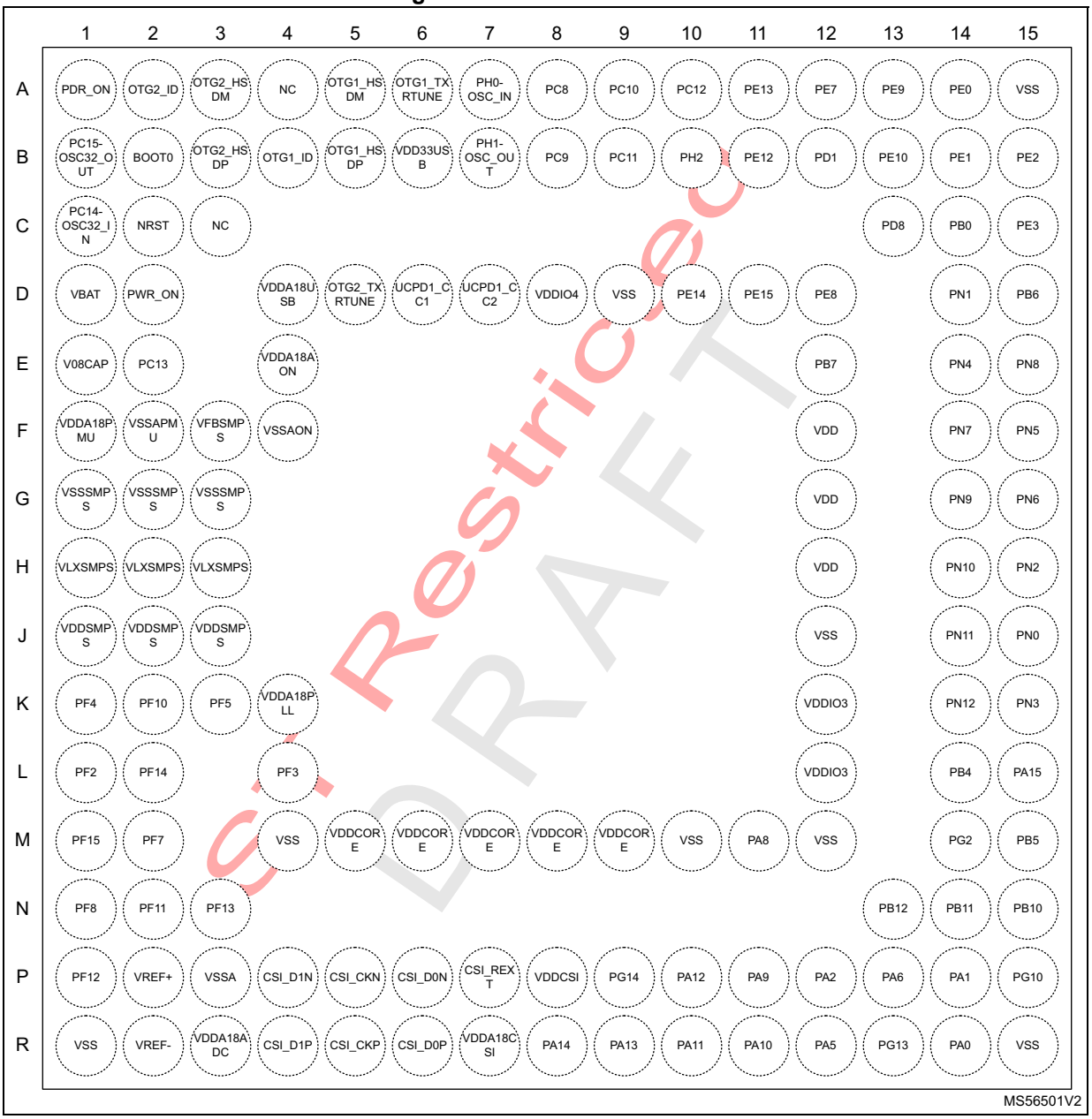
Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The ETM operates with third party debugger software tools.

# 4 Pinout, pin description and alternate functions

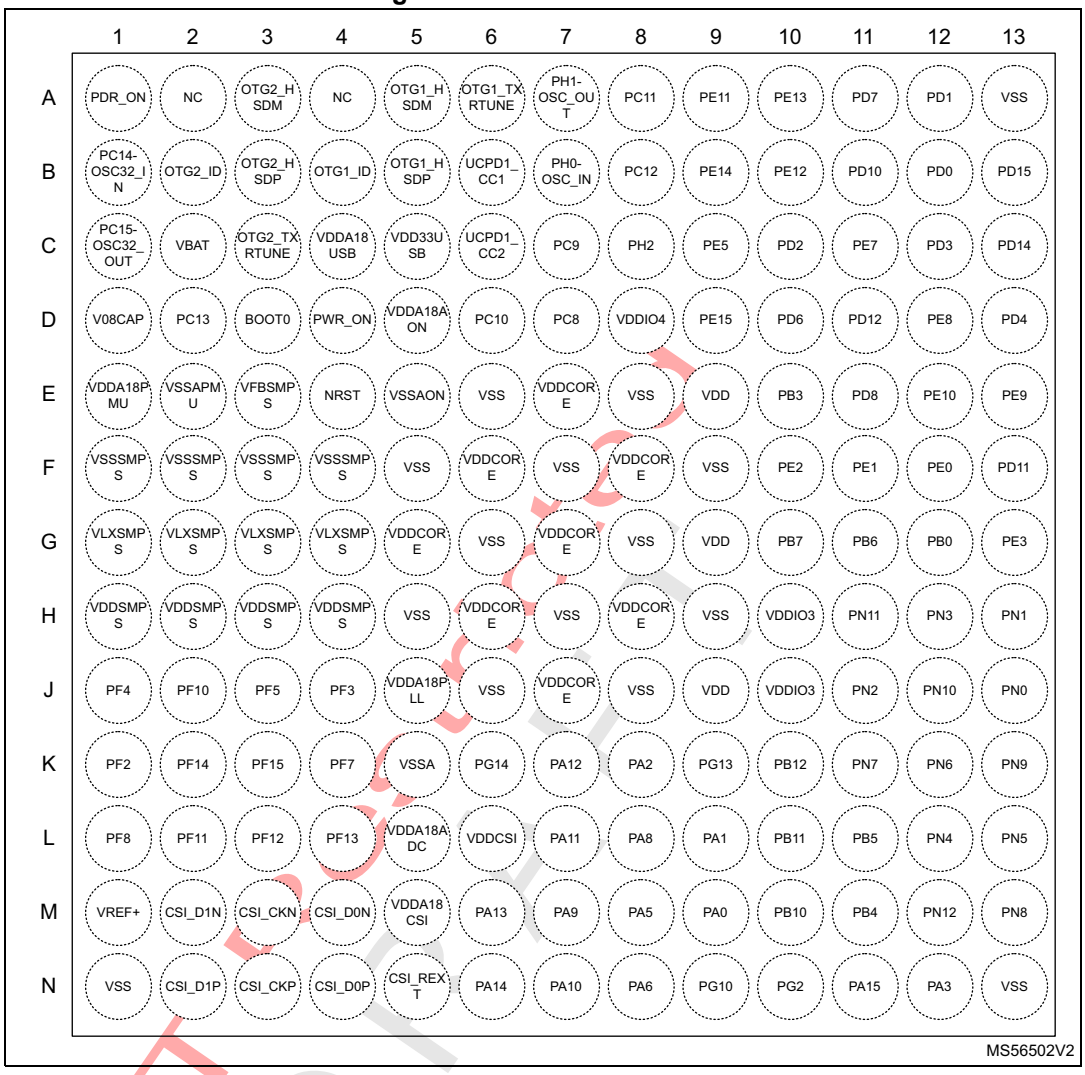
## 4.1 Pinout/ballout schematics

**Figure 7. VFBGA142 ballout**




1. The above figure shows the package top view.

**Figure 8. VFBGA169 ballout**

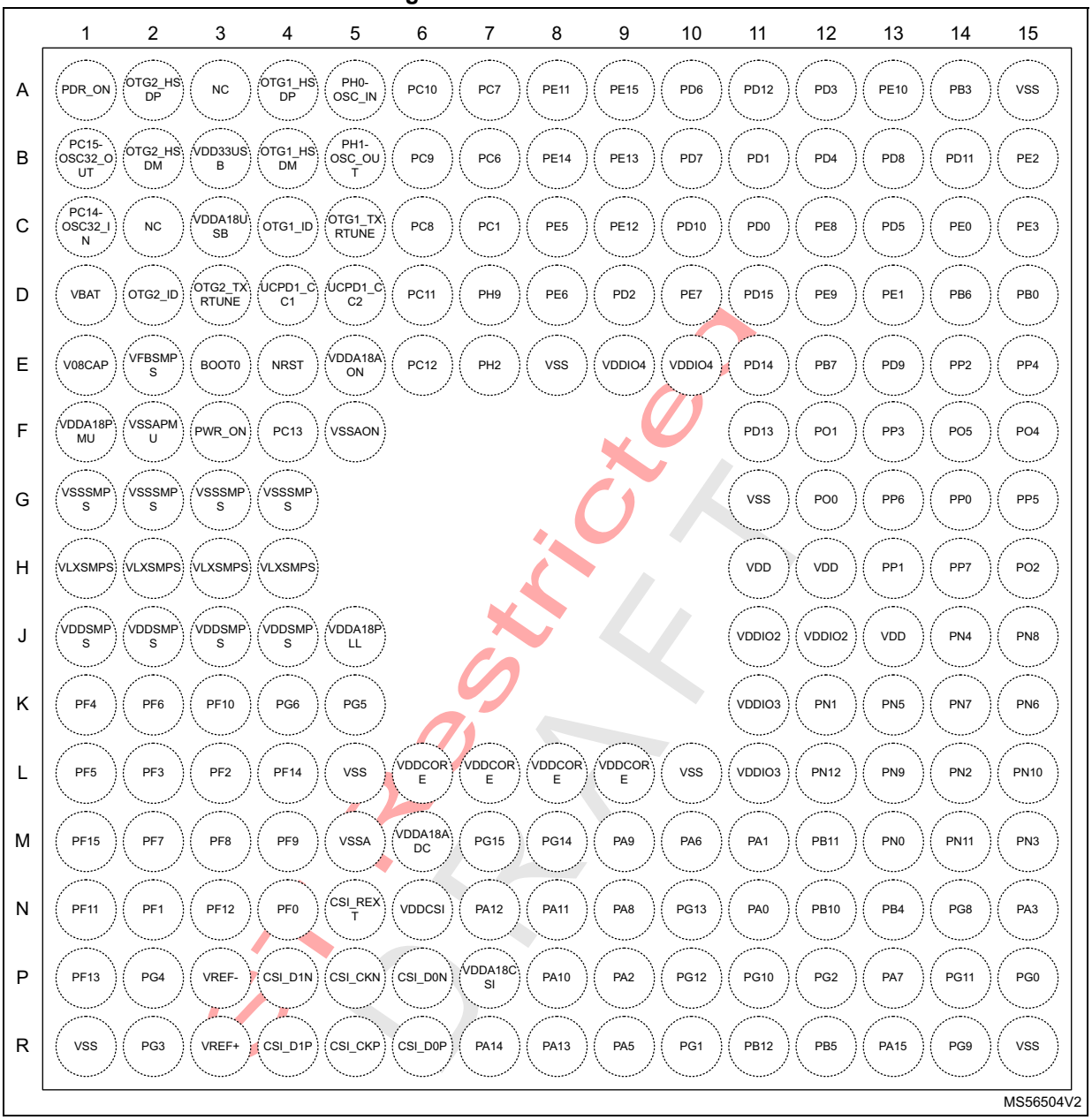



1. The above figure shows the package top view.

**Figure 9. VFBGA178 ballout**

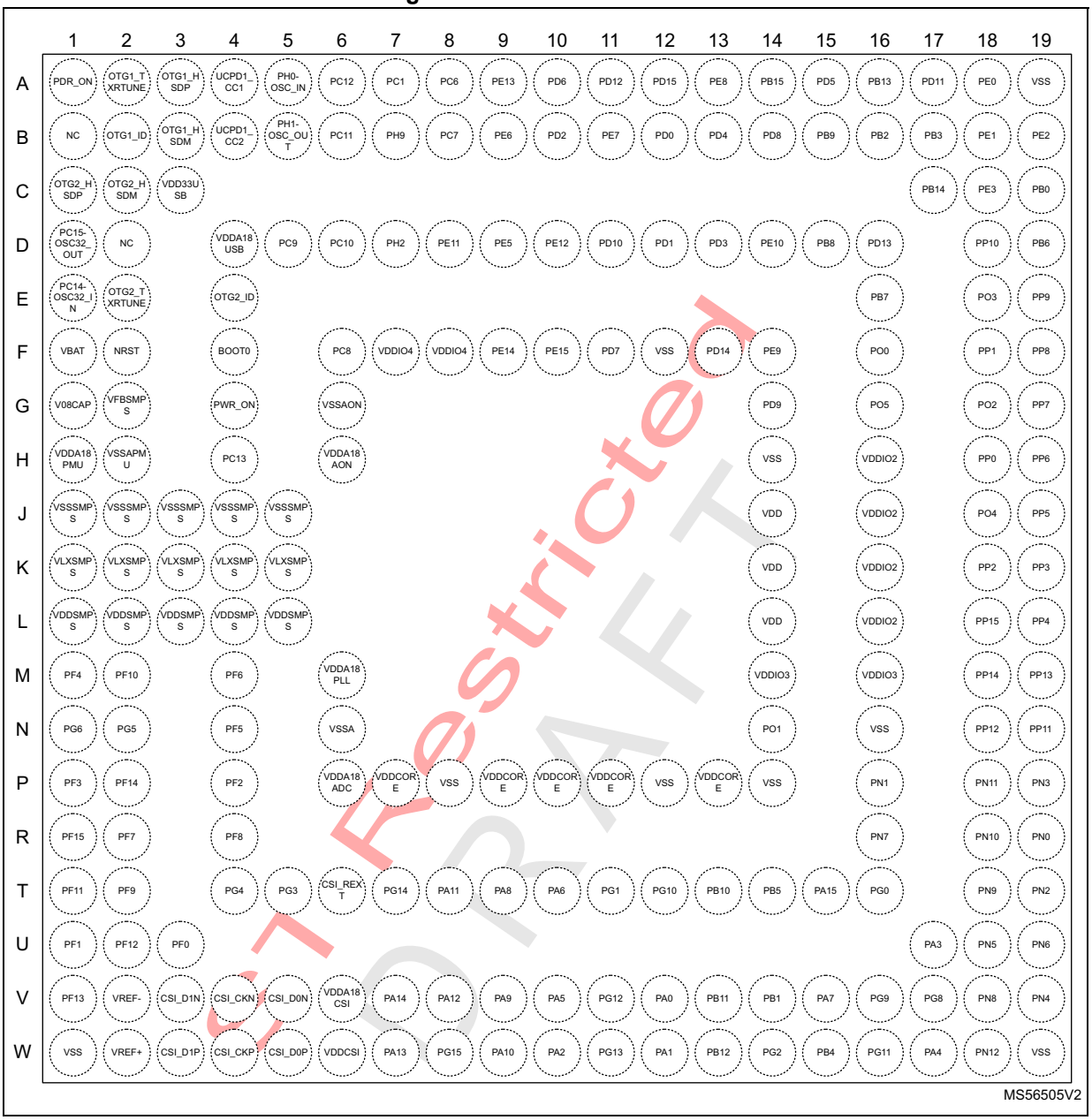

1. The above figure shows the package top view.

**Figure 10. VFBGA198 ballout**



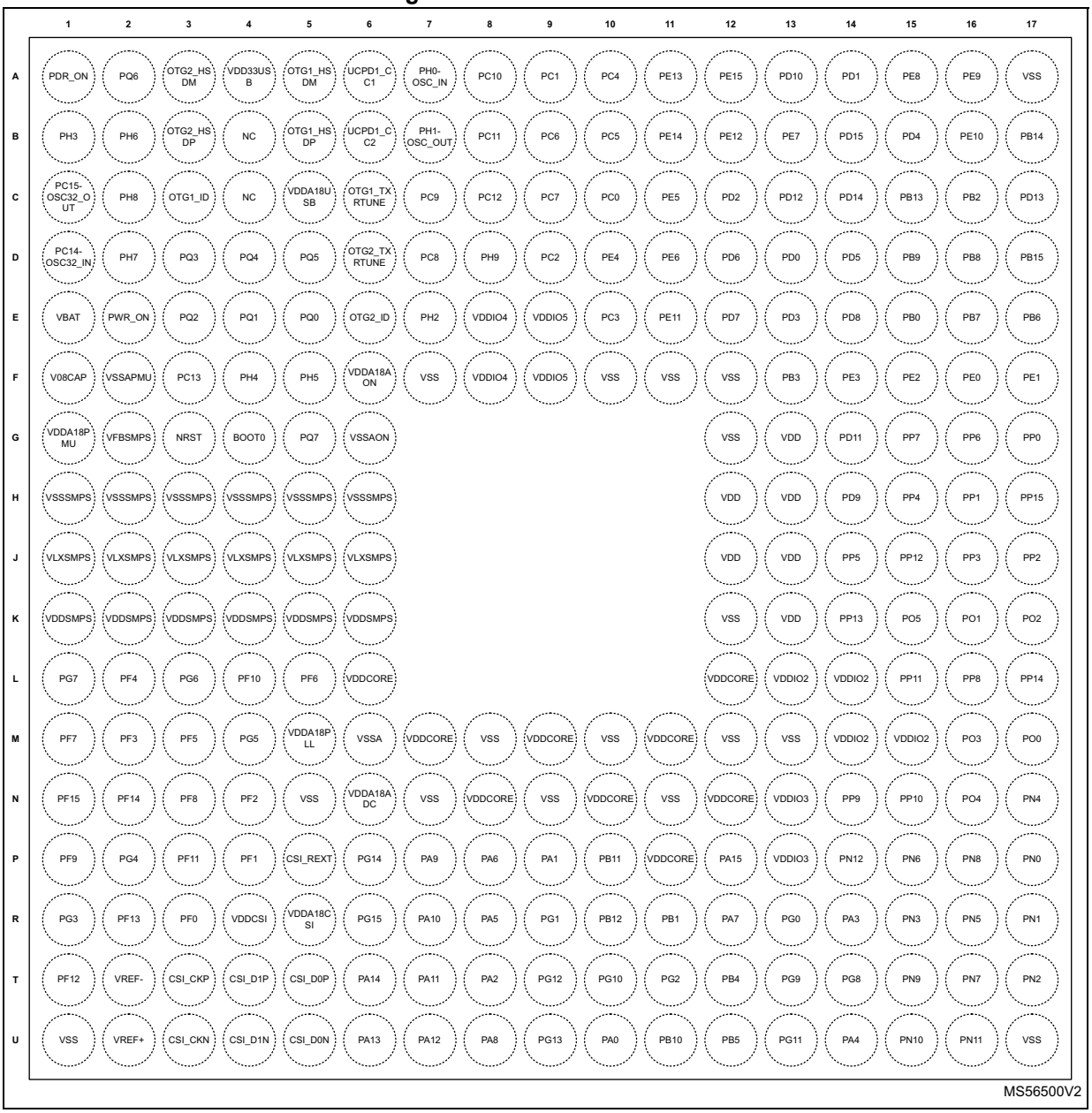

1. The above figure shows the package top view.

**Figure 11. VFBGA223 ballout**




1. The above figure shows the package top view.

**Figure 12. VFBGA264 ballout**




1. The above figure shows the package top view.

## 4.2 Pin description

**Table 14. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | S | Supply pin |
| | | I | Input only pin |
| | | I/O | Input/output pin |
| I/O structure | | FT | 5 V-tolerant I/O |
| | | TT | 3.6 V-tolerant I/O |
| | | DSI | 1.2 V I/O for DSI interface |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| | | **Option for TT or FT I/Os(1)** | |
| | | _a | I/O, with analog switch function supplied by $V_{DDA}$ |
| | | _c | I/O with USB Type-C power delivery function |
| | | _d | I/O with USB Type-C power delivery dead battery function |
| | | _f | I/O, Fm+ capable |
| | | _h | I/O with high speed low voltage mode |
| | | _p | I/O with differential clock capability CLKP/CLKN |
| | | _s | I/O supplied only by $V_{DDIO2}$ |
| | | _t | I/O with tamper function functional in VBAT mode |
| | | _u | I/O, with USB function supplied by $V_{DDUSB}$ |
| | | _v | I/O very high-speed capable |
| Notes | | Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset. | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

1. The related I/O structures in the following table are a concatenation of various options. Examples: FT_hat, FT_fs, FT_u, TT_a.

**Table 15. STM32N657xx pin description**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| R2 | - | N1 | P3 | V2 | T2 | VREF- | I/O | - | - | - | -- |
| P2 | M1 | M1 | R3 | W2 | U2 | VREF+ | I/O | - | - | - | - |
| D2 | D4 | E3 | F3 | G4 | E2 | PWR_ON | I | - | - | - | - |
| A1 | A1 | A1 | A1 | A1 | A1 | PDR_ON | I | - | - | - | - |
| B2 | D3 | D3 | E3 | F4 | G4 | BOOT0 | I | - | - | - | - |
| C2 | E4 | E4 | E4 | F2 | G3 | NRST | I | - | - | - | - |
| P5 | M3 | N3 | P5 | V4 | U3 | CSI_CKN | I | - | - | - | - |
| R5 | N3 | P3 | R5 | W4 | T3 | CSI_CKP | I | - | - | - | - |
| P6 | M4 | N4 | P6 | V5 | U5 | CSI_D0N | I | - | - | - | - |
| R6 | N4 | P4 | R6 | W5 | T5 | CSI_D0P | I | - | - | - | - |
| P4 | M2 | N2 | P4 | V3 | U4 | CSI_D1N | I | - | - | - | - |
| R4 | N2 | P2 | R4 | W3 | T4 | CSI_D1P | I | - | - | - | - |
| P7 | N5 | N5 | N5 | T6 | P5 | CSI_REXT | I/O | - | - | - | - |
| A3 | A3 | A2 | B2 | C2 | A3 | OTG2_HSDM | I/O | - | - | - | - |
| B3 | B3 | B2 | A2 | C1 | B3 | OTG2_HSDP | I/O | - | - | - | - |
| A2 | B2 | C5 | D2 | E4 | E6 | OTG2_ID | I/O | - | - | - | - |
| C3 | A2 | C4 | C2 | D2 | C4 | NC | - | - | - | - | - |
| D5 | C3 | B4 | D3 | E2 | D6 | OTG2_TXRTUNE | I/O | - | - | - | - |
| A5 | A5 | A5 | B4 | B3 | A5 | OTG1_HSDM | I/O | - | - | - | - |
| B5 | B5 | B5 | A4 | A3 | B5 | OTG1_HSDP | I/O | - | - | - | - |
| B4 | B4 | B3 | C4 | B2 | C3 | OTG1_ID | I/O | - | - | - | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| A4 | A4 | A3 | A3 | B1 | B4 | NC | - | - | - | - | - |
| A6 | A6 | D5 | C5 | A2 | C6 | OTG1_TXRTUNE | I/O | - | - | - | - |
| D6 | B6 | A6 | D4 | A4 | A6 | UCPD1_CC1 | I/O | - | - | - | - |
| D7 | C6 | B6 | D5 | B4 | B6 | UCPD1_CC2 | I/O | - | - | - | - |
| F3 | E3 | D2 | E2 | G2 | G2 | VFBSMPS | | - | - | - | - |
| R14 | M9 | P10 | N11 | V12 | U10 | PA0 | I/O | - | - | TIM2_CH1, TIM5_CH1, TIM9_CH1, TIM15_BKIN, SPI6_NSS/I2S6_WS, USART2_CTS/USART2_NSS, UART4_TX, SAI2_SD_B, SDMMC2_CMD, FMC_AD7/FMC_D7, LCD_G3, HDP0 | ADC12_INP0, ADC12_INN1, WKUP1 |
| P14 | L9 | L9 | M11 | W12 | P9 | PA1 | I/O | - | - | TIM2_CH2, TIM5_CH2, LPTIM3_IN1, TIM15_CH1N, USART2_RTS, UART4_RX, DCMIPP_D0/DCMI_D0/PSSI_D0, SAI2_MCLK_B, FMC_AD6/FMC_D6, LCD_G2, HDP1 | ADC12_INP1 |
| P12 | K8 | N8 | P9 | W10 | T8 | PA2 | I/O | - | - | TIM2_CH3, TIM5_CH3, LPTIM3_IN2, TIM15_CH1, USART2_TX, SAI2_SCK_B, MDIOS_MDIO, FMC_AD5/FMC_D5, LCD_B7, HDP2 | ADC12_INP14, WKUP2 |
| - | N12 | K11 | N15 | U17 | R14 | PA3 | I/O | - | - | TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, FMC_A17/FMC_ALE, EVENTOUT | - |
| - | - | - | - | W17 | U14 | PA4 | I/O | | - | SPI5_MOSI, USART6_RX, DCMIPP_D3/DCMI_D3/PSSI_D3, FMC_A13, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| R12 | M8 | M8 | R9 | V10 | R8 | PA5 | I/O | - | - | PWR_CSTOP, TIM2_CH1, TIM2_ETR, TIM9_CH2, I3C1_SCL, SPI1_SCK/I2S1_CK, SPI6_SCK/I2S6_CK, DCMIPP_D8/DCMI_D8/PSSI_D8, TIM10_CH1, FMC_NOE, LCD_CLK, HDP5 | ADC2_INP18 |
| P13 | N8 | L8 | M10 | T10 | P8 | PA6 | I/O | - | - | BOOT1, TIM1_BKIN, TIM3_CH1, LPTIM3_ETR, I3C1_SDA, SPI1_MISO/I2S1_SDI, SPI6_MISO/I2S6_SDI, DCMIPP_PIXCLK/DCMI_PIXCLK/PSSI_PDCK, TIM13_CH1, MDIOS_MDC, LCD_B7, LCD_HSYNC, HDP6 | ADC12_INP3 |
| - | - | P12 | P13 | V15 | R12 | PA7 | I/O | - | - | TIM1_CH1N, TIM3_CH2, SPI1_MOSI/I2S1_SDO, USART1_RX, SPI6_MOSI/I2S6_SDO, LCD_R4, TIM14_CH1, FMC_RNB, LCD_B1, HDP7 | - |
| M11 | L8 | P8 | N9 | T9 | U8 | PA8 | I/O | - | - | MCO1, TIM1_CH1, I3C2_SCL, I2C3_SCL, USART1_CK, TIM11_CH1, UART7_RX, FMC_AD4/FMC_D4, LCD_B6, HDP0 | ADC12_INP5 |
| P11 | M7 | M7 | M9 | V9 | P7 | PA9 | I/O | - | - | TIM1_CH2, I3C2_SDA, LPUART1_TX, I2C3_SDA, SPI2_SCK/I2S2_CK, USART1_TX, DCMIPP_D0/DCMI_D0/PSSI_D0, FMC_AD3/FMC_D3, LCD_B5, HDP1 | ADC12_INP10 |
| R11 | N7 | N7 | P8 | W9 | R7 | PA10 | I/O | - | - | PWR_CSLEEP, TIM1_CH3, LPUART1_RX, USART1_RX, DCMIPP_D1/DCMI_D1/PSSI_D1, MDIOS_MDIO, FMC_AD2/FMC_D2, LCD_B4, HDP2 | ADC12_INP11, ADC12_INN10 |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| R10 | L7 | M6 | N8 | T8 | T7 | PA11 | I/O | - | - | TIM1_CH4, LPUART1_CTS, SPI2_NSS/I2S2_WS, FDCAN1_RX, USART1_CTS/USART1_NSS, UART4_RX, FMC_AD1/FMC_D1, LCD_B3, HDP3 | ADC12_INP12, ADC12_INN11 |
| P10 | K7 | L6 | N7 | V8 | U7 | PA12 | I/O | - | - | TIM1_ETR, LPUART1_RTS, SPI2_SCK/I2S2_CK, FDCAN1_TX, USART1_RTS, UART4_TX, SAI2_FS_B, FMC_AD0/FMC_D0, LCD_B2, HDP4 | ADC12_INP13, ADC12_INN12 |
| R9 | M6 | P7 | R8 | W7 | U6 | PA13 (JTMS/SWDIO) | I/O | - | - | JTMS/SWDIO, HDP5 | - |
| R8 | N6 | P6 | R7 | V7 | T6 | PA14 (JTCK/SWCLK) | I/O | - | - | JTCK/SWCLK, HDP6 | - |
| L15 | N11 | N12 | R13 | T15 | P12 | PA15(JTDI) | I/O | - | - | JTDI, TIM2_CH1, TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS/I2S6_WS, UART4_RTS, UART7_TX, FMC_D15/FMC_AD15, LCD_R5, HDP7 | - |
| C14 | G12 | G14 | D15 | C19 | E15 | PB0 | I/O | - | - | TRACED1, TIM1_CH4, SAI1_D2, ADF1_SDI0, MDF1_SDI2, SPI4_NSS, SAI1_FS_A, TIM15_CH1N, DCMIPP_D4/DCMI_D4/PSSI_D4, FMC_D13/FMC_AD13, EVENTOUT | - |
| - | - | - | - | V14 | R11 | PB1 | I/O | - | - | TIM1_CH3N, TIM3_CH4, TIM9_CH2, FDCAN2_TX, USART2_TX, FMC_NOE, [RNG_S2], LCD_R1, HDP1 | - |
| - | - | E13 | - | B16 | C16 | PB2 | I/O | - | - | RTC_OUT2, TIM1_CH1, SAI1_D1, ADF1_SDI0, MDF1_SDI1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, FMC_D2/FMC_AD2, LCD_B2, HDP2 | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | E10 | E12 | A14 | B17 | F13 | PB3 | I/O | - | - | TRACECLK, TIM1_CH4N, GFXTIM_FCKCAL, MDF1_CKI1, USART1_CK, SAI2_FS_B, FMC_NBL1, GFXTIM_LCKCAL, FMC_A23, HDP0 | - |
| L14 | M11 | L11 | N13 | W15 | T12 | PB4 (NJTRST) | I/O | - | - | NJTRST, TIM16_BKIN, TIM3_CH1, LPTIM4_ETR, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO/I2S6_SDI, DCMIPP_VSYNC/DCMI_VSYNC/PSSI_RDY, UART7_TX, SDMMC2_D3, FMC_D13/FMC_AD13, LCD_R3, HDP4 | - |
| M15 | L11 | M11 | R12 | T14 | U12 | PB5 (JTDO/TRACESWO) | I/O | - | - | JTDO/TRACESWO, TIM17_BKIN, TIM3_CH2, LPTIM4_OUT, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, FDCAN2_RX, SPI3_MOSI/I2S3_SDO, SPI6_MOSI/I2S6_SDO, DCMIPP_D10/DCMI_D10/PSSI_D10, UART5_RX, FMC_D12/FMC_AD12, LCD_R2, HDP5 | - |
| D15 | G11 | H14 | D14 | D19 | E17 | PB6 | I/O | - | - | TRACED2, SAI1_CK2, ADF1_CCK1, MDF1_CCK1, SPI4_MISO, SAI1_SCK_A, TIM15_CH1, DCMIPP_D6/DCMI_D6/PSSI_D6, FMC_D14/FMC_AD14, EVENTOUT | - |
| E12 | G10 | H13 | E12 | E16 | E16 | PB7 | I/O | - | - | TRACED3, TIM1_BKIN2, SAI1_D1, ADF1_SDI0, MDF1_SDI1, SPI4_MOSI, SAI1_SD_A, TIM15_CH2, DCMIPP_D7/DCMI_D7/PSSI_D7, SAI2_MCLK_B, FMC_D15/FMC_AD15, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | - | - | D15 | D16 | PB8 | I/O | - | - | SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX1_IN3, DCMIPP_VSYNC/DCMI_VSYNC/PSSI_RDY, SAI2_FS_B, SDMMC2_D0, FMC_D1/FMC_AD1, EVENTOUT | - |
| - | - | - | - | B15 | D15 | PB9 | I/O | - | - | LPTIM1_IN2, SPI1_SCK/I2S1_CK, USART10_TX, SPDIFRX1_IN0, DCMIPP_D3/DCMI_D3/PSSI_D3, SDMMC2_D2, FMC_D3/FMC_AD3, EVENTOUT | - |
| N15 | M10 | P11 | N12 | T13 | U11 | PB10 | I/O | - | - | TIM2_CH3, I3C2_SCL, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, FMC_D11/FMC_AD11, LCD_G7, HDP2 | ADC12_INP8, ADC12_INN4 |
| N14 | L10 | L10 | M12 | V13 | P10 | PB11 | I/O | - | - | TIM2_CH4, I3C2_SDA, LPTIM2_ETR, I2C2_SDA, USART3_RX, FMC_D10/FMC_AD10, LCD_G6, HDP3 | ADC12_INP4 |
| N13 | K10 | M10 | R11 | W13 | R10 | PB12 | I/O | - | - | TIM1_BKIN, LPTIM2_IN2, I2C2_SMBA, SPI2_NSS/I2S2_WS, FDCAN2_RX, USART3_CK, UART5_RX, FMC_D9/FMC_AD9, LCD_G5, HDP4 | - |
| - | - | - | - | A16 | C15 | PB13 | I/O | - | - | TRACED0, LPTIM1_CH1, TIM8_CH3N, SPI6_SCK/I2S6_CK, USART10_CTS/USART10_NSS, USART6_CTS/USART6_NSS, SDMMC2_D6, FMC_D5/FMC_AD5, LCD_CLK, EVENTOUT | - |
| - | - | - | - | C17 | B17 | PB14 | I/O | - | - | LPTIM1_CH2, TIM8_CH4N, USART10_CK, USART6_CTS/USART6_NSS, DCMIPP_D10/DCMI_D10/PSSI_D10, FMC_D7/FMC_AD7, LCD_HSYNC, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | - | - | A14 | D17 | PB15 | I/O | - | - | SPI6_NSS/I2S6_WS, USART6_RTS, SPDIFRX1_IN2, FMC_D0/FMC_AD0, LCD_G4, EVENTOUT | - |
| - | - | - | - | - | C10 | PC0 | I/O | - | - | TIM2_CH2, LPTIM4_IN1, MDF1_CKI1, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK/I2S6_CK, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, UART7_RX, SDMMC2_D2, FMC_D14/FMC_AD14, LCD_R4, HDP3 | - |
| - | - | B8 | C7 | A7 | A9 | PC1 | I/O | - | - | TIM17_CH1, TIM4_CH4, I2C1_SDA, SPI2_NSS/I2S2_WS, FDCAN1_TX, I3C1_SDA, UART4_TX, DCMIPP_D7/DCMI_D7/PSSI_D7, SDMMC1_D5, SDMMC2_D5, SDMMC1_CDIR, HDP1 | - |
| - | - | - | - | - | D9 | PC2 | I/O | - | - | SAI1_D1, ADF1_SDI0, MDF1_SDI1, SPI3_MOSI/I2S3_SDO, SAI1_SCK_A, USART2_RX, DCMIPP_D13/DCMI_D13/PSSI_D13, SDMMC2_CK(boot), FMC_NE3, FMC_RNB, EVENTOUT | - |
| - | - | - | - | - | E10 | PC3 | I/O | - | - | SPI1_MOSI/I2S1_SDO, USART2_CK, SPDIFRX1_IN0, DCMIPP_D2/DCMI_D2/PSSI_D2, SDMMC2_CMD(boot), FMC_D8/FMC_AD8, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | - | - | - | A10 | PC4 | I/O | - | - | TIM1_CH2N, TIM12_CH1, LPTIM2_CH2, USART1_TX, SPI2_MISO/I2S2_SDI, USART3_RTS, UART4_RTS, LCD_VSYNC, SDMMC2_D0(boot), FMC_NE1, LCD_DE, HDP6 | - |
| - | - | - | - | - | B10 | PC5 | I/O | - | - | SPI1_NSS/I2S1_WS, DCMIPP_D2/DCMI_D2/PSSI_D2, SAI2_SD_B, SDMMC2_D1, FMC_NWE, EVENTOUT | - |
| - | - | A8 | B7 | A8 | B9 | PC6 | I/O | - | - | TIM1_CH1, TIM3_CH1, TIM9_CH1, I2S2_MCK, USART6_TX, DCMIPP_D1/DCMI_D1/PSSI_D1, SDMMC1_D6, SDMMC2_D6, SDMMC1_D0DIR, HDP6 | - |
| - | - | A9 | A7 | B8 | C9 | PC7 | I/O | - | - | DBTRGIO, TIM16_CH1N, TIM3_CH2, TIM9_CH2, I2S3_MCK, USART6_RX, DCMIPP_D1/DCMI_D1/PSSI_D1, SDMMC1_D7, SDMMC2_D7, SDMMC1_D123DIR, HDP7 | - |
| A8 | D7 | C6 | C6 | F6 | D7 | PC8 | I/O | - | - | TRACED1, TIM3_CH3, I2C3_SMBA, UCPD1_FRSTX1, USART6_CK, DCMIPP_D2/DCMI_D2/PSSI_D2, SDMMC1_D0(boot), UART5_RTS, FMC_NE4, LCD_B0, HDP0 | - |
| B8 | C7 | D6 | B6 | D5 | C7 | PC9 | I/O | - | - | MCO2, TIM3_CH4, I2C3_SDA, AUDIOCLK, UCPD1_FRSTX2, USART6_RX, DCMIPP_D3/DCMI_D3/PSSI_D3, SDMMC1_D1, UART5_CTS, LCD_B3, HDP1 | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| A9 | D6 | D8 | A6 | D6 | A8 | PC10 | I/O | - | - | TIM1_BKIN, I3C2_SCL, I2C4_SCL, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, DCMIPP_D14/PSSI_D14, SDMMC1_D2, FMC_CLK, HDP2 | - |
| B9 | A8 | C7 | D6 | B6 | B8 | PC11 | I/O | - | - | I3C2_SDA, I2C4_SDA, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, DCMIPP_D4/DCMI_D4/PSSI_D4, SDMMC1_D3, HDP3 | - |
| A10 | B8 | D7 | E6 | A6 | C8 | PC12 | I/O | - | - | TRACED3, TIM1_CH4, TIM15_CH1, SPI6_SCK/I2S6_CK, SPI3_MOSI/I2S3_SDO, USART3_CK, DCMIPP_D9/DCMI_D9/PSSI_D9, SDMMC1_CK(boot), UART5_TX, FMC_NL, HDP4 | - |
| E2 | D2 | C3 | F4 | H4 | F3 | PC13 | I/O | - | - | HDP5 | TAMP_IN1/TAMP_OUT2, RTC_OUT1/RTC_TS, WKUP3 |
| C1 | B1 | B1 | C1 | E1 | D1 | PC14-OSC32_IN (OSC32_IN) | I/O | - | - | - | OSC32_IN |
| B1 | C1 | C1 | B1 | D1 | C1 | PC15-OSC32_OUT (OSC32_OUT) | I/O | - | - | | OSC32_OUT |
| - | B12 | A12 | C11 | B12 | D13 | PD0 | I/O | - | - | TIM1_ETR, FDCAN1_RX, UART9_CTS, UART4_RX, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, FMC_A6, FMC_A22, EVENTOUT | - |
| B12 | A12 | B12 | B11 | D12 | A14 | PD1 | I/O | - | - | FDCAN1_TX, UART4_TX, ETH1_MDC, FMC_A7, FMC_A23, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | C10 | E10 | D9 | B10 | C12 | PD2 | I/O | - | - | TRACED0, TIM1_CH3, SAI1_D1, ADF1_SDI0, MDF1_SDI1, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, TIM15_CH1N, MDIOS_MDC, SDMMC2_CK, FMC_A0, FMC_A16/FMC_CLE, HDP1 | WKUP4 |
| - | C12 | A13 | A12 | D13 | E13 | PD3 | I/O | - | - | I2C2_SMBA, USART10_RX, USART6_CTS, DCMIPP_D14/PSSI_D14, ETH1_PHY_INTN, FMC_A10, EVENTOUT | - |
| - | D13 | B13 | B12 | B13 | B15 | PD4 | I/O | - | - | TIM1_BKIN2, I2C2_SDA, SPI5_MISO, USART6_RTS, DCMIPP_D9/DCMI_D9/PSSI_D9, FMC_A11, EVENTOUT | TAMP_IN7/TAMP_OUT8 |
| - | - | D14 | C13 | A15 | D14 | PD5 | I/O | - | - | TIM1_CH4N, USART2_TX, DCMIPP_PIXCLK/DCMI_PIXCLK/PSSI_PDCK, SDMMC2_D7, FMC_D6/FMC_AD6, EVENTOUT | - |
| - | D10 | A11 | A10 | A10 | D12 | PD6 | I/O | - | - | TIM1_CH1, TIM15_CH2, SPI2_MISO/I2S2_SDI, FMC_A1, FMC_A17/FMC_ALE, HDP2 | - |
| - | A11 | B11 | B10 | F11 | E12 | PD7 | I/O | - | - | TIM1_CH2, TIM15_CH1N, SPI2_MOSI/I2S2_SDO, SPI3_NSS/I2S3_WS, DCMIPP_D0/DCMI_D0/PSSI_D0, FMC_A2, FMC_A18, HDP3 | - |
| C13 | E11 | D13 | B13 | B14 | E14 | PD8 | I/O | - | - | USART3_TX, SPDIFRX1_IN1, DCMIPP_D11/DCMI_D11/PSSI_D11, FMC_NBL0, LCD_R7, EVENTOUT | TAMP_IN3/TAMP_OUT4 |
| - | - | H12 | E13 | G14 | H14 | PD9 | I/O | - | - | USART3_RX, DCMIPP_D11/DCMI_D11/PSSI_D11, FMC_SDCLK, LCD_R1, EVENTOUT | TAMP_IN5/TAMP_OUT6 |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | B11 | C11 | C10 | D11 | A13 | PD10 | I/O | - | - | TRACECLK, TIM1_ETR, MDF1_CKI3, I2S1_MCK, UCPD1_FRSTX1, SPDIFRX1_IN2, SAI2_FS_B, FMC_A3, GFXTIM_TE, FMC_A19, HDP4 | - |
| - | F13 | F11 | B14 | A17 | G14 | PD11 | I/O | - | - | I2C4_SDA, SPI2_MISO/I2S2_SDI, UCPD1_FRSTX1, DCMIPP_D15/PSSI_D15, SDMMC1_D0, FMC_D8/FMC_AD8, EVENTOUT | - |
| - | D11 | E11 | A11 | A11 | C13 | PD12 | I/O | - | - | SAI1_D3, MDF1_SDI3, UCPD1_FRSTX2, SPDIFRX1_IN3, DCMIPP_D12/DCMI_D12/PSSI_D12, ETH1_MDIO, FMC_A5, FMC_A21, HDP5 | - |
| - | - | E14 | F11 | D16 | C17 | PD13 | I/O | - | - | LPTIM1_CH1, TIM4_CH2, UCPD1_FRSTX2, UART9_RTS, DCMIPP_D13/DCMI_D13/PSSI_D13, SAI2_SCK_A, FMC_D4/FMC_AD4, LCD_R6, EVENTOUT | - |
| - | C13 | D12 | E11 | F13 | C14 | PD14 | I/O | - | - | I2C2_SCL, USART10_RX, FMC_A9, EVENTOUT | - |
| - | B13 | C12 | D11 | A12 | B14 | PD15 | I/O | - | - | I2C2_SDA, USART10_TX, FMC_A8, LCD_R2, EVENTOUT | - |
| A14 | F12 | F12 | C14 | A18 | F16 | PE0 | I/O | - | - | LPTIM1_ETR, TIM4_ETR, LPTIM2_ETR, USART3_RX, UART8_RX, DCMIPP_D2/DCMI_D2/PSSI_D2, SAI2_MCLK_A, FMC_D9/FMC_AD9, EVENTOUT | TAMP_IN6/TAMP_OUT5 |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| B14 | F11 | F13 | D13 | B18 | F17 | PE1 | I/O | - | - | LPTIM1_IN2, LPTIM2_CH2, USART3_TX, UART8_TX, DCMIPP_D8/DCMI_D8/PSSI_D8, FMC_D10/FMC_AD10, EVENTOUT | - |
| B15 | F10 | F14 | B15 | B19 | F15 | PE2 | I/O | - | - | TRACECLK, LPTIM5_IN1, SAI1_CK1, ADF1_CCK0, MDF1_CCK0, SPI4_SCK, SAI1_MCLK_A, UCPD1_FRSTX1, FMC_D11/FMC_AD11, TIM1_CH2N, EVENTOUT | - |
| C15 | G13 | G13 | C15 | C18 | F14 | PE3 | I/O | - | - | TRACED0, LPTIM5_ETR, MDF1_CKI2, SAI1_SD_B, TIM15_BKIN, FMC_D12/FMC_AD12, EVENTOUT | - |
| - | - | - | - | - | D10 | PE4 | I/O | - | - | LPTIM1_IN1, SPI6_MISO/I2S6_SDI, USART10_RX, USART6_RTS, SPDIFRX1_IN1, DCMIPP_D5/DCMI_D5/PSSI_D5, SDMMC2_D3, FMC_RNB, LCD_G1, EVENTOUT | - |
| - | C9 | D9 | C8 | D9 | C11 | PE5 | I/O | - | - | TIM16_CH1N, TIM4_CH1, LPUART1_TX, I2C1_SCL, I3C1_SCL, FDCAN2_TX, USART1_TX(boot), DCMIPP_D5/DCMI_D5/PSSI_D5, UART5_TX, FMC_SDNE1, HDP6 | - |
| - | - | A10 | D8 | B9 | D11 | PE6 | I/O | - | - | TIM17_CH1N, TIM4_CH2, LPUART1_RX, I2C1_SDA, I3C1_SDA, USART1_RX(boot), DCMIPP_VSYNC/DCMI_VSYNC/PSSI_RDY, DCMIPP_D1/DCMI_D1/PSSI_D1, UART5_TX, FMC_SDCKE1, HDP7 | - |
| A12 | C11 | D11 | D10 | B11 | B13 | PE7 | I/O | - | - | TIM1_ETR, MDF1_CKI0, UART7_RX, SAI2_SD_B, FMC_A4, FMC_A20, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| D12 | D12 | C13 | C12 | A13 | A15 | PE8 | I/O | - | - | TIM1_CH1N, MDF1_SDI0, USART3_TX, UART7_TX, DCMIPP_D4/DCMI_D4/PSSI_D4, FMC_A12, EVENTOUT | - |
| A13 | E13 | B14 | D12 | F14 | A16 | PE9 | I/O | - | - | TIM1_CH1, MDF1_CKI4, UART7_RTS, FMC_A14/FMC_BA0, EVENTOUT | - |
| B13 | E12 | C14 | A13 | D14 | B16 | PE10 | I/O | - | - | TRACECLK, TIM1_CH2N, MDF1_SDI4, USART3_RX, UART7_CTS, DCMIPP_D3/DCMI_D3/PSSI_D3, FMC_A15/FMC_BA1, EVENTOUT | - |
| - | A9 | B9 | A8 | D8 | E11 | PE11 | I/O | - | - | TIM1_CH2, MDF1_CKI5, SPI4_NSS, FDCAN3_TX, SAI2_SD_B, FMC_SDNWE, LCD_VSYNC, EVENTOUT | - |
| B11 | B10 | D10 | C9 | D10 | B12 | PE12 | I/O | - | - | TIM1_CH3N, MDF1_SDI5, SPI4_SCK, FDCAN3_RX, SAI2_SCK_B, FMC_NRAS, EVENTOUT | - |
| A11 | A10 | C10 | B9 | A9 | A11 | PE13 | I/O | - | - | TIM1_CH3, ADF1_CCK0, I2C4_SCL, SPI4_MISO, SAI2_FS_B, FMC_NCAS, EVENTOUT | - |
| D10 | B9 | C9 | B8 | F9 | B11 | PE14 | I/O | - | - | TIM1_CH4, GFXTIM_FCKCAL, ADF1_CCK1, I2C4_SDA, SPI4_MOSI, SAI2_MCLK_B, FMC_SDNE0, GFXTIM_LCKCAL, FMC_NWE, EVENTOUT | - |
| D11 | D9 | B10 | A9 | F10 | A12 | PE15 | I/O | - | - | TIM1_BKIN, GFXTIM_LCKCAL, I2C4_SMBA, SPI5_SCK, USART10_CK, USART2_CK, SDMMC1_D0, FMC_SDCKE0, GFXTIM_FCKCAL, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | - | N4 | U3 | R3 | PF0 | I/O | - | - | LPTIM5_OUT, TIM4_CH4, UCPD1_FRSTX2, UART9_TX, UART8_RTS, DCMIPP_D9/DCMI_D9/PSSI_D9, ETH1_MII_TX_CLK, ETH1_RGMII_GTX_CLK, EVENTOUT | - |
| - | - | - | N2 | U1 | P4 | PF1 | I/O | - | - | LPTIM1_CH2, TIM4_CH3, LPTIM2_CH1, UCPD1_FRSTX1, UART9_RX, UART8_CTS, DCMIPP_D7/DCMI_D7/PSSI_D7, ETH1_TX_ER, EVENTOUT | - |
| L1 | K1 | K1 | L3 | P4 | N4 | PF2 | I/O | - | - | TIM1_CH3N, SPI2_SCK/I2S2_CK, FDCAN3_TX, USART2_CTS/USART2_NSS, ETH1_RGMII_CLK125, FMC_NWAIT, LCD_B1, EVENTOUT | - |
| L4 | J4 | J5 | L2 | P1 | M2 | PF3 | I/O | - | - | FDCAN3_RX, USART2_RTS, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, ETH1_PPS_OUT, FMC_NL, LCD_R4, EVENTOUT | ADC1_INP16 |
| K1 | J1 | J1 | K1 | M1 | L2 | PF4 | I/O | - | - | TIM5_ETR, LPTIM3_CH2, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS/I2S6_WS, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, ETH1_MDIO, LCD_R3, HDP4 | ADC1_INP18 |
| K3 | J3 | J4 | L1 | N4 | M3 | PF5 | I/O | - | - | TIM1_ETR, LPTIM2_IN2, USART3_CTS/USART3_NSS, DCMIPP_D6/DCMI_D6/PSSI_D6, SAI2_SD_A, ETH1_CLK, FMC_NE3, LCD_G0, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | J2 | K2 | M4 | L5 | PF6 | I/O | - | - | TIM2_CH4, TIM5_CH4, LPTIM3_CH1, TIM15_CH2, I2S6_MCK, SPI4_RDY, USART2_RX(boot), GFXTIM_LCKCAL, SPI5_RDY, SPI1_RDY, ETH1_MII_COL, GFXTIM_FCKCAL, TIM1_CH3, LCD_DE, HDP3 | ADC12_INP15 |
| M2 | K4 | K4 | M2 | R2 | M1 | PF7 | I/O | - | - | TIM1_CH2N, TIM3_CH3, TIM9_CH1, SPI1_SCK/I2S1_CK, UART4_CTS, ETH1_MII_RX_CLK/ETH1_RMII_REF_CLK/ETH1_RGMII_RX_CLK, GFXTIM_TE, [RNG_S1], LCD_VSYNC, HDP0 | ADC12_INP9, ADC12_INN5 |
| N1 | L1 | L1 | M3 | R4 | N3 | PF8 | I/O | - | - | TRACECLK, UART9_TX, ETH1_MII_RXD2/ETH1_RGMII_RXD2, FMC_NWE, LCD_R6, EVENTOUT | - |
| - | - | - | M4 | T2 | P1 | PF9 | I/O | - | - | TRACED0, ETH1_MII_RXD3/ETH1_RGMII_RXD3, LCD_HSYNC, EVENTOUT | - |
| K2 | J2 | J3 | K3 | M2 | L4 | PF10 | I/O | - | - | TIM16_BKIN, SAI1_D3, MDF1_SDI3, UCPD1_FRSTX1, UART7_RX, DCMIPP_D11/DCMI_D11/PSSI_D11, DCMIPP_D15/PSSI_D15, ETH1_MII_RX_DV/ETH1_RMII_CRS_DV/ETH1_RGMII_RX_CTL, LCD_R1, EVENTOUT | - |
| N2 | L2 | L2 | N1 | T1 | P3 | PF11 | I/O | | - | SPI5_MOSI, DCMIPP_D15/PSSI_D15, SAI2_SD_B, ETH1_MII_TX_EN/ETH1_RMII_TX_EN/ETH1_RGMII_TX_CTL, LCD_B0, EVENTOUT | ADC1_INP2 |
| P1 | L3 | L3 | N3 | U2 | T1 | PF12 | I/O | - | - | USART1_RX, SPI5_MISO, DCMIPP_D13/DCMI_D13/PSSI_D13, ETH1_MII_TXD0/ETH1_RMII_TXD0/ETH1_RGMII_TXD0, EVENTOUT | ADC1_INP6, ADC1_INN2 |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| N3 | L4 | M2 | P1 | V1 | R2 | PF13 | I/O | - | - | USART1_TX, SPI5_NSS, DCMIPP_D10/DCMI_D10/PSSI_D10, ETH1_MII_TXD1/ETH1_RMII_TXD1/ETH1_RGMII_TXD1, EVENTOUT | ADC2_INP2 |
| L2 | K2 | K2 | L4 | P2 | N2 | PF14 | I/O | - | - | TIM2_CH2, USART1_CTS, SPI5_MOSI, ETH1_MII_RXD0/ETH1_RMII_RXD0/ETH1_RGMII_RXD0, LCD_G0, EVENTOUT | ADC2_INP6, ADC2_INN2 |
| M1 | K3 | K3 | M1 | R1 | N1 | PF15 | I/O | - | - | USART1_RTS, SPI5_SCK, ETH1_MII_RXD1/ETH1_RMII_RXD1/ETH1_RGMII_RXD1, LCD_G1, EVENTOUT | - |
| - | - | M12 | P15 | T16 | R13 | PG0 | I/O | - | - | TIM1_CH4N, TIM12_CH1, UART9_RX, LCD_VSYNC, ETH1_PHY_INTN, LCD_R0, EVENTOUT | - |
| - | - | M9 | R10 | T11 | R9 | PG1 | I/O | - | - | TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS, DCMIPP_PIXCLK/DCMI_PIXCLK/PSSI_PDCK, TIM13_CH1, FMC_A19, LCD_G1, EVENTOUT | - |
| M14 | N10 | N11 | P12 | W14 | T11 | PG2 | I/O | - | - | TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, USART3_RTS, UART7_CTS, DCMIPP_D6/DCMI_D6/PSSI_D6, SAI2_MCLK_B, TIM14_CH1, FMC_A21, LCD_R0, EVENTOUT | - |
| - | - | - | R2 | T5 | R1 | PG3 | I/O | - | - | TRACED1, USART2_TX, DCMIPP_HSYNC/DCMI_HSYNC/PSSI_DE, ETH1_MII_TXD2/ETH1_RGMII_TXD2, EVENTOUT | - |
| - | - | - | P2 | T4 | P2 | PG4 | I/O | - | - | TIM1_BKIN2, ETH1_MII_TXD3/ETH1_RGMII_TXD3, LCD_B0, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | - | K5 | N2 | M4 | PG5 | I/O | - | - | TIM1_ETR, USART2_CTS/USART2_NSS, ETH1_MII_RX_ER, LCD_B1, EVENTOUT | - |
| - | - | - | K4 | N1 | L3 | PG6 | I/O | - | - | TIM17_BKIN, USART6_CK, DCMIPP_D12/DCMI_D12/PSSI_D12, ETH1_MII_CRS, LCD_B3, EVENTOUT | - |
| - | - | - | - | - | L1 | PG7 | I/O | - | - | TRACECLK, SAI1_MCLK_A, USART6_CK, DCMIPP_D13/DCMI_D13/PSSI_D13, ETH1_PHY_INTN, EVENTOUT | - |
| - | - | L12 | N14 | V17 | T14 | PG8 | I/O | - | - | RTC_REFIN, TIM1_CH3N, TIM12_CH2, USART1_RX, SPI2_MOSI/I2S2_SDO, SAI1_SCK_B, UART4_CTS, SDMMC2_D1, FMC_A20, LCD_G7, HDP7 | PVD_IN |
| - | - | - | R14 | V16 | T13 | PG9 | I/O | - | (1) | FMC_D8/FMC_AD8, LCD_R7, EVENTOUT | - |
| P15 | N9 | N10 | P11 | T12 | T10 | PG10 | I/O | - | - | TIM1_CH1N, LPTIM2_CH1, SPI2_SCK/I2S2_CK, FDCAN2_TX, USART3_CTS/USART3_NSS, DCMIPP_D2/DCMI_D2/PSSI_D2, UART5_TX, FMC_A16/FMC_CLE, LCD_G4, HDP5 | - |
| - | - | - | P14 | W16 | U13 | PG11 | I/O | - | (1) | UART7_RX, ETH1_MDC, LCD_R6, EVENTOUT | - |
| - | - | N9 | P10 | V11 | T9 | PG12 | I/O | - | - | TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, FMC_A18, LCD_G0, EVENTOUT | - |
| R13 | K9 | P9 | N10 | W11 | U9 | PG13 | I/O | - | - | LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, USART3_RTS, DCMIPP_D12/DCMI_D12/PSSI_D12, SAI2_FS_A, FMC_NE1, LCD_DE, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| P9 | K6 | L5 | M8 | T7 | P6 | PG14 | I/O | - | - | TRACED1, LPTIM1_ETR, TIM8_CH4, SPI6_MOSI/I2S6_SDO, USART10_RTS, USART6_TX, USART2_RTS, DCMIPP_D11/DCMI_D11/PSSI_D11, FMC_NCE, FMC_NE2, LCD_B1, EVENTOUT | - |
| - | - | M5 | M7 | W8 | R6 | PG15 | I/O | - | - | TIM1_CH4, SPI5_RDY, SPI4_RDY, USART3_CK, DCMIPP_D4/DCMI_D4/PSSI_D4, SPI1_RDY, ETH1_MII_RX_CLK/ETH1_RMII_REF_CLK, FMC_CLK, LCD_B0, EVENTOUT | ADC12_INP7, ADC12_INN3 |
| A7 | B7 | B7 | A5 | A5 | A7 | PH0-OSC_IN(PH0) | I/O | - | - | EVENTOUT | OSC_IN |
| B7 | A7 | A7 | B5 | B5 | B7 | PH1-OSC_OUT(PH1) | I/O | - | - | EVENTOUT | OSC_OUT |
| B10 | C8 | E6 | E7 | D7 | E7 | PH2 | I/O | - | - | TRACED2, TIM1_ETR, TIM3_ETR, TIM15_BKIN, FDCAN1_TX, DCMIPP_D11/DCMI_D11/PSSI_D11, SDMMC1_CMD(boot), UART5_RX, FMC_NE3, EVENTOUT | - |
| - | - | - | - | - | B1 | PH3 | I/O | - | (1) | TRACECLK, UART7_TX, LCD_B4, EVENTOUT | - |
| - | - | - | - | - | F4 | PH4 | I/O | - | (1) | UART7_TX, LCD_R4, EVENTOUT | TAMP_IN4/TAMP_OUT3 |
| - | - | - | - | - | F5 | PH5 | I/O | - | - | SPI5_SCK, ETH1_MDC, EVENTOUT | - |
| - | - | - | - | - | B2 | PH6 | I/O | - | - | SPI5_NSS, LCD_B5, EVENTOUT | - |
| - | - | - | - | - | D2 | PH7 | I/O | - | (1) | I3C2_SCL, SPI5_MOSI, EVENTOUT | - |
| - | - | - | - | - | C2 | PH8 | I/O | | (1) | I3C2_SDA, SPI5_MISO, EVENTOUT | |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | C8 | D7 | B7 | D8 | PH9 | I/O | - | - | TIM16_CH1, TIM4_CH3, USART3_CK, I2C1_SCL, FDCAN1_RX, I3C1_SCL, UART4_RX, DCMIPP_D6/DCMI_D6/PSSI_D6, SDMMC1_D4, SDMMC2_D4, SDMMC1_CKIN, FMC_D9/FMC_AD9, HDP0 | - |
| J15 | J13 | M13 | M13 | R19 | P17 | PN0 | I/O | - | - | XSPIM_P2_DQS0(boot), FMC_A25, EVENTOUT | - |
| D14 | H13 | P13 | K12 | P16 | R17 | PN1 | I/O | - | - | XSPIM_P2_NCS1(boot), FMC_A24, EVENTOUT | - |
| H15 | J11 | L13 | L14 | T19 | T17 | PN2 | I/O | - | - | XSPIM_P2_IO0(boot), FMC_A23, EVENTOUT | - |
| K15 | H12 | N13 | M15 | P19 | R15 | PN3 | I/O | - | - | XSPIM_P2_IO1(boot), FMC_A22, EVENTOUT | - |
| E14 | L12 | J13 | J14 | V19 | N17 | PN4 | I/O | - | - | XSPIM_P2_IO2(boot), EVENTOUT | - |
| F15 | L13 | K14 | K13 | U18 | R16 | PN5 | I/O | - | - | XSPIM_P2_IO3(boot), EVENTOUT | - |
| G15 | K12 | K12 | K15 | U19 | P15 | PN6 | I/O | - | - | XSPIM_P2_CLK(boot), EVENTOUT | - |
| F14 | K11 | K13 | K14 | R16 | T16 | PN7 | I/O | - | - | XSPIM_P2_NCLK(boot), EVENTOUT | - |
| E15 | M13 | J14 | J15 | V18 | P16 | PN8 | I/O | - | - | XSPIM_P2_IO4(boot), EVENTOUT | - |
| G14 | K13 | L14 | L13 | T18 | T15 | PN9 | I/O | - | - | XSPIM_P2_IO5(boot), DCMIPP_D5/DCMI_D5/PSSI_D5, EVENTOUT | - |
| H14 | J12 | M14 | L15 | R18 | U15 | PN10 | I/O | - | - | XSPIM_P2_IO6(boot), LCD_B4, EVENTOUT | - |
| J14 | H11 | N14 | M14 | P18 | U16 | PN11 | I/O | - | - | XSPIM_P2_IO7(boot), LCD_B6, EVENTOUT | - |
| K14 | M12 | J12 | L12 | W18 | P14 | PN12 | I/O | - | - | XSPIM_P2_NCS2, EVENTOUT | - |
| - | - | - | G12 | F16 | M17 | PO0 | I/O | - | - | XSPIM_P1_NCS1, FMC_A22, EVENTOUT | - |
| - | - | - | F12 | N14 | K16 | PO1 | I/O | - | - | XSPIM_P1_NCS2, FMC_A23, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | - | H15 | G18 | K17 | PO2 | I/O | - | - | XSPIM_P1_DQS0, FMC_A24, LCD_B7, EVENTOUT | - |
| - | - | - | - | E18 | M16 | PO3 | I/O | - | - | XSPIM_P1_DQS1, FMC_A25, LCD_G3, EVENTOUT | - |
| - | - | - | F15 | J18 | N16 | PO4 | I/O | - | - | XSPIM_P1_CLK, LCD_B4, FMC_A24, FMC_NBL2, EVENTOUT | - |
| - | - | - | F14 | G16 | K15 | PO5 | I/O | - | - | XSPIM_P1_NCLK, FMC_A25, FMC_NBL3, EVENTOUT | - |
| - | - | - | G14 | H18 | G17 | PP0 | I/O | - | - | XSPIM_P1_IO0, FMC_D16, EVENTOUT | - |
| - | - | - | H13 | F18 | H16 | PP1 | I/O | - | - | XSPIM_P1_IO1, FMC_D17, EVENTOUT | - |
| - | - | - | E14 | K18 | J17 | PP2 | I/O | - | - | XSPIM_P1_IO2, FMC_D18, EVENTOUT | - |
| - | - | - | F13 | K19 | J16 | PP3 | I/O | - | - | XSPIM_P1_IO3, FMC_D19, EVENTOUT | - |
| - | - | - | E15 | L19 | H15 | PP4 | I/O | - | - | XSPIM_P1_IO4, FMC_D20, EVENTOUT | - |
| - | - | - | G15 | J19 | J14 | PP5 | I/O | - | - | XSPIM_P1_IO5, FMC_D21, EVENTOUT | - |
| - | - | - | G13 | H19 | G16 | PP6 | I/O | - | - | XSPIM_P1_IO6, FMC_D22, EVENTOUT | - |
| - | - | - | H14 | G19 | G15 | PP7 | I/O | - | - | XSPIM_P1_IO7, FMC_D23, EVENTOUT | - |
| - | - | - | - | F19 | L16 | PP8 | I/O | - | - | SPI2_MISO, XSPIM_P1_IO8, FMC_D24, EVENTOUT | - |
| - | - | - | - | E19 | N14 | PP9 | I/O | - | - | SPI2_MOSI, XSPIM_P1_IO9, FMC_D25, EVENTOUT | - |
| - | - | - | - | D18 | N15 | PP10 | I/O | - | - | XSPIM_P1_IO10, ETH1_MDC, FMC_D26, EVENTOUT | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | - | - | N19 | L15 | PP11 | I/O | | - | XSPIM_P1_IO11, FMC_D27, EVENTOUT | - |
| - | - | - | - | N18 | J15 | PP12 | I/O | - | - | XSPIM_P1_IO12, FMC_D28, EVENTOUT | - |
| - | - | - | - | M19 | K14 | PP13 | I/O | - | - | XSPIM_P1_IO13, FMC_D29, EVENTOUT | - |
| - | - | - | - | M18 | L17 | PP14 | I/O | - | - | XSPIM_P1_IO14, FMC_D30, EVENTOUT | - |
| - | - | - | - | L18 | H17 | PP15 | I/O | - | - | XSPIM_P1_IO15, FMC_D31, LCD_B5, EVENTOUT | - |
| - | - | - | - | - | E5 | PQ0 | I/O | - | - | TRACECLK, TIM8_ETR, EVENTOUT | - |
| - | - | - | - | - | E4 | PQ1 | I/O | - | - | TIM8_BKIN, EVENTOUT | - |
| - | - | - | - | - | E3 | PQ2 | I/O | - | - | TIM8_BKIN2, SAI2_SCK_B, EVENTOUT | - |
| - | - | - | - | - | D3 | PQ3 | I/O | - | - | TIM8_CH1, EVENTOUT | - |
| - | - | - | - | - | D4 | PQ4 | I/O | - | - | TIM8_CH1N, EVENTOUT | - |
| - | - | - | - | - | D5 | PQ5 | I/O | - | - | TIM8_CH2, SAI2_FS_B, EVENTOUT | - |
| - | - | - | - | - | A2 | PQ6 | I/O | - | - | TIM8_CH2N, SAI2_SD_B, EVENTOUT | - |
| - | - | - | - | - | G5 | PQ7 | I/O | - | - | TIM8_CH3, SAI2_MCLK_B, EVENTOUT | TAMP_IN2/TAMP_OUT1 |
| D1 | C2 | C2 | D1 | F1 | E1 | VBAT | S | - | - | - | - |
| K4 | J5 | L4 | J5 | M6 | M5 | VDDA18PLL | S | - | - | - | - |
| - | - | - | J11 | H16 | L13 | VDDIO2 | S | - | - | - | - |
| - | - | - | J12 | J16 | L14 | VDDIO2 | S | - | - | - | - |
| - | - | - | - | K16 | M14 | VDDIO2 | S | - | - | - | - |
| - | - | - | - | L16 | M15 | VDDIO2 | S | - | - | - | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| K12 | H10 | J10 | K11 | M14 | N13 | VDDIO3 | S | - | - | - | - |
| L12 | J10 | J11 | L11 | M16 | P13 | VDDIO3 | S | - | - | - | - |
| D8 | D8 | E8 | E9 | F7 | E8 | VDDIO4 | S | - | - | - | - |
| - | - | E9 | E10 | F8 | F8 | VDDIO4 | S | - | - | - | - |
| - | - | - | - | - | E9 | VDDIO5 | S | - | - | - | - |
| - | - | - | - | - | F9 | VDDIO5 | S | - | - | - | - |
| P8 | L6 | N6 | N6 | W6 | R4 | VDDCSI | S | - | - | - | - |
| R7 | M5 | P5 | P7 | V6 | R5 | VDDA18CSI | S | - | - | - | - |
| F1 | E1 | E1 | F1 | H1 | G1 | VDDA18PMU | S | - | - | - | - |
| F2 | E2 | E2 | F2 | H2 | F2 | VSSAPMU | S | - | - | - | - |
| J1 | H1 | H1 | J1 | L1 | K1 | VDDSMPS | S | - | - | - | - |
| G1 | F1 | F1 | G1 | J1 | H1 | VSSSMPS | S | - | - | - | - |
| J2 | H2 | H2 | J2 | L2 | K2 | VDDSMPS | S | - | - | - | - |
| G2 | F2 | F2 | G2 | J2 | H2 | VSSSMPS | S | - | - | - | - |
| J3 | H3 | H3 | J3 | L3 | K3 | VDDSMPS | S | - | - | - | - |
| G3 | F3 | F3 | G3 | J3 | H3 | VSSSMPS | S | - | - | - | - |
| - | H4 | H4 | J4 | L4 | K4 | VDDSMPS | S | - | - | - | - |
| - | F4 | F4 | G4 | J4 | H4 | VSSSMPS | S | - | - | - | - |
| - | - | - | - | L5 | K5 | VDDSMPS | S | - | - | - | - |
| - | - | - | - | J5 | H5 | VSSSMPS | S | - | - | - | - |

Table 15. STM32N657xx pin description (continued)

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | - | - | - | K6 | VDDSMPS | S | - | - | - | - |
| - | - | - | - | - | H6 | VSSSMPS | S | - | - | - | - |
| E1 | D1 | D1 | E1 | G1 | F1 | V08CAP | S | - | - | - | - |
| H1 | G1 | G1 | H1 | K1 | J1 | VLXSMPS | S | - | - | - | - |
| H2 | G2 | G2 | H2 | K2 | J2 | VLXSMPS | S | - | - | - | - |
| H3 | G3 | G3 | H3 | K3 | J3 | VLXSMPS | S | - | - | - | - |
| - | G4 | G4 | H4 | K4 | J4 | VLXSMPS | S | - | - | - | - |
| - | - | - | - | K5 | J5 | VLXSMPS | S | - | - | - | - |
| - | - | - | - | - | J6 | VLXSMPS | S | - | - | - | - |
| D4 | C4 | D4 | C3 | D4 | C5 | VDDA18USB | S | - | - | - | - |
| B6 | C5 | A4 | B3 | C3 | A4 | VDD33USB | S | - | - | - | - |
| R3 | L5 | M3 | M6 | P6 | N6 | VDDA18ADC | S | - | - | - | - |
| P3 | K5 | M4 | M5 | N6 | M6 | VSSA | S | - | - | - | - |
| E4 | D5 | E5 | E5 | H6 | F6 | VDDA18AON | S | - | - | - | - |
| F4 | E5 | F5 | F5 | G6 | G6 | VSSAON | S | - | - | - | - |
| F12 | E9 | G10 | H11 | J14 | G13 | VDD | S | - | - | - | - |
| G12 | G9 | G11 | H12 | K14 | H12 | VDD | S | - | - | - | - |
| H12 | J9 | G12 | J13 | L14 | H13 | VDD | S | - | - | - | - |
| - | - | - | - | - | J12 | VDD | S | - | - | - | - |
| - | - | - | - | - | J13 | VDD | S | - | - | - | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | - | - | - | - | K13 | VDD | S | - | - | - | - |
| M5 | E7 | K6 | L6 | P7 | L6 | VDDCORE | S | - | - | - | - |
| M6 | F6 | K7 | L7 | P9 | L12 | VDDCORE | S | - | - | - | - |
| M7 | F8 | K8 | L8 | P10 | M7 | VDDCORE | S | - | - | - | - |
| M8 | G5 | K9 | L9 | P11 | M9 | VDDCORE | S | - | - | - | - |
| M9 | G7 | L7 | - | P13 | M11 | VDDCORE | S | - | - | - | - |
| - | H6 | - | - | - | N8 | VDDCORE | S | - | - | - | - |
| - | H8 | - | - | - | N10 | VDDCORE | S | - | - | - | - |
| - | J7 | - | - | - | N12 | VDDCORE | S | - | - | - | - |
| - | - | - | - | - | P11 | VDDCORE | S | - | - | - | - |
| - | A13 | A14 | A15 | A19 | A17 | VSS | S | - | - | - | - |
| - | E6 | E7 | E8 | F12 | F7 | VSS | S | - | - | - | - |
| - | E8 | F10 | G11 | H14 | F10 | VSS | S | - | - | - | - |
| - | F5 | H10 | L5 | N16 | F11 | VSS | S | - | - | - | - |
| M10 | F7 | H11 | L10 | P8 | F12 | VSS | S | - | - | - | - |
| M12 | F9 | K5 | R1 | P12 | G12 | VSS | S | - | - | - | - |
| R1 | G6 | K10 | R15 | P14 | K12 | VSS | S | - | - | - | - |
| R15 | G8 | P1 | - | W1 | M8 | VSS | S | - | - | - | - |
| - | H5 | P14 | - | W19 | M10 | VSS | S | - | - | - | - |
| - | H7 | - | - | - | M12 | VSS | S | - | - | - | - |

**Table 15. STM32N657xx pin description (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VFBGA142 | VFBGA169 | VFBGA178 | VFBGA198 | VFBGA223 | VFBGA264 | | | | | | |
| - | H9 | - | - | - | M13 | VSS | S | - | - | - | - |
| - | J6 | - | - | - | N5 | VSS | S | - | - | - | - |
| - | J8 | - | - | - | N7 | VSS | S | - | - | - | - |
| - | N1 | - | - | - | N9 | VSS | S | - | - | - | - |
| - | N13 | - | - | - | N11 | VSS | S | - | - | - | - |
| - | - | - | - | - | U1 | VSS | S | - | - | - | - |
| - | - | - | - | - | U17 | VSS | S | - | - | - | - |

1. Power supply is VDDIOM/VDDUSB.

## 4.3 Alternate functions

Table 16. Alternate functions: AF0 to AF7

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port A | PA0 | - | TIM2_CH1 | TIM5_CH1 | TIM9_CH1 | TIM15_BKIN | SPI6_NSS/I2S6_WS | | USART2_CTS/U SART2_NSS |
| | PA1 | - | TIM2_CH2 | TIM5_CH2 | LPTIM3_IN1 | TIM15_CH1N | - | - | USART2_RTS |
| | PA2 | - | TIM2_CH3 | TIM5_CH3 | LPTIM3_IN2 | TIM15_CH1 | - | - | USART2_TX |
| | PA3 | - | TIM16_CH1 | - | - | - | SPI5_NSS | SAI1_SD_B | - |
| | PA4 | - | - | - | - | - | SPI5_MOSI | - | USART6_RX |
| | PA5 | PWR_CSTOP | TIM2_CH1 | TIM2_ETR | TIM9_CH2 | I3C1_SCL | SPI1_SCK/I2S1_CK | - | - |
| | PA6 | BOOT1 | TIM1_BKIN | TIM3_CH1 | LPTIM3_ETR | I3C1_SDA | SPI1_MISO/ I2S1_SDI | - | - |
| | PA7 | - | TIM1_CH1N | TIM3_CH2 | - | - | SPI1_MOSI/ I2S1_SDO | - | USART1_RX |
| | PA8 | MCO1 | TIM1_CH1 | I3C2_SCL | - | I2C3_SCL | - | - | USART1_CK |
| | PA9 | - | TIM1_CH2 | I3C2_SDA | LPUART1_TX | I2C3_SDA | SPI2_SCK/I2S2_CK | - | USART1_TX |
| | PA10 | PWR_CSLEEP | TIM1_CH3 | - | LPUART1_RX | - | - | - | USART1_RX |
| | PA11 | - | TIM1_CH4 | - | LPUART1_CTS | - | SPI2_NSS/I2S2_WS | FDCAN1_RX | USART1_CTS/U SART1_NSS |
| | PA12 | - | TIM1_ETR | - | LPUART1_RTS | - | SPI2_SCK/I2S2_CK | FDCAN1_TX | USART1_RTS |
| | PA13 | JTMS/SWDIO | - | - | - | - | - | - | - |
| | PA14 | JTCK/SWCLK | - | - | - | - | - | - | - |
| | PA15 | JTDI | TIM2_CH1 | TIM2_ETR | - | - | SPI1_NSS/I2S1_WS | SPI3_NSS/ I2S3_WS | SPI6_NSS/ I2S6_WS |

**Table 16. Alternate functions: AF0 to AF7 (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port B | PB0 | TRACED1 | TIM1_CH4 | SAI1_D2 | ADF1_SDI0 | MDF1_SDI2 | SPI4_NSS | SAI1_FS_A | TIM15_CH1N |
| | PB1 | - | TIM1_CH3N | TIM3_CH4 | TIM9_CH2 | - | - | FDCAN2_TX | USART2_TX |
| | PB2 | RTC_OUT2 | TIM1_CH1 | SAI1_D1 | ADF1_SDI0 | MDF1_SDI1 | - | SAI1_SD_A | SPI3_MOSI/ I2S3_SDO |
| | PB3 | TRACECLK | TIM1_CH4N | GFXTIM_FCK CAL | - | MDF1_CKI1 | - | - | USART1_CK |
| | PB4 | NJTRST | TIM16_BKIN | TIM3_CH1 | LPTIM4_ETR | - | SPI1_MISO/ I2S1_SDI | SPI3_MISO/ I2S3_SDI | SPI2_NSS/ I2S2_WS |
| | PB5 | JTDO/ TRACESWO | TIM17_BKIN | TIM3_CH2 | LPTIM4_OUT | I2C1_SMBA | SPI1_MOSI/ I2S1_SDO | FDCAN2_RX | SPI3_MOSI/ I2S3_SDO |
| | PB6 | TRACED2 | - | SAI1_CK2 | ADF1_CCK1 | MDF1_CCK1 | SPI4_MISO | SAI1_SCK_A | TIM15_CH1 |
| | PB7 | TRACED3 | TIM1_BKIN2 | SAI1_D1 | ADF1_SDI0 | MDF1_SDI1 | SPI4_MOSI | SAI1_SD_A | TIM15_CH2 |
| | PB8 | - | - | - | - | - | SPI1_MISO/ I2S1_SDI | - | USART6_RX |
| | PB9 | - | LPTIM1_IN2 | - | - | - | SPI1_SCK/I2S1_CK | USART10_TX | - |
| | PB10 | - | TIM2_CH3 | I3C2_SCL | LPTIM2_IN1 | I2C2_SCL | SPI2_SCK/I2S2_CK | - | USART3_TX |
| | PB11 | - | TIM2_CH4 | I3C2_SDA | LPTIM2_ETR | I2C2_SDA | - | - | USART3_RX |
| | PB12 | - | TIM1_BKIN | - | LPTIM2_IN2 | I2C2_SMBA | SPI2_NSS/I2S2_WS | FDCAN2_RX | USART3_CK |
| | PB13 | TRACED0 | LPTIM1_CH1 | TIM8_CH3N | - | - | SPI6_SCK/I2S6_CK | USART10_CTS/ USART10_NSS | USART6_CTS/U SART6_NSS |
| | PB14 | - | LPTIM1_CH2 | TIM8_CH4N | - | - | - | USART10_CK | USART6_CTS/U SART6_NSS |
| | PB15 | - | - | - | - | - | SPI6_NSS/I2S6_WS | - | USART6_RTS |

Table 16. Alternate functions: AF0 to AF7 (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port C | PC0 | - | TIM2_CH2 | - | LPTIM4_IN1 | MDF1_CKI1 | SPI1_SCK/I2S1_CK | SPI3_SCK/ I2S3_CK | - |
| | PC1 | - | TIM17_CH1 | TIM4_CH4 | - | I2C1_SDA | SPI2_NSS/I2S2_WS | FDCAN1_TX | I3C1_SDA |
| | PC2 | - | - | SAI1_D1 | ADF1_SDI0 | MDF1_SDI1 | SPI3_MOSI/ I2S3_SDO | SAI1_SCK_A | USART2_RX |
| | PC3 | - | - | - | - | - | SPI1_MOSI/ I2S1_SDO | - | USART2_CK |
| | PC4 | - | TIM1_CH2N | TIM12_CH1 | LPTIM2_CH2 | USART1_TX | SPI2_MISO/ I2S2_SDI | - | USART3_RTS |
| | PC5 | - | - | - | - | - | SPI1_NSS/I2S1_WS | - | - |
| | PC6 | - | TIM1_CH1 | TIM3_CH1 | TIM9_CH1 | - | I2S2_MCK | - | USART6_TX |
| | PC7 | DBTRGIO | TIM16_CH1N | TIM3_CH2 | TIM9_CH2 | - | - | I2S3_MCK | USART6_RX |
| | PC8 | TRACED1 | - | TIM3_CH3 | - | I2C3_SMBA | - | UCPD1_FRSTX1 | USART6_CK |
| | PC9 | MCO2 | - | TIM3_CH4 | - | I2C3_SDA | AUDIOCLK | UCPD1_FRSTX2 | USART6_RX |
| | PC10 | - | TIM1_BKIN | I3C2_SCL | - | I2C4_SCL | - | SPI3_SCK/ I2S3_CK | USART3_TX |
| | PC11 | - | - | I3C2_SDA | - | I2C4_SDA | - | SPI3_MISO/ I2S3_SDI | USART3_RX |
| | PC12 | TRACED3 | TIM1_CH4 | - | - | TIM15_CH1 | SPI6_SCK/I2S6_CK | SPI3_MOSI/ I2S3_SDO | USART3_CK |
| | PC13 | - | - | - | - | - | - | - | - |
| | PC14 | - | - | - | - | - | - | - | - |
| | PC15 | - | - | - | - | - | - | - | - |

Table 16. Alternate functions: AF0 to AF7 (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port D | PD0 | - | TIM1_ETR | - | - | - | - | FDCAN1_RX | UART9_CTS |
| | PD1 | - | - | - | - | - | - | FDCAN1_TX | - |
| | PD2 | TRACED0 | TIM1_CH3 | SAI1_D1 | ADF1_SDI0 | MDF1_SDI1 | SPI2_MOSI/ I2S2_SDO | SAI1_SD_A | TIM15_CH1N |
| | PD3 | - | - | - | - | I2C2_SMBA | - | USART10_RX | USART6_CTS |
| | PD4 | - | TIM1_BKIN2 | - | - | I2C2_SDA | SPI5_MISO | - | USART6_RTS |
| | PD5 | - | TIM1_CH4N | - | - | - | - | - | USART2_TX |
| | PD6 | - | TIM1_CH1 | - | - | TIM15_CH2 | SPI2_MISO/ I2S2_SDI | - | - |
| | PD7 | - | TIM1_CH2 | - | - | TIM15_CH1N | SPI2_MOSI/ I2S2_SDO | SPI3_NSS/I2S3_ WS | - |
| | PD8 | - | - | - | - | - | - | - | USART3_TX |
| | PD9 | - | - | - | - | - | - | - | USART3_RX |
| | PD10 | TRACECLK | TIM1_ETR | - | - | MDF1_CKI3 | I2S1_MCK | UCPD1_FRSTX1 | - |
| | PD11 | - | - | - | - | I2C4_SDA | SPI2_MISO/ I2S2_SDI | UCPD1_FRSTX1 | - |
| | PD12 | - | - | SAI1_D3 | - | MDF1_SDI3 | - | UCPD1_FRSTX2 | - |
| | PD13 | - | LPTIM1_CH1 | TIM4_CH2 | - | - | - | UCPD1_FRSTX2 | UART9_RTS |
| | PD14 | - | - | - | - | I2C2_SCL | - | USART10_RX | - |
| | PD15 | - | - | - | - | I2C2_SDA | - | USART10_TX | - |

Table 16. Alternate functions: AF0 to AF7 (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port E | PE0 | - | LPTIM1_ETR | TIM4_ETR | LPTIM2_ETR | - | - | - | USART3_RX |
| | PE1 | - | LPTIM1_IN2 | - | LPTIM2_CH2 | - | - | - | USART3_TX |
| | PE2 | TRACECLK | LPTIM5_IN1 | SAI1_CK1 | ADF1_CCK0 | MDF1_CCK0 | SPI4_SCK | SAI1_MCLK_A | UCPD1_FRSTX1 |
| | PE3 | TRACED0 | LPTIM5_ETR | - | - | MDF1_CKI2 | - | SAI1_SD_B | TIM15_BKIN |
| | PE4 | - | LPTIM1_IN1 | - | - | - | SPI6_MISO/ I2S6_SDI | USART10_RX | USART6_RTS |
| | PE5 | - | TIM16_CH1N | TIM4_CH1 | LPUART1_TX | I2C1_SCL | I3C1_SCL | FDCAN2_TX | USART1_TX |
| | PE6 | - | TIM17_CH1N | TIM4_CH2 | LPUART1_RX | I2C1_SDA | I3C1_SDA | - | USART1_RX |
| | PE7 | - | TIM1_ETR | - | - | MDF1_CKI0 | - | - | - |
| | PE8 | - | TIM1_CH1N | - | - | MDF1_SDI0 | - | - | USART3_TX |
| | PE9 | - | TIM1_CH1 | - | - | MDF1_CKI4 | - | - | - |
| | PE10 | TRACECLK | TIM1_CH2N | - | - | MDF1_SDI4 | - | - | USART3_RX |
| | PE11 | - | TIM1_CH2 | - | - | MDF1_CKI5 | SPI4_NSS | FDCAN3_TX | - |
| | PE12 | - | TIM1_CH3N | - | - | MDF1_SDI5 | SPI4_SCK | FDCAN3_RX | - |
| | PE13 | - | TIM1_CH3 | - | ADF1_CCK0 | I2C4_SCL | SPI4_MISO | - | - |
| | PE14 | - | TIM1_CH4 | GFXTIM_FCK CAL | ADF1_CCK1 | I2C4_SDA | SPI4_MOSI | - | - |
| | PE15 | - | TIM1_BKIN | GFXTIM_LCK CAL | - | I2C4_SMBA | SPI5_SCK | USART10_CK | USART2_CK |

Table 16. Alternate functions: AF0 to AF7 (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port F | PF0 | - | LPTIM5_OUT | TIM4_CH4 | - | - | - | UCPD1_FRSTX2 | UART9_TX |
| | PF1 | - | LPTIM1_CH2 | TIM4_CH3 | LPTIM2_CH1 | - | - | UCPD1_FRSTX1 | UART9_RX |
| | PF2 | - | TIM1_CH3N | - | - | - | SPI2_SCK/I2S2_CK | FDCAN3_TX | USART2_CTS/ USART2_NSS |
| | PF3 | - | - | - | - | - | - | FDCAN3_RX | USART2_RTS |
| | PF4 | - | - | TIM5_ETR | LPTIM3_CH2 | - | SPI1_NSS/I2S1_WS | SPI3_NSS/I 2S3_WS | USART2_CK |
| | PF5 | - | TIM1_ETR | - | LPTIM2_IN2 | - | - | - | USART3_CTS/ USART3_NSS |
| | PF6 | - | TIM2_CH4 | TIM5_CH4 | LPTIM3_CH1 | TIM15_CH2 | I2S6_MCK | SPI4_RDY | USART2_RX |
| | PF7 | - | TIM1_CH2N | TIM3_CH3 | TIM9_CH1 | - | SPI1_SCK/I2S1_CK | - | - |
| | PF8 | TRACECLK | - | - | - | - | - | - | UART9_TX |
| | PF9 | TRACED0 | - | - | - | - | - | - | - |
| | PF10 | - | TIM16_BKIN | SAI1_D3 | - | MDF1_SDI3 | | UCPD1_FRSTX1 | - |
| | PF11 | - | - | - | - | - | SPI5_MOSI | - | - |
| | PF12 | - | - | - | - | USART1_RX | SPI5_MISO | - | - |
| | PF13 | - | - | - | - | USART1_TX | SPI5_NSS | - | - |
| | PF14 | - | TIM2_CH2 | - | - | USART1_CTS | SPI5_MOSI | - | - |
| | PF15 | - | - | - | - | USART1_RTS | SPI5_SCK | - | - |

**Table 16. Alternate functions: AF0 to AF7 (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port G | PG0 | - | TIM1_CH4N | TIM12_CH1 | - | - | - | - | UART9_RX |
| | PG1 | - | TIM16_CH1N | - | - | - | SPI5_MISO | SAI1_SCK_B | |
| | PG2 | - | TIM17_CH1N | - | - | - | SPI5_MOSI | SAI1_FS_B | USART3_RTS |
| | PG3 | TRACED1 | - | - | - | - | - | - | USART2_TX |
| | PG4 | - | TIM1_BKIN2 | - | - | - | - | - | |
| | PG5 | - | TIM1_ETR | - | - | - | - | - | USART2_CTS/ USART2_NSS |
| | PG6 | - | TIM17_BKIN | - | - | - | - | - | USART6_CK |
| | PG7 | TRACECLK | | - | - | - | - | SAI1_MCLK_A | USART6_CK |
| | PG8 | RTC_REFIN | TIM1_CH3N | TIM12_CH2 | - | USART1_RX | SPI2_MOSI/ I2S2_SDO | SAI1_SCK_B | - |
| | PG9 | - | - | - | - | - | - | - | - |
| | PG10 | - | TIM1_CH1N | | LPTIM2_CH1 | - | SPI2_SCK/I2S2_CK | FDCAN2_TX | USART3_CTS/ USART3_NSS |
| | PG11 | - | - | - | - | - | - | - | - |
| | PG12 | - | TIM17_CH1 | - | - | - | SPI5_SCK | SAI1_MCLK_B | |
| | PG13 | - | LPTIM1_IN1 | TIM4_CH1 | LPTIM2_IN1 | - | - | - | USART3_RTS |
| | PG14 | TRACED1 | LPTIM1_ETR | TIM8_CH4 | - | - | SPI6_MOSI/ I2S6_SDO | USART10_RTS | USART6_TX |
| | PG15 | - | TIM1_CH4 | - | - | - | SPI5_RDY | SPI4_RDY | USART3_CK |

Table 16. Alternate functions: AF0 to AF7 (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port H | PH0 | - | - | - | - | - | - | - | - |
| | PH1 | - | - | - | - | - | - | - | - |
| | PH2 | TRACED2 | TIM1_ETR | TIM3_ETR | - | TIM15_BKIN | - | FDCAN1_TX | - |
| | PH3 | TRACECLK | - | - | - | - | - | - | - |
| | PH4 | - | - | - | - | - | - | - | - |
| | PH5 | - | - | - | - | - | SPI5_SCK | - | - |
| | PH6 | - | - | - | - | - | SPI5_NSS | - | - |
| | PH7 | - | - | I3C2_SCL | - | - | SPI5_MOSI | - | - |
| | PH8 | - | - | I3C2_SDA | - | - | SPI5_MISO | - | - |
| | PH9 | - | TIM16_CH1 | TIM4_CH3 | USART3_CK | I2C1_SCL | - | FDCAN1_RX | I3C1_SCL |
| | PH10 | - | - | - | - | - | - | - | - |
| | PH11 | - | - | - | - | - | - | - | - |
| | PH12 | - | - | - | - | - | - | - | - |
| | PH13 | - | - | - | - | - | - | - | - |
| | PH14 | - | - | - | - | - | - | - | - |
| | PH15 | - | - | - | - | - | - | - | - |

Table 16. Alternate functions: AF0 to AF7 (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port N | PN0 | - | - | - | - | - | - | - | - |
| | PN1 | - | - | - | - | - | - | - | - |
| | PN2 | - | - | - | - | - | - | - | - |
| | PN3 | - | - | - | - | - | - | - | - |
| | PN4 | - | - | - | - | - | - | - | - |
| | PN5 | - | - | - | - | - | - | - | - |
| | PN6 | - | - | - | - | - | - | - | - |
| | PN7 | - | - | - | - | - | - | - | - |
| | PN8 | - | - | - | - | - | - | - | - |
| | PN9 | - | - | - | - | - | - | - | - |
| | PN10 | - | - | - | - | - | - | - | - |
| | PN11 | - | - | - | - | - | - | - | - |
| | PN12 | - | - | - | - | - | - | - | - |
| Port O | PO0 | - | - | - | - | - | - | - | - |
| | PO1 | - | - | - | - | - | - | - | - |
| | PO2 | - | - | - | - | - | - | - | - |
| | PO3 | - | - | - | - | - | - | - | - |
| | PO4 | - | - | - | - | - | - | - | - |
| | PO5 | - | - | - | - | - | - | - | - |

**Table 16. Alternate functions: AF0 to AF7 (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port P | PP0 | - | - | - | - | - | - | - | - |
| | PP1 | - | - | - | - | - | - | - | - |
| | PP2 | - | - | - | - | - | - | - | - |
| | PP3 | - | - | - | - | - | - | - | - |
| | PP4 | - | - | - | - | - | - | - | - |
| | PP5 | - | - | - | - | - | - | - | - |
| | PP6 | - | - | - | - | - | - | - | - |
| | PP7 | - | - | - | - | - | - | - | - |
| | PP8 | - | - | - | - | - | SPI2_MISO | - | - |
| | PP9 | - | - | - | - | - | SPI2_MOSI | - | - |
| | PP10 | - | - | - | - | - | - | - | - |
| | PP11 | - | - | - | - | - | - | - | - |
| | PP12 | - | - | - | - | - | - | - | - |
| | PP13 | - | - | - | - | - | - | - | - |
| | PP14 | - | - | - | - | - | - | - | - |
| | PP15 | - | - | - | - | - | - | - | - |

Table 16. Alternate functions: AF0 to AF7 (continued)

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/ LPTIM1 | PDM_SAI1/ TIM3/4/5/12/15 | LPUART1/ TIM8/LPTIM2/3/ DFSDM1/ OCSPI1/2 | I2C1/2/3/4/ USART1/ TIM15/LPTIM2/ DFSDM1/2/ DCMI/PSSI/CEC | SPI1/I2S1/SPI2/I2S2 /SPI3/I2S3/SPI4/5/6/ I2S6/CEC | SPI3/I2S3/SAI1/ I2C4/UART4/ DFSDM1/2/ OCSPI1/ USB_PD | SPI2/I2S2/SPI3/ I2S3/SPI6/I2S6/ USART1/2/3/6/ UART7/ OCSPI2/SDIO1 |
| Port Q | PQ0 | TRACECLK | - | TIM8_ETR | - | - | - | - | - |
| | PQ1 | - | - | TIM8_BKIN | - | - | - | - | - |
| | PQ2 | - | - | TIM8_BKIN2 | - | - | - | - | - |
| | PQ3 | - | - | TIM8_CH1 | - | - | - | - | - |
| | PQ4 | - | - | TIM8_CH1N | - | - | - | - | - |
| | PQ5 | - | - | TIM8_CH2 | - | - | - | - | - |
| | PQ6 | - | - | TIM8_CH2N | - | - | - | - | - |
| | PQ7 | - | - | TIM8_CH3 | - | - | - | - | - |

**Table 17. Alternate functions: AF8 to AF15**

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port A | PA0 | UART4_TX | - | SAI2_SD_B | SDMMC2_CMD | FMC_AD7/ FMC_D7 | - | LCD_G3 | HDP0 |
| | PA1 | UART4_RX | DCMIPP_D0/ DCMI_D0/PSSI_D0 | SAI2_MCLK_B | - | FMC_AD6/ FMC_D6 | - | - | LCD_G2 |
| | PA2 | - | - | SAI2_SCK_B | MDIOS_MDIO | FMC_AD5/ FMC_D5 | - | - | LCD_B7 |
| | PA3 | UART7_RX | - | - | - | FMC_A17/ FMC_ALE | - | - | - |
| | PA4 | | DCMIPP_D3/ DCMI_D3/PSSI_D3 | - | - | FMC_A13 | - | - | - |
| | PA5 | SPI6_SCK/ I2S6_CK | DCMIPP_D8/ DCMI_D8/PSSI_D8 | TIM10_CH1 | - | FMC_NOE | - | - | LCD_CLK |
| | PA6 | SPI6_MISO/ I2S6_SDI | DCMIPP_PIXCLK/ DCMI_PIXCLK/ PSSI_PDCK | TIM13_CH1 | MDIOS_MDC | LCD_B7 | - | - | LCD_HSYNC |
| | PA7 | SPI6_MOSI/ I2S6_SDO | | LCD_R4 | TIM14_CH1 | FMC_RNB | - | - | LCD_B1 |
| | PA8 | - | TIM11_CH1 | UART7_RX | | FMC_AD4/ FMC_D4 | - | - | LCD_B6 |
| | PA9 | - | DCMIPP_D0/ DCMI_D0/PSSI_D0 | - | | FMC_AD3/ FMC_D3 | - | - | LCD_B5 |
| | PA10 | - | DCMIPP_D1/ DCMI_D1/PSSI_D1 | - | MDIOS_MDIO | FMC_AD2/ FMC_D2 | - | - | LCD_B4 |
| | PA11 | UART4_RX | - | - | - | FMC_AD1/ FMC_D1 | - | - | LCD_B3 |
| | PA12 | UART4_TX | - | SAI2_FS_B | - | FMC_AD0/ FMC_D0 | - | | LCD_B2 |
| | PA13 | - | - | - | - | - | - | - | - |
| | PA14 | - | - | - | - | - | - | - | - |
| | PA15 | UART4_RTS | - | UART7_TX | - | FMC_D15/ FMC_AD15 | - | - | LCD_R5 |

## Table 17. Alternate functions: AF8 to AF15 (continued)

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port B | PB0 | - | DCMIPP_D4/DCMI_D4/PSSI_D4 | - | - | FMC_D13/ FMC_AD13 | - | - | EVENTOUT |
| | PB1 | - | - | - | - | FMC_NOE | [RNG_S2] | LCD_R1 | HDP1 |
| | PB2 | - | - | - | - | FMC_D2/ FMC_AD2 | - | LCD_B2 | HDP2 |
| | PB3 | - | - | SAI2_FS_B | - | FMC_NBL1 | GFXTIM_LCKCAL | FMC_A23 | HDP0 |
| | PB4 | SPI6_MISO/ I2S6_SDI | DCMIPP_VSYNC/ DCMI_VSYNC/ PSSI_RDY | UART7_TX | SDMMC2_D3 | FMC_D13/ FMC_AD13 | - | LCD_R3 | HDP4 |
| | PB5 | SPI6_MOSI/ I2S6_SDO | DCMIPP_D10/ DCMI_D10/PSSI_D10 | - | UART5_RX | FMC_D12/ FMC_AD12 | - | LCD_R2 | HDP5 |
| | PB6 | - | DCMIPP_D6/DCMI_D6/PSSI_D6 | - | - | FMC_D14/ FMC_AD14 | - | - | EVENTOUT |
| | PB7 | - | DCMIPP_D7/DCMI_D7/PSSI_D7 | SAI2_MCLK_B | - | FMC_D15/ FMC_AD15 | - | - | EVENTOUT |
| | PB8 | SPDIFRX1_IN3 | DCMIPP_VSYNC/ DCMI_VSYNC/ PSSI_RDY | SAI2_FS_B | SDMMC2_D0 | FMC_D1/ FMC_AD1 | - | - | EVENTOUT |
| | PB9 | SPDIFRX1_IN0 | DCMIPP_D3/DCMI_D3/PSSI_D3 | - | SDMMC2_D2 | FMC_D3/ FMC_AD3 | - | - | EVENTOUT |
| | PB10 | - | - | - | - | FMC_D11/ FMC_AD11 | - | LCD_G7 | HDP2 |
| | PB11 | - | - | - | - | FMC_D10/ FMC_AD10 | - | LCD_G6 | HDP3 |
| | PB12 | - | - | - | UART5_RX | FMC_D9/ FMC_AD9 | - | LCD_G5 | HDP4 |
| | PB13 | - | - | - | SDMMC2_D6 | FMC_D5/ FMC_AD5 | - | LCD_CLK | EVENTOUT |
| | PB14 | - | DCMIPP_D10/ DCMI_D10/PSSI_D10 | - | - | FMC_D7/ FMC_AD7 | - | LCD_HSYNC | EVENTOUT |
| | PB15 | SPDIFRX1_IN2 | - | - | - | FMC_D0/ FMC_AD0 | - | LCD_G4 | EVENTOUT |

**Table 17. Alternate functions: AF8 to AF15 (continued)**

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port C | PC0 | SPI6_SCK/ I2S6_CK | DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE | UART7_RX | SDMMC2_D2 | FMC_D14/ FMC_AD14 | - | LCD_R4 | HDP3 |
| | PC1 | UART4_TX | DCMIPP_D7/DCMI_D7/ PSSI_D7 | SDMMC1_D5 | SDMMC2_D5 | SDMMC1_CDIR | - | - | HDP1 |
| | PC2 | - | DCMIPP_D13/ DCMI_D13/PSSI_D13 | - | SDMMC2_CK | FMC_NE3 | - | FMC_RNB | EVENTOUT |
| | PC3 | SPDIFRX1_IN0 | DCMIPP_D2/DCMI_D2/ PSSI_D2 | - | SDMMC2_CMD | FMC_D8/ FMC_AD8 | - | - | EVENTOUT |
| | PC4 | UART4_RTS | - | LCD_VSYNC | SDMMC2_D0 | FMC_NE1 | - | LCD_DE | HDP6 |
| | PC5 | - | DCMIPP_D2/DCMI_D2/ PSSI_D2 | SAI2_SD_B | SDMMC2_D1 | FMC_NWE | - | - | EVENTOUT |
| | PC6 | - | DCMIPP_D1/DCMI_D1/ PSSI_D1 | SDMMC1_D6 | SDMMC2_D6 | SDMMC1_D0DIR | - | - | HDP6 |
| | PC7 | - | DCMIPP_D1/DCMI_D1/ PSSI_D1 | SDMMC1_D7 | SDMMC2_D7 | SDMMC1_D123DIR | - | - | HDP7 |
| | PC8 | - | DCMIPP_D2/DCMI_D2/ PSSI_D2 | SDMMC1_D0 | UART5_RTS | FMC_NE4 | - | LCD_B0 | HDP0 |
| | PC9 | - | DCMIPP_D3/DCMI_D3/ PSSI_D3 | SDMMC1_D1 | UART5_CTS | - | - | LCD_B3 | HDP1 |
| | PC10 | UART4_TX | DCMIPP_D14/PSSI_D14 | SDMMC1_D2 | - | FMC_CLK | - | - | HDP2 |
| | PC11 | UART4_RX | DCMIPP_D4/DCMI_D4/ PSSI_D4 | SDMMC1_D3 | - | - | - | - | HDP3 |
| | PC12 | - | DCMIPP_D9/DCMI_D9/ PSSI_D9 | SDMMC1_CK | UART5_TX | FMC_NL | - | - | HDP4 |
| | PC13 | - | - | - | - | - | - | - | HDP5 |
| | PC14 | - | - | - | - | - | - | - | - |
| | PC15 | - | - | - | - | - | - | - | - |

**Table 17. Alternate functions: AF8 to AF15 (continued)**

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port D | PD0 | UART4_RX | DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE | - | - | FMC_A6 | - | FMC_A22 | EVENTOUT |
| | PD1 | UART4_TX | - | - | ETH1_MDC | FMC_A7 | - | FMC_A23 | EVENTOUT |
| | PD2 | - | - | MDIOS_MDC | SDMMC2_CK | FMC_A0 | - | FMC_A16/ FMC_CLE | HDP1 |
| | PD3 | - | DCMIPP_D14/PSSI_D14 | - | ETH1_PHY_INTN | FMC_A10 | - | - | EVENTOUT |
| | PD4 | - | DCMIPP_D9/DCMI_D9/ PSSI_D9 | - | - | FMC_A11 | - | - | EVENTOUT |
| | PD5 | - | DCMIPP_PIXCLK/ DCMI_PIXCLK/ PSSI_PDCK | - | SDMMC2_D7 | FMC_D6/FMC_AD6 | - | - | EVENTOUT |
| | PD6 | - | - | - | - | FMC_A1 | - | FMC_A17/ FMC_ALE | HDP2 |
| | PD7 | - | DCMIPP_D0/DCMI_D0/ PSSI_D0 | - | - | FMC_A2 | - | FMC_A18 | HDP3 |
| | PD8 | SPDIFRX1_IN1 | DCMIPP_D11/ DCMI_D11/PSSI_D11 | - | - | FMC_NBL0 | - | LCD_R7 | EVENTOUT |
| | PD9 | - | DCMIPP_D11/ DCMI_D11/PSSI_D11 | - | - | FMC_SDCLK | - | LCD_R1 | EVENTOUT |
| | PD10 | SPDIFRX1_IN2 | - | SAI2_FS_B | - | FMC_A3 | GFXTIM_TE | FMC_A19 | HDP4 |
| | PD11 | - | DCMIPP_D15/PSSI_D15 | SDMMC1_D0 | - | FMC_D8/FMC_AD8 | - | - | EVENTOUT |
| | PD12 | SPDIFRX1_IN3 | DCMIPP_D12/ DCMI_D12/PSSI_D12 | - | ETH1_MDIO | FMC_A5 | - | FMC_A21 | HDP5 |
| | PD13 | - | DCMIPP_D13/ DCMI_D13/PSSI_D13 | SAI2_SCK_A | - | FMC_D4/FMC_AD4 | - | LCD_R6 | EVENTOUT |
| | PD14 | - | - | - | - | FMC_A9 | - | - | EVENTOUT |
| | PD15 | - | - | - | - | FMC_A8 | - | LCD_R2 | EVENTOUT |

**Table 17. Alternate functions: AF8 to AF15 (continued)**

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port E | PE0 | UART8_RX | DCMIPP_D2/DCMI_D2/ PSSI_D2 | SAI2_MCLK_A | - | FMC_D9/FMC_AD9 | - | - | EVENTOUT |
| | PE1 | UART8_TX | DCMIPP_D8/DCMI_D8/ PSSI_D8 | - | - | FMC_D10/FMC_AD10 | - | - | EVENTOUT |
| | PE2 | - | - | - | - | FMC_D11/FMC_AD11 | TIM1_CH2N | - | EVENTOUT |
| | PE3 | - | - | - | - | FMC_D12/FMC_AD12 | - | - | EVENTOUT |
| | PE4 | SPDIFRX1_IN1 | DCMIPP_D5/DCMI_D5/ PSSI_D5 | | SDMMC2_D3 | FMC_RNB | - | LCD_G1 | EVENTOUT |
| | PE5 | - | DCMIPP_D5/DCMI_D5/ PSSI_D5 | | UART5_TX | FMC_SDNE1 | - | - | HDP6 |
| | PE6 | - | DCMIPP_VSYNC/ DCMI_VSYNC/PSSI_RDY | DCMIPP_D1/DCMI_D1/ PSSI_D1 | UART5_TX | FMC_SDCKE1 | - | - | HDP7 |
| | PE7 | UART7_RX | - | SAI2_SD_B | - | FMC_A4 | - | FMC_A20 | EVENTOUT |
| | PE8 | UART7_TX | DCMIPP_D4/DCMI_D4/ PSSI_D4 | - | - | FMC_A12 | - | - | EVENTOUT |
| | PE9 | UART7_RTS | - | - | - | FMC_A14/FMC_BA0 | - | - | EVENTOUT |
| | PE10 | UART7_CTS | DCMIPP_D3/DCMI_D3/ PSSI_D3 | - | - | FMC_A15/FMC_BA1 | - | - | EVENTOUT |
| | PE11 | - | - | SAI2_SD_B | - | FMC_SDNWE | - | LCD_VSYNC | EVENTOUT |
| | PE12 | - | - | SAI2_SCK_B | - | FMC_NRAS | - | - | EVENTOUT |
| | PE13 | - | - | SAI2_FS_B | - | FMC_NCAS | - | - | EVENTOUT |
| | PE14 | - | - | SAI2_MCLK_B | - | FMC_SDNE0 | GFXTIM_LCKCAL | FMC_NWE | EVENTOUT |
| | PE15 | - | - | SDMMC1_D0 | - | FMC_SDCKE0 | GFXTIM_FCKCAL | - | EVENTOUT |

**Table 17. Alternate functions: AF8 to AF15 (continued)**

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port F | PF0 | UART8_RTS | DCMIPP_D9/DCMI_D9/ PSSI_D9 | - | ETH1_MII_TX_CLK | ETH1_RGMII_GTX_CLK | - | - | EVENTOUT |
| | PF1 | UART8_CTS | DCMIPP_D7/DCMI_D7/ PSSI_D7 | - | ETH1_TX_ER | - | - | - | EVENTOUT |
| | PF2 | - | - | - | ETH1_RGMII_CLK125 | FMC_NWAIT | - | LCD_B1 | EVENTOUT |
| | PF3 | - | DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE | - | ETH1_PPS_OUT | FMC_NL | - | LCD_R4 | EVENTOUT |
| | PF4 | SPI6_NSS/ I2S6_WS | DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE | - | ETH1_MDIO | - | - | LCD_R3 | HDP4 |
| | PF5 | - | DCMIPP_D6/DCMI_D6/ PSSI_D6 | SAI2_SD_A | ETH1_CLK | FMC_NE3 | - | LCD_G0 | EVENTOUT |
| | PF6 | - | SPI5_RDY | SPI1_RDY | ETH1_MII_COL | GFXTIM_FCKCAL | TIM1_CH3 | LCD_DE | HDP3 |
| | PF7 | UART4_CTS | - | - | ETH1_MII_RX_CLK/ ETH1_RMII_REF_CLK/ ETH1_RGMII_RX_CLK | GFXTIM_TE | [RNG_S1] | LCD_VSYNC | HDP0 |
| | PF8 | - | - | - | ETH1_MII_RXD2/ ETH1_RGMII_RXD2 | FMC_NWE | - | LCD_R6 | EVENTOUT |
| | PF9 | - | - | - | ETH1_MII_RXD3/ ETH1_RGMII_RXD3 | - | - | LCD_HSYNC | EVENTOUT |
| | PF10 | UART7_RX | DCMIPP_D11/DCMI_D11/ PSSI_D11 | DCMIPP_D15/ PSSI_D15 | ETH1_MII_RX_DV/ ETH1_RMII_CRS_DV/ ETH1_RGMII_RX_CTL | - | - | LCD_R1 | EVENTOUT |
| | PF11 | - | DCMIPP_D15/PSSI_D15 | SAI2_SD_B | ETH1_MII_TX_EN/ ETH1_RMII_TX_EN/ ETH1_RGMII_TX_CTL | - | - | LCD_B0 | EVENTOUT |
| | PF12 | - | DCMIPP_D13/DCMI_D13/ PSSI_D13 | - | ETH1_MII_TXD0/ ETH1_RMII_TXD0/ ETH1_RGMII_TXD0 | - | - | | EVENTOUT |
| | PF13 | - | DCMIPP_D10/DCMI_D10/ PSSI_D10 | - | ETH1_MII_TXD1/ ETH1_RMII_TXD1/ ETH1_RGMII_TXD1 | - | - | | EVENTOUT |
| | PF14 | - | - | - | ETH1_MII_RXD0/ ETH1_RMII_RXD0/ ETH1_RGMII_RXD0 | - | - | LCD_G0 | EVENTOUT |
| | PF15 | - | - | - | ETH1_MII_RXD1/ ETH1_RMII_RXD1/ ETH1_RGMII_RXD1 | - | - | LCD_G1 | EVENTOUT |

**Table 17. Alternate functions: AF8 to AF15 (continued)**

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port G | PG0 | - | - | LCD_VSYNC | ETH1_PHY_INTN | - | - | LCD_R0 | EVENTOUT |
| | PG1 | UART7_RTS | DCMIPP_PIXCLK/ DCMI_PIXCLK/ PSSI_PDCK | TIM13_CH1 | - | FMC_A19 | - | LCD_G1 | EVENTOUT |
| | PG2 | UART7_CTS | DCMIPP_D6/DCMI_D6/ PSSI_D6 | SAI2_MCLK_B | TIM14_CH1 | FMC_A21 | - | LCD_R0 | EVENTOUT |
| | PG3 | - | DCMIPP_HSYNC/ DCMI_HSYNC/PSSI_DE | - | ETH1_MII_TXD2/ ETH1_RGMII_TXD2 | - | - | - | EVENTOUT |
| | PG4 | - | - | - | ETH1_MII_TXD3/ ETH1_RGMII_TXD3 | - | - | LCD_B0 | EVENTOUT |
| | PG5 | - | - | - | ETH1_MII_RX_ER | - | - | LCD_B1 | EVENTOUT |
| | PG6 | - | DCMIPP_D12/DCMI_D12/ PSSI_D12 | - | ETH1_MII_CRS | - | - | LCD_B3 | EVENTOUT |
| | PG7 | - | DCMIPP_D13/DCMI_D13/ PSSI_D13 | - | ETH1_PHY_INTN | - | - | - | EVENTOUT |
| | PG8 | UART4_CTS | - | - | SDMMC2_D1 | FMC_A20 | - | LCD_G7 | HDP7 |
| | PG9 | - | - | - | - | FMC_D8/FMC_AD8 | - | LCD_R7 | EVENTOUT |
| | PG10 | - | DCMIPP_D2/DCMI_D2/ PSSI_D2 | - | UART5_TX | FMC_A16/FMC_CLE | - | LCD_G4 | HDP5 |
| | PG11 | UART7_RX | - | - | ETH1_MDC | - | - | LCD_R6 | EVENTOUT |
| | PG12 | UART7_TX | - | - | - | FMC_A18 | - | LCD_G0 | EVENTOUT |
| | PG13 | - | DCMIPP_D12/DCMI_D12/ PSSI_D12 | SAI2_FS_A | - | FMC_NE1 | - | LCD_DE | EVENTOUT |
| | PG14 | USART2_RTS | DCMIPP_D11/DCMI_D11/ PSSI_D11 | FMC_NCE | - | FMC_NE2 | - | LCD_B1 | EVENTOUT |
| | PG15 | - | DCMIPP_D4/DCMI_D4/ PSSI_D4 | SPI1_RDY | ETH1_MII_RX_CLK/ ETH1_RMII_REF_CLK | FMC_CLK | - | LCD_B0 | EVENTOUT |

**Table 17. Alternate functions: AF8 to AF15 (continued)**

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port H | PH0 | - | - | - | - | - | - | - | EVENTOUT |
| | PH1 | - | - | - | - | - | - | - | EVENTOUT |
| | PH2 | - | DCMIPP_D11/DCMI_D11/ PSSI_D11 | SDMMC1_CMD | UART5_RX | FMC_NE3 | - | - | EVENTOUT |
| | PH3 | UART7_TX | - | - | - | - | - | LCD_B4 | EVENTOUT |
| | PH4 | UART7_TX | - | - | - | - | - | LCD_R4 | EVENTOUT |
| | PH5 | - | - | - | ETH1_MDC | | - | | EVENTOUT |
| | PH6 | - | - | - | - | - | - | LCD_B5 | EVENTOUT |
| | PH7 | - | - | - | - | - | - | | EVENTOUT |
| | PH8 | - | - | - | - | - | - | | EVENTOUT |
| | PH9 | UART4_RX | DCMIPP_D6/DCMI_D6/ PSSI_D6 | SDMMC1_D4 | SDMMC2_D4 | SDMMC1_CKIN | - | FMC_D9/ FMC_AD9 | HDP0 |
| | PH10 | - | - | - | - | - | - | - | - |
| | PH11 | - | - | - | - | - | - | - | - |
| | PH12 | - | - | - | - | - | - | - | - |
| | PH13 | - | - | - | - | - | - | - | - |
| | PH14 | - | - | - | - | - | - | - | - |
| | PH15 | - | - | - | - | - | - | - | - |

**Table 17. Alternate functions: AF8 to AF15 (continued)**

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port N | PN0 | - | XSPIM_P2_DQS0 | - | - | FMC_A25 | - | - | EVENTOUT |
| | PN1 | - | XSPIM_P2_NCS1 | - | - | FMC_A24 | - | - | EVENTOUT |
| | PN2 | - | XSPIM_P2_IO0 | - | - | FMC_A23 | - | - | EVENTOUT |
| | PN3 | - | XSPIM_P2_IO1 | - | - | FMC_A22 | - | - | EVENTOUT |
| | PN4 | - | XSPIM_P2_IO2 | - | - | - | - | - | EVENTOUT |
| | PN5 | - | XSPIM_P2_IO3 | - | - | - | - | - | EVENTOUT |
| | PN6 | - | XSPIM_P2_CLK | - | - | - | - | - | EVENTOUT |
| | PN7 | - | XSPIM_P2_NCLK | - | - | - | - | - | EVENTOUT |
| | PN8 | - | XSPIM_P2_IO4 | - | - | - | - | - | EVENTOUT |
| | PN9 | - | XSPIM_P2_IO5 | DCMIPP_D5/DCMI_D5/ PSSI_D5 | - | - | - | - | EVENTOUT |
| | PN10 | - | XSPIM_P2_IO6 | - | - | - | - | LCD_B4 | EVENTOUT |
| | PN11 | - | XSPIM_P2_IO7 | - | - | - | - | LCD_B6 | EVENTOUT |
| | PN12 | - | XSPIM_P2_NCS2 | - | - | - | - | - | EVENTOUT |
| Port O | PO0 | - | XSPIM_P1_NCS1 | - | - | FMC_A22 | - | - | EVENTOUT |
| | PO1 | - | XSPIM_P1_NCS2 | - | - | FMC_A23 | - | - | EVENTOUT |
| | PO2 | - | XSPIM_P1_DQS0 | - | - | FMC_A24 | - | LCD_B7 | EVENTOUT |
| | PO3 | - | XSPIM_P1_DQS1 | - | - | FMC_A25 | - | LCD_G3 | EVENTOUT |
| | PO4 | - | XSPIM_P1_CLK | LCD_B4 | - | FMC_A24 | - | FMC_NBL2 | EVENTOUT |
| | PO5 | - | XSPIM_P1_NCLK | - | - | FMC_A25 | - | FMC_NBL3 | EVENTOUT |

## Table 17. Alternate functions: AF8 to AF15 (continued)

| Port | | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI6/I2S6/SAI2/ UART4/5/8/ LPUART1/SDIO1/ USB_PD/SPDIFRX | FDCAN1/2/ TIM13/14/ OCSPI1/2/FMC/ SDIO2/LCD/SPDIFRX | SAI2/TIM8/OCSPI1/ FMC/SDIO2/ OTG1_HS/OTG1_FS/ LCD/COMP/CRS | I2C4/USART10/UART7/9/ SWPMI1/TIM1/8/DFSDM1/2/ OCSPI1/SDIO2/MDIOS/ USB_PD/LCD/COMP | TIM1/8/FMC/SDIO1/ MDIOS/LCD/COMP | TIM1/DCMI/ PSSI/LCD/COMP | UART5/LCD | SYS |
| Port P | PP0 | - | XSPIM_P1_IO0 | - | - | FMC_D16 | - | - | EVENTOUT |
| | PP1 | - | XSPIM_P1_IO1 | - | - | FMC_D17 | - | - | EVENTOUT |
| | PP2 | - | XSPIM_P1_IO2 | - | - | FMC_D18 | - | - | EVENTOUT |
| | PP3 | - | XSPIM_P1_IO3 | - | - | FMC_D19 | - | - | EVENTOUT |
| | PP4 | - | XSPIM_P1_IO4 | - | - | FMC_D20 | - | - | EVENTOUT |
| | PP5 | - | XSPIM_P1_IO5 | - | - | FMC_D21 | - | - | EVENTOUT |
| | PP6 | - | XSPIM_P1_IO6 | - | - | FMC_D22 | - | - | EVENTOUT |
| | PP7 | - | XSPIM_P1_IO7 | - | - | FMC_D23 | - | - | EVENTOUT |
| | PP8 | - | XSPIM_P1_IO8 | - | - | FMC_D24 | - | - | EVENTOUT |
| | PP9 | - | XSPIM_P1_IO9 | - | - | FMC_D25 | - | - | EVENTOUT |
| | PP10 | - | XSPIM_P1_IO1O | - | ETH1_MDC | FMC_D26 | - | - | EVENTOUT |
| | PP11 | - | XSPIM_P1_IO11 | - | - | FMC_D27 | - | - | EVENTOUT |
| | PP12 | - | XSPIM_P1_IO12 | - | - | FMC_D28 | - | - | EVENTOUT |
| | PP13 | - | XSPIM_P1_IO13 | - | - | FMC_D29 | - | - | EVENTOUT |
| | PP14 | - | XSPIM_P1_IO14 | - | - | FMC_D30 | - | - | EVENTOUT |
| | PP15 | - | XSPIM_P1_IO15 | - | - | FMC_D31 | - | LCD_B5 | EVENTOUT |
| Port Q | PQ0 | - | - | - | - | - | - | - | EVENTOUT |
| | PQ1 | - | - | - | - | - | - | - | EVENTOUT |
| | PQ2 | - | SAI2_SCK_B | - | - | - | - | - | EVENTOUT |
| | PQ3 | - | - | - | - | - | - | - | EVENTOUT |
| | PQ4 | - | - | - | - | - | - | - | EVENTOUT |
| | PQ5 | - | SAI2_FS_B | - | - | - | - | - | EVENTOUT |
| | PQ6 | - | SAI2_SD_B | - | - | - | - | - | EVENTOUT |
| | PQ7 | - | SAI2_MCLK_B | - | - | - | - | - | EVENTOUT |

# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

## 5.1 Device marking

Refer to "*Reference device marking schematics for STM32 microcontrollers and microprocessors*" (TN1433), available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

## 5.2 VFBGA142 package information (B0GM)

This VFBGA is a 142-ball, 8 x 8 mm, 0.50 mm pitch, very thin fine pitch ball grid array package.

*Note: See list of notes in the notes section.*

**Figure 13. VFBGA142 - Outline(13)**

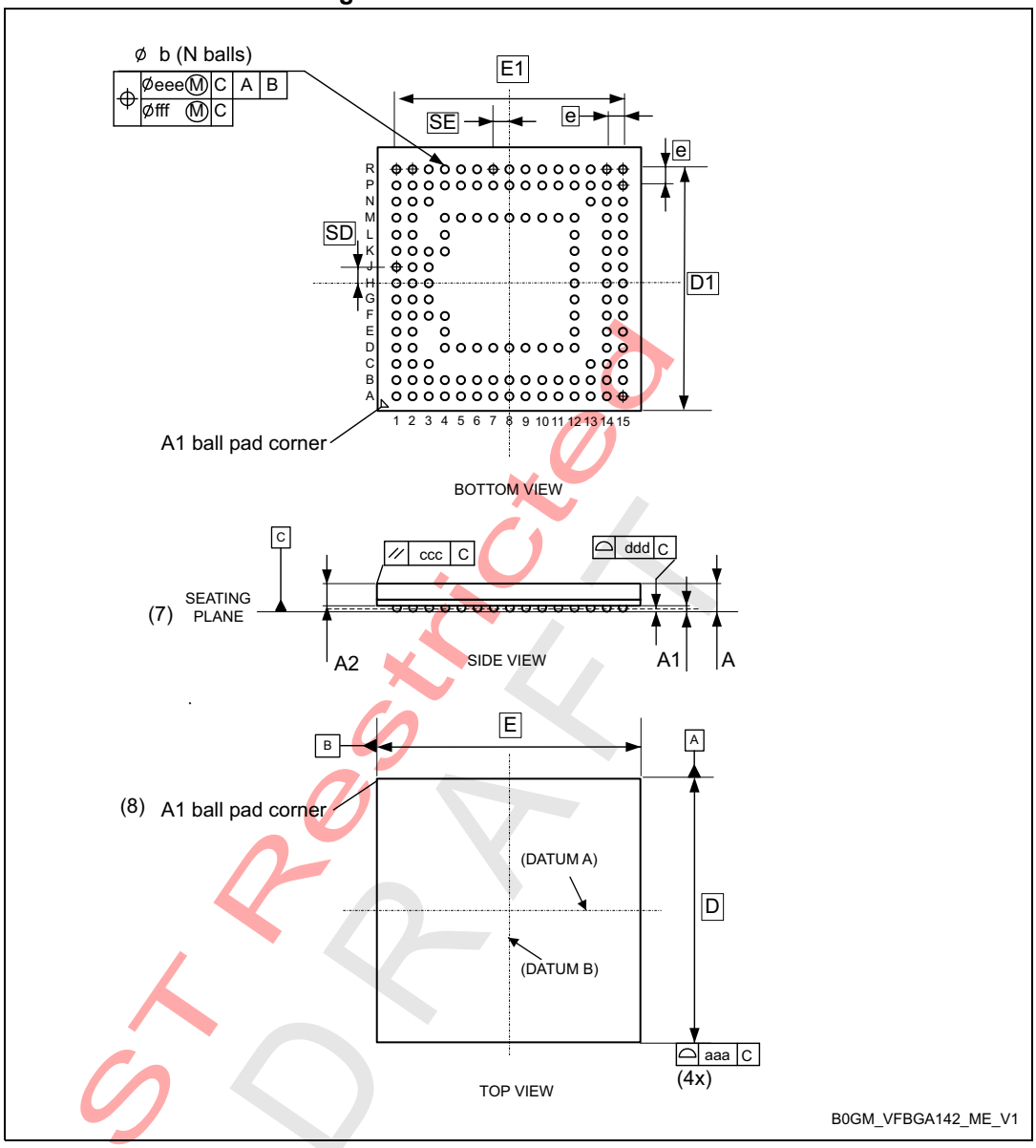


**Table 18. VFBGA142 - Mechanical data**

| Symbol | millimeters[1] | | | inches[12] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A[2][3] | - | - | 1.00 | - | - | 0.0394 |
| A1[4] | 0.13 | - | - | 0.0051 | - | - |
| A2 | - | 0.59 | - | - | 0.0232 | - |
| b[5] | 0.26 | 0.31 | 0.36 | 0.0102 | 0.0122 | 0.0142 |
| D[6] | 8.00 BSC | | | 0.3149 BSC | | |
| D1 | 7.00 BSC | | | 0.2756 BSC | | |
| E | 8.00 BSC | | | 0.3149 BSC | | |
| E1 | 7.00 BSC | | | 0.2756 BSC | | |
| e[9] | 0.50 BSC | | | 0.0197 BSC | | |
| N[10] | 142 | | | | | |
| SD[11] | 0.50 BSC | | | 0.0197 BSC | | |
| SE[11] | 0.50 BSC | | | 0.0197 BSC | | |
| aaa | 0.15 | | | 0.0059 | | |
| ccc | 0.20 | | | 0.0079 | | |
| ddd | 0.08 | | | 0.0031 | | |
| eee | 0.15 | | | 0.0059 | | |
| fff | 0.05 | | | 0.0020 | | |

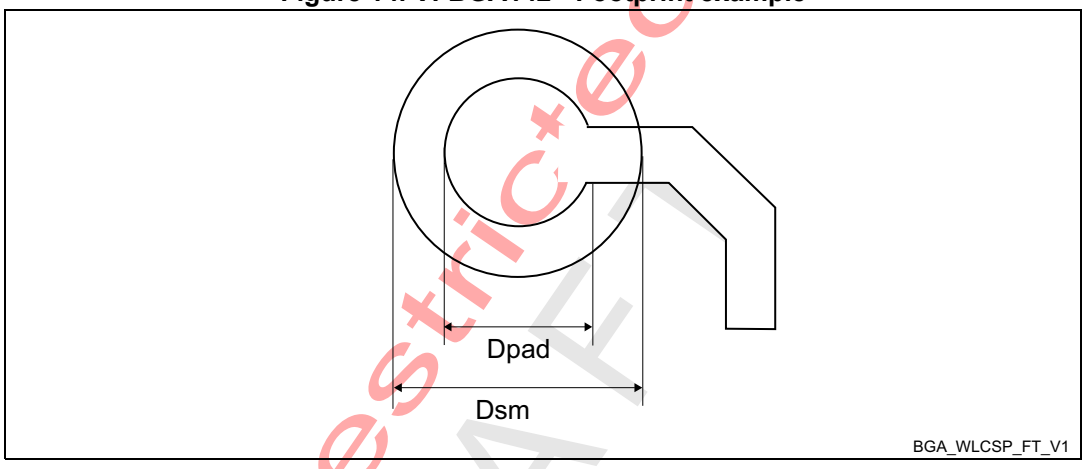


**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.

8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

**Figure 14. VFBGA142 - Footprint example**




1. Dimensions are expressed in millimeters.

**Table 19. VFBGA142 - Example of PCB design rules (0.50 mm pitch BGA)**

| Dimension | Values |
|---|---|
| Pitch | 0.50 mm |
| Dpad | 0.300 mm |
| Dsm | 0.300 mm typ. |
| Stencil opening | 0.350 mm |
| Stencil thickness | 0.140 mm |

## 5.3 VFBGA169 package information (B0LA)

This VFBGA is a 169-ball, 6 x 6 mm, 0.4 mm pitch, very thin fine pitch ball grid array package.

*Note: See list of notes in the notes section.*

**Figure 15. VFBGA169 - Outline(13)**

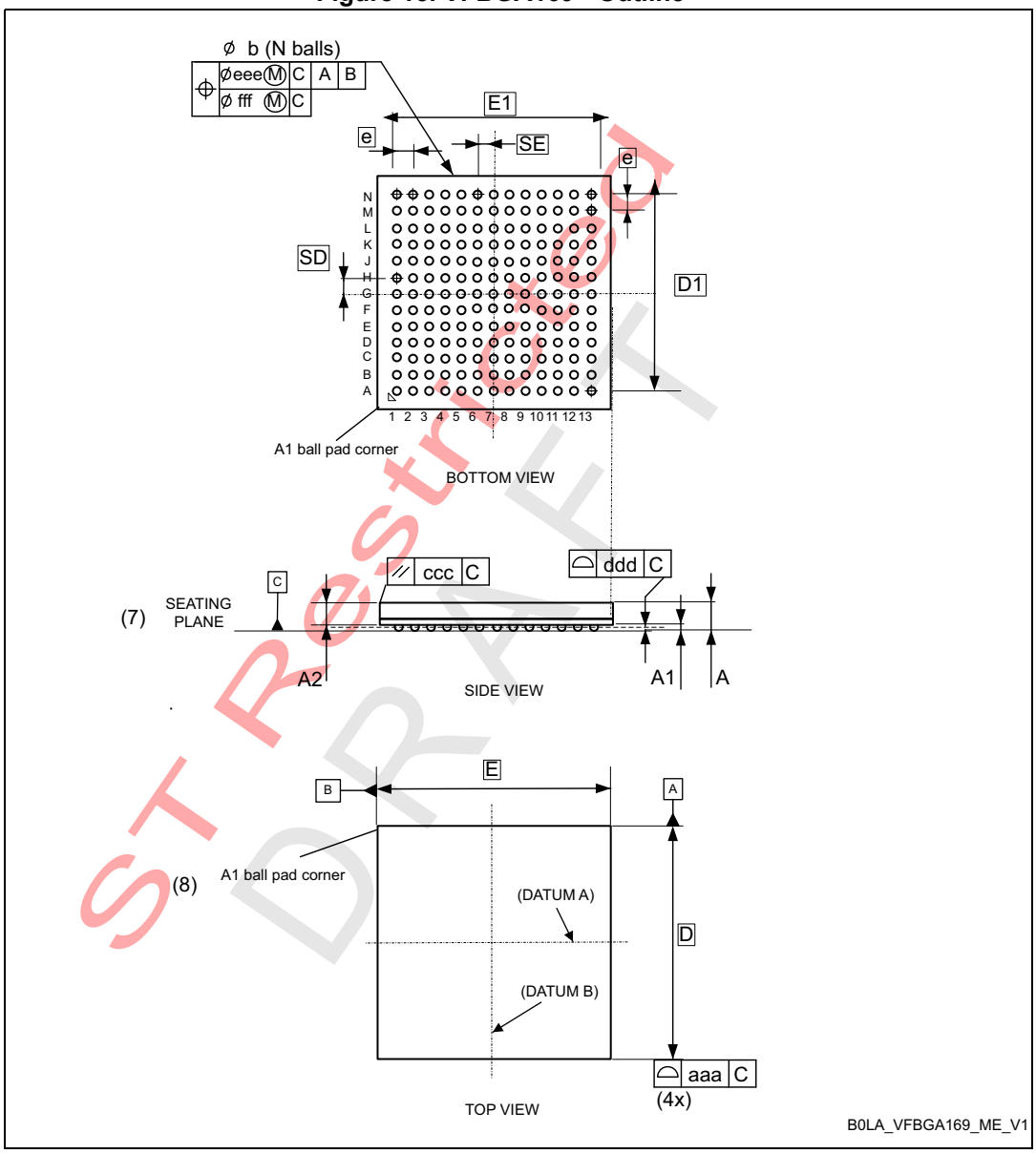


**Table 20. VFBGA169 - Mechanical data**

| Symbol | millimeters[1] | | | inches[12] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A[2][3] | - | - | 1.00 | - | - | 0.0394 |
| A1[4] | 0.11 | - | - | 0.0043 | - | - |
| A2 | - | 0.62 | - | - | 0.0344 | - |
| b[5] | 0.22 | 0.26 | 0.30 | 0.0087 | 0.0102 | 0.0118 |
| D[6] | 6.00 BSC | | | 0.2362 BSC | | |
| D1 | 4.80 BSC | | | 0.1890 BSC | | |
| E | 6.00 BSC | | | 0.2362 BSC | | |
| E1 | 4.80 BSC | | | 0.1890 BSC | | |
| e[9] | 0.40 BSC | | | 0.0157 BSC | | |
| N[10] | 169 | | | | | |
| SD[11] | 0.40 BSC | | | 0.0157 BSC | | |
| SE[11] | 0.40 BSC | | | 0.0157 BSC | | |
| aaa | 0,10 | | | 0.0039 | | |
| ccc | 0.20 | | | 0.0079 | | |
| ddd | 0.08 | | | 0.0031 | | |
| eee | 0.15 | | | 0.0059 | | |
| fff | 0.05 | | | 0.0020 | | |



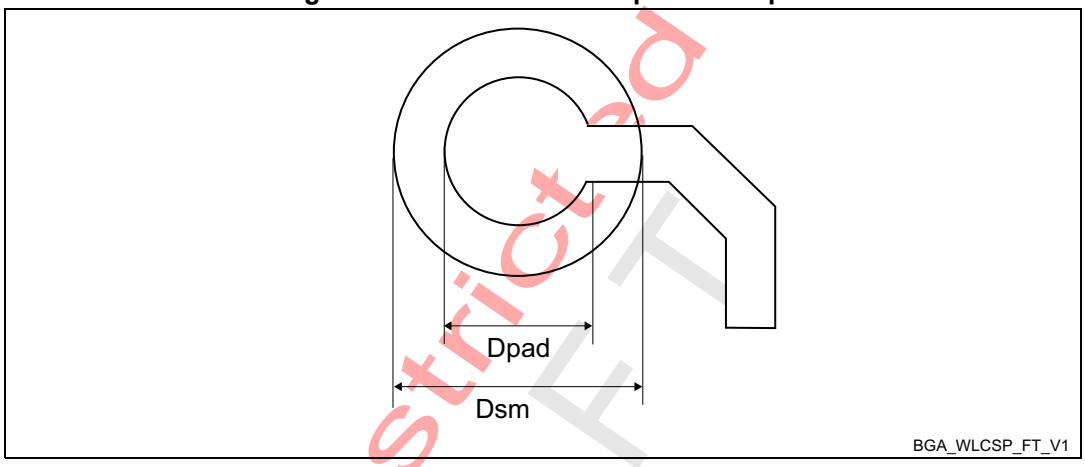
**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2018.
2. VFBGA stands for very thin fine pitch ball grid array: 0.80 mm < A ≤ 1.00 mm / Fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or

integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD & SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

**Figure 16. VFBGA169 - Footprint example**




1. Dimensions are expressed in millimeters.

**Table 21. VFBGA169 - Example of PCB design rules (0.4 mm pitch BGA)**

| Dimension | Values |
|---|---|
| Pitch | 0.4 mm |
| Dpad | 0.250 mm |
| Dsm | 0.230 mm typ. |
| Stencil opening | 0.475 mm |
| Stencil thickness | 0.120 mm |

## 5.4 VFBGA178 package information (B0GL)

This VFBGA is a 178-ball, 12 x 12 mm, 0.80 mm pitch, very thin fine pitch ball grid array package.

*Note: See list of notes in the notes section.*

**Figure 17. VFBGA178 - Outline(13)**

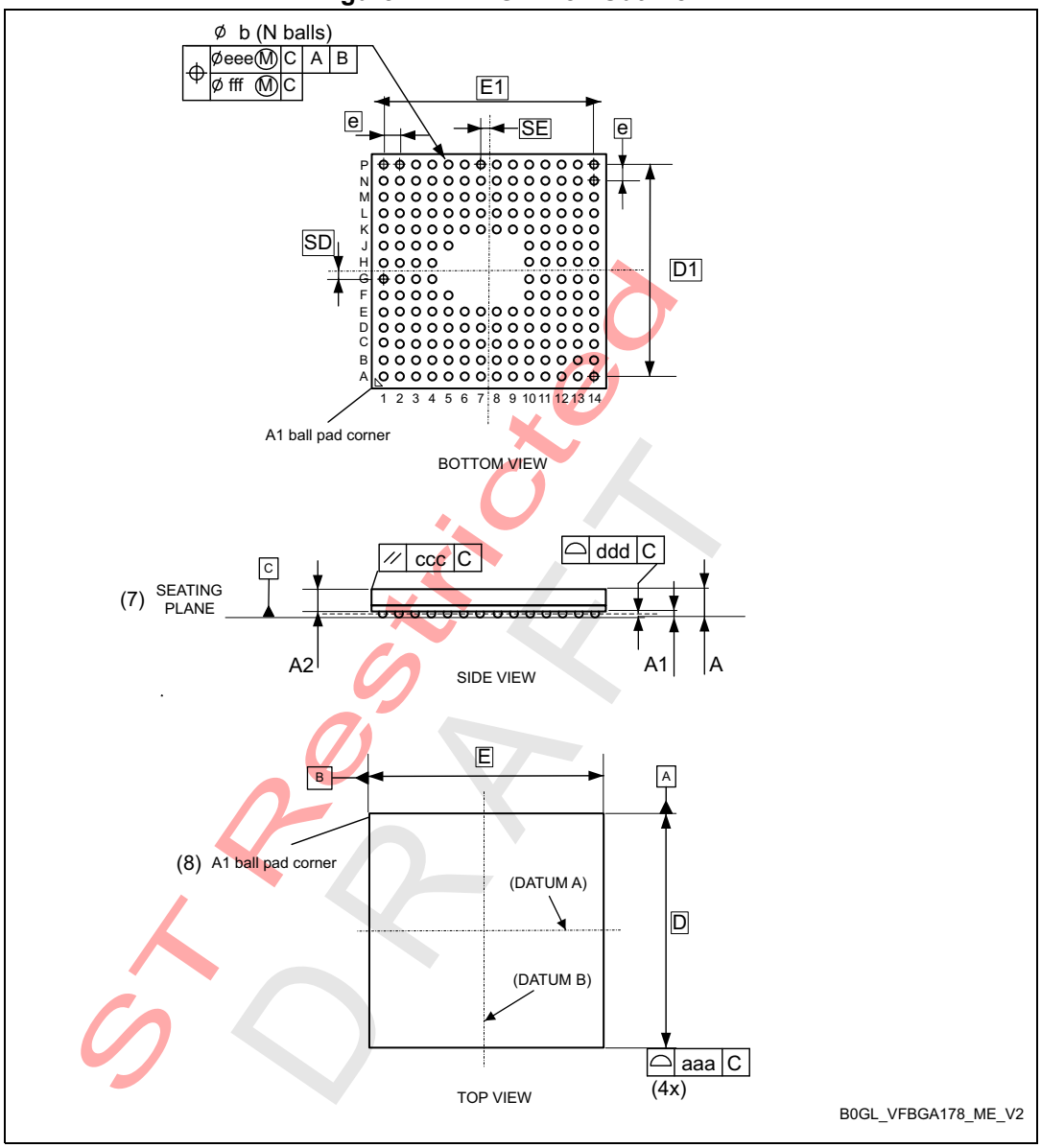


**Table 22. VFBGA178 - Mechanical data**

| Symbol | millimeters[1] | | | inches[12] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A[2][3] | - | - | 1.00 | - | - | 0.0394 |
| A1[4] | 0.21 | - | - | 0.0082 | - | - |
| A2 | - | 0.51 | - | - | 0.0201 | - |
| b[5] | 0.38 | 0.43 | 0.48 | 0.150 | 0.0170 | 0.189 |
| D[6] | 12.00 BSC | | | 0.4724 BSC | | |
| D1 | 10.40 BSC | | | 0.4094 BSC | | |
| E | 12.00 BSC | | | 0.4724 BSC | | |
| E1 | 10.40 BSC | | | 0.4094 BSC | | |
| e[9] | 0.80 BSC | | | 0.0315 BSC | | |
| N[10] | 178 | | | | | |
| SD[11] | 0.40 BSC | | | 0.0157 BSC | | |
| SE[11] | 0.40 BSC | | | 0.0157 BSC | | |
| aaa | 0.15 | | | 0.0059 | | |
| ccc | 0.20 | | | 0.0079 | | |
| ddd | 0.10 | | | 0.0039 | | |
| eee | 0.15 | | | 0.0059 | | |
| fff | 0.08 | | | 0.0031 | | |

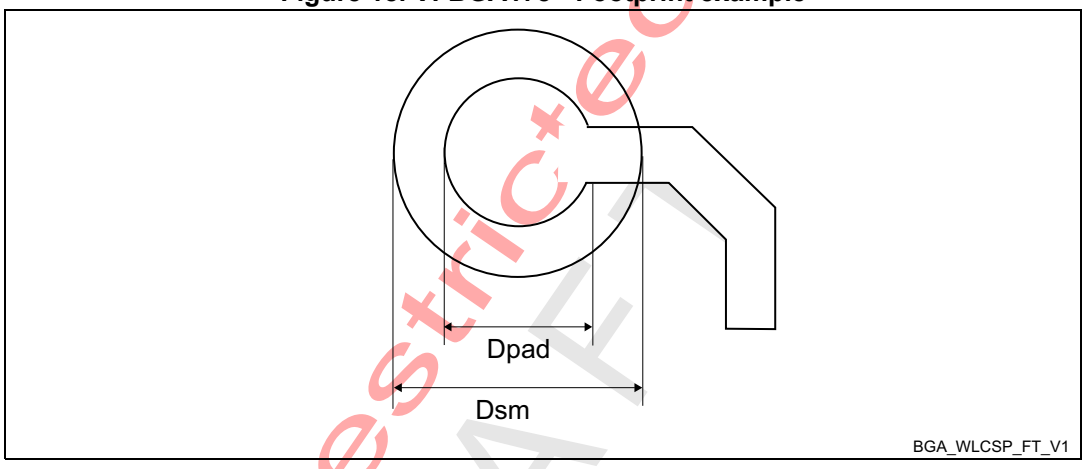


**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.

8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

**Figure 18. VFBGA178 - Footprint example**




1. Dimensions are expressed in millimeters.

**Table 23. VFBGA178 - Example of PCB design rules (0.80 mm pitch BGA)**

| Dimension | Values |
|---|---|
| Pitch | 0.8 mm |
| Dpad | 0.400 mm |
| Dsm | 0.470 mm typ. |
| Stencil opening | 0.400 mm |
| Stencil thickness | 0.100 mm |

## 5.5 VFBGA198 package information (B0GJ)

This VFBGA is a 198-ball, 10 x 10 mm, 0.65 mm pitch, very thin fine pitch ball grid array package.

*Note: See list of notes in the notes section.*

**Figure 19. VFBGA198 - Outline(13)**

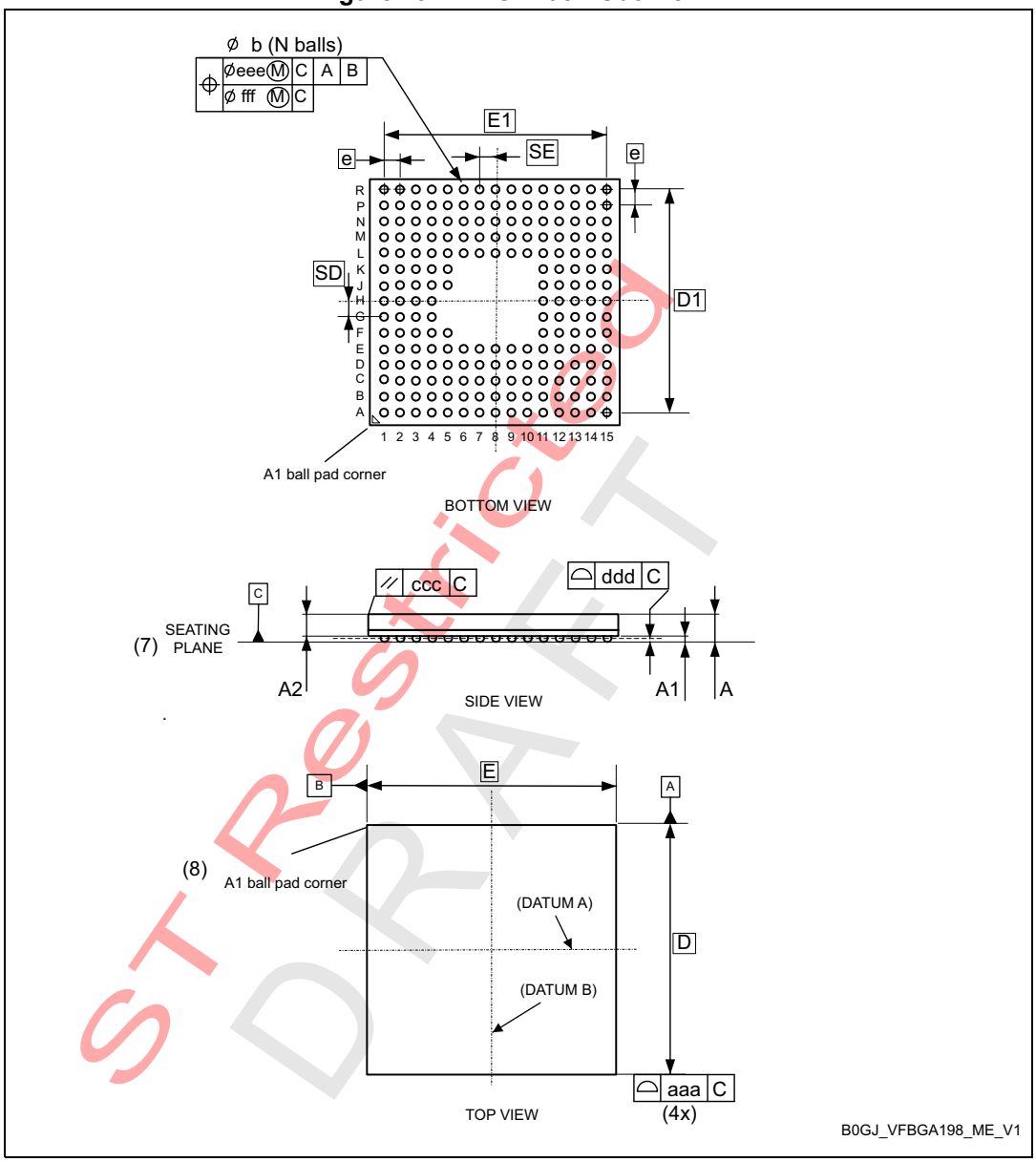


**Table 24. VFBGA198 - Mechanical data**

| Symbol | millimeters[1] | | | inches[12] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A[2][3] | - | - | 1.00 | - | - | 0.0394 |
| A1[4] | 0.21 | - | - | 0.0082 | - | - |
| A2 | - | 0.51 | - | - | 0.0201 | - |
| b[5] | 0.35 | 0.40 | 0.45 | 0.0138 | 0.0157 | 0.0177 |
| D[6] | 10.00 BSC | | | 0.3937BSC | | |
| D1 | 9.10 BSC | | | 0.3583 BSC | | |
| E | 10.00 BSC | | | 0.3937BSC | | |
| E1 | 9.10 BSC | | | 0.3583 BSC | | |
| e[9] | 0.65 BSC | | | 0.0256 BSC | | |
| N[10] | 198 | | | | | |
| SD[11] | 0.65 BSC | | | 0.0256 BSC | | |
| SE[11] | 0.65 BSC | | | 0.0256 BSC | | |
| aaa | 0.15 | | | 0.0059 | | |
| ccc | 0.20 | | | 0.0079 | | |
| ddd | 0.10 | | | 0.0039 | | |
| eee | 0.15 | | | 0.0059 | | |
| fff | 0.08 | | | 0.00315 | | |

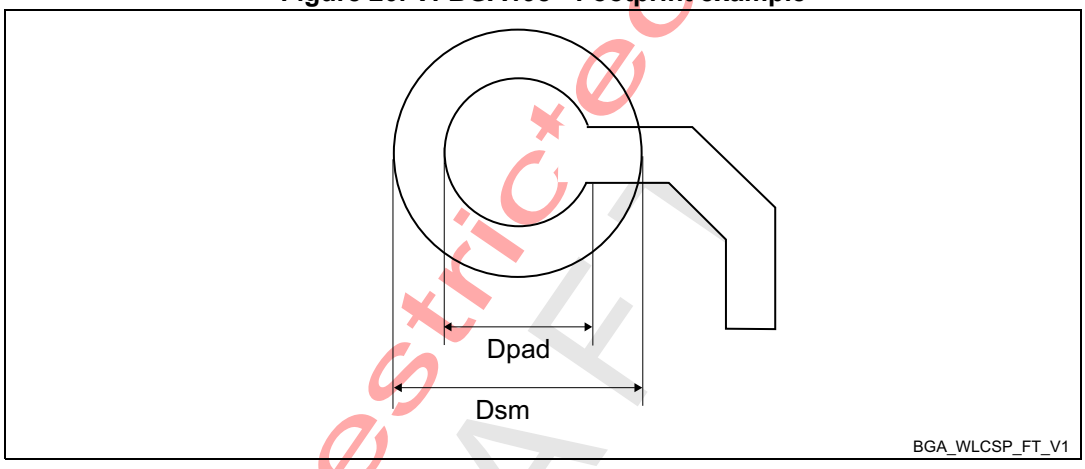


**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.

8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

**Figure 20. VFBGA198 - Footprint example**




1. Dimensions are expressed in millimeters.

**Table 25. VFBGA198 - Example of PCB design rules (0.65 mm pitch BGA)**

| Dimension | Values |
|---|---|
| Pitch | 0.65 mm |
| Dpad | 0.350 mm |
| Dsm | 0.350 mm typ. |
| Stencil opening | 0.400 mm |
| Stencil thickness | 0.170 mm |

## 5.6 VFBGA223 package information (B0GK)

This VFBGA is a 223-ball, 10 x 10 mm, 0.50 mm pitch, very thin fine pitch ball grid array package.

*Note: See list of notes in the notes section.*

**Figure 21. VFBGA223 - Outline(13)**

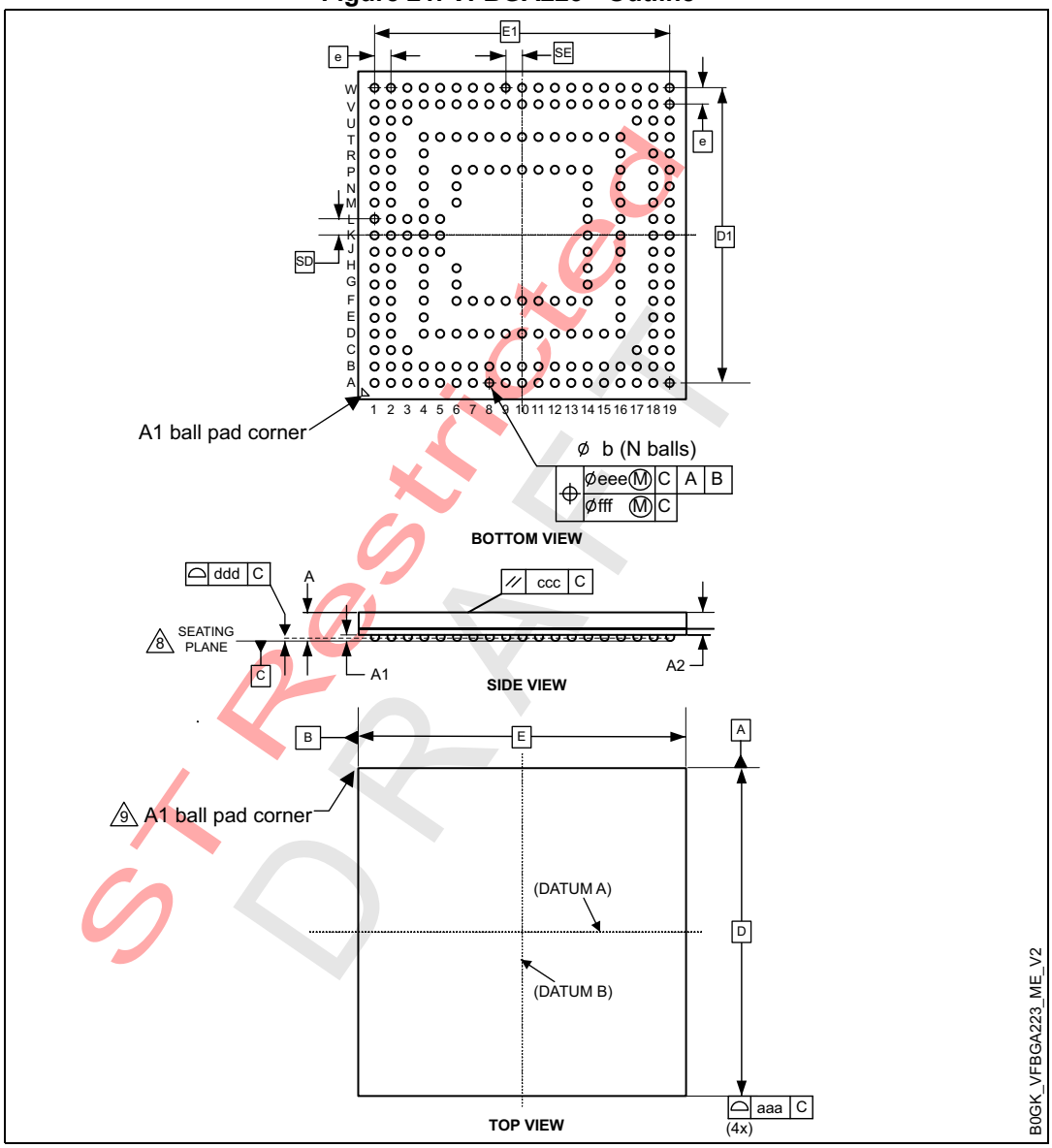


**Table 26. VFBGA223 - Mechanical data**

| Symbol | millimeters[1] | | | inches[12] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A[2][3] | - | - | 1.00 | - | - | 0.0394 |
| A1[4] | 0.13 | - | - | 0.0051 | - | - |
| A2 | - | 0.51 | - | - | 0.0201 | - |
| b[5] | 0.26 | 0.31 | 0.36 | 0.0102 | 0.0122 | 0.0142 |
| D[6] | 10.00 BSC | | | 0.3937BSC | | |
| D1 | 9.00 BSC | | | 0.3543 BSC | | |
| E | 10.00 BSC | | | 0.3937BSC | | |
| E1 | 9.00 BSC | | | 0.3543 BSC | | |
| e[9] | 0.50 BSC | | | 0.0197 BSC | | |
| N[10] | 223 | | | | | |
| SD[11] | 0.50 BSC | | | 0.0197 BSC | | |
| SE[11] | 0.50 BSC | | | 0.0197 BSC | | |
| aaa[12] | 0.15 | | | 0.0059 | | |
| ccc[12] | 0.20 | | | 0.0079 | | |
| ddd[12] | 0.08 | | | 0.0031 | | |
| eee[12] | 0.15 | | | 0.0059 | | |
| fff[12] | 0.05 | | | 0.0020 | | |



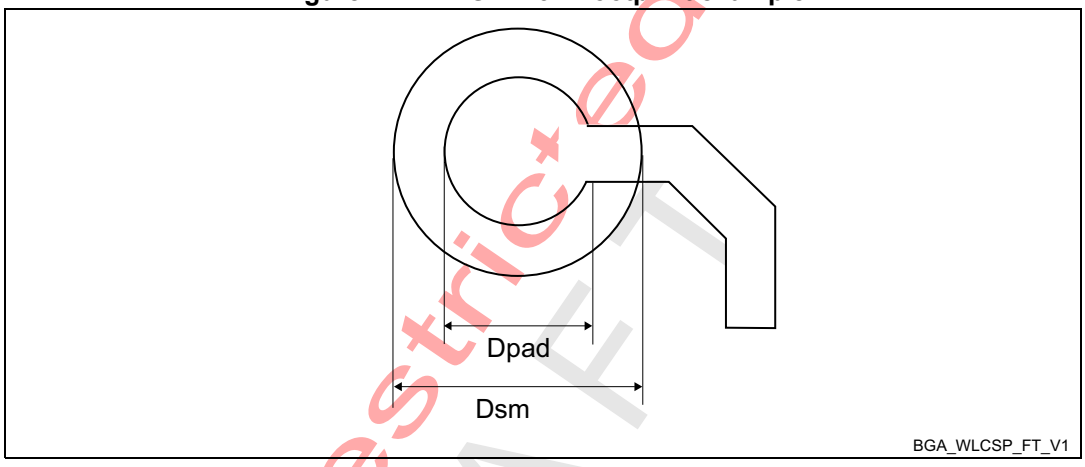
**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2009 apart European projection.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or

integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Tolerance of form and position drawing.
13. Values in inches are converted from mm and rounded to 4 decimal digits.
14. Drawing is not to scale.

**Figure 22. VFBGA223 - Footprint example**




1. Dimensions are expressed in millimeters.

**Table 27. VFBGA223 - Example of PCB design rules (0.50 mm pitch BGA)**

| Dimension | Values |
|---|---|
| Pitch | 0.50 mm |
| Dpad | 0.300 mm |
| Dsm | 0.300 mm typ. |
| Stencil opening | 0.350 mm |
| Stencil thickness | 0.140 mm |

## 5.7 VFBGA264 package information (B0GH)

This VFBGA is a 264-ball, 14 x 14 mm, 0.8 mm pitch, very thin fine pitch ball grid array package.

*Note: See list of notes in the notes section.*

**Figure 23. VFBGA264 - Outline(13)**

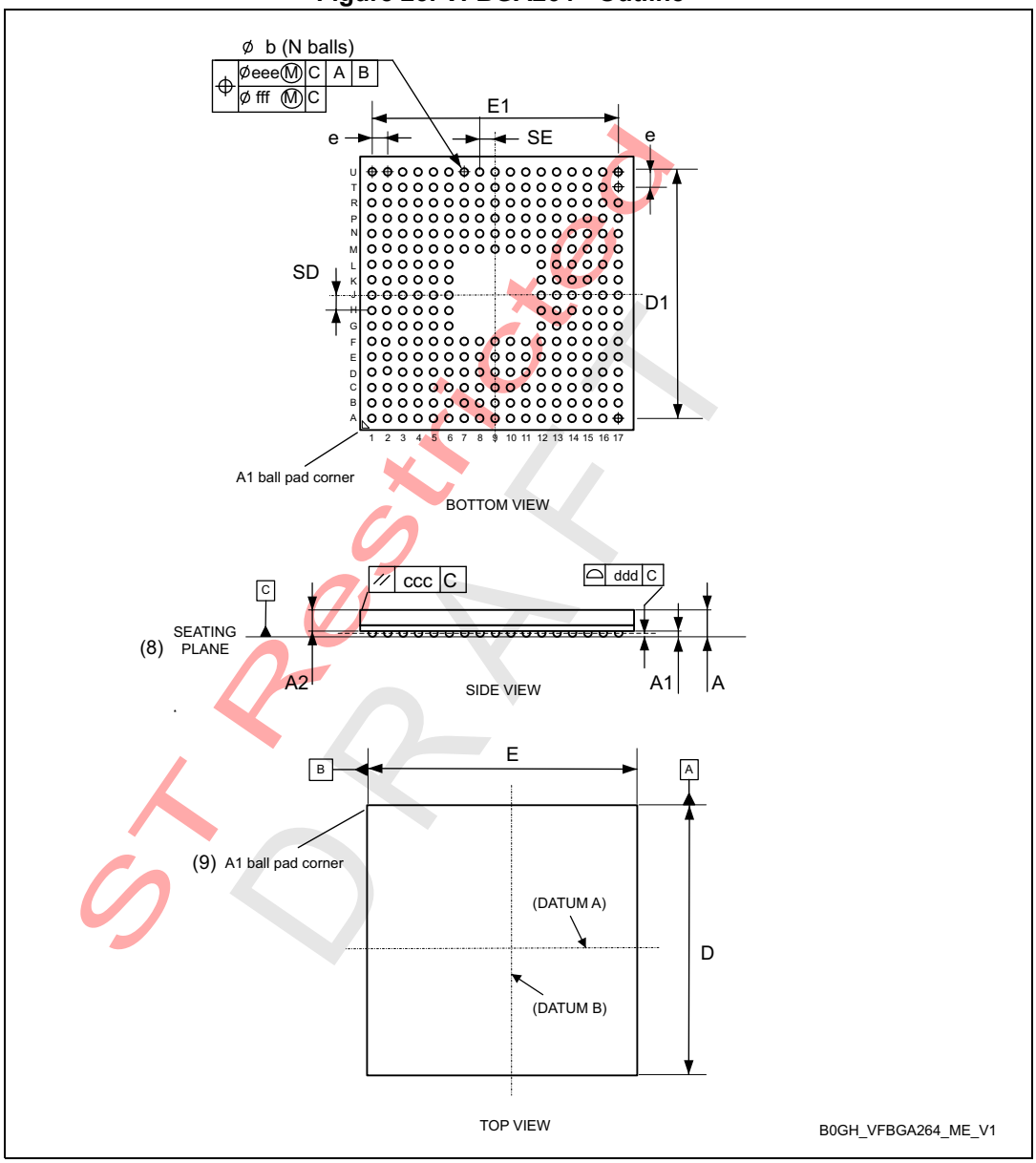


**Table 28. VFBGA264 - Mechanical data**

| Symbol | millimeters[1] | | | inches[12] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A[2][3] | - | - | 1.00 | - | - | 0.0394 |
| A1[4] | 0.21 | - | - | 0.0082 | - | - |
| A2 | - | 0.59 | - | - | 0.0232 | - |
| b[5] | 0.38 | 0.43 | 0.48 | 0.150 | 0.0170 | 0.189 |
| D[6] | 14.00 BSC | | | 0.5512 BSC | | |
| D1 | 12.80 BSC | | | 0.5039 BSC | | |
| E | 14.00 BSC | | | 0.5512 BSC | | |
| E1 | 12.80 BSC | | | 0.5039 BSC | | |
| e[9] | 0.80 BSC | | | 0.03149 BSC | | |
| N[10] | 264 | | | | | |
| SD[11] | 0.80 BSC | | | 0.03149 BSC | | |
| SE[11] | 0.80 BSC | | | 0.03149 BSC | | |
| aaa | 0.15 | | | 0.0059 | | |
| ccc | 0.20 | | | 0.0079 | | |
| ddd | 0.10 | | | 0.0039 | | |
| eee | 0.15 | | | 0.0059 | | |
| fff | 0.08 | | | 0.00315 | | |

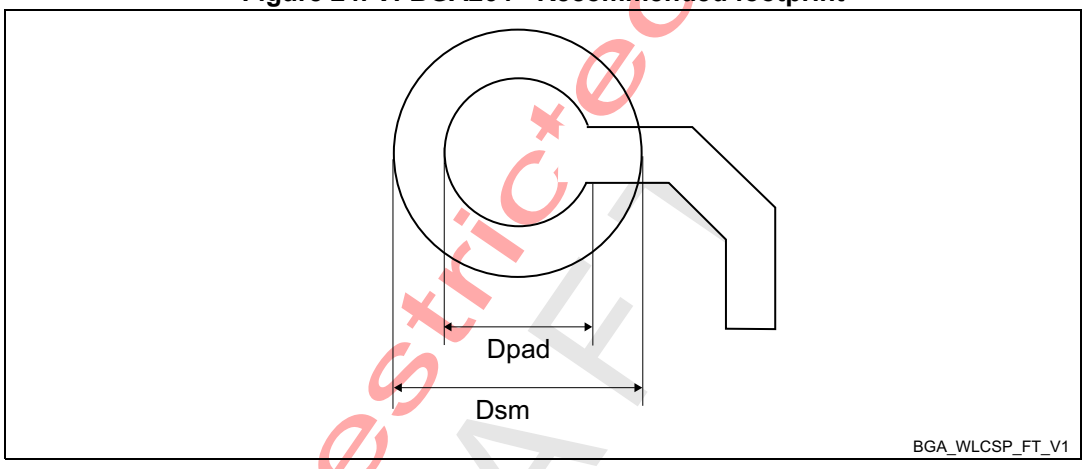


**Notes:**

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. VFBGA stands for very thin profile fine pitch ball grid array: 0.8 mm < A ≤ 1.00 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.

8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to four decimal digits.
13. Drawing is not to scale.

**Figure 24. VFBGA264 - Recommended footprint**




1. Dimensions are expressed in millimeters.

**Table 29. VFBGA264 - Recommended PCB design rules (0.8 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.8 mm |
| Dpad | 0.400 mm |
| Dsm | 0.470 mm typ. |
| Stencil opening | 0.400 mm |
| Stencil thickness | 0.100 mm |

# 6 Ordering information

Example: STM32 N 6 5 7 X 0 H 3 Q U

**Device family**

STM32 = Arm® based 32-bit microcontroller

**Product type**

N = neural

**Device subfamily**

6 = Cortex M55 core

**Die**

4 = Neural-ART, 4 Mbytes

5 = Neural-ART, 4 Mbytes, crypto

**Line**

5 = base

7 = artificial intelligence

**Pin/ball count**

Z = 142
A = 169
I = 178
B = 198
L = 223
X = 264

**Flash memory size**

0 = 0-1 Kbytes

**Package**

H = VFBGA

**Temperature range**

7 = Industrial temperature range, -40 to 105 °C

3 = Industrial temperature range, -40 to 125 °C

**Dedicated pinout**

Q = Internal SMPS step-down converter

**Packing**

U = universal part (not for production, sampling, and tools)

For a list of available options (such as speed or package) or for further information on any aspect of this device, contact the nearest ST sales office.

# 7 Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on www.st.com for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.
- All security features of ST products (inclusive of any hardware, software, documentation, and the like), including but not limited to any enhanced security features added by ST, are provided on an "AS IS" BASIS. AS SUCH, TO THE EXTENT PERMITTED BY APPLICABLE LAW, ST DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, unless the applicable written and signed contract terms specifically provide otherwise.

# 8 Revision history

**Table 30. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 22-Jan-2021 | 0.1 | Initial draft release. |
| 24-Sep-2021 | 0.2 | Updated:<br>– proposed packages<br>– Number of I/Os in *General-purpose I/Os* |
| 15-Apr-2022 | 0.3 | Updated:<br>– *Features*<br>– New *Section 7: Important security notice* |
| 30-May-2023 | 0.4 | Updated image on cover page.<br>Updated document title, *Features*, and *Section 6: Ordering information*.<br>Added *Table 1: Device summary*.<br>Added *Section 3: Functional overview*, *Section 4: Pinout, pin description and alternate functions*, *Section 5: Package information*, and their subsections.<br>For internal use only. |
| 06-Sep-2023 | 0.5 | Updated image on cover page.<br>Updated *Features*, *Section 3.4.4: SMPS usage*, and *Section 6: Ordering information*.<br>Updated *Table 2: STM32N657xx features and peripheral counts* and *Table 15: STM32N657xx pin description*. |
| 25-Sep-2023 | 0.6 | Updated figures *7* to *12*.<br>Added *Section 5.1: Device marking*. |
| 23-Nov-2023 | 0.7 | Updated document title and *Section 3.52: USB on-the-go highspeed (OTG)*.<br>Updated *Table 15: STM32N657xx pin description*, *Table 16: Alternate functions: AF0 to AF7*, and *Table 17: Alternate functions: AF8 to AF15*.<br>Updated figures *7* to *12*. |
| 02-Jan-2024 | 0.8 | Updated *Figure 21: VFBGA223 - Outline*[13] and *Table 26: VFBGA223 - Mechanical data*. |

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.