Experiment #5
PV Power Electronics Laboratory

Completed By:
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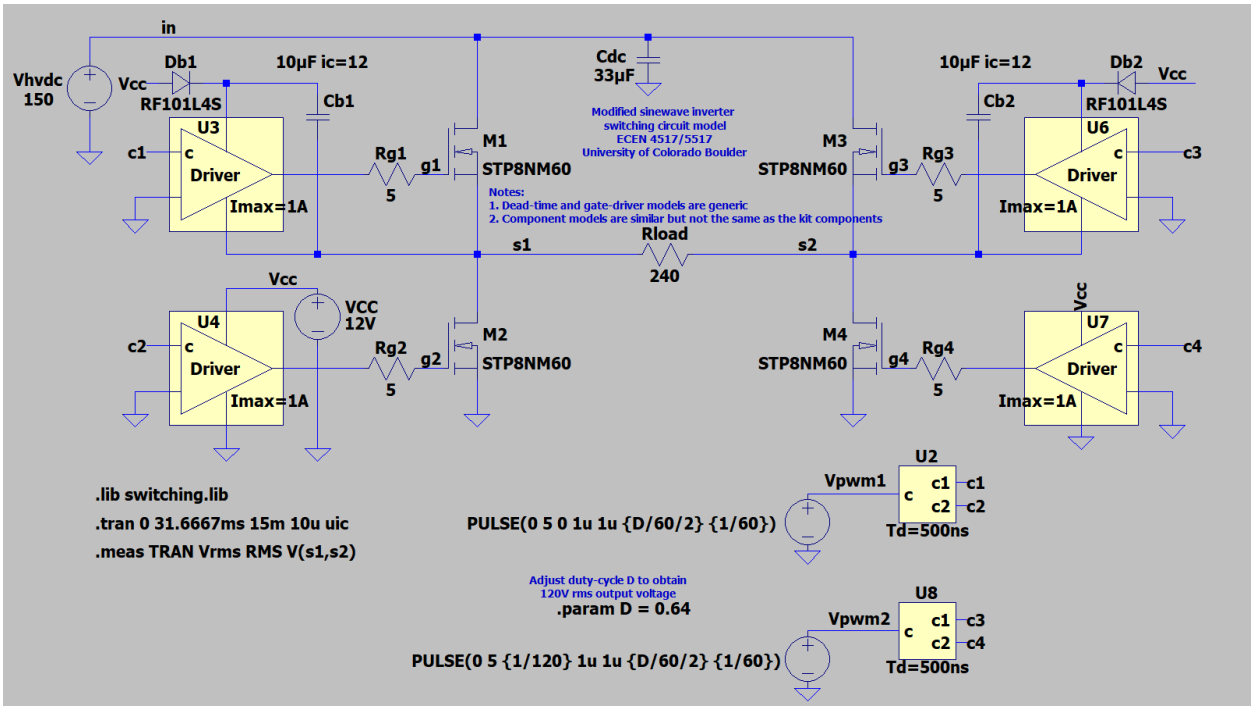
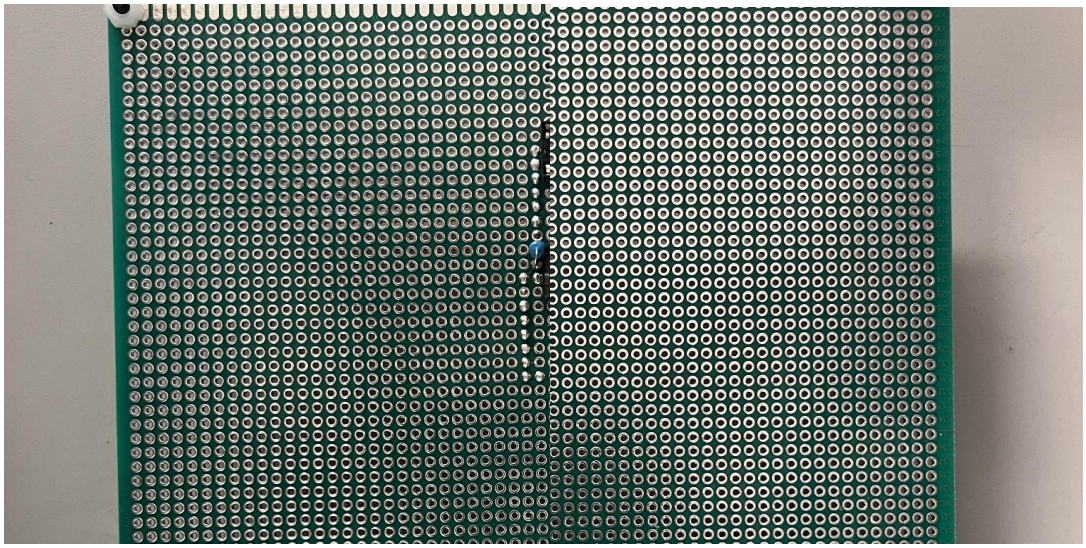
Step 1:



Modified Sine Wave Schematic

Step 2:



Inverter Top Side **Inverter Bottom Side**

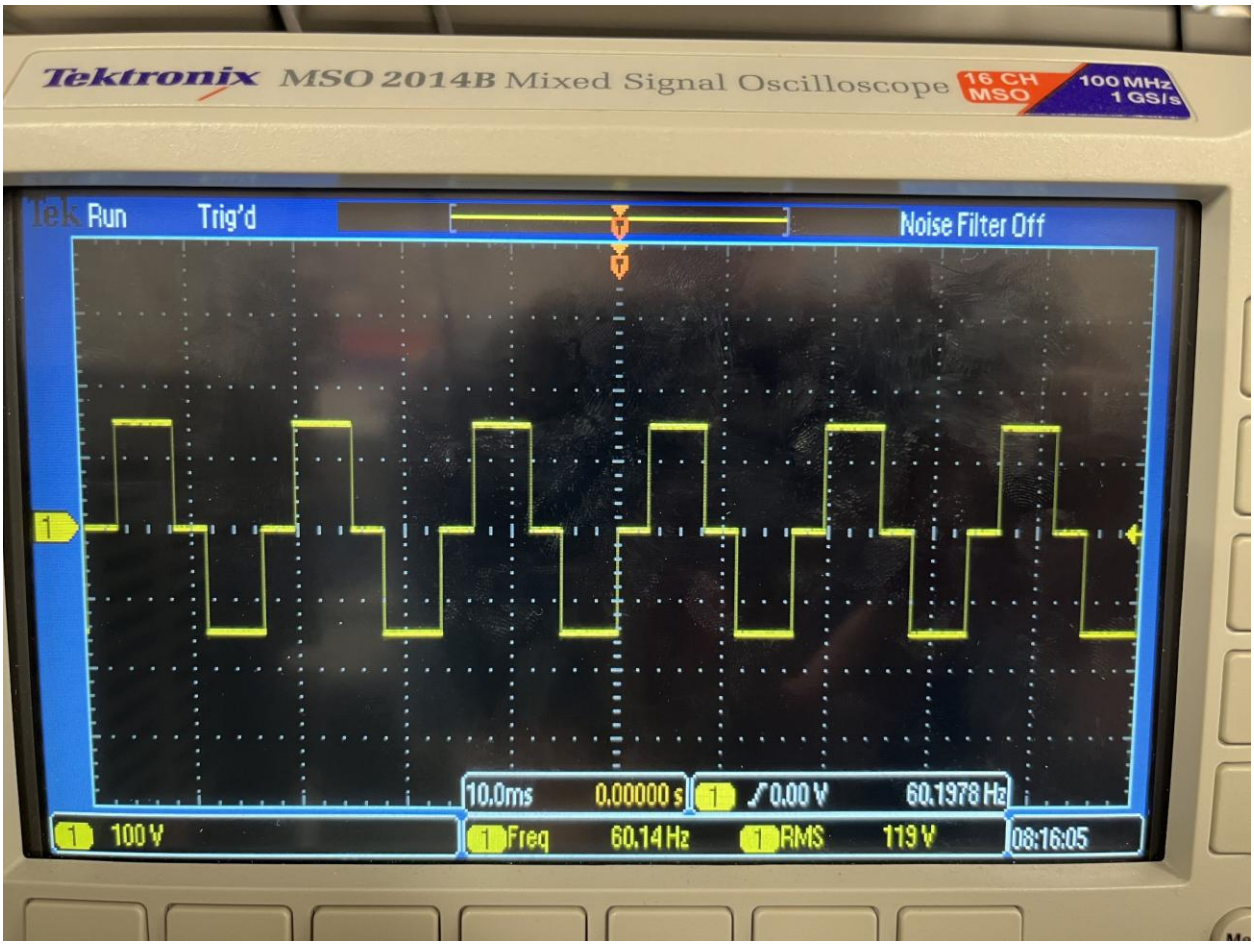
Step 3:

Modified sine-wave gate control signals:

Note that the shown frequency is 120 Hz, however, this was due to an incorrect variable value in our PWM-ADC3 code that we have fixed. The following steps will show our system operating at 60 Hz.

Step 4:

Measured Duty Cycle: 32%
Input VDC: 149.8V (It was very difficult to set the voltage source to 150VDC precisely)
Output V_{RMS}: 119V
Output I_{RMS}: 247 mA



Output Voltage Waveform $120V_{RMS}$, 60Hz