Board 2 Report
ECEN 3730 - PCB Design and Manufacturing

Completed by:
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Introduction

The purpose of this project is to show how different PCB layout choices can affect switching noise in a circuit. By comparing both good and bad design examples, we can see how layout decisions directly impact noise levels and signal integrity in measurable ways.

What does it mean to work?

To say that a board is “working” means that it performs according to the design expectations and specifications laid out in the project. For instance, the 555 timer IC should produce a signal with the desired frequency and duty cycle, such as 500 Hz and 60%, as specified by the POR. The Hex inverter (74AC14) should correctly invert the signal from the 555 timer, producing an output that is the digital opposite of the input. Additionally, components like LEDs should light up when connected to the proper outputs, confirming signal flow and functionality. The voltage regulator (LDO) must reliably convert 5V to 3.3V, ensuring stable power supply to the components. The overall functionality is validated through test points allowing us to check if the board behaves as expected during testing.

Board 2 Plan of Record (POR)

1. Convert 5 V into 3.3 V
2. Create a clock signal of about 500 Hz and about 50% duty cycle
3. Drive four of the inputs of a hex inverter used to demonstrate good layout and bad layout
4. Use the C6942 Hex inverter and operate at a 5 V or 3.3 V rail
5. Switch to selectively connect the 555 output to the various inputs of the good and bad layout
6. Red LEDs and 50Ω resistors as the load to three of the switching outputs of each hex inverter
7. Estimate the current you expect to draw from the inverter for the LED and 50Ω resistor load
8. Extract the Thevenin resistance of the output pin of one of the I/O
9. Connect the output of the fourth switching inverter to a test point to act as a trigger for the scope
10. Set up one output of each hex inverter as a quiet HIGH and one output as a quiet LOW
11. Demonstrate indicator LEDs, test points and circuit isolation switches as appropriate
12. Engineer one side of the board to have best design practices and other side with worst design practices
13. Part placement and routing should be identical for both sides (except for the decoupling capacitor)

14. Test points
    a. The scope trigger output
    b. Voltage across one of the 50Ω resistors
    c. Voltage across the output of one of the inverters driving the LED and resistor
    d. The quiet high
    e. The quiet low
    f. The 555 output signal
    g. The 3.3 V rail on the board
    h. The 5 V rail on the board
15. Use best scope measurement practices when you test your board

Schematics and Design

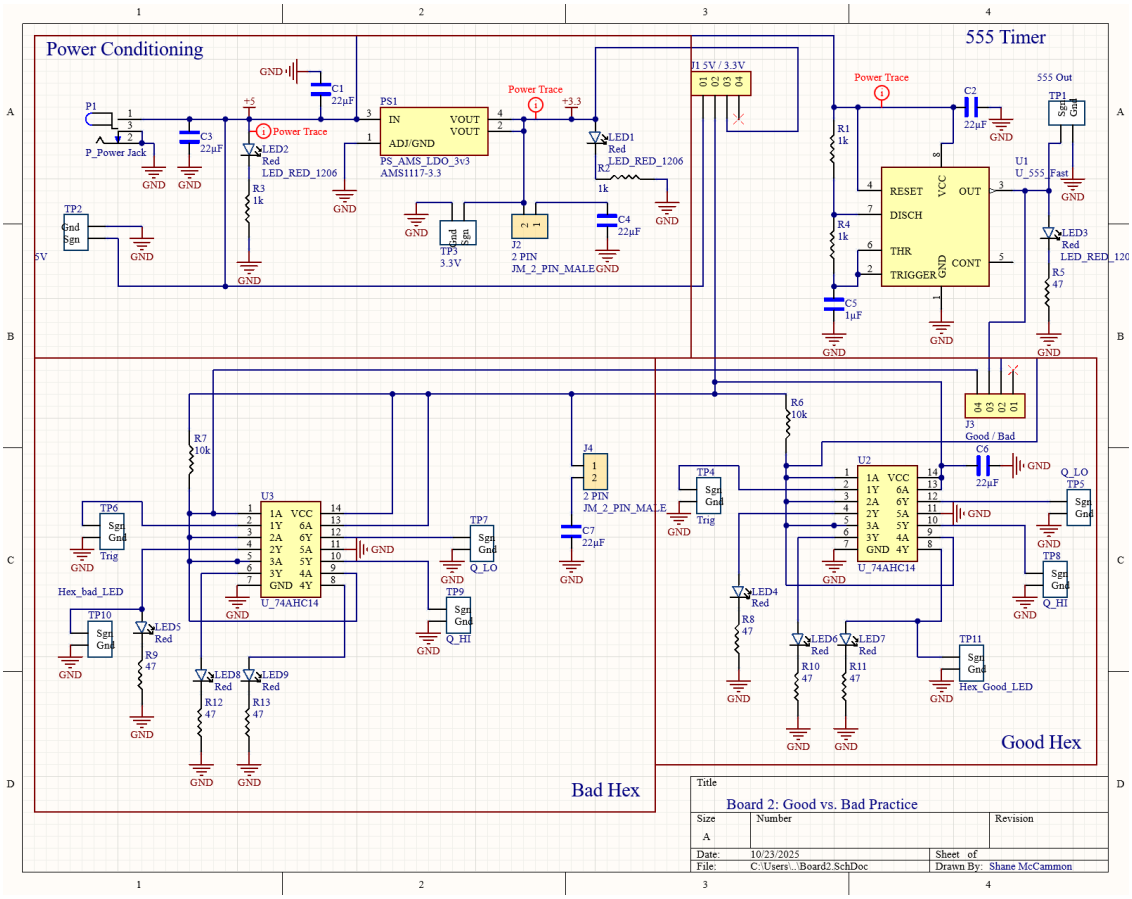

Figure 1: Altium schematic of Board 2

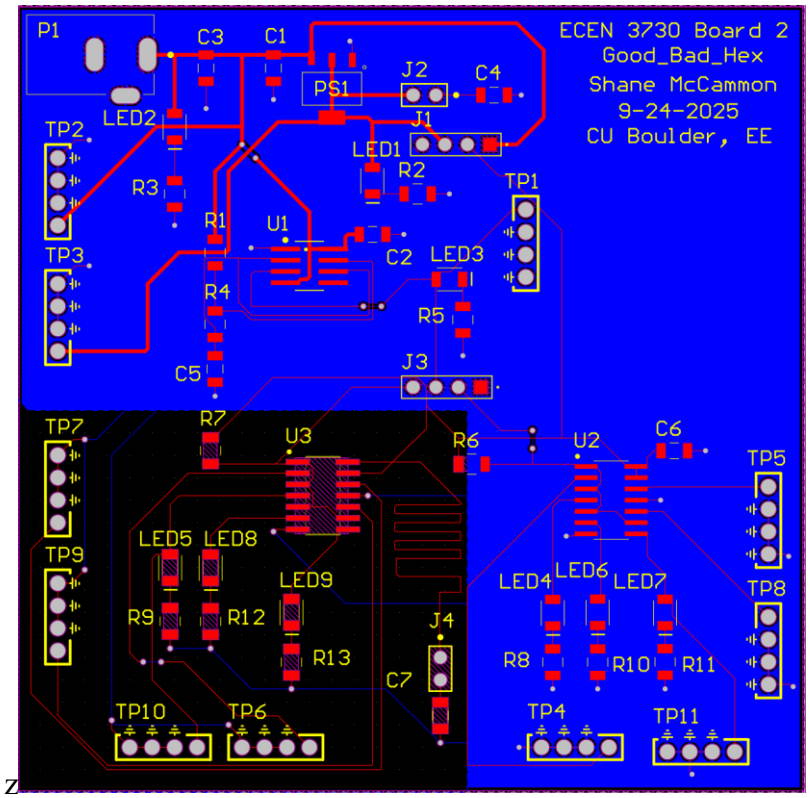

Figure 2: Altium board assembly

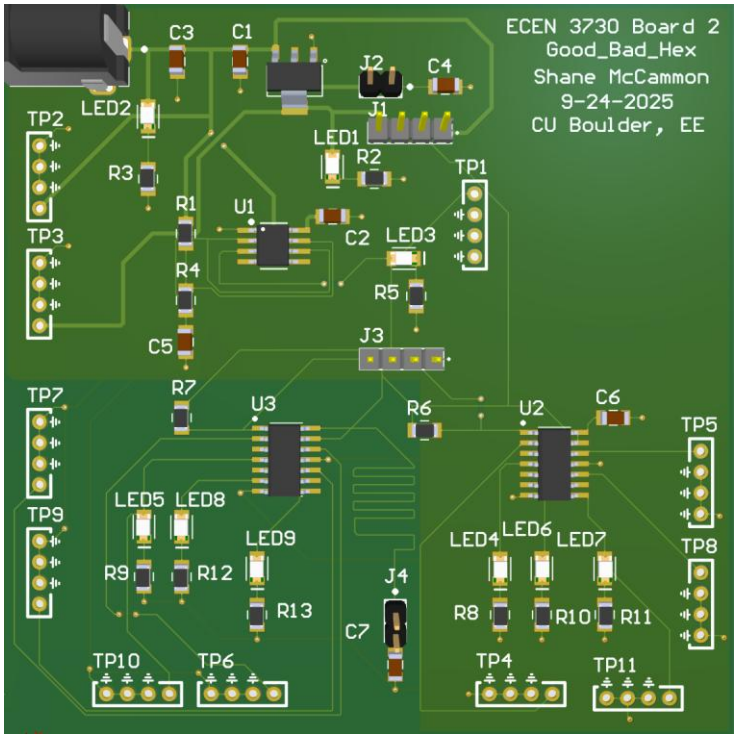

Figure 3: Printed and Assembled Board 1

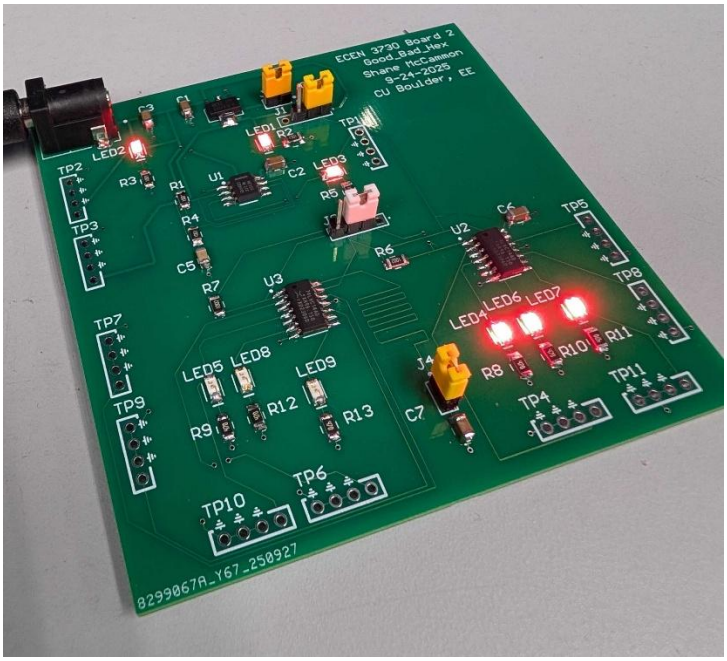

Figure 4: Functioning Board 2

Output Waveforms

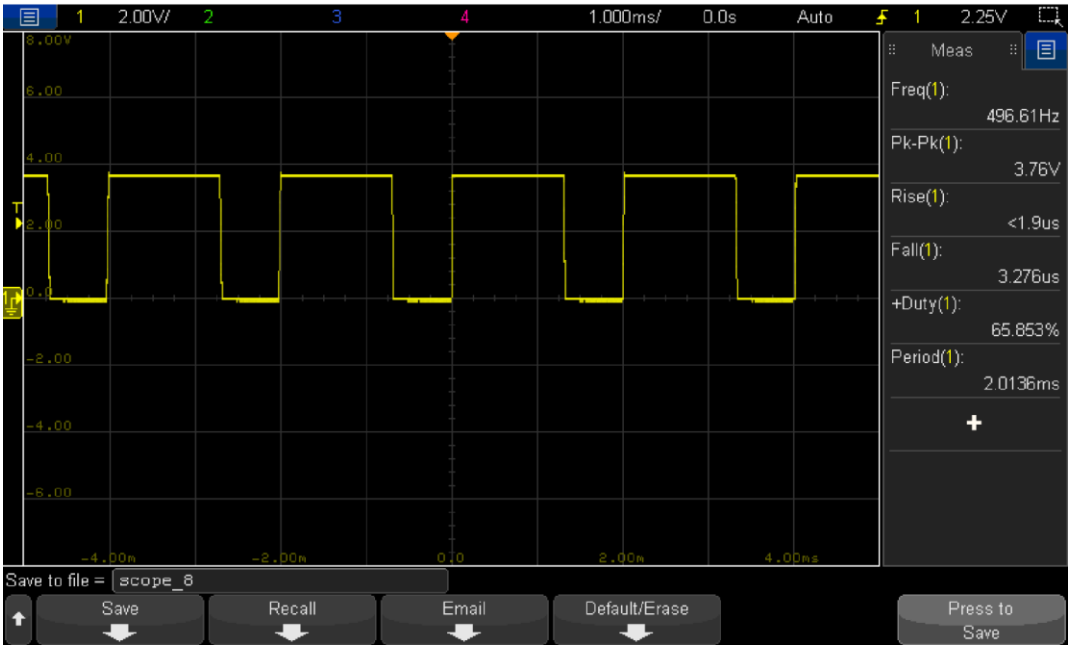

Figure 5: 555 Timer Output

Figure 6: Rise & Fall Time of 555 Timer

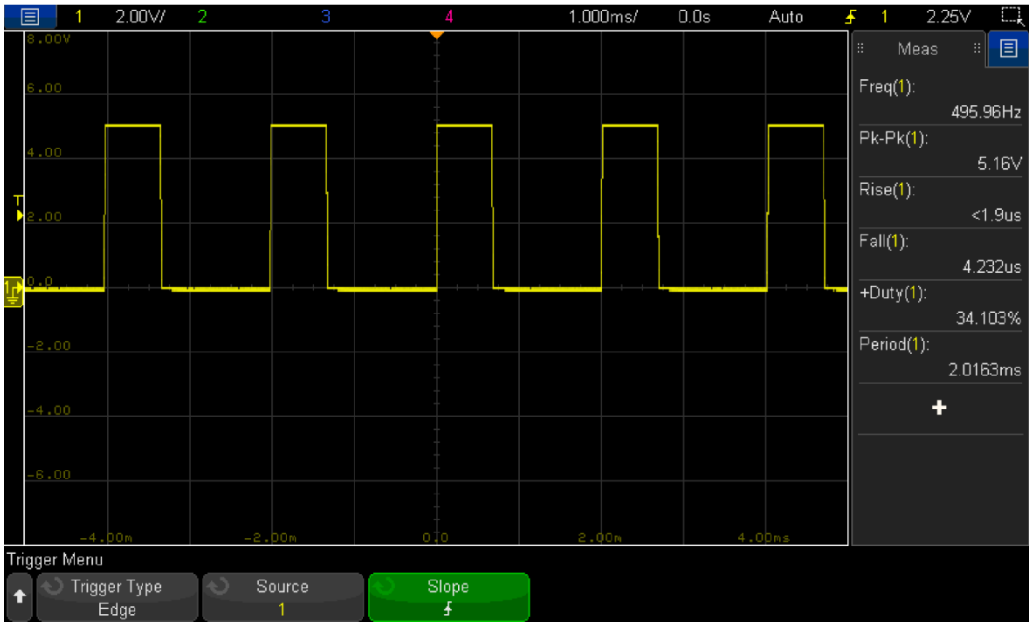

Figure 7: Hex Trigger Output [Good Hex]

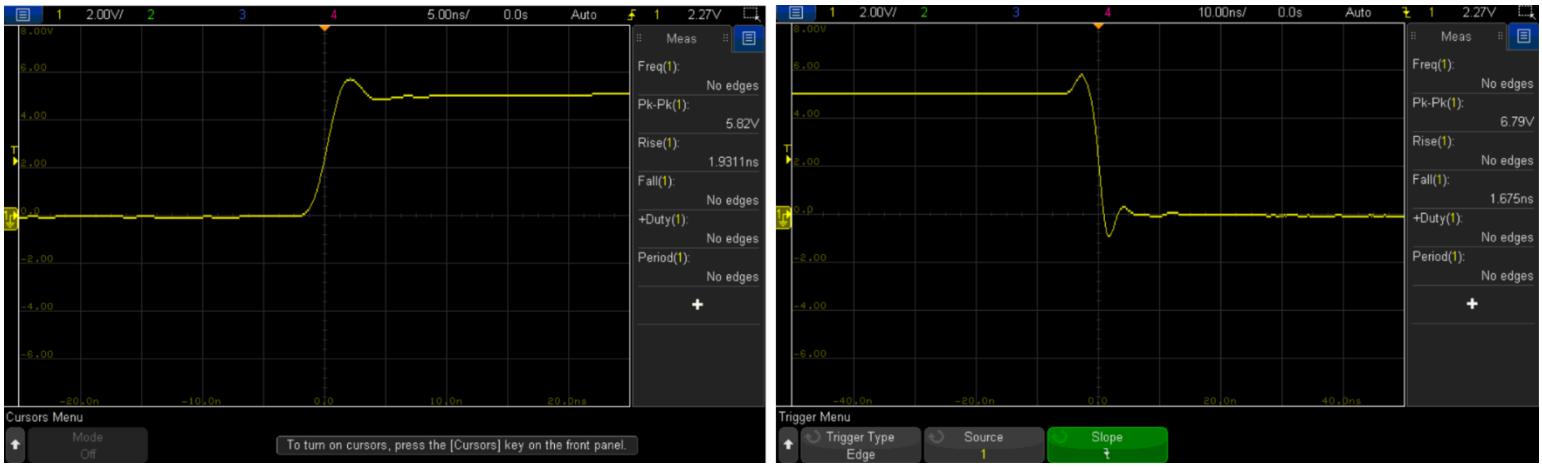

Figure 8: Rise & Fall Times [Good Hex]

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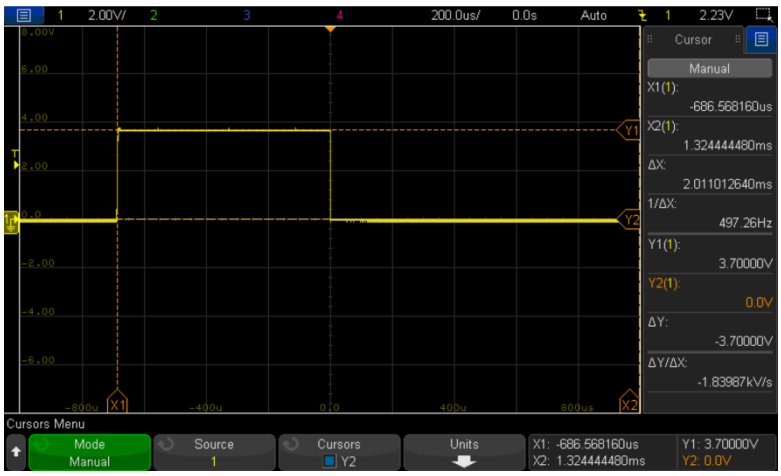

Figure 9: Voltage Drop of LED [Good Hex]

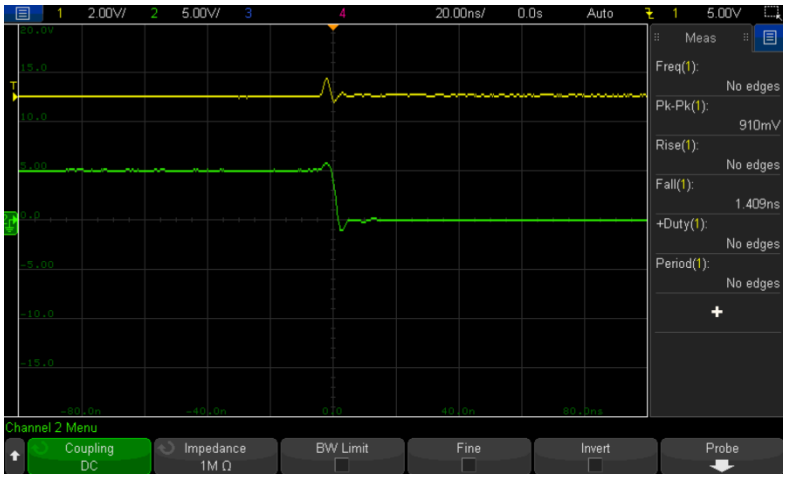

Figure 10: Noise Comparison: Quiet High [Yellow] vs. Trigger Output [Green]

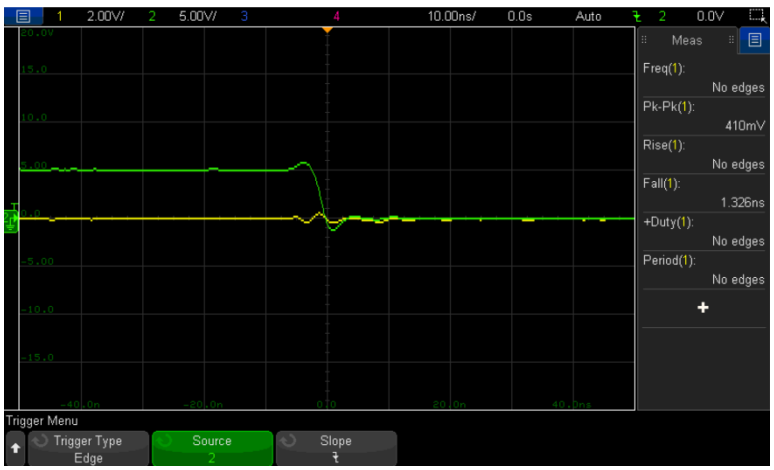

Figure 11: Noise Comparison: Quite Low [Yellow] vs. Trigger Output [Green]

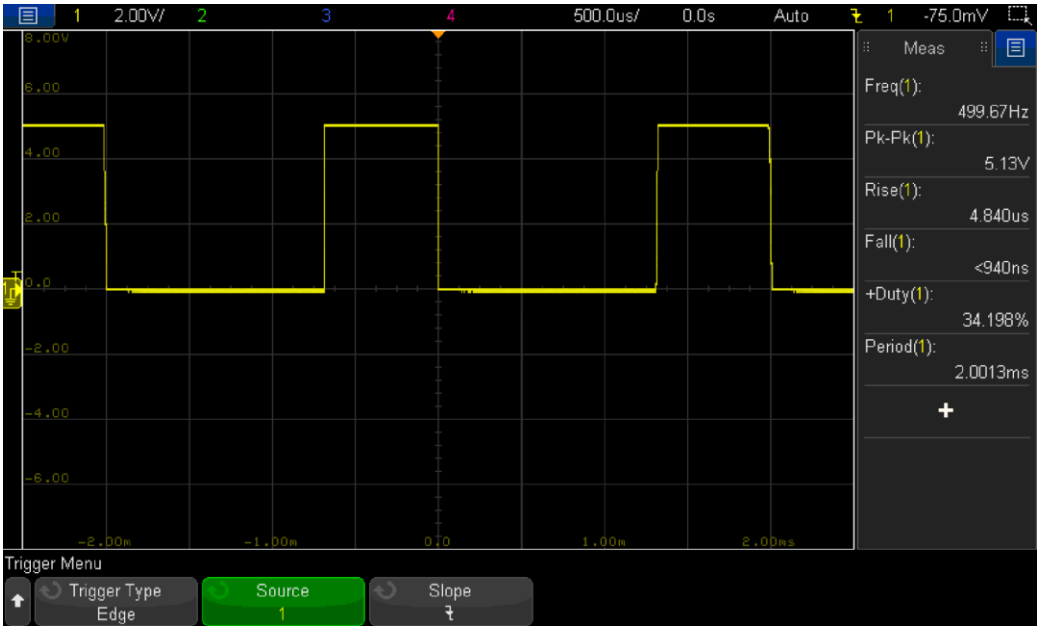

Figure 12: Hex Trigger Output [Bad Hex]

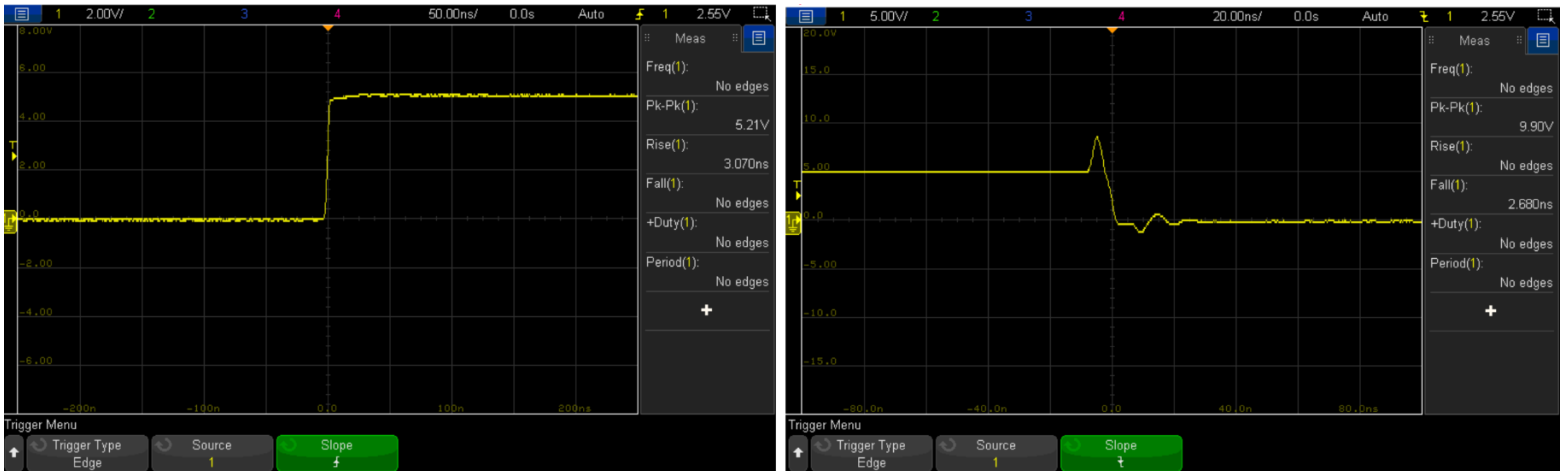

Figure 13: Rise & Fall Times [Bad Hex]

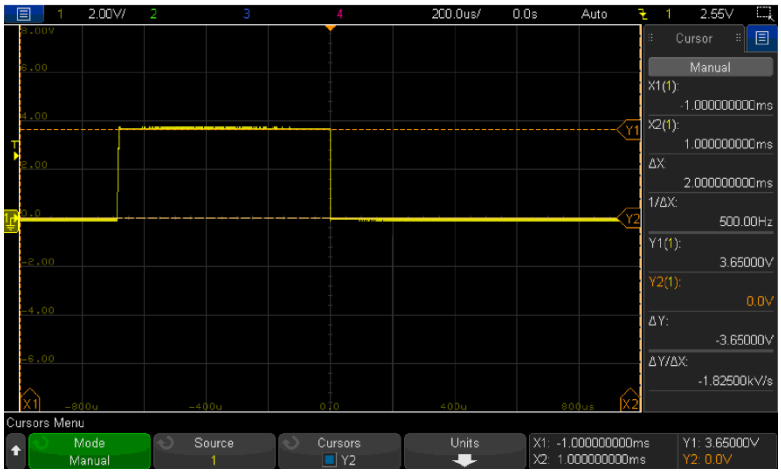

Figure 14: Voltage Drop of LED [Bad Hex]

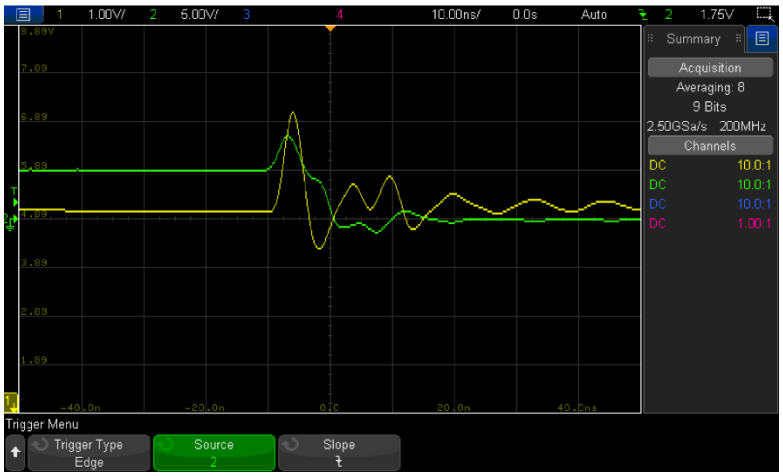

Figure 15: Noise Comparison: Quiet High [Yellow] vs. Trigger Output [Green]

Figure 16: Quiet High with [Yellow] and without [Orange] Decoupling Capacitor

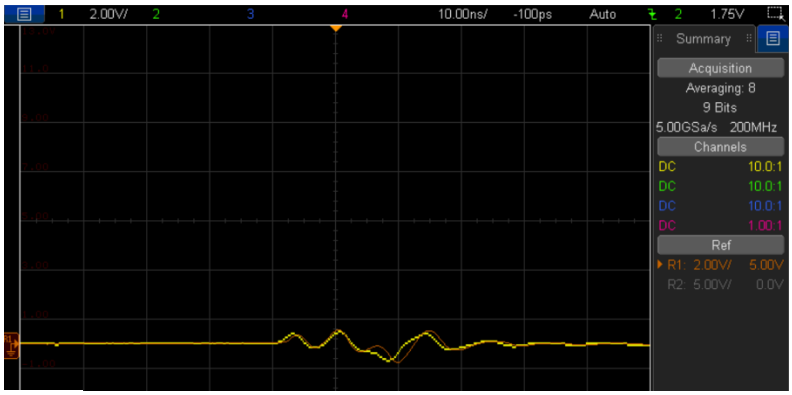

Figure 17: Quiet Low with [Yellow] and without [Orange] Decoupling Capacitor

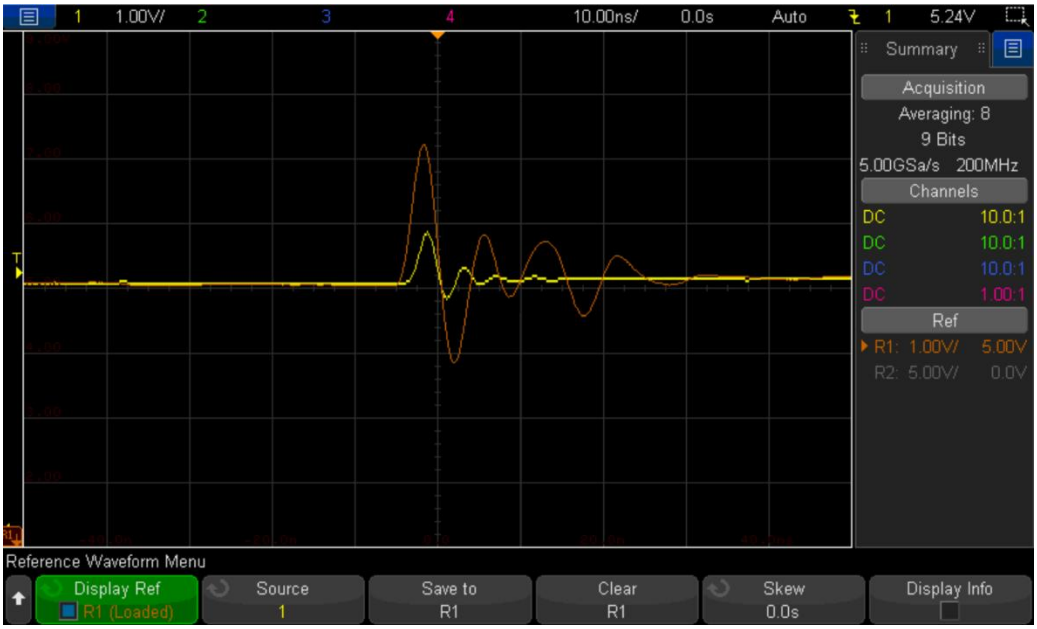

Figure 18: Good [Yellow] vs Bad [Orange] Outputs of Quiet High

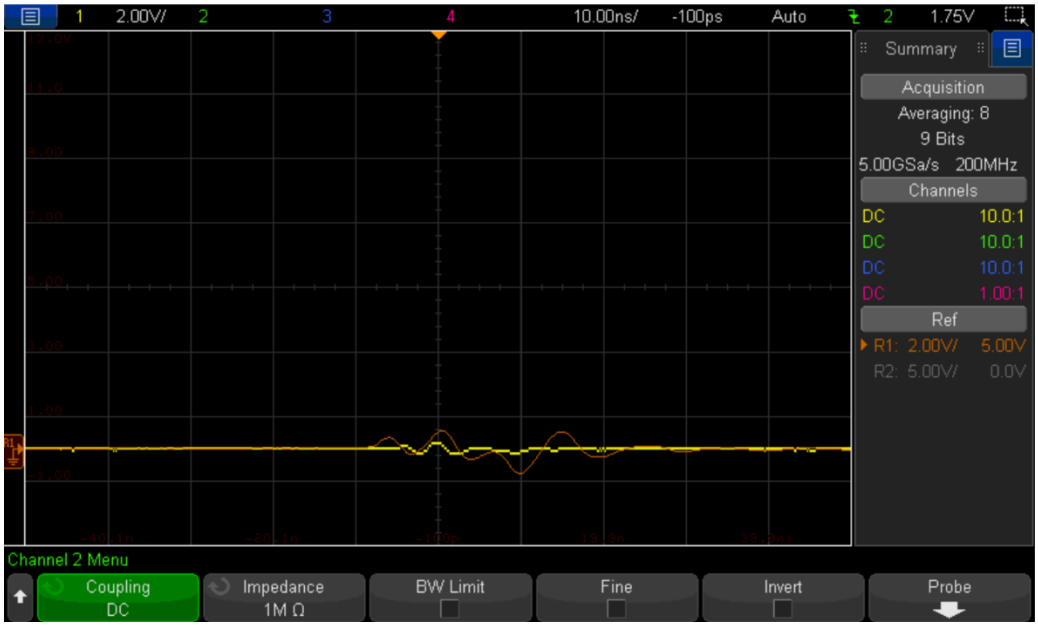

Figure 19: Good [Yellow] vs. Bad [Orange] Outputs of Quiet Low

Good Hex Data

Frequency	495.96 Hz
Pk – Pk Voltage	5.16V
Rise Time	1.9211 ns
Quiet High Pk-Pk	910mV
LED Voltage	3.7 V
Period	2.0163 ms
Duty Cycle	65.86%
Fall Time	1.675 ns
Quiet Low Pk-Pk	410 mV

Bad Hex Data

Frequency	499.7 Hz
Pk – Pk Voltage	5.13 V
Rise Time	3.07 ns
Quiet High Pk-Pk	3 V
LED Voltage	3.65 V
Period	2.0013 ms
Duty Cycle	34.198%
Fall Time	2.68 ns
Quiet Low Pk-Pk	750 mV

Note: Much more noise and slower rise and fall times

Analysis

Analyzing the two layouts reveals how proper PCB design practices can significantly reduce switching noise and improve signal integrity. In the good layout, the decoupling capacitor is placed close to the IC, minimizing inductance and stabilizing the voltage supply. This results in smoother and cleaner signal waveforms, with noticeably lower noise on the quiet high and quiet low outputs. The bad layout, on the other hand, shows the opposite effect. Poor capacitor placement and longer, winding traces increase inductance, leading to higher levels of switching noise. The signals become less stable, and the overall waveform quality decreases. Rise and Fall times of the signal are also slower. This comparison clearly illustrates the importance of thoughtful PCB layout. Shorter traces, proper grounding, and careful placement of key components, especially decoupling capacitors, help reduce interference and improve signal transitions. In the good layout, these factors contribute to faster, more consistent signal edges and significantly lower noise levels. Ultimately, even small layout adjustments can have a major impact on circuit reliability and performance.

Conclusion

The board performed as expected, with all outputs matching the intended behaviors during testing. The differences between the good and bad layouts clearly showed how layout quality affects switching noise and signal stability. One improvement I want to focus on is layout quality as I believe I can make things look more symmetrical and reduce board size. Through this project, I gained a deeper understanding of effective PCB design practices and how they influence signal integrity. Key takeaways include:

- Placing decoupling capacitors close to IC power pins minimizes inductance and reduces switching noise.
- The bad layout produced noticeably higher noise on quiet high and quiet low signals compared to the good layout as well as slower rise and fall times.
- Using 6 mil traces for standard connections and 20 mil traces for power lines helps manage current flow and heat more effectively.
- Stitching vias near cross-unders help reduce loop area and EMI

Lab 15 Board Measurements [Lab Makeup]

To supplement lab 15, I took measurements of the “good” portion of the given Good/Bad Hex board and compared it to the “good” circuit on my board 2.

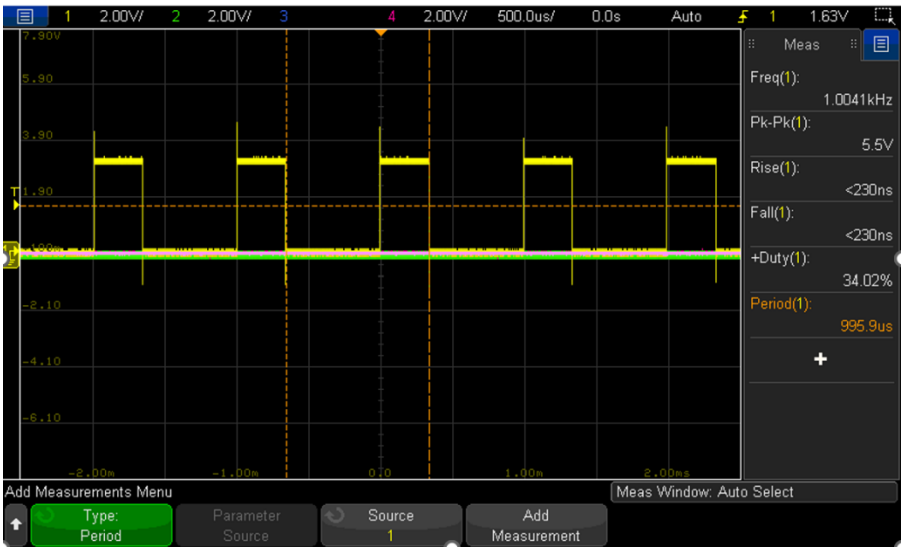

Figure 20: Lab 15 Good Hex Trigger Output

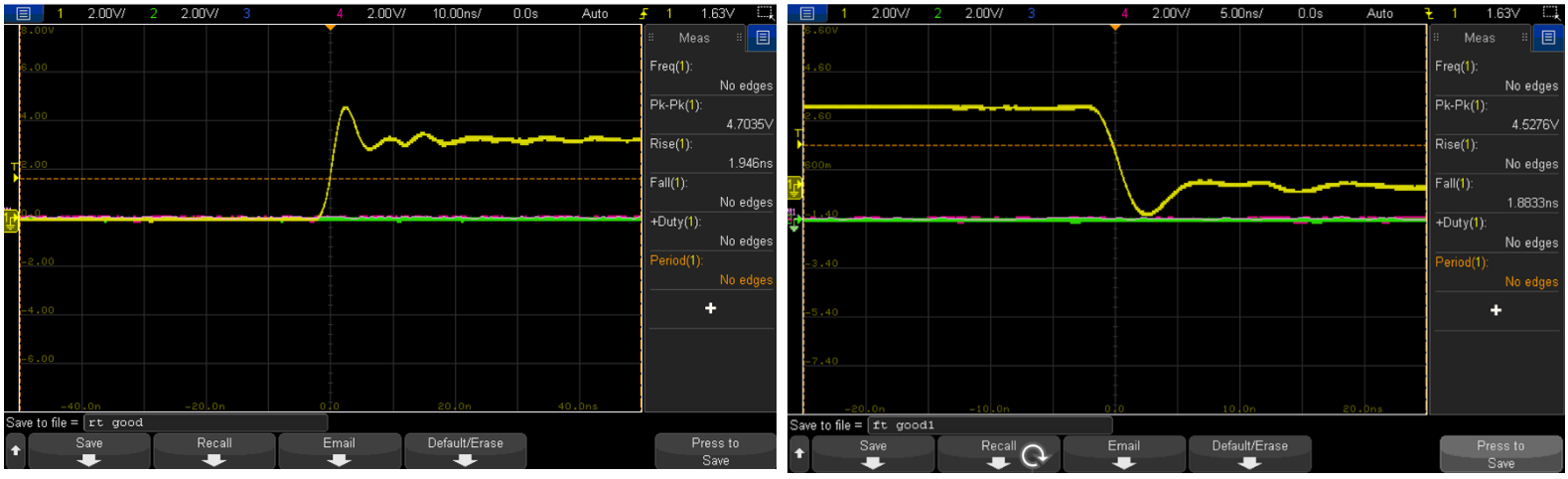

Figure 21: Rise & Fall times of Provided “Good Hex”

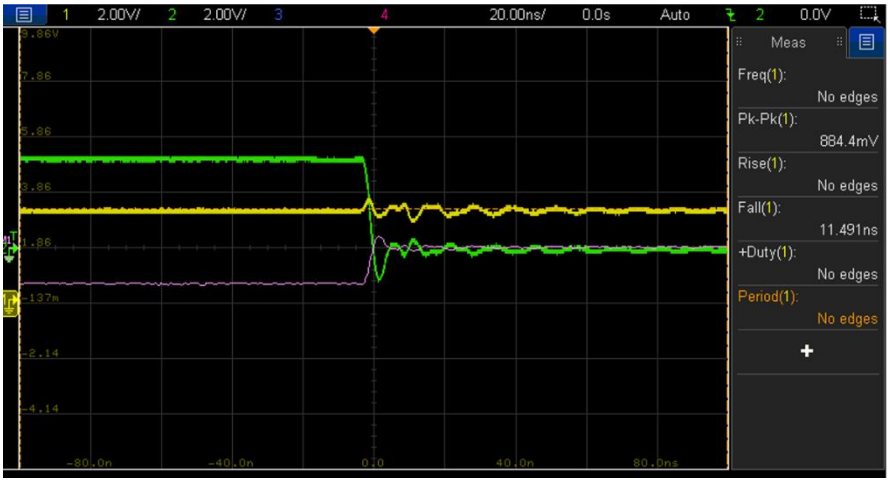

Figure 22: Quiet High Noise [Yellow] vs. Trigger Output [Green]

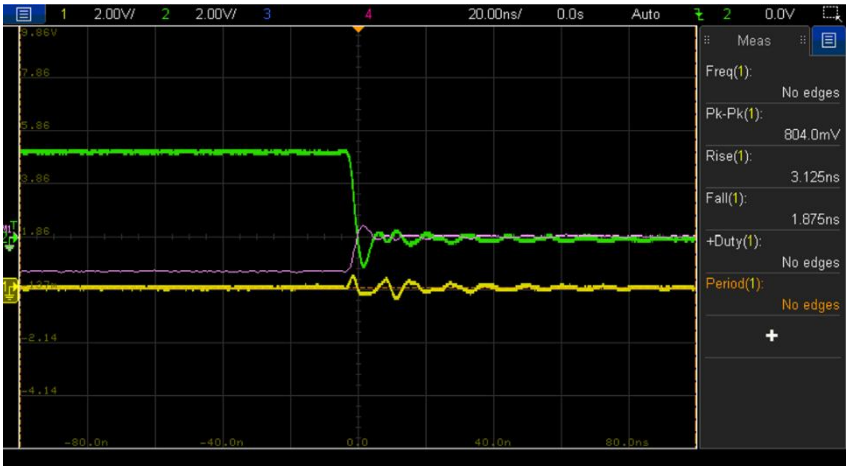

Figure 23: Quiet Low Noise [Yellow] vs. Tigger Output [Green]

Comparison Conclusion

My Board 2

Frequency	495.96 Hz
Pk – Pk Voltage	5.16V
Rise Time	1.9211 ns
Quiet High Pk-Pk	910mV
LED Voltage	3.7 V
Period	2.0163 ms
Duty Cycle	65.86%
Fall Time	1.675 ns
Quiet Low Pk-Pk	410 mV

Professor Board 2

Frequency	1kHz
Pk – Pk Voltage	5.5V
Rise Time	1.946 ns
Quiet High Pk-Pk	884mV
LED Voltage	3.7 V
Period	9.95 us
Duty Cycle	34%
Fall Time	1.883 ns
Quiet Low Pk-Pk	804 mV

Comparing the data from our two boards many specifications appear to be different. The overall Pk-Pk voltage of Professor's board was higher and he was able to reduce more noise on the quiet high line. However, I was able to halve the amount of noise found on the quiet low line with my board design. These differences appear mostly because of layout differences and placement of components. It is likely there is EMI, cross-talk, or something injecting a voltage into the professors ground plane. Ground location could also impact noise found on the quiet low line.