

| | ADDI | ADDS | B | B.LT | BL | BR | CBZ | LOVE | STUR | SUBS |
|-------------|------|------|---|------|----|----|--------|------|------|------|
| 3.LT | 0 | 0 | X | 1 | X | X | 0 | 0 | 0 | 0 |
| BL | 0 | 0 | X | X | 1 | 0 | 0 | 0 | G | 0 |
| BR | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | G | 0 |
| Set | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Mem2Reg | 0 | 0 | X | X | X | X | X | 1 | X | 0 |
| Reg2Loc | 0 | 0 | X | X | X | X | 1 | 0 | 1 | 0 |
| ALU op | ADD | ADD | X | X | X | X | pass B | ADD | ADD | SUB |
| ALU src | 1 | 0 | X | X | X | X | 0 | 1 | 1 | 0 |
| Vnc. Branch | 0 | 0 | 1 | 0 | 1 | X | 0 | 0 | 0 | 0 |
| MemWrite | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| RegWrite | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| ADDI | 1 | X | X | X | X | X | X | 0 | 0 | X |

CondBranch 0 0 X 0 X X 1 0 0 0

Control signals



= need low

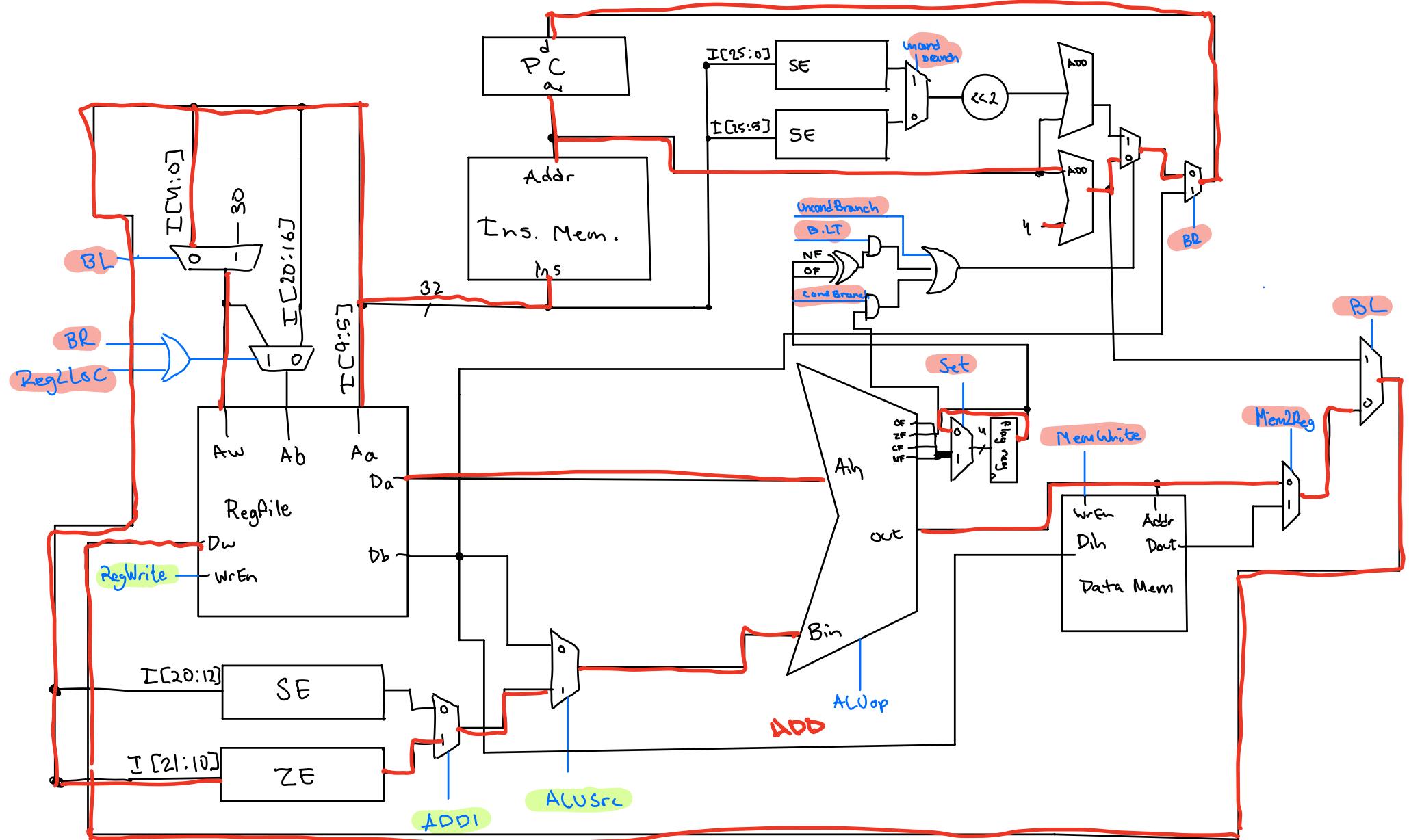


= dont care

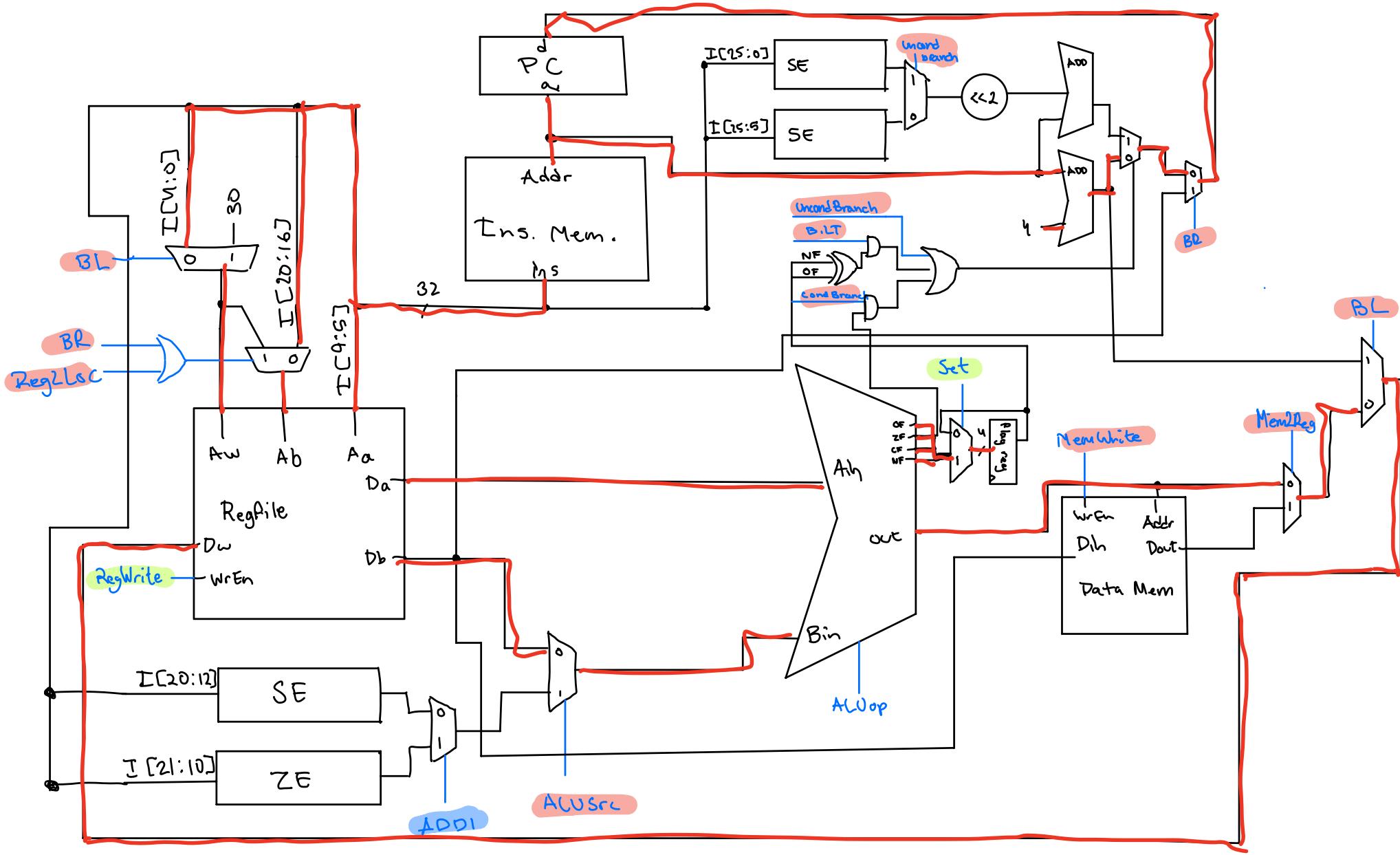


= need high

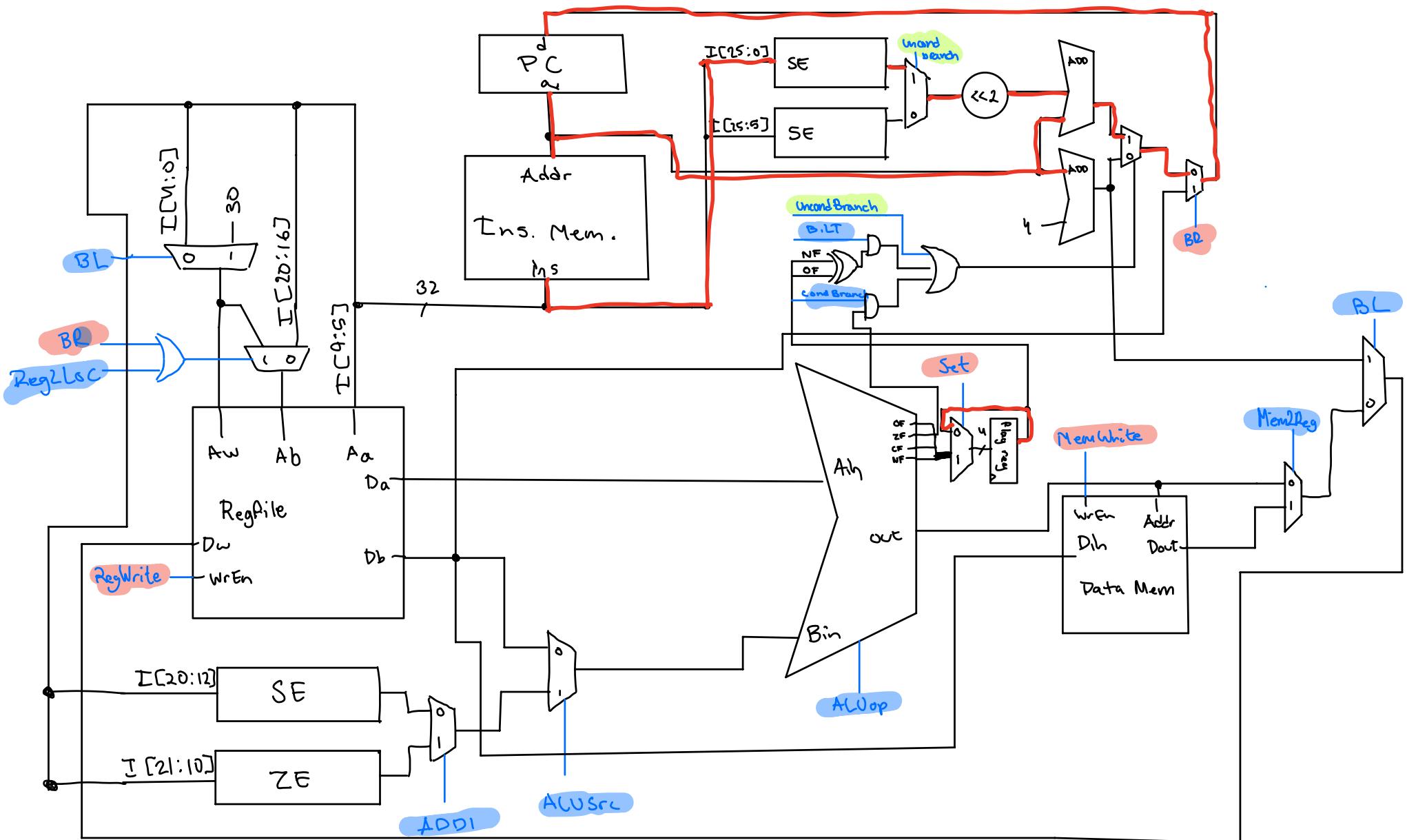
ADD Data path



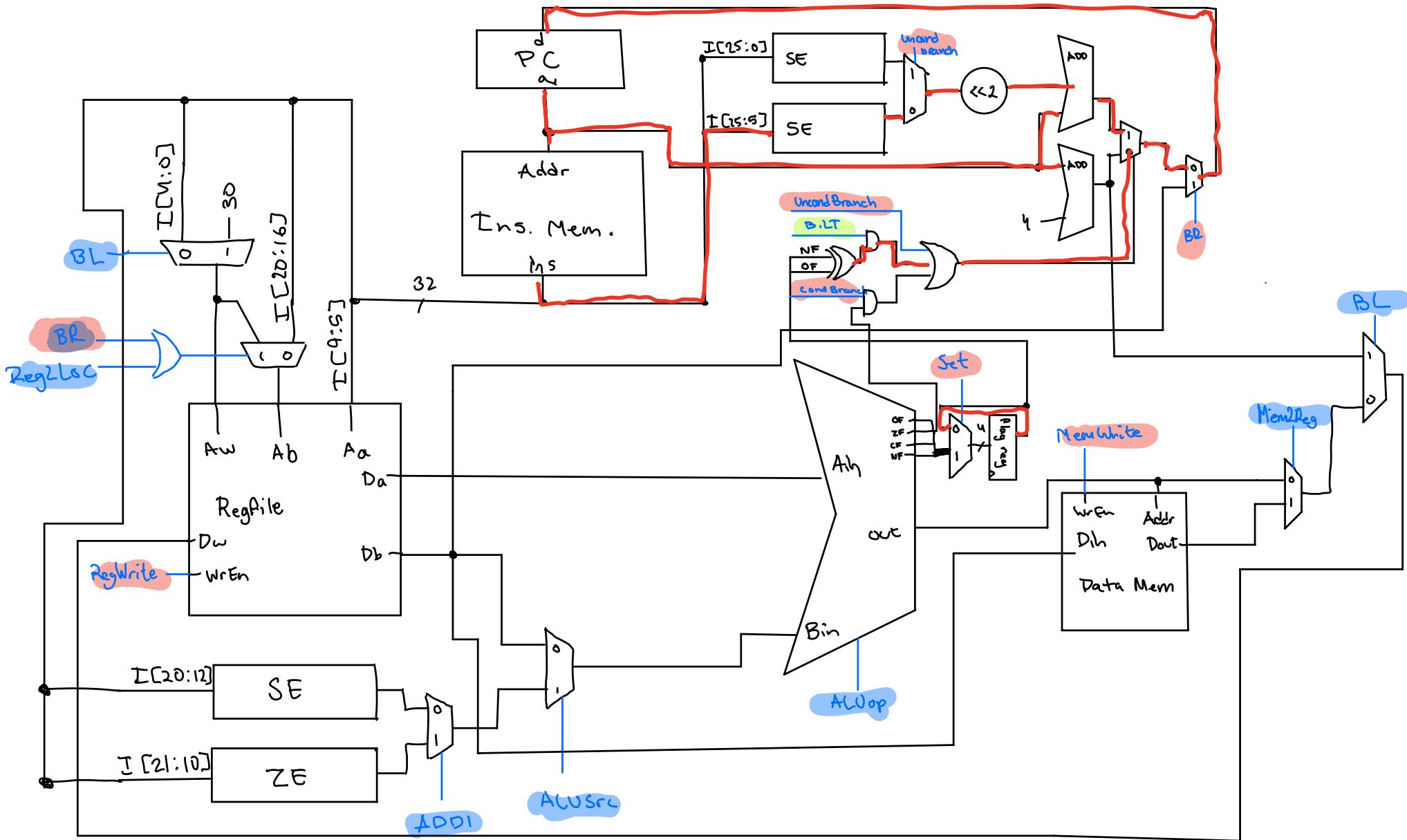
ADDS Datapath



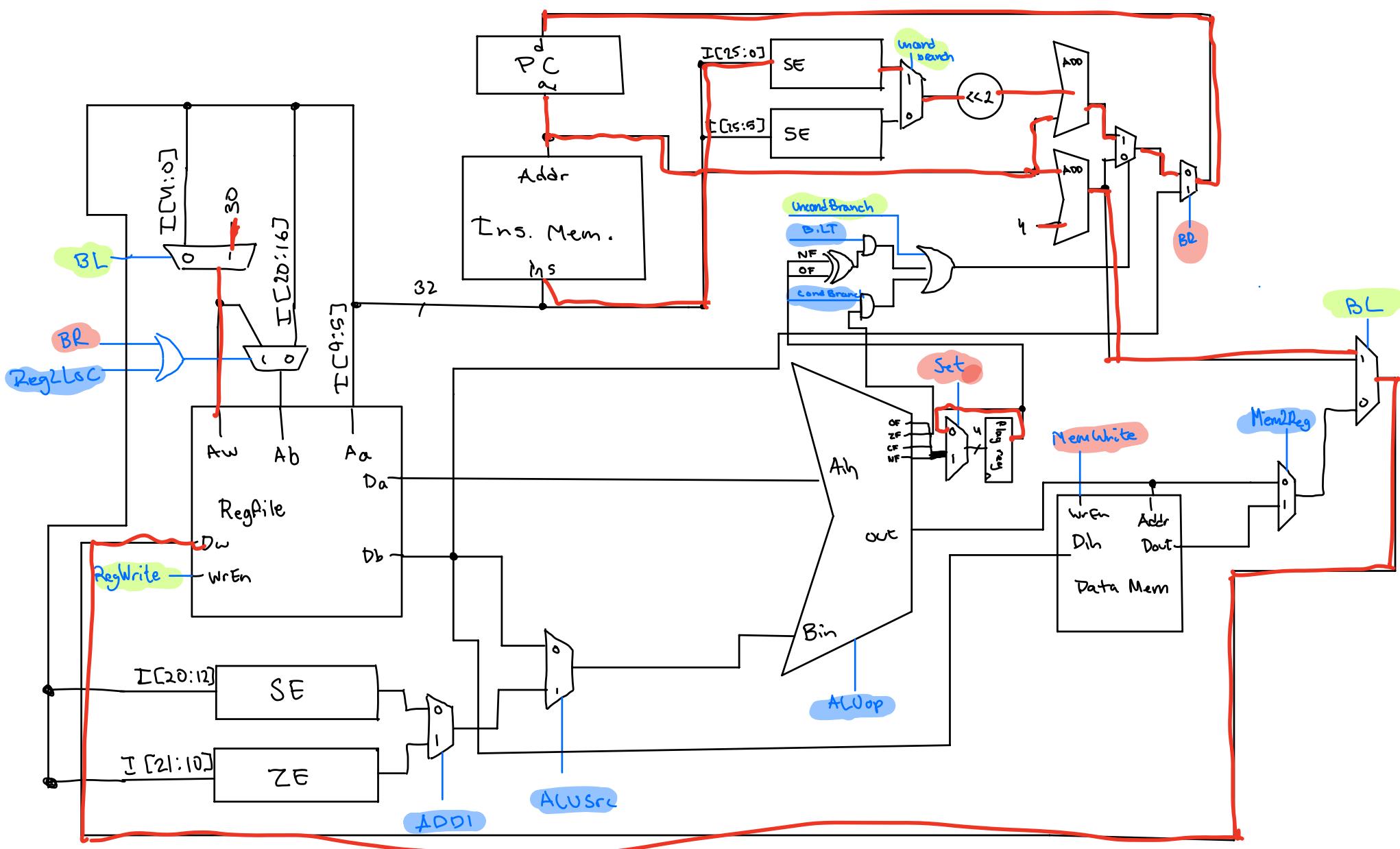
B Datapath



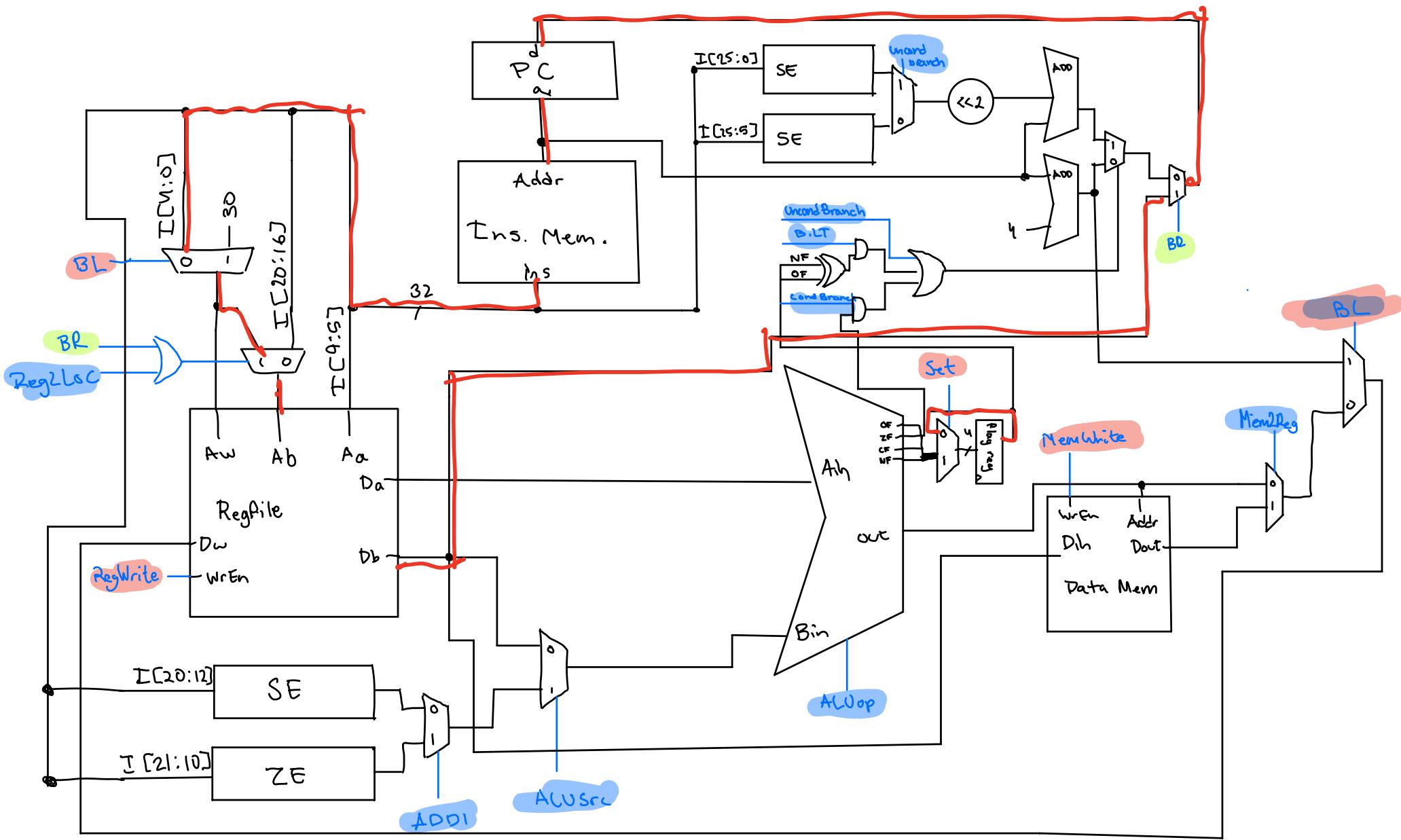
B.LT Datapath



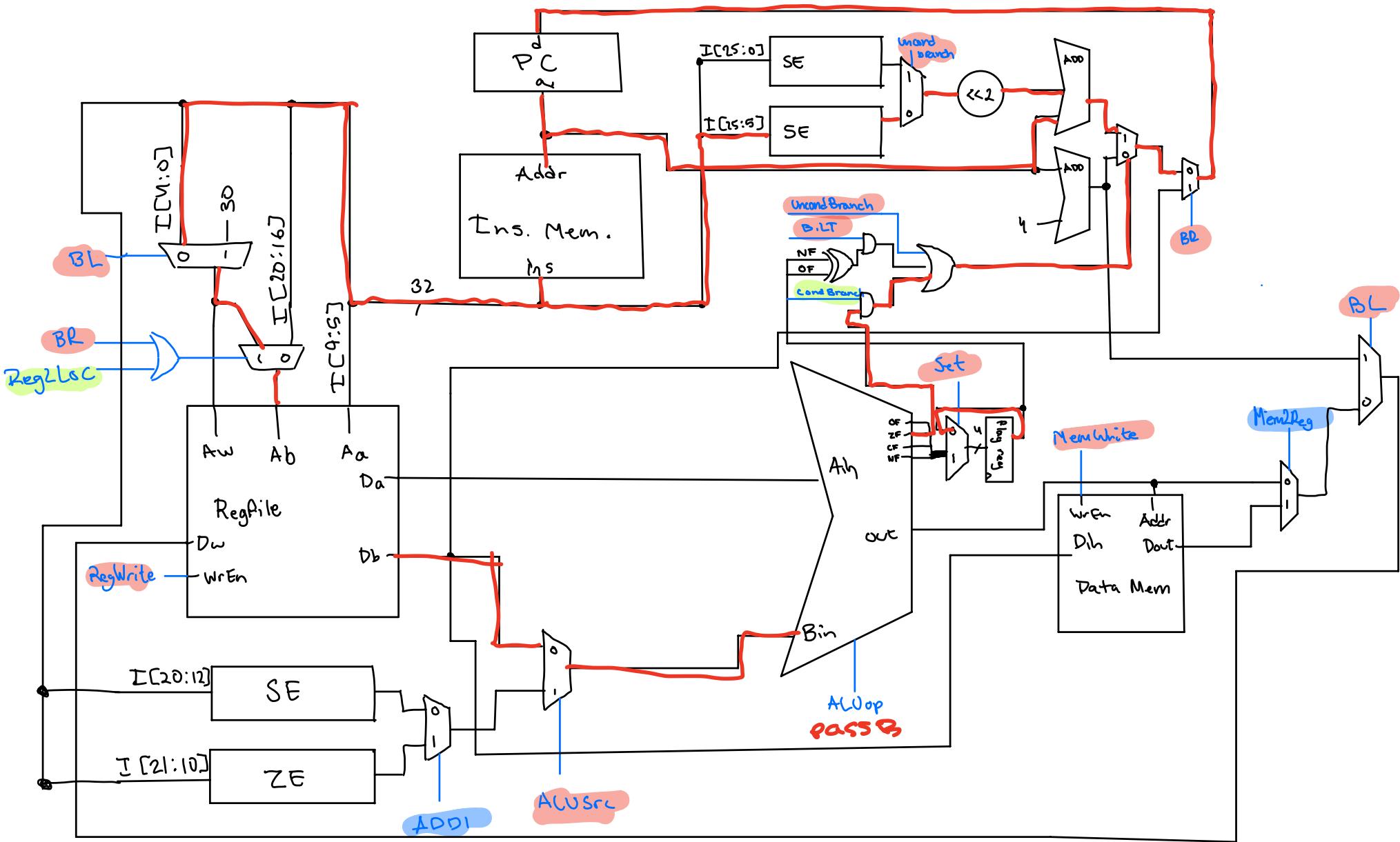
BL Octopath



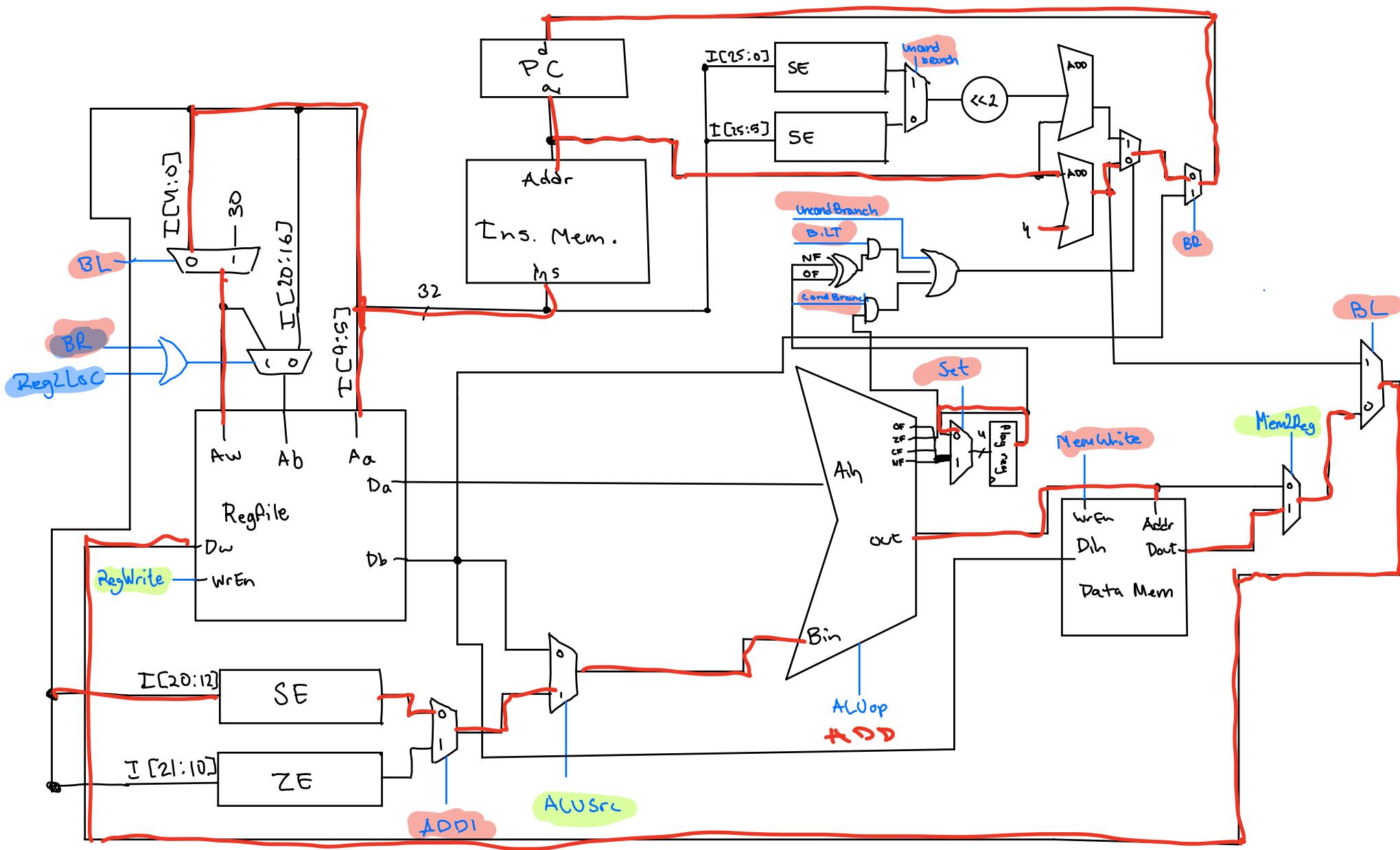
BR Datapath



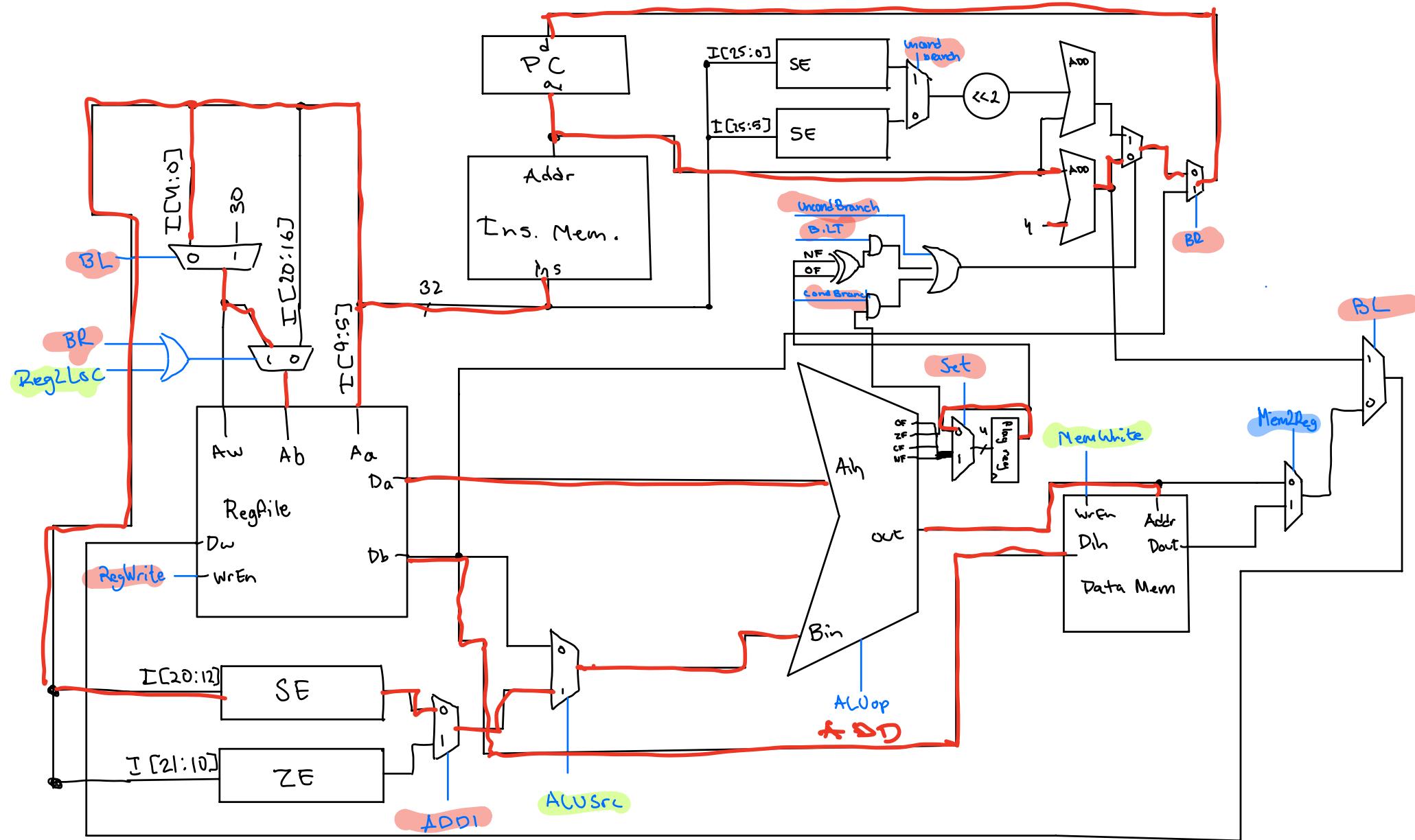
CBZ Datapath



LDUR datapath



STUR Datapath



SUBS Datapath

