MARVELL®

88DE2750 Digital Video Format Converter

Section 1: General Information

1.1 Overview

The 88DE2750 is a high performance, low cost **digital video format converter (VFC)** that takes standard definition and high definition uncompressed digital video and digital graphics inputs and processes them to produce an extremely high quality uncompressed **deep color** (12-bit) output in any desired standard digital video format up to **1080p60 or 4Kx2K@24**

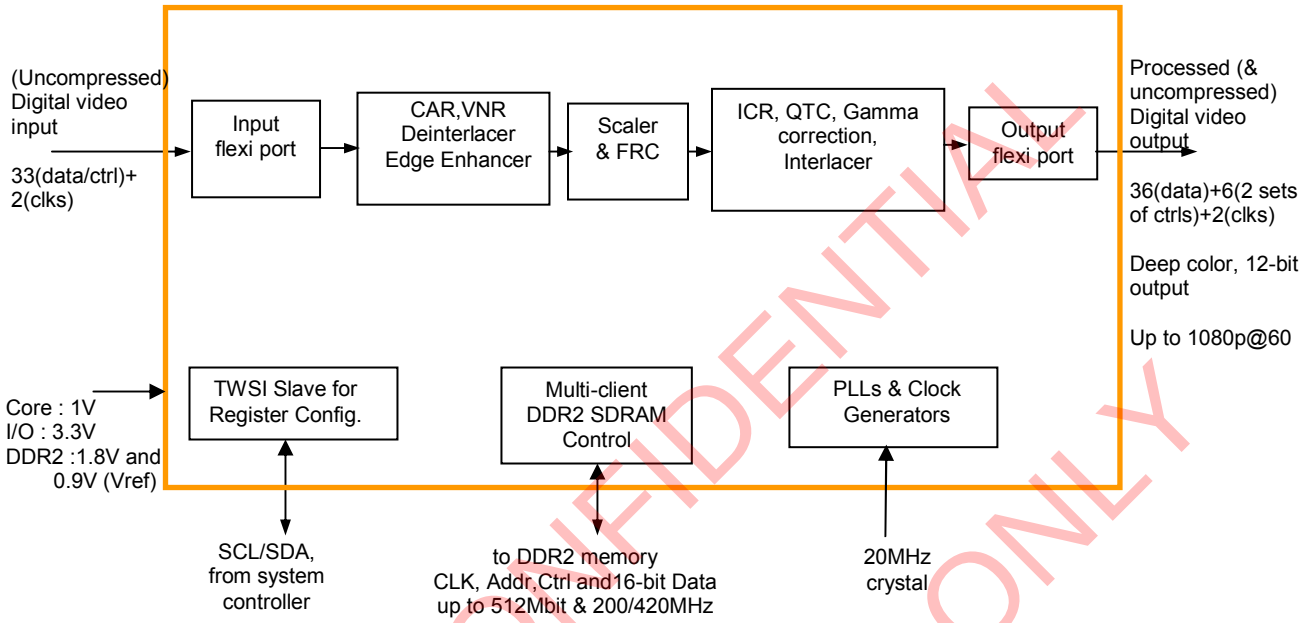
The 88DE2750 VFC builds on the award winning Qdeo™ video processing technology, implementing a high quality video pipeline with enhanced motion-adaptive 3D video noise reducer(VNR), compression artifact (mosquito and block noise) reducer (CAR), motion-adaptive 3D deinterlacing with edge adaptive Vector Interpolation (VI), advanced & high quality scaler, Intelligent Color Remapper (ICR), and Qdeo True Color ™ (QTC) along with Gamma correction enabling a high quality deep color capable 12-bit output.

88DE2750 is available in an 1mm pitch 256-ball BGA package and comes in two speed grades: speed grade-2 for 200MHz(400Mbps) DDR2 interface operation and speed grade-4 for 420MHz(840Mbps) DDR2 interface operation. 8DDE2750-4 is to be used for format conversion cases that require HD/1080i deinterlacing as well as frame rate conversion, like 1080i50 to 1080p60. For most of the other format conversion cases, 88DE2750 -2 will suffice.

88DE2750 takes 1V supply for core, 3.3V for I/O and 1.8V for DDR2 interface. The input and output digital ports are fully flexible enabling any input pin to connect to any input “bit”, and correspondingly for the output port. The registers are programmed through a simple Two-Wire-Serial-Interface (TWSI), compatible with industry standard I2C protocol. All the necessary clocks are generated through on-chip PLLs using the external 20MHz crystal.

Applications include AV devices such as Blu-ray Recorders, Blu-ray Players, DVD players and recorders, Set Top Boxes, Digital signage, Security surveillance, and DTV.

1.2 Simplified Block Diagram



Modules that use off-chip DDR2 memory for processing

1) Video Noise Reducer (VNR)
2) De-interlacer
3) Scaler and/or Frame Rate Conversion (FRC)
4) Edge enhancer

1.3 Features

1.3.1 Inputs

88DE2750 accepts **uncompressed** digital video input in a variety of formats through the generic **input digital port of 35 pins** (33 flexible pins for data and sync controls + 2 dedicated clock pins). The input port allows any data/sync control bit to be connected to any of the 33 pins.

88DE2750 is capable of accepting 2 video inputs (though only one of them would be selected, at a given time, by an internal multiplexer and processed) as long as the total pin requirement is within the maximum of 35.

Any video input timing can be handled including the standard CEA861 and SMPTE, through appropriate programming of the front end timing generator (FETG)

The supported input resolutions are

- SD : 480i59.94/60 or 576i50 (13.5MHz or pixel duplicated 27MHz)
- HD : up to **1080p60** (148.5MHz)
- Graphics : up to **1600x1200@60** (165MHz)

1.3.2 Outputs

88DE2750 outputs the processed (and **uncompressed)** digital video in a variety of formats through the generic **output digital port of 44 pins** (42 flexible pins for data and sync controls + 2 dedicated clock pins). The output port allows any data/sync control bit to be connected to any of the 42 pins.

Any video output timing can be generated including the standard CEA861 and SMPTE, through appropriate programming of the backend timing generator (BETG)

The output can either be interlaced or progressive. In case of interlaced output without scaling, the output lines can be the original input lines or processed & flicker-filtered lines.

The supported output resolutions are

- SD : 480i59.94/60 or 576i50 (13.5MHz or pixel duplicated 27MHz)
- HD : up to **1080p60** (148.5MHz)
- Graphics : up to **1600x1200@60 or 4Kx2K@24**

For output resolutions with rates less than 166Mpixels/sec, both single edge and dual edge clocking options are available. For pixel rates greater than 166Mpixels/sec, only double edge clocking is supported.

1.3.3 Video processing features

- **Auto-detection** of graphics and video formats (**Sync instrumentation**)
- **Auto-detection** of letterbox and pillar-box videos (**Data instrumentation**)
- High quality **dithering** from 12-bits down to 10-bits or 8-bits
- Advanced 3D spatio-temporal **video noise reduction (VNR)** for SD and HD video
  - Per-pixel Motion-adaptive, Flesh-tone adaptive, and Edge adaptive
  - Enhanced motion detection
  - Independent luma and chroma pipelines allowing both to be set optimally
  - Option to use luma motion instead of chroma motion for noise reduction to facilitate effective cross color reduction

- Advanced **Compression Artifact Reducer (CAR)** for SD and HD video
  - Automatically adapts to amount of block and mosquito noise
  - Enhanced block detection, for automatic block boundary detection for native as well as scaled input, reduces blockiness for native resolution content with no softness or side-effects for good content
  - Improved MNR reduces mosquito noise reduction without softening edges

- Vertical filtering to **eliminate Chroma Upsampling Error** (CUE) and **Interlaced Chroma Problem** (ICP)
  - Two levels of vertical filtering, one operating in the interlaced domain and the other in the progressive domain, providing maximum flexibility and effectiveness for eliminating CUE and ICP for both progressive and interlaced content.

- Advanced 3D **deinterlacing** for SD(480i/576i) and HD(1080i) video
  - Automatic content detection – Film versus Video
  - Two-region cadence detection (for 3:2 and 2:2 cadences) allows optimal handling of film with video overlay, such as the most common case of scrolling video text ticker over the bottom of film content
  - Video deinterlacing

    Per-pixel motion-adaptive spatio(2D)-temporal(3D) interpolation

    Spatial de-interlacing through an augmented edge-adaptive Vector Interpolation (VI) technique enabling very smooth edges for ultra-shallow angles

    Choice of luma motion or chroma motion detection, or combination of both, for chroma deinterlacing
  - Film deinterlacing

    Film cadence detection supports 3:2, 2:2, 2:2:2:4, 2:3:3:3, 3:2:3:2:2, 5:5, 6:4 and 8:7, as well as two additional user programmable cadences. Deinterlacing done through appropriate weaving of fields and repeating them (inverse pulldown)

    Manual film-mode option to use external repeat field flag from MPEG decoder to do weaving,

- High quality **Scaler** with
  - 12 taps horizontal, 5 or 8 taps vertical based on horizontal resoution
  - Non-linear 3-zone scaling to retain 4:3 content's aspect ratio on a 16:9 display without cropping or using pillar box
- Intelligent (tearless) **frame-rate-conversion** for both SD and HD content
  - Arbitrary output frame rates, including 24p, 48p, 50i, 50p, 60i, 60p, 75i, 72p, 75p, 100i, 100p, 120i and 120p (subject to pixel clock rate and DDR bandwidth limitations)
  - Smooth movie mode option converts 3:2 cadence @ 60 Hz, to 24Hz *N (N=1,2,3)
  - Progressive detection of 3:2 cadence @ 60Hz to 24Hz * N (N = 1,2,3)
  - 8DDE2750-4 is to be used for format conversion cases that require HD/1080i deinterlacing as well as frame rate conversion, like 1080i50 to 1080p60. For most of the other format conversion cases, 88DE2750 -2 will suffice.

- Advanced **edge detection and enhancements (EE)**
  - Scale-invariant horizontal and vertical detail enhancement brings out details even in highly up-scaled images
  - Horizontal Luma Transient Improvement (LTI) sharpens large-amplitude vertical edges
  - Horizontal Chroma Transient Improvement (CTI) sharpens large-amplitude vertical chroma boundaries

- Enhanced **Film-grain generation** for film-look

- Intelligent Color Remapper (ICR) at 10-bit resolution to improve the visual quality by enhancing user defined colors and fleshtone

- High-quality **Qdeo True Color ™ (QTC)** gives true 10-bits (1024 grey levels), while removing contouring (very visible when displaying 8-bit input data on 10-bit/12-bit panels)

- Independent three channel gamma **Look Up Tables (LUTs)** (RGB or YCbCr) with 10-bit input and 12-bit output

1.3.4 Other Video processing functions/features

- Fully programmable (3 x 3) and (3 x 1) matrices for linear **Color Space Conversion (CSC)** as well as full **picture controls** - brightness, contrast, hue and saturation
- Output (timings) can be locked to input (timings) or run asynchronously
- An external reference signal can be driven on EXT_IN for the on chip PLLs as a locking source.
- Programmable luma and chroma delay adjustments to ensure luma and chroma are aligned.
- Low power **standby mode**

1.3.5 Programming interface

- Two wire serial interface (TWSI) for register programming running up to 400KHz and compatible with the industry standard I2C protocol

1.3.6 Memory interface

- Supports 16-bit DDR2 memory interface
- 88DE2750-2 supports a max 200MHz (400Mbps) memory interface, whereas 88DE2750-4 supports a max 420MHz (840Mbps)
- Maximum addressable space is 512Mbits

1.3.7 Package

- 88DE2750 is available in a 1mm pitch, 17mm x 17mm 256-ball BGA

Section 2: Functional Block Descriptions

2.1 Digital Input Video Interface

88DE2750 can accept uncompressed digital video input in a variety of formats through the flexible **input digital port of 35 pins** (33 flexible pins for data and sync controls + 2 dedicated clock pins). A bank of 33 multiplexers, each of 33:1 allow any data/sync control to be connected to any of the 33pins.

88DE2750 is capable of accepting 2 video inputs (though only one of them would be selected by an internal multiplexer and processed). The two video inputs can be any of the following formats as long as the total pin(Clk + Ctrl + Data) requirement is within or equal to 35.

Any video input timing can be handled including the standard CEA861 and SMPTE, through appropriate programming of the front end timing generator (FETG)

The supported output resolutions are

- SD : 480i59.94/60 or 576i50 (13.5MHz or pixel duplicated 27MHz)
- HD : up to **1080p60** (148.5MHz)
- Graphics : up to **1600x1200@60 (165MHz)**

  - 8-bit : 4:2:2 YCbCr 8-bit
    - SD only
    - 2x clock
    - Embedded(BT656) or Discrete(BT601) syncs
  - 10-bit : 4:2:2 YCbCr 10-bit
    - SD only
    - 2x clock
    - Embedded(BT656) or Discrete(BT601) syncs
  - 16-bit : 4:2:2 YCbCr 8-bit
    - SD or HD
    - 1x or 2x clock(pixel duplicated) for SD, 1x clock for HD
    - Embedded (BT1120) or Discrete syncs (CEA861/SMPTE)
  - 20-bit : 4:2:2 YCbCr 10-bit
    - SD or HD
    - 1x or 2x clock(pixel duplicated) for SD, 1x clock for HD
    - Embedded (BT1120) or Discrete syncs (CEA861/SMPTE)
  - 24-bit : 4:2:2 YCbCr 12-bit
    - SD or HD
    - 1x or 2x clock(pixel duplicated) for SD, 1x clock for HD
    - Embedded (BT1120) or Discrete syncs (CEA861/SMPTE)
  - 24-bit : 4:4:4 8-bit

- SD or HD, RGB or YCbCr
- 1x or 2x clock(pixel duplicated) for SD, 1x clock for HD
- Only Discrete syncs (CEA861/SMPTE)

o 30-bit : 4:4:4 10-bit

- SD or HD, RGB or YCbCr
- 1x or 2x clock(pixel duplicated) for SD, 1x clock for HD
- Only Discrete syncs (CEA861/SMPTE)

In case of discrete syncs, the associated controls are - **Hsync/DE, Vsync** and (optional) **FieldID**. The HS pin can also be configured to accept (composite) DE.

Note: ITU-R-BT656 decoder can also decode BTA-T1004 54MHz digital input.

2.1.1 Dither

The dither block reduces the pixel precision from 12-bits down to 10-bits or 8-bits.

2.1.2 Delay Balance

This module adjusts any delay imbalance in the incoming YCbCr or RGB data.

The input video window of interest to be processed by 88DE2750 is identified by two signals called Hde(Horizontal Data Enable) and Vde (Vertical Data Enable). The process of generating these two key signals is dependent on the incoming video format as explained below (2.1.3, 2.1.4 and 2.1.5) – accordingly the relevant blocks have to be programmatically enabled.

2.1.3 Composite Data Enable Handler

If the input to 88DE2750 is with composite DE, then the composite DE Handler decomposes it into Hde and Vde.

2.1.4 Front-end Timing Generator

If the input to 88DE2750 is with Hsync and Vsync, then the Front-end Timing Generator(FETG) generates Hde and Vde with reference to incoming HSync and Vsync. The generic FETG implementation (of two counters – pixels and lines) allows 88DE2750 to accept not only the standard CEA861 and SMPTE timings but also any non-standard timing.

2.1.5 BT656/BT1120 Decoder

If the input to 88DE2750 is with embedded syncs, like BT656 (for SD) or BT1120 (for HD) formatted video, then this block decodes the embedded SAV & EAV control words in the data stream to generate Hde and Vde.

2.2 Digital Output Video Interface

88DE2750 outputs the processed (and uncompressed) digital video in a variety of formats through the generic **output digital port of 44 pins** (42 flexible pins for data and sync controls + 2 dedicated clock pins). A bank of 42 multiplexers, each of 42:1 allow any data/sync control to be connected to any of the 42 pins.

Any video output timing can be generated including the standard CEA861 and SMPTE, through appropriate programming of the backend timing generator (BETG)

The output can either be interlaced or progressive. In case of interlaced output without scaling, the output lines can be original input lines or processed & flicker-filtered lines.

The supported output resolutions are

- SD : 480i59.94/60 or 576i50 (13.5MHz or pixel duplicated 27MHz)
- HD : up to **1080p60** (148.5MHz)
- Graphics : up to **1600x1200@60 or 4Kx2K@24**

For output resolutions with rates less than 166Mpixels/sec, both single edge and dual edge clocking options are available. For pixel rates greater than 166Mpixels/sec, only double edge clocking is supported.

The supported data formats are

- 16-bit : 4:2:2 8-bit
- 20-bit : 4:2:2 10-bit
- 24-bit : 4:2:2 12-bit
- 24-bit : 4:4:4 8-bit
- 30-bit : 4:4:4 10-bit
- 36-bit : 4:4:4 12-bit

In all the above cases, the processed video output can be

- SD or HD
- 1x or 2x clock(pixel duplicated) for SD, 1x clock for HD
- RGB or 4:2:2/4:4:4YCbCr
- **Only discrete syncs** (CEA861/SMPTE) – **two sets** of output timing signals (**HS, VS and FieldID/DE**) are generated to allow the same output data to be fed into two devices – for example HDMI-Tx that typically follows CEA timing specification and a Video encoder that typically follows SMPTE timing specification. FieldID pin can also be configured to drive out (composite) DE

2.2.1 Backend Timing Generator (BETG)

The Backend Generator generates the 88DE2750's output timing i.e. places Hsync and Vsync with respect to the DE window. The generic BETG implementation (of two counters – pixels and lines) allows 88DE2750 to generate not only the standard CEA861 and SMPTE timings but also any non-standard timing.

2.2.2 Interlacer

The interlacer block drops alternate lines from the internally generated progressive image to create interlaced output.

For format conversion cases like 1080i to 1080i, where the output is interlaced and the input is also interaced with no scaling involved, then the interlacer block can drop the created lines and pick up the original input lines from the internally created progressive image, or can perform an averaging operation for flicker filtered output.

2.3 TWSI Interface

The registers in 88DE2750 are accessed through the simple **TWSI interface (two-wire-serial-interface).** 88DE2750 is a slave device and the TWSI transactions are initiated by a master device, typically an off-

chip Micro-controller.The TWSI interface is compatible with I2C and works at the standard SCL frequencies of 100KHz and 400KHz.

88DE2750's TWSI interface uses **page-wise** register access mechanism i.e. all the programmable registers are grouped into multiple pages with each page holding a maximum of 256 registers (register offset address 0x00 to 0xff). Hence, accessing a register in 88DE2750 is a two step process:

First, **select the page,** using device addresses **{A and A+1}**: A to select the page and (A+1) to read the selected page. Then, **access the specific register** in that page, using device addresses **{B and B+1}:** B to write to the register and (B+1) to read from the register.

State of Ball N14 during Reset	TWSI Device address "A"
0	0x20
1	0x40

To **select a page**, TWSI command is
{Device-Address(A), **Fixed-offset-addr(0x00)**, Page-number-of-interest(0x00 to 0xff)}

To **read the selected page**, TWSI command is
{Device-Address(A+1), **Fixed-offset-addr(0x00)**}

State of Ball N14 during Reset	TWSI Device address "B"
0	0x22
1	0x42

To **write to a register**, TWSI command is
{Device-Address(B), Offset-addr-of-register-of-interest(0x00 to 0xff), data}

To **read from a register**, TWSI command is
{Device-Address(B+1), Offset-addr-of-register-of-interest(0x00 to 0xff)}

2.4 Color Space Converter (CSC)

88DE2750 has multiple color space converters at various points in the data path. All the color space converters are fully programmable - implemented by 3x3 matrix multiplication and 3x1 vector addition and can be used for any linear color space conversion - RGB to YCbCr, YCbCr to RGB, $YCbCr_{601}$ to $YCbCr_{709}$ etc through appropriate programming of the 9 coefficients (3x3 matrix) and the 3 offsets (3x1 matrix). Color space conversion works in 4:4:4 domain.

CSC that is towards the end of the data path (close to output) is also used for picture controls like brightness, contrast, hue and saturation.

2.5 Data and Sync Instrumentation

Data and Sync Instrumentation are performed on the input either continuously or in a single triggered fashion.

The Data Instrumentation block gives the values of "first pixel", "last pixel" and also the position of the first pixel that match with the programmed pixel value. This block also identifies the "first non-black line" and the "last non-black line" in each frame or field, where the black is defined by a programmable user threshold. These help in letterbox and pillar box detection.

The Sync Instrumentation block monitors the stability of input sync and clock signals. It also measures the period of the syncs for auto detection of incoming video format.

2.6 Compression Artifact Reducer (CAR)

The CAR module consists of a mosquito noise reducer and block noise reducer. Both of them work on input luma only. Both of them adapt to the quality of the input and thus prevent filtering of good quality video. The mosquito noise reducer filters only those pixels that are identified as mosquito noise. The block noise reducer identifies the blocking grid that is visible in compressed video and filters pixels in the vicinity of the block grid. It can identify both standard (8x8) blocks as well as bigger block sizes (upto 21x21) that may occur due to the input video being pre-scaled. The CAR module works on 4:2:2 YCbCr SD/HD video, interlaced as well as progressive.

2.7 3D Video Noise Reducer (VNR)

The 3D Video Noise Reducer reduces Additive White Gaussian Noise (AWGN) present in the incoming video and works on 16 bit 4:2:2 YC data, interlaced or progressive, SD or HD. Noise reduction is done by using a per pixel, motion adaptive, spatio-temporal architecture that reduces noise while minimizing artifacts such as blurring and ghosting. Spatial noise reduction is used on moving areas of the video while temporal noise reduction is done on stationary areas. Robust motion detection ensures correct switching of spatio/temporal modes. Noise reduction can be done independently on luma and chroma channels. For cross color suppression, luma motion can be used for chroma path.

2.8 3D Deinterlacer

Deinterlacer converts SD/HD interlaced inputs to progressive format. The deinterlacer operates on 4:2:2 YCbCr input. It automatically detects if the input is video or film and handles these two types of content appropriately.

The video deinterlacer consists of a per-pixel, motion adaptive, spatio-temporal blender. The spatial deinterlacer uses the proprietary Vector Interpolation technology to reduce “jaggies” or staircase effects on even ultra shallow edges. Advanced motion detection algorithms prevent artifacts such as feathering.

The film deinterlacer detects a variety of film cadences – 3:2, 2:2, 2:2:2:4, 2:3:3:2, 3:2:3:2:2, 6:4, 5:5 and 8:7 and two user programmable film cadences. Film deinterlacing is done by weaving input video fields in the correct order such that resolution is not lost. Film mode detection is robust enough to handle mixed cadence sequences.

There is also a two zone feature that is intended for film material that has text on the bottom (either scrolling text or subtitles). This feature ensures that the bottom part of the input (that contains the text) is treated as video while the rest of the frame is treated as film.

2.9 Edge enhancer

The luma edge enhancer sharpens the video by enhancing fine details and sharpening soft edges. The fine detail enhancer works on the principles of un-sharp masking. It extracts high frequency components and boosts them by applying a gain. In the extracted detail map, the large edges are masked and the detail map is scaled independently and then blended with the up-scaled video.

Horizontal Luma Transient Improvement (LTI) is performed on the up-scaled video. It sharpens large-amplitude vertical edges and slanted edges. The final enhanced video is a combination of the scaled video, scaled detail map and the LTI signal.

Horizontal Chroma Transient Improvement (CTI) sharpens large-amplitude vertical and slanted chroma boundaries.

2.10 Scaler

88DE2750 has a very high quality flexible video scaler. The horizontal scaling is achieved by a 12 tap, 64 phase polyphase filter. The vertical scaling filter has either 5 or 8 taps depending on the horizontal resolution and also has 64 phases. The coefficients of the scaler filters are programmable.

Scaler can be used for both upscaling and downscaling with independent horizontal and vertical scaling ratios.

The horizontal scaler is capable of 3-zone non-linear (anamorphic) scaling to show 4:3 content on a 16:9 display, without cropping or using pillar box. It has three separate scaling zones preserving the aspect ratio at the center of the picture, at the expense of increased aspect ratio distortion towards the sides of the screen.

2.11 Frame Rate Conversion (FRC)

Frame rate conversion (FRC) is used to convert the final output video of 8DDE2750 to match the desired refresh rate of the display. FRC is done either by dropping or repeating the input frames. The FRC block has logic to prevent tearing of video .

8DDE2750-4 is to be used for format conversion cases that require HD/1080i deinterlacing as well as frame rate conversion, like 1080i50 to 1080p60. For most of the other format conversion cases, 88DE2750 -2 will suffice.

2.12 Film Grain Generator

The Film Grain Generator adds specially shaped noise to the video to give a smoother effect. This gives a film like look to the video, like the one shot by an analog film camera.

2.13 Color Management Unit (CMU)

CMU has advanced color management and enhancement capabilities and has the modules as outlined below.

2.13.1 2D Fleshtone Correction

Flesh tones can be adjusted by applying a 2x2 matrix on the chroma (U and V) of flesh tone pixels. Flesh tone pixels are detected by programming inner and outer ranges in the U-V color wheel. Every pixel is marked with an 8-bit “flesh value” depending on location with respect to the inner and outer ranges. Pixels with highest flesh bits are corrected the most and the correction automatically tapers down on pixels with lower flesh bits. This smooth correction ensures that the output picture is free of artifacts caused by abrupt enhancement changes.

2.13.2 Intelligent Color Remapper (ICR)

This module allows colors to be adjusted independently by dividing the u-v color wheel into 13 regions using 14 programmable axes. Each of these axes is associated with a programmable Hue and Saturation change. The enhancement of a given pixel depends on the region it falls in and also on the hue and saturation changes associated with adjacent axes forming the region. In this way, only specific colors, such as grass green or sky blue, can be enhanced or modified without affecting any other color. The pixel values are monitored to make sure the results produced are always valid and no clipping or loss of detail occurs even when the saturation enhancement is set to maximum.

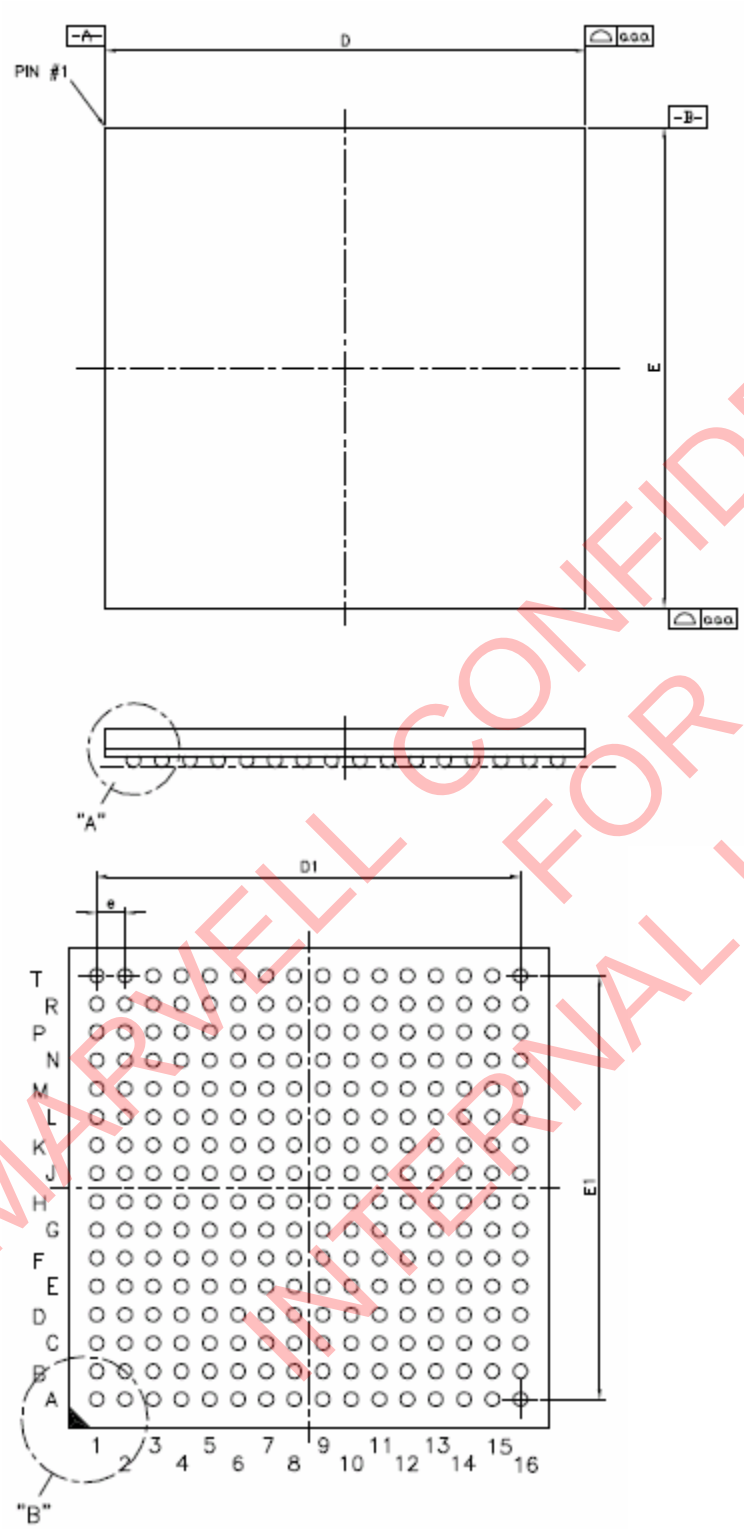
2.13.3 Qdeo True Color (QTC)

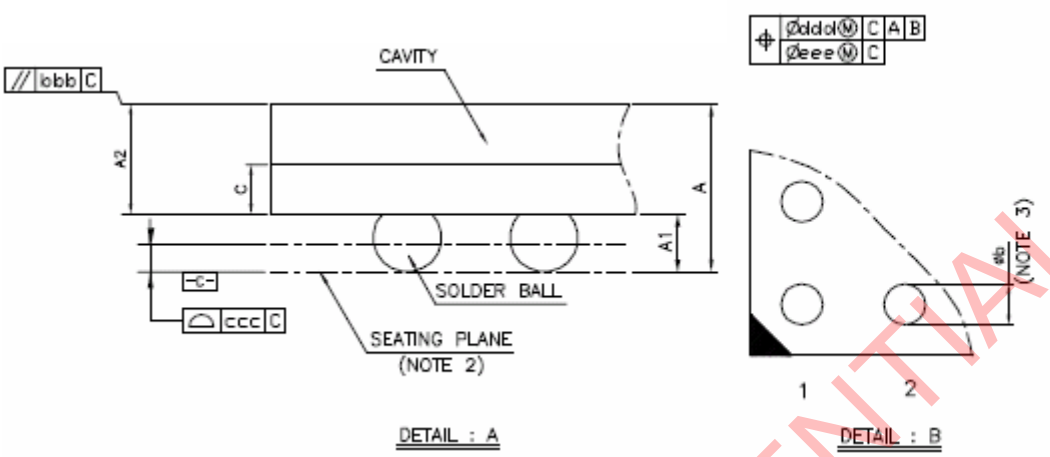
High-quality QTC converts 8-bit video (256 grey levels) to true 10-bits (1024 grey levels) and reduces contouring

2.13.4 Gamma Correction

Three independent gamma LUTs (lookup tables, 3x1024x12) are provided, one for each of the three channels – R/Cr, G/Y, B/Cb, to map 10-bit input to 12-bit output.

Section 3 : Packaging





Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.50	---	---	0.059
A1	0.30	0.40	0.50	0.012	0.016	0.020
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	---	0.36	---	---	0.014	---
D	16.80	17.00	17.20	0.661	0.669	0.677
E	16.80	17.00	17.20	0.661	0.669	0.677
D1	---	15.00	---	---	0.591	---
E1	---	15.00	---	---	0.591	---
e	---	1.00	---	---	0.039	---
b	0.40	0.50	0.60	0.016	0.020	0.024
aaa	0.10			0.004		
bbb	0.20			0.008		
ccc	0.15			0.006		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	16/16			16/16		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

Section 4 : BallOut

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	DATA_IN[13]	DATA_IN[14]	DATA_IN[16]	DATA_IN[19]	DATA_IN[23]	DATA_IN[26]	CLK_IN2	RESETZ	EXT_IN	TDI	DATA_OUT[33]	IOVDD	DATA_OUT[27]	DATA_OUT[25]	IOVDD
B	DATA_IN[12]	VSS	DATA_IN[15]	DATA_IN[17]	DATA_IN[20]	IOVDD	DATA_IN[27]	FD_SEL	SDA	TCK	TDO	DATA_OUT[32]	DATA_OUT[29]	DATA_OUT[26]	IOVDD	DATA_OUT[24]
C	DATA_IN[10]	DATA_IN[11]	VSS	DATA_IN[18]	DATA_IN[21]	DATA_IN[24]	DATA_IN[28]	TEST	SCL	TMS	DATA_OUT[35]	DATA_OUT[31]	DATA_OUT[28]	IOVDD	DATA_OUT[22]	DATA_OUT[23]
D	DATA_IN[7]	DATA_IN[8]	DATA_IN[9]	VSS	DATA_IN[22]	DATA_IN[25]	DATA_IN[29]	DVDD	IOVDD	TRST	DATA_OUT[34]	DATA_OUT[30]	IOVDD	DATA_OUT[19]	DATA_OUT[20]	DATA_OUT[21]
E	DATA_IN[3]	DATA_IN[4]	DATA_IN[5]	DATA_IN[6]	VSS	VSS	VSS	DVDD	DVDD	IOVDD	IOVDD	IOVDD	DATA_OUT[16]	VSS	DATA_OUT[17]	DATA_OUT[18]
F	CLK_IN1	IOVDD	DATA_IN[1]	DATA_IN[2]	DVDD	VSS	VSS	VSS	VSS	VSS	VSS	IOVDD	DATA_OUT[13]	DATA_OUT[14]	IOVDD	DATA_OUT[15]
G	FD_IN	VS_IN	HS_IN	DATA_IN[0]	DVDD	VSS	VSS	VSS	VSS	VSS	VSS	IOVDD	DATA_OUT[9]	DATA_OUT[10]	DATA_OUT[11]	DATA_OUT[12]
H	DDRREF	CAL	MVDD	DVDD	DVDD	VSS	VSS	VSS	VSS	VSS	VSS	IOVDD	DATA_OUT[6]	DATA_OUT[7]	VSS	DATA_OUT[8]
J	VSS	MDT[0]	MDT[1]	MDT[2]	MVDD	VSS	VSS	VSS	VSS	VSS	VSS	IOVDD	DATA_OUT[3]	IOVDD	DATA_OUT[4]	DATA_OUT[5]
K	DQSB[0]	MVDD	MDT[3]	MDT[4]	MVDD	VSS	VSS	VSS	VSS	VSS	VSS	DVDD	DATA_OUT[0]	DATA_OUT[1]	DATA_OUT[2]	IOVDD
L	DQS[0]	VSS	MDT[5]	MDT[6]	MVDD	VSS	VSS	VSS	VSS	VSS	VSS	DVDD	FD_OUT1	VS_OUT1	HS_OUT1	CLK_OUT1
M	MVDD	MDT[7]	CSZ	CKE	MVDD	MVDD	MVDD	MVDD	DVDD	DVDD	DVDD	DVDD	VSS	DVDD	VSS	IOVDD
N	MAD[0]	MAD[1]	MAD[2]	MVDD	MAD[8]	RASZ	WEZ	MDT[9]	MDT[11]	MDT[13]	VSS	PVDDA	DVDD	VS_OUT2	HS_OUT2	CLK_OUT2
P	MAD[3]	MAD[4]	MVDD	MAD[7]	MAD[12]	CASZ	BA[0]	MDT[8]	MDT[10]	MDT[12]	MDT[15]	PVSSA	ATEST	DVDD	FD_OUT2	IOVDD
R	VSS	MVDD	MAD[6]	MAD[11]	VSS	ODT	BA[1]	VSS	MVDD	VSS	MDT[14]	MVDD	XTVSS	VSS	DVDD	DVDD
T	MVDD	MAD[5]	MAD[9]	DDR_AVDD	MAD[10]	CLK	CLKZ	MVDD	DQSB[1]	DQS[1]	MVDD	VSS	XTAL1	XTAL2	DVDD	DVDD

4.1 Ball descriptions

Ball name	Ball#	Type	#of balls
DDR2 interface			
MAD0	N1		13
MAD1	N2		
MAD2	N3		
MAD3	P1		
MAD4	P2		
MAD5	T2		
MAD6	R3		
MAD7	P4		
MAD8	N5		
MAD9	T3		
MAD10	T5		
MAD11	R4		
MAD12	P5		
BA0	P7	Address bus, SSTL18, **Output**	2
BA1	R7		
RASZ	N6		6
CASZ	P6		
WEZ	N7		
CSZ	M3		
CKE	M4		
ODT	R6		
CLK	T6	Control bus, SSTL18, **Output**	2
CLKZ	T7		
MDT0	J2		10
MDT1	J3		
MDT2	J4		
MDT3	K3		
MDT4	K4		
MDT5	L3		
MDT6	L4		
MDT7	M2	Lower byte of the 16-bit data bus and the associated data strobe, SSTL18, **bidirectional**	
DQS0	L1		
DQSB0	K1		
MDT8	P8	Upper byte of the 16-bit data bus and the associated data strobe, SSTL18, **bidirectional**	10
MDT9	N8		
MDT10	P9		
MDT11	N9		
MDT12	P10		
MDT13	N10		
MDT14	R11		
MDT15	P11		

DQS1	T10		
DQSB1	T9		
CAL	H2	DDR2 pad impedance control, connect 300ohm to GND	1
Digital Video Input Port			
DATA_IN[0]	G4	**33-bit flexible bus**, any bit/control can go on any of the 33-pins, **Input**, LVTTL. The control set should consist of three signals, either {HS,VS,FD} or {Composite DE, VS, FD}.	30
DATA_IN[1]	F3		
DATA_IN[2]	F4		
DATA_IN[3]	E1		
DATA_IN[4]	E2		
DATA_IN[5]	E3		
DATA_IN[6]	E4		
DATA_IN[7]	D1		
DATA_IN[8]	D2		
DATA_IN[9]	D3		
DATA_IN[10]	C1		
DATA_IN[11]	C2		
DATA_IN[12]	B1		
DATA_IN[13]	A2		
DATA_IN[14]	A3		
DATA_IN[15]	B3		
DATA_IN[16]	A4		
DATA_IN[17]	B4		
DATA_IN[18]	C4		
DATA_IN[19]	A5		
DATA_IN[20]	B5		
DATA_IN[21]	C5		
DATA_IN[22]	D5		
DATA_IN[23]	A6		
DATA_IN[24]	C6		
DATA_IN[25]	D6		
DATA_IN[26]	A7		
DATA_IN[27]	B7		
DATA_IN[28]	C7		
DATA_IN[29]	D7		
HS_IN	G3		3
VS_IN	G2		
FD_IN	G1		
FD_SEL	B8	Repeat Field Flag (RFF) pin from a MPEG decoder, can be used for weaving the fields by the deinterlacer, in case of film content, **Input**, LVTTL	1
CLK_IN1	F1	Clock associated with the input video, **Input**, LVTTL. Two video inputs can be simultaneously fed into 88DE2750 as long as the total pin	2
CLK_IN2	A8		

		requirement is less than 35 (including all - data + ctrl + clk), though only one of the two inputs is selected and processed.	
Digital Video Output Port			
DATA_OUT[0]	K13	**42-bit flexible bus**, any bit/control can go on any of the 42-pins, **Output** (except bidirectional pin N14), LVTTL. Two sets of output controls are provided so that the same max 36-bit data out can be driven into two output devices following two different timing specifications - say HDMI-Tx following CEA861 timings spec and a Video encoder following SMPTE timing spec. The control set can be either {HS, VS, FiD} or {HS, VS, DE} **N14** is a dual use pin. The state of Pin N14 is used as I2C device address selection and will be latched during reset cycle – If LOW 88DE2750's **I2C slave address** is set to {0x20, 0x22}. If HIGH, it is set to {0x40, 0x42).	36
DATA_OUT[1]	K14		
DATA_OUT[2]	K15		
DATA_OUT[3]	J13		
DATA_OUT[4]	J15		
DATA_OUT[5]	J16		
DATA_OUT[6]	H13		
DATA_OUT[7]	H14		
DATA_OUT[8]	H16		
DATA_OUT[9]	G13		
DATA_OUT[10]	G14		
DATA_OUT[11]	G15		
DATA_OUT[12]	G16		
DATA_OUT[13]	F13		
DATA_OUT[14]	F14		
DATA_OUT[15]	F16		
DATA_OUT[16]	E13		
DATA_OUT[17]	E15		
DATA_OUT[18]	E16		
DATA_OUT[19]	D14		
DATA_OUT[20]	D15		
DATA_OUT[21]	D16		
DATA_OUT[22]	C15		
DATA_OUT[23]	C16		
DATA_OUT[24]	B16		
DATA_OUT[25]	A15		
DATA_OUT[26]	B14		
DATA_OUT[27]	A14		
DATA_OUT[28]	C13		
DATA_OUT[29]	B13		
DATA_OUT[30]	D12		
DATA_OUT[31]	C12		
DATA_OUT[32]	B12		
DATA_OUT[33]	A12		
DATA_OUT[34]	D11		
DATA_OUT[35]	C11		
HS_OUT1	L15		6
VS_OUT1	L14		
FD_OUT1	L13		
HS_OUT2	N15		
VS_OUT2	N14		
FD_OUT2	P15		
CLK_OUT1	L16	Two output clocks associated with the two set of output controls LVTTL, **output**	2
CLK_OUT2	N16		

Miscellaneous			
XTAL1	T13	Connect a 20MHz crystal, see the reference schematic	2
XTAL2	T14		
SCL	C9	TWSI (two-wire-serial-interface), I2C compatible bus, LVTTL, SCL is **input** and SDA is **bidirectional**	2
SDA	B9		
RESETZ	A9	Active low reset - 88DE2750 is under reset when this pin is low, LVTTL, **input**	1
EXT_IN	A10	External reference signal as a locking source for the onchip PLLs, LVTTL, **input**	1
TCK	B10	JTAG interface, LVTTL, {**Input, Input, Input, Input, Output**}	5
TMS	C10		
TRST	D10		
TDI	A11		
TDO	B11		
TEST	C8	Must be LOW for normal operation, **Input**, LVTTL	2
ATEST	P13	Analog test output, No Connect (NC) for normal use **Output**, LVTTL	
Power and GND			
PVDDA	N12	Power for Analog PLLs and Crystal oscillator, 1.8V	1
MVDD	J5, K5, L5, M5, N4, P3, R2, T1, M6,M7,M8,T8,R9,T11,R12,M1,H3,K2	Power for DDR2 interface, 1.8V	18
IOVDD	A13, A16, B6, B15, C14, D13, E10, E11, E12, F2, F12, F15, G12, H12, J12, J14, K16, M16, P16, D9	Power for I/O, 3.3V	20
DVDD	F5, G5, E8, E9, D8, H4, H5, K12, L12, M9, M10, M11, M12, M14, N13, R15, R16, T15, T16, P14	Power for Core, 1V	20
DDR_AVDD	T4	Power for DDR2 PHY PLL, 1.8V	1
XTVSS	R13	GND	1
PVSSA	P12	GND	1

VSS	A1, B2, C3, D4, E5, E6, E7, E14, F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, H15, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L2, L6, L7, L8, L9, L10, L11, M13, M15, N11, R1, R5, R8, R10, R14, T12, J1	GND	56
DDRREF	H1	Reference for DDR2 interface, 0.9V	1
		Total	**256**

Section 5 : Electrical Characteristics

5.1 Absolute Maximum Ratings

Core Supply Voltage (DVDD)	−0.5V to +1.35V
IO Supply Voltage (IOVDD)	−0.5V to +3.9V
1.8V Supply Voltage (MVDD, PVDDA, DDR_AVDD)	−0.5V to +2.15V
Junction Temperature	+125°C
Storage Temperature	−45°C to +125°C
Power dissipation	2.9W for -4 1.4W for -2
ESD voltage using Human Body Model (HBM)	+/-2 KV
ESD voltage using Charge Device Model (CDM)	+/- 500V

5.2 Recommended Operating Conditions

	Min	Typ	Max	Units
DVDD Supply Voltage (Core)	0.9	1.0	1.1	volts
IOVDD Supply Voltage (IO)	3.1	3.3	3.6	volts
PVDDA Supply Voltage (APLL)	1.65	1.8	1.95	volts
MVDD Supply Voltage (DDRAM)	1.65	1.8	1.95	volts
DDR_AVDD Supply Voltage (DDR PHY PLL)	1.65	1.8	1.95	volts
Ambient Operating Temperature		70		°C
Junction Operating Temperature		100		°C
IOVDD supply noise (peak to peak)		4% of IOVDD		volts

5.2.1 Crystal Oscillator

Recommended crystal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{XTAL}	Crystal frequency	Parallel resonance, load = 18 pF		20.00		MHz
Δf_{XTAL}	Accuracy	@25°C	-20		+20	ppm
Δtf_{XTAL}	Temperature drift	0° to 70°C	-30		+30	ppm
R_S	Series resistance				50	Ω
C_S	Shunt capacitance			2	7	pF
C_L	Recommended load capacitance			15		pF

5.3 DC Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

5.3.1 TTL compatible Inputs

Symbol	Parameter	Conditions	Min	Max	Units
V_{INLO}	Logic 0 input voltage		-0.3	0.3 * IOVDD	V
V_{INHI}	Logic 1 input voltage		0.7 * IOVDD	IOVDD+0.3	V

5.3.2 TTL compatible Outputs

Symbol	Parameter	Conditions	Min	Max	Units
V_{OUTLO}	Logic 0 output voltage	I_{OUT} = 4 mA	-	0.4	V
V_{OUTHI}	Logic 1 output voltage	I_{OUT} = -4 mA	IOVDD-0.4	-	V
I_{OZ}	Output Tri-state current		-10	+10	µA

5.3.3 TTL compatible I^2C Bus

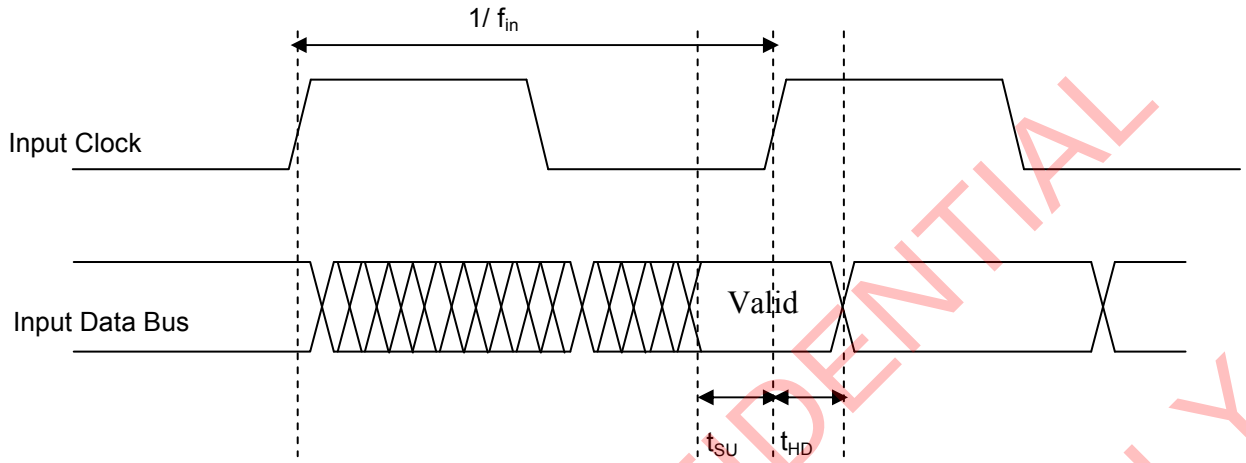
Symbol	Parameter	Conditions	Min	Max	Units
V_{OUTLO}	Logic 0 output voltage	I_{OUT} = 24 mA (open drain)	0	0.4	V
V_{INLO}	Logic 0 input voltage		-0.3	0.8	V
V_{INHI}	Logic 1 input voltage		2.0	IOVDD+0.3	V
I_{INLO}	Logic 0 input current	V_{IN} = 0 V	0	10	µA
I_{INHI}	Logic 1 input current	V_{IN} = V_{DD33}	-10	0	µA

5.3.4 DDRAM Interface - DDR Memory

Symbol	Parameter	Conditions	Min	Max	Units
V_{INLO}	Logic 0 input voltage		-0.3	DDRREF -0.125	V
V_{INHI}	Logic 1 input voltage		DDRREF+0.125	MVDD+0.3	V
V_{IL} (AC)	Logic 0 input AC voltage			DDRREF - 0.2	
V_{IH} (AC)	Logic 1 input AC voltage		DDRREF + 0.2		
V_{OUTLO}	Logic 0 output voltage		0.1 * MVDD		V
V_{OUTHI}	Logic 1 output voltage		0.9 * MVDD		V
$V_{CLKDIFF}$	Differential voltage between CLK and CLKZ		0.5	MVDD + 0.6	V
DDRREF	I/O Reference voltage		0.49xMVDD	0.51 x MVDD	V
V_{TT}	I/O Termination voltage		DDRREF - 0.04	DDRREF + 0.04	V

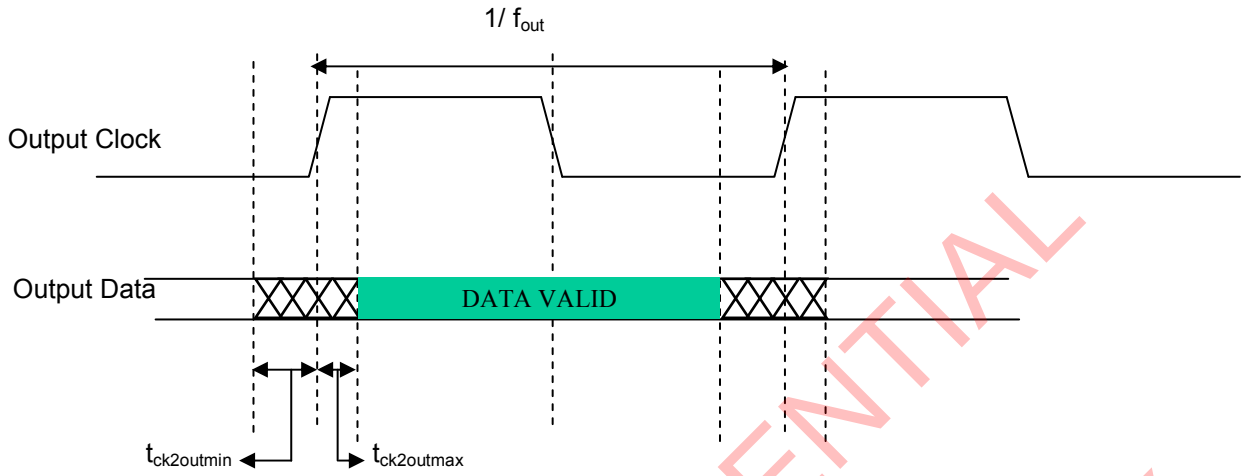
5.4 AC Characteristics

Over recommended operating supply and temperature ranges. 20% & 80% signal edges relative to 50% point of the clock edge unless otherwise specified.

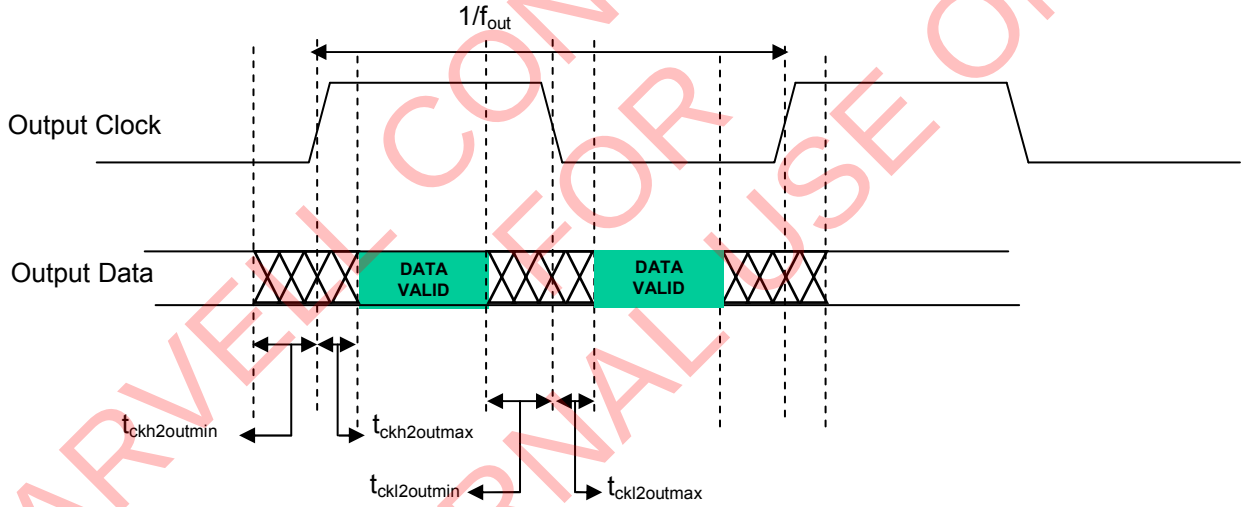


5.4.1 Timing Requirements for Digital Input Port *					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Units**
t_{SU}	Data valid to clock setup time		1.5		ns
t_{HD}	Data valid to clock hold time		0.5		ns
f_{in}	Clock frequency			166	MHz

* Guaranteed by design. Not actual tested values.



5.4.2 Timing Requirements for Digital Output (SDR – Single clock edge Mode)**					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Units**
t_{ck2out}	Clock to Output Data		-1.2	0.75	ns
f_{out}	Output clock frequency			166	MHz

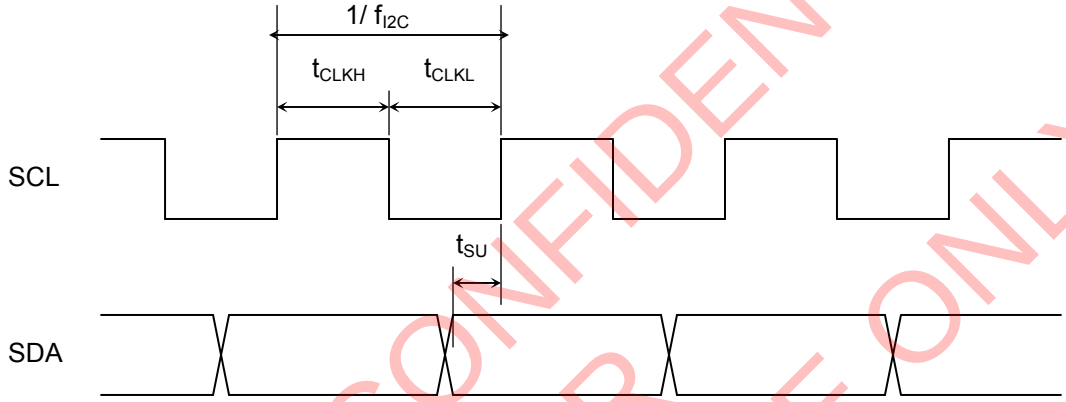


5.4.3 Timing Requirements for Digital Output (DDR – Dual clock edge Mode)**					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Units**
$t_{ckh2out}$	Clock to Output Data, rising edge		-1.2	0.55	ns
$t_{ckl2out}$	Clock to Output Data, failing edge		-1.2	0.55	ns
f_{out}	Output clock frequency			150	MHz

**Notes:

- Guaranteed by design. Not actual tested values
- Outgoing clock is FPLL2 Clock, Waveform drawn at clock-phase zero
- Data provided without polarity inversion on outgoing clock
- Difference between tck2out(max) and tck2out(min) gives the data invalid window
- The clock phase has to be adjusted through register programming to move the clock edges into the data valid windows. Phase granularity of period by 16 can be achieved through register programming

5.4.4 I²C Bus					
Symbol	**Paramater**	**Conditions**	**Min**	**Max**	**Units**
f_{I2C}	Clock frequency			400	KHz
t_{CLKH}	High period of clock	SCL		600	ns
t_{CLKL}	Low period of clock	SCL		1300	ns
t_{SU}	Data setup time	SDA to SCL		100	ns



5.4.5 DDR2 Memory Interface (for speed grade -2)

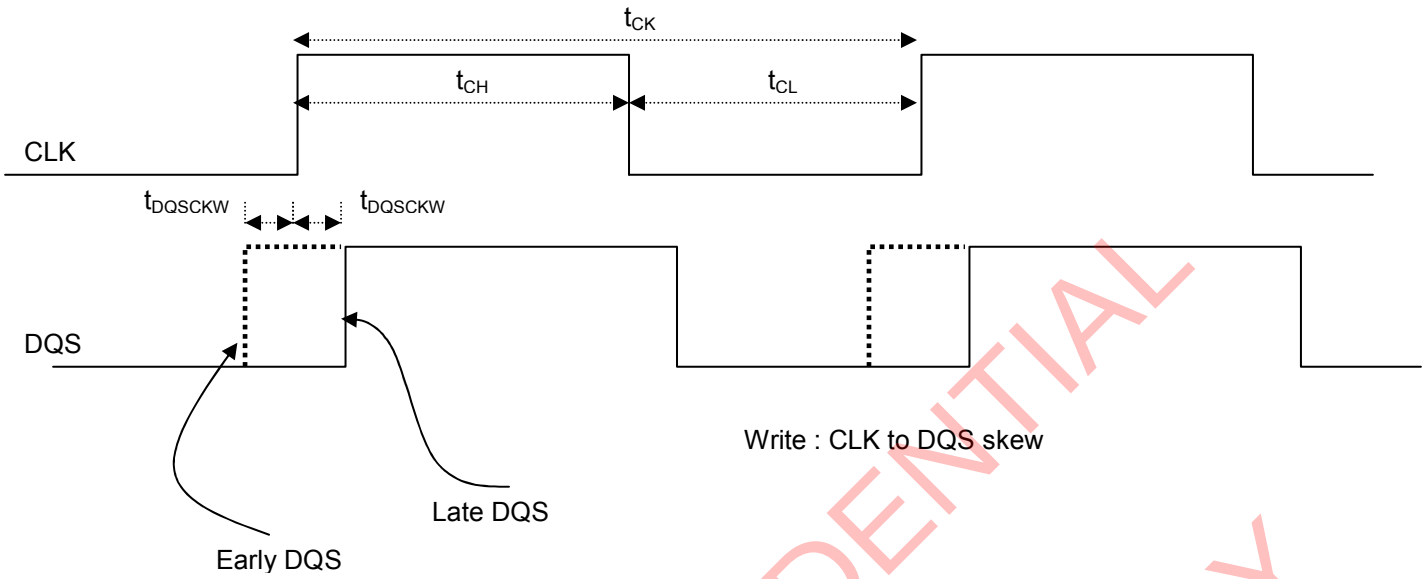
Symbol	Description	Min	Typical	Max	Units	Notes
tCK	CLK,CLKZ period		5.0		ns	
tCH	CLK,CLKZ high level width	0.45		0.55	tCK	
tCL	CLK,CLKZ low level width	0.45		0.55	tCK	
tHP	CLK,CLKZ half period	min(tCH, tCL)				
tDQSH	DQS high pulse width for write	0.45		0.55	tCK	
tDQSL	DQS low pulse width for write	0.45		0.55	tCK	
tDQSS	Write command to first DQS latching transition	1		1	tCK	
tDSSW	DQ Valid time before DQS, setup for write	0.915	—	—	ns	1
tDSHW	DQ Valid time after DQS, hold for write	0.915	—	—	ns	1
tDQSCKW	Skew of DQS to CLK during Write	-	-	0.05	ns	1
tCTLCKS	Addr and Ctrl outputs to CLK output setup time[Last Addr or Ctrl to go valid, to CLK]			2.1	ns	1
tCTLCKH	CLK output to Addr and Ctrl outputs hold time[First Addr or Ctrl to go invalid, from CLK]			2.1	ns	1
tBPR	DQ to DQS setup for read during high period			1	ns	
tCPR	DQ to DQS hold for read during high period			1.5	ns	
tBNR	DQ to DQS setup for read during low period			1	ns	
tCNR	DQ to DQS hold for read during low period			1.5	ns	

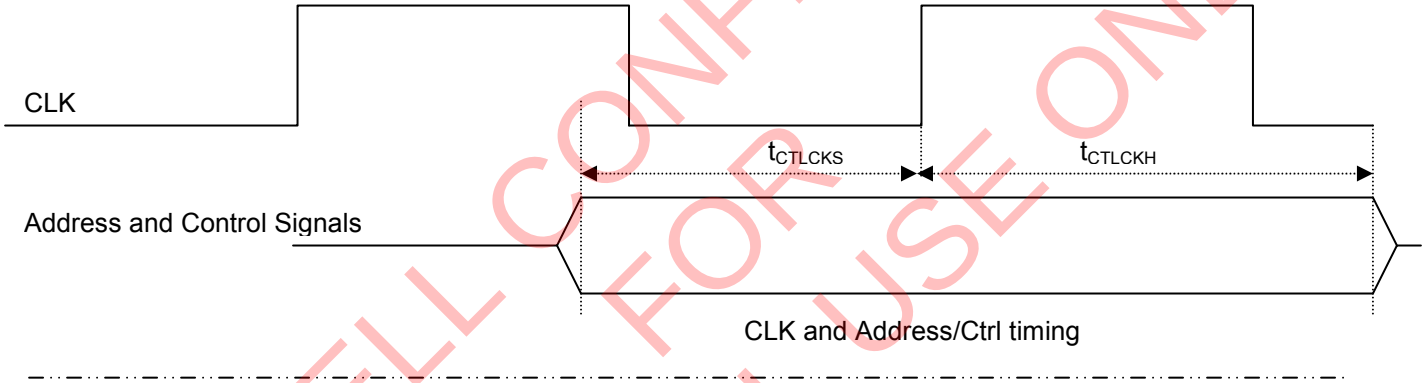
NOTE: 1. Timing Specified to Reference Load 25 Ohms to VTT. All timings are measured relative differential zero crossings of CLK/CLKZ and DQS/DQSB

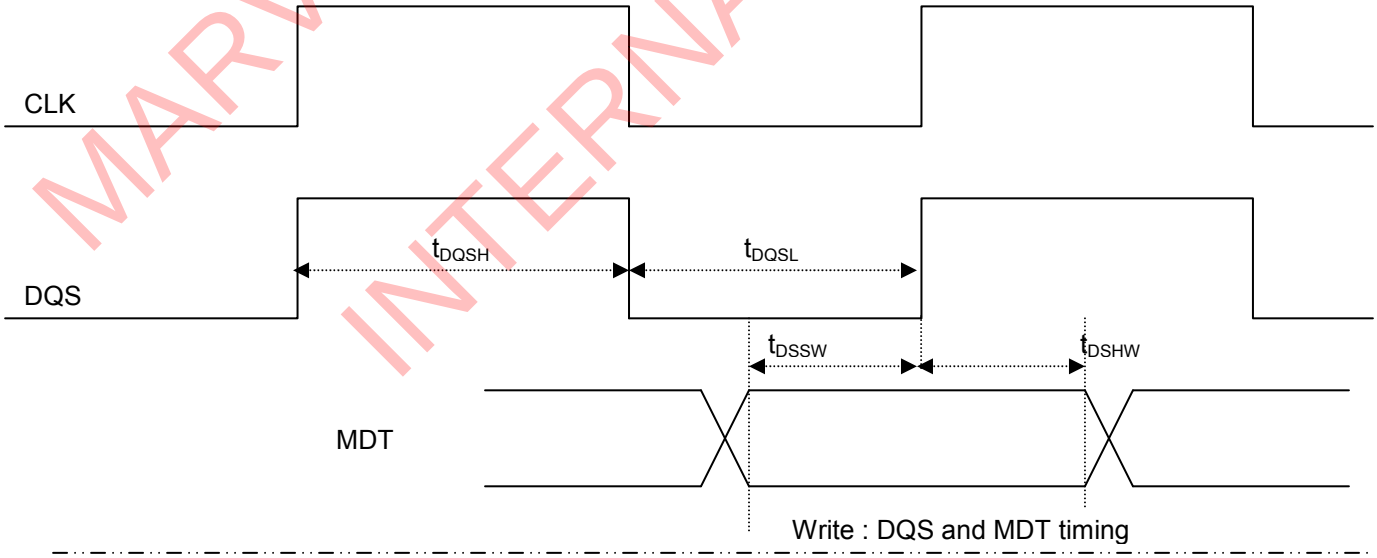
5.4.6 DDR2 Memory Interface (for speed grade -4)

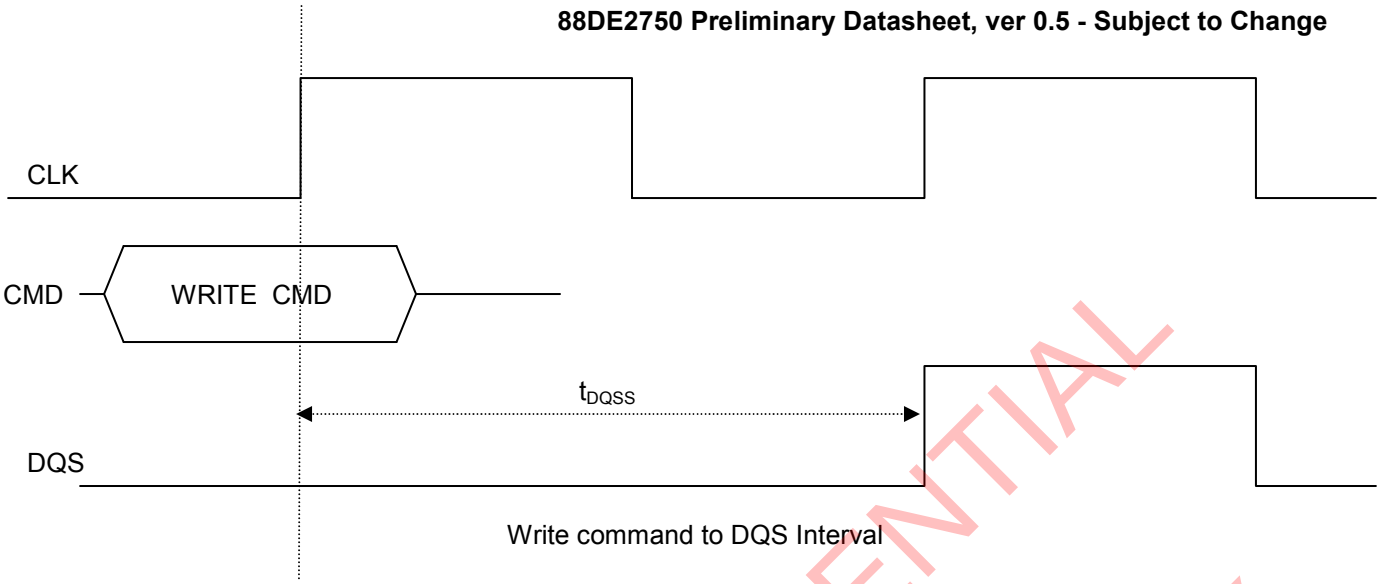
Symbol	Description	Min	Typical	Max	Units	Notes
tCK	CLK,CLKZ period		2.5		ns	
tCH	CLK,CLKZ high level width	0.45		0.55	tCK	
tCL	CLK,CLKZ low level width	0.45		0.55	tCK	
tHP	CLK,CLKZ half period	min(tCH, tCL)				
tDQSH	DQS high pulse width for write	0.45		0.55	tCK	
tDQSL	DQS low pulse width for write	0.45		0.55	tCK	
tDQSS	Write command to first DQS latching transition	1		1	tCK	
tDSSW	DQ Valid time before DQS, setup for write	0.29	—	—	ns	1
tDSHW	DQ Valid time after DQS, hold for write	0.29	—	—	ns	1
tDQSCKW	Skew of DQS to CLK during Write	-	-	0.05	ns	1
tCTLCKS	Addr and Ctrl outputs to CLK output setup time[Last Addr or Ctrl to go valid, to CLK]			0.88	ns	1
tCTLCKH	CLK output to Addr and Ctrl outputs hold time[First Addr or Ctrl to go invalid, from CLK]			0.88	ns	1
tBPR	DQ to DQS setup for read during high period			0.375	ns	
tCPR	DQ to DQS hold for read during high period			0.875	ns	
tBNR	DQ to DQS setup for read during low period			0.375	ns	
tCNR	DQ to DQS hold for read during low period			0.875	ns	

NOTE: 1. Timing Specified to Reference Load 25 Ohms to VTT. All timings are measured relative differential zero crossings of CLK/CLKZ and DQS/DQSB

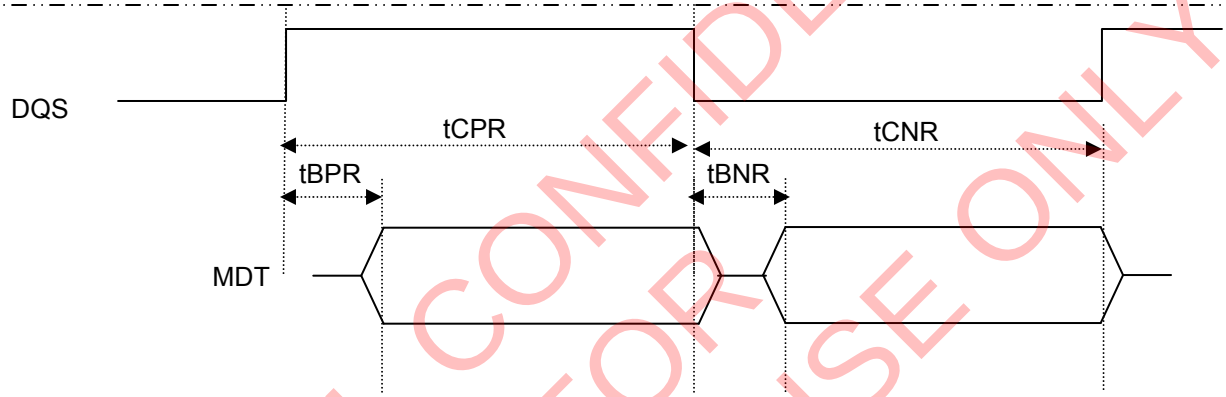




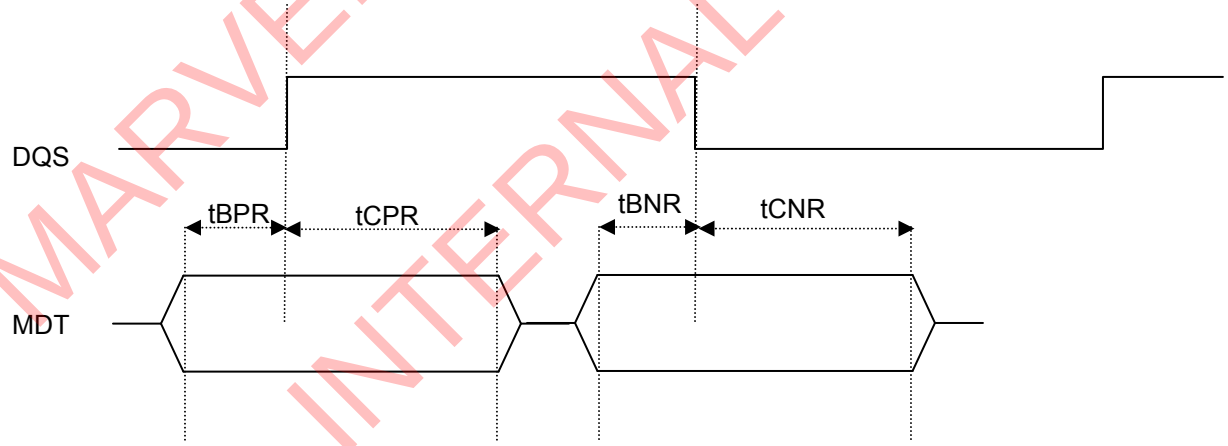




Write command to DQS Interval

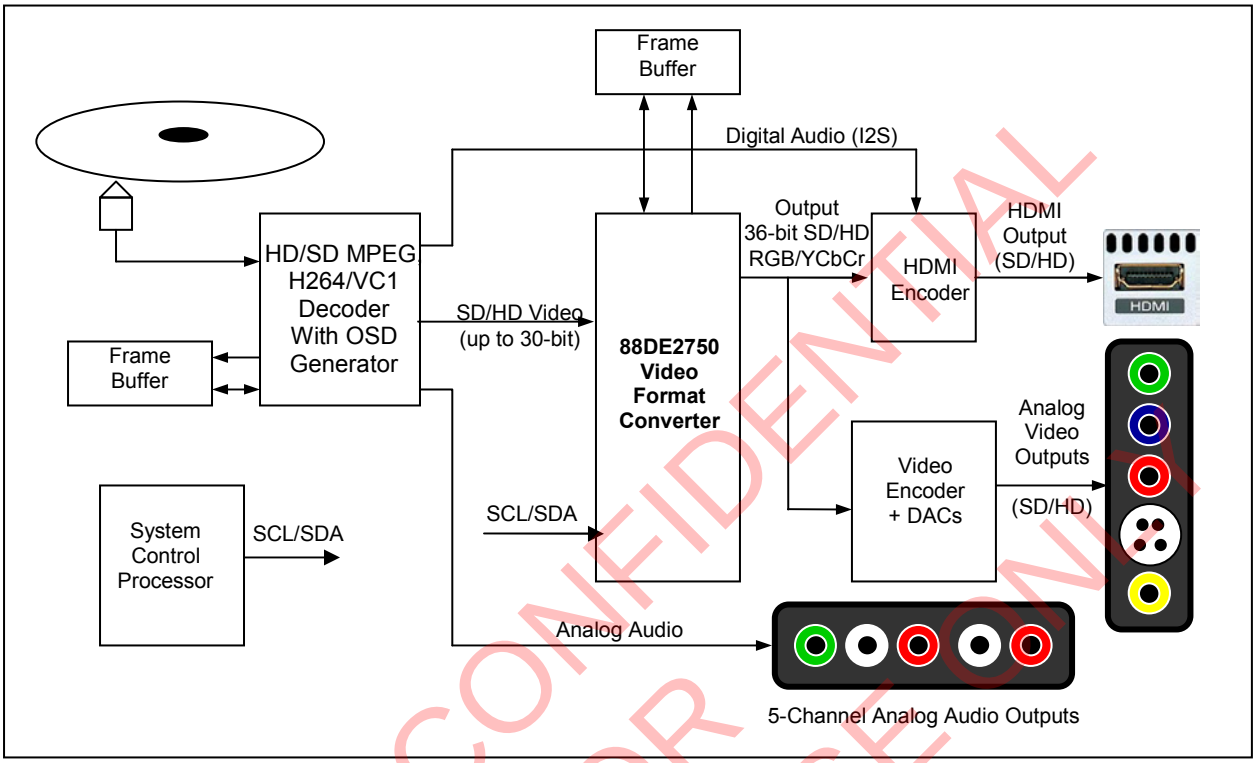


Read operation, late DQS : DQS and MDT timing



Read operation, early DQS : DQS and MDT timing

Section 6 : Typical System Configuration



DVD/Blu-ray Recorder (Playback section only) or Blu-ray Player

- SD and HD DVD playback capability
- HDMI and Analog HD YPbPr outputs
- 5-channel Analog and Digital audio outputs