$$CPI \quad \left[\frac{C}{I}\right] \times \frac{S}{10^6 \times I} \quad \frac{10^6 \times I}{S}$$

$$MIPS = \left[\frac{10^6 \times I}{S}\right]$$

Computer Organization & Assembly Languages

Final Exam – 2006/1/9

Dept. of Engineering Science, National Cheng Kung University

1. [21 points] True/False: Write your response.

T (1) If all other factors are the same, a computer with a higher throughput on some workload has better performance compared to a computer with a lower throughput.

T (2) The best benchmark of a computer consists of real programs that you will routinely use.

T (3) Reordering code is a possible way to avoid pipeline stalls.

T (4) Forwarding is primarily an attempt to fix data hazards in a pipeline.

F (5) In an instruction set like the 80x86, where instructions are not of the same length, pipelining is considerably easier.

F (6) In a pipelined system, forwarding will eliminate the need of any stalls.

F (7) Pipelining increases throughput and reduces individual instruction execution time.

2. [6 points] Suppose Microsoft Excel takes 2 seconds to recalculate the grades for Computer Organization on a 150MHz PC, which exhibits an average CPI of 2.5. What MIPS (millions of instructions per second) rating does the PC have for this benchmark situation?

$\frac{I \times 2.5}{150M} = 2$, $\frac{2 \times 150M}{2.5} = 120M$, $\frac{150M \times 2}{2.5} = 60$

3. [6 points] Suppose you wrote a program which executes in 100μs that loads a string into memory and prints it out. You discover a trick to loading the string into memory which will speed up that part of the program by 4 times. If loading the string took 80% of the execution before, what will the execution time be after making this change?

$100 \times \frac{80}{100} \times \frac{1}{4} + 100 \times \frac{20}{100} = 20 + 20 = 40.$

80%

20%

4. [13 points] Two machine designs have been proposed, A and B. Assume that Machine A's clock rate is *500MHz* and Machine B's clock rate is *400MHz*. Both machines have three classes of instructions. The **cycle counts** per instruction for the three classes are as follows:

	Machine A	Machine B
Class X	4	2
Class Y	3	4
Class Z	2	1

Two programs of interest that will be run on these machines require the following

number of instructions (in billions) for each instruction class:

	Program 1	Program 2
Class X	1	1
Class Y	2	2
Class Z	5	10

(1) Which program is faster on Machine A? Please calculate the average CPI for both programs. (4 points)

(2) Which program will execute faster according to MIPS (million instruction per second) on Machine A? (4 points)

(3) How much faster (or slower) is Machine A compared to Machine B if two programs were run successively on these two machines? (5 points)

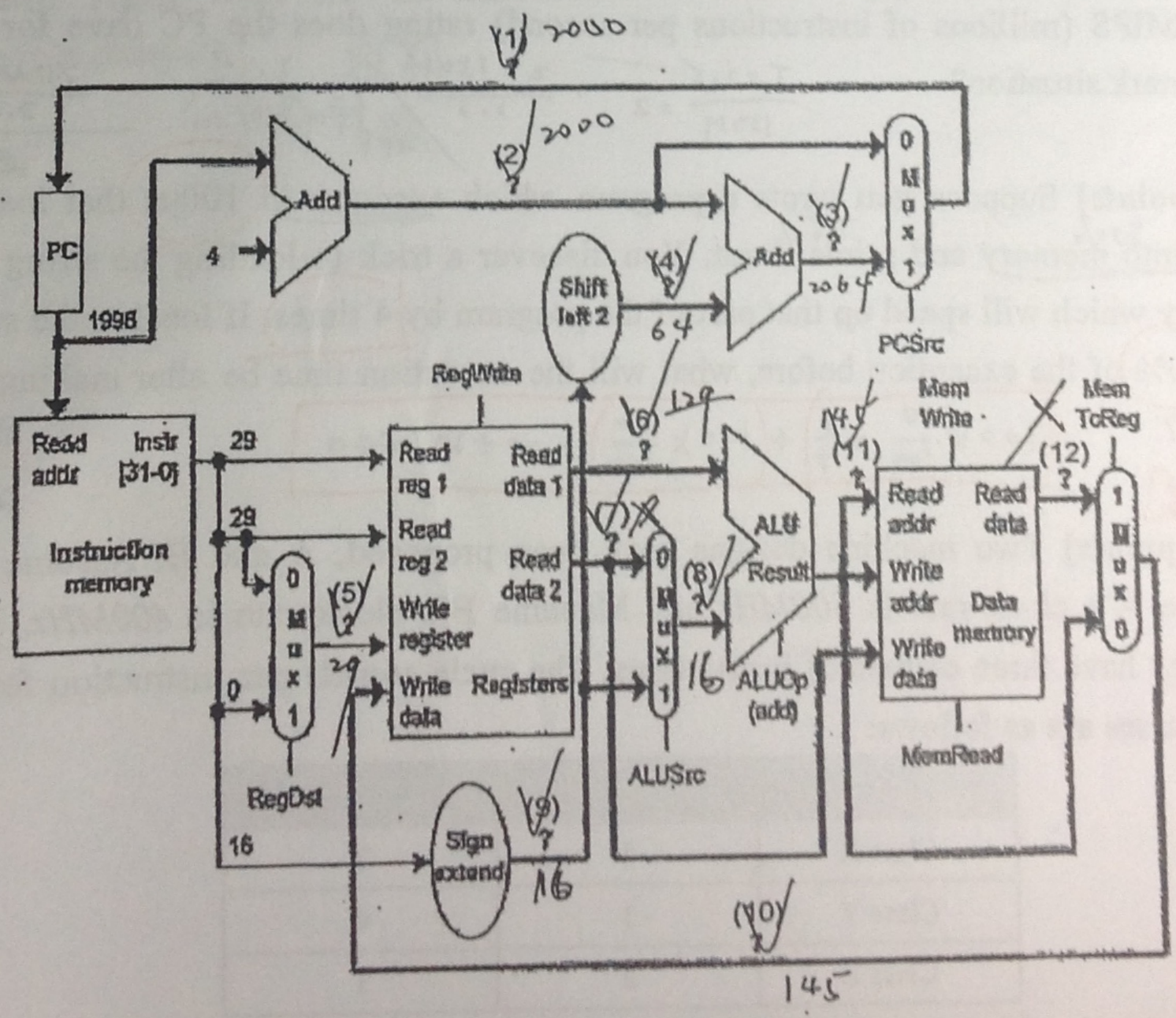
5. [12 points] Let's say we want to execute the following immediate addition instruction in the single-cycle datapath:

```
addi $29, $29, 16
```

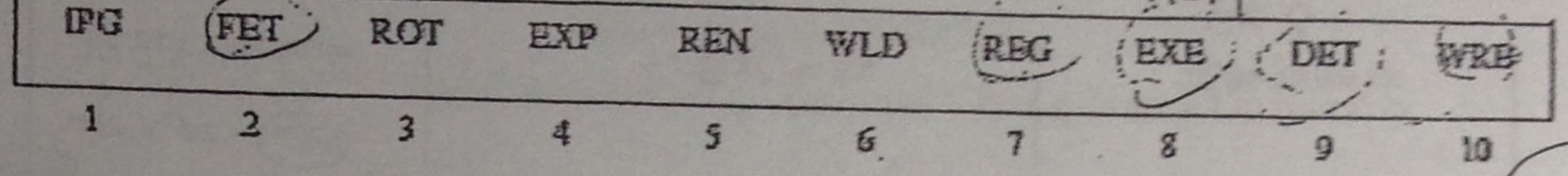
The single-cycle datapath diagram below shows the execution of this instruction. Several of the datapath values are filled in already. You are to provide values for the twelve remaining signals in the diagram, which are marked with a '?' symbol.

You should:

- Show decimal values.
- Assume register $29 initially contains the number 129.
- If a value cannot be determined, mark it as 'X'.



6. [16 points]



One CPU manufacturer proposed the 10-stage pipeline above for a 500MHz (2ns clock cycle) machine. Here are the correspondences between this and the MIPS pipeline:

- Instructions are fetched in the FET stage.
- Register reading is performed in the REG stage.
- ALU operations and memory access are both done in the EXE stage.
- Branches are resolved in the DET stage.
- WRB is the writeback stage.

(1) How much time is required to execute one million instructions on this processor, assuming there are no dependencies or branches in the code? (3 points)

(2) Without forwarding, how many stall cycles are needed for the following code fragment? Assume that the register file could be written and read in the same clock cycle. (3 points) What is this hazard called? (2 points)

```
lw   $t0, 0($a0)
add  $v1, $t0,$t0
```

(3) If a branch is mispredicted, how many instructions would have to be flushed from the pipeline? (3 points)

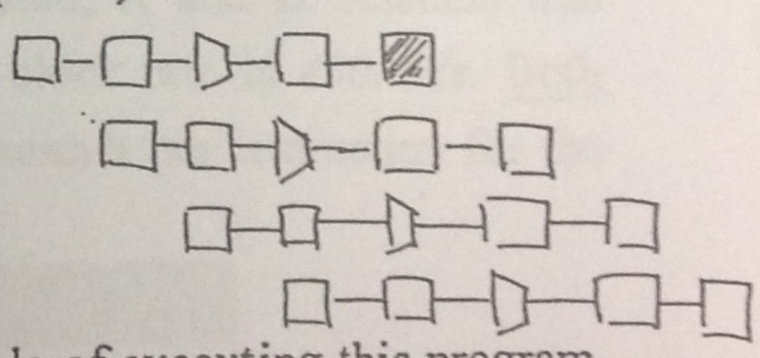
(4) Assume that a program executes one million instructions. Of these, 15% are load instructions which stall, and 10% of the instructions are branches. The CPU predicts branches correctly 75% of the time. How much time will it take to execute this program? (5 points)

7. [18 points]

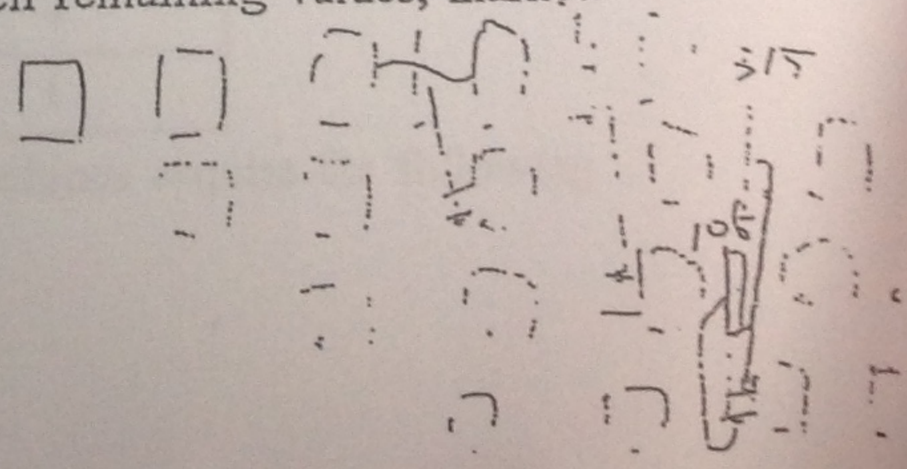
(1) Show or list all of the dependencies in this program. For each dependency, indicate which instructions and register are involved. (8 points)

```
add $8, $5, $5
add $2, $5, $8
sub $3, $8, $4
add $2, $2, $3
```

1 → 2, 3
2 → 4
3 → 4

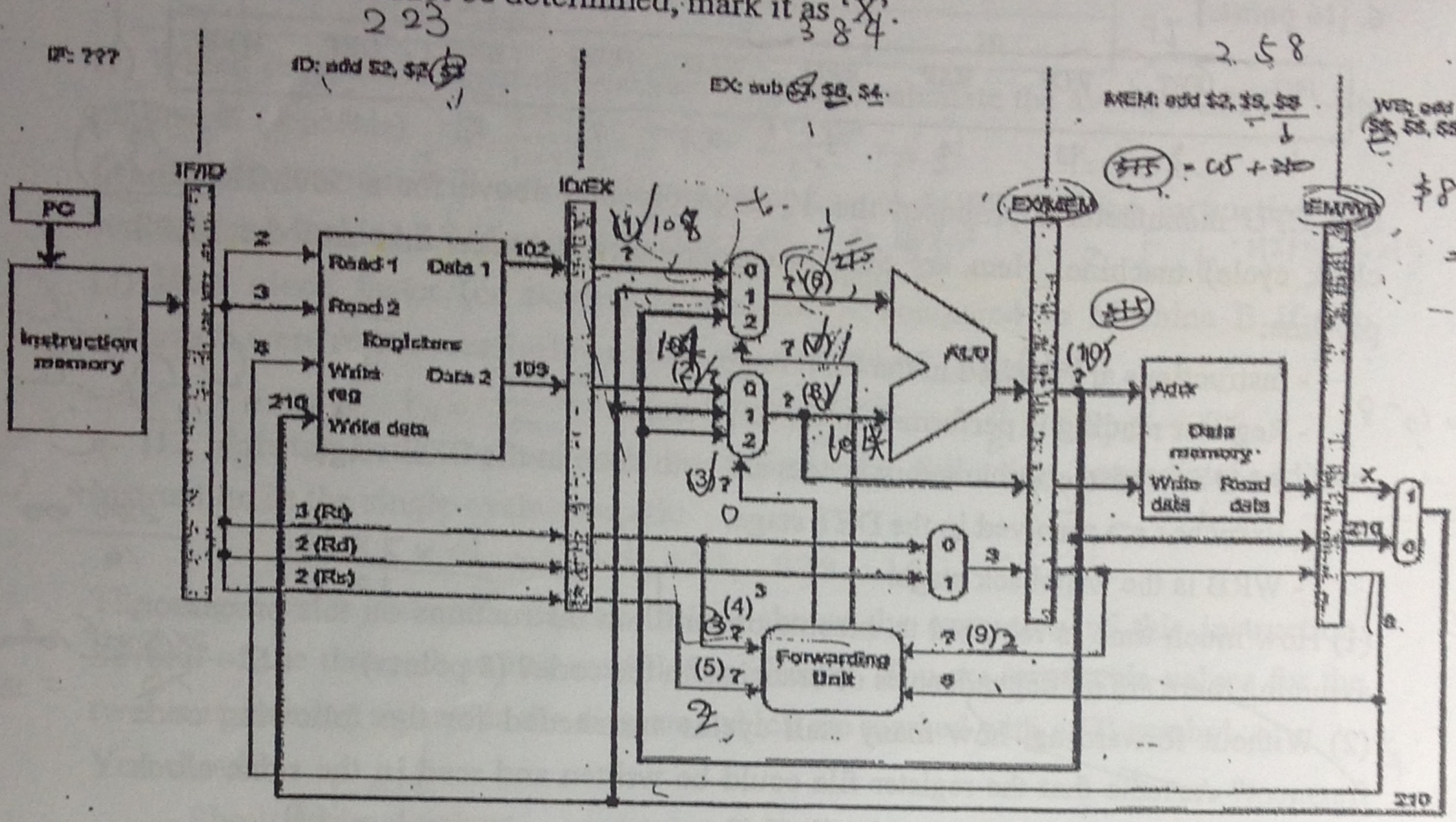


(2) The following pipelined datapath shows the fifth cycle of executing this program, including values for several of the stages. Fill in the ten remaining values, marked with a '?' symbol. (10 points)



Again, please:

- Show decimal values.
- Assume that registers initially contain their number plus 100: $2 contains 102, $8 contains 108, etc.
- If a value cannot be determined, mark it as 'X'.



8. [8 points] What are the similarities between a pipelined datapath and a single-cycle datapath? Also, what are the similarities between a pipelined datapath and a multicycle datapath?