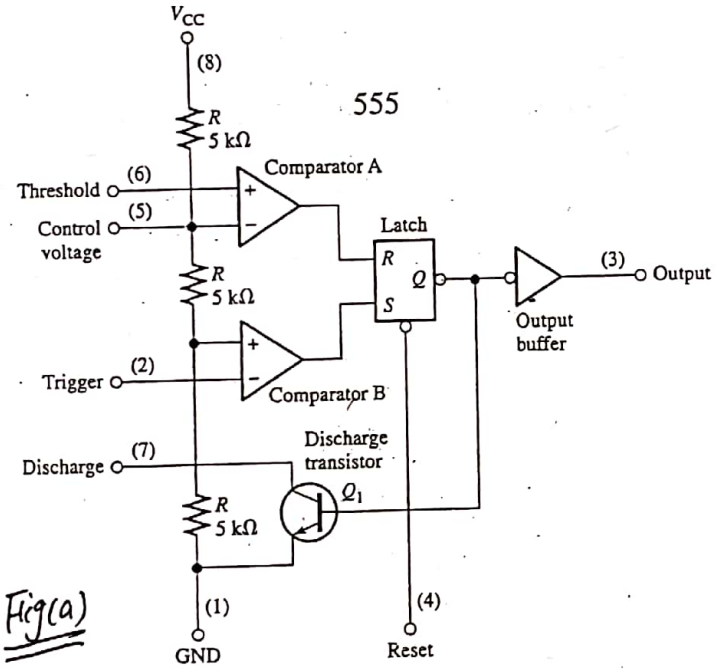
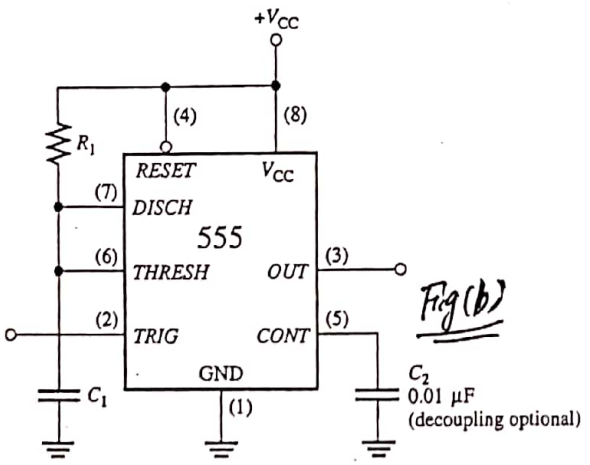
Time: 9:10~11:00 AM

NOTE: For all of the following design problems, you **MUST** show **the design procedures** in details, otherwise no score will be got.

1. How to design a D-type flip-flop by using a JK flip-flop and some gates. (5%)
2. Show the characteristic tables, excitation tables, and the next state equations of T-type and JK-type flip flops, respectively. (10%)
3. What is the difference between frequency divisor and counter? Explain it with an example. (10%)
4. What is a counter decoder? Explain it with example. (10%)
5. Design a module-5 asynchronous counter. (10%)
6. Use JK flip-flops to design an **up/down** synchronous counter which with 0,2,3,5,1,4,7,6,0… counting **up** sequence. (20%)
7. Design a sequential circuit with an input binary sequence x and an output z. The output z=1 after it receives **exact** three continuum bits of 1 each time. You must consider the asynchronous initialization signal. (20%)
8. Fig.(a) shows the internal functional diagram of 555 IC chip. For the Fig.(b) and (c), explain the functions and the detail operation principles, respectively. (15%)



Fig(a)



Fig(b)

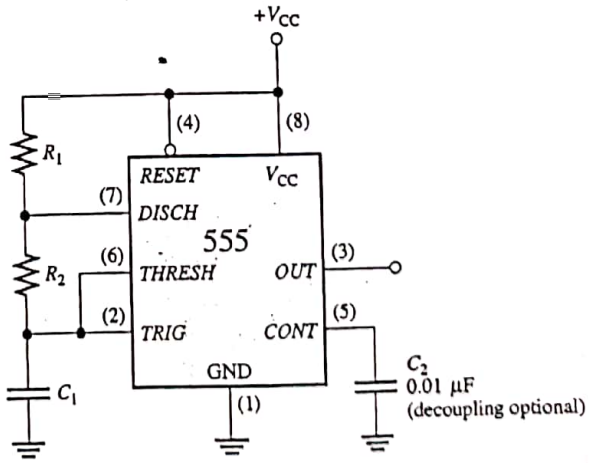


Fig (c)

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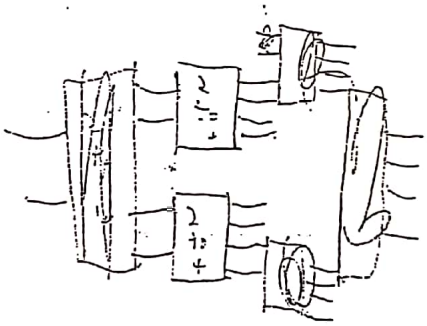
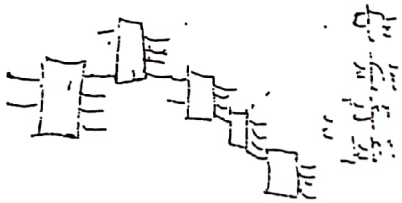
Time: 9:15 to 11:00 AM

1. Implement a binary full adder with a dual 4-to-1 line multiplexer and a single inverter.. (10%)
2. Design an excess-3 to Gray code converter, requiring that all invalid input combinations give 0000 as the output code. (15%)

Bin → Gray

3. Design a combinational circuit that accepts a 2-bit number and generates a 4-bit binary number output equal to the square of the input number. (15%)
4. Construct a 4-to-16 lines decoder with an enable input using five 2-to-4 lines decoders with enable inputs. (15%)
5. Design one pentad (五) digit adder. It means that the adder has two 3-bit inputs, each to represent 0 to 7, and one bit of carry input, the output with 3-bit of sum and one bit of carry. (20%)
6. Design a 3-bit binary comparator. (15%)
7. Show that all of the digital circuits can be implemented by using NAND gates only. (10%)





9:10~11:00

1. 假設某一循序電路有兩個 JK 正反器 A 與 B、兩個輸入 X 與 Y 以及一個輸出 Z；下列為正反器的輸入方程式與輸出方程式：(20%)

$$J_A = BX + \bar{B}\bar{Y} \qquad K_A = B \cdot X\bar{Y}$$

$$J_B = A + X\bar{Y} \qquad K_B = A + X\bar{Y}$$

$$Z = AXY + \bar{B}\bar{X}\bar{Y}$$

(a) 試繪此電路的邏輯圖。

(b) 試求其狀態表與狀態圖。

2. 試設計一個有兩個 JK 正反器 A 與 B 以及兩個輸入 E 與 X。若 E=0，無論 X 的值為何，電路維持原來狀態。當 E=1 且 X=1，則此電路產生由 00 到 01 到 10 到 11 再到 00 的一連串狀態改變，且一直重覆。當 E=1 且 X=0 時，此電路產生由 00 到 11 到 10 到 01 再到 00 的一連串狀態改變，且一直重覆。(20%)

(a) 試求其狀態表與狀態圖。

(b) 試繪此電路的邏輯圖。

3. 是利用 JK 正反器設計一個同步 BCD 計數器。(20%)

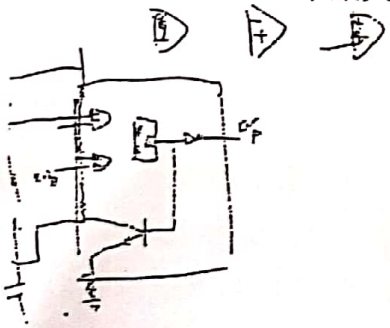
(a) 試求其狀態表與狀態圖。

(b) 試繪此電路的邏輯圖。

4. 設計一個可並行載入之四位元移位暫存器。它有兩條控制線輸入，一條用來控制移位(Shift)，另一條用來控制載入。請使用 D 型正反器與基本邏輯閘完成並說明運作過程。(此提可使用二元以上輸入的邏輯閘) (15%)

5. 請使用 JK 型正反器設計出 D 型與 T 型正反器，並詳細說明狀態變化與激勵表(Excitation Table)。(10%)

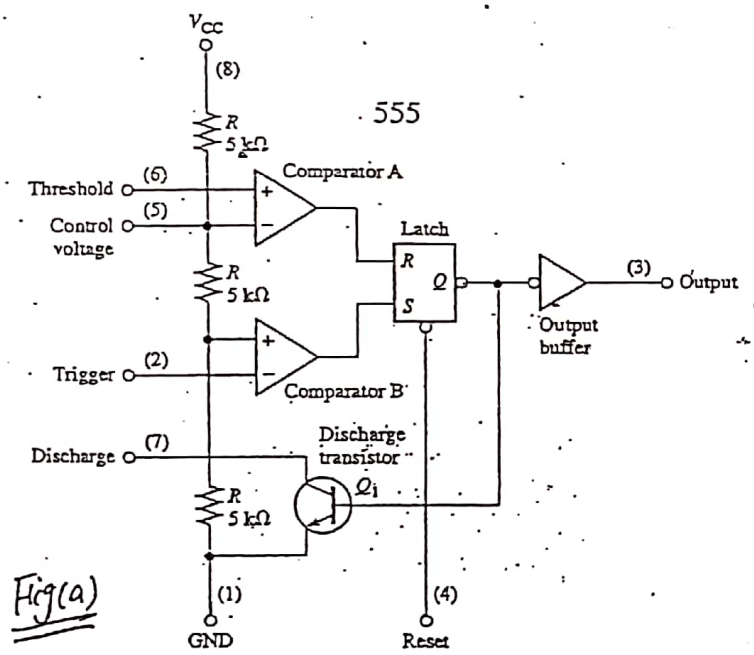
6. 請繪 555 單諧與多諧震盪電路，並說明其工作原理。(15%)



Time: 9:10~11:00 AM

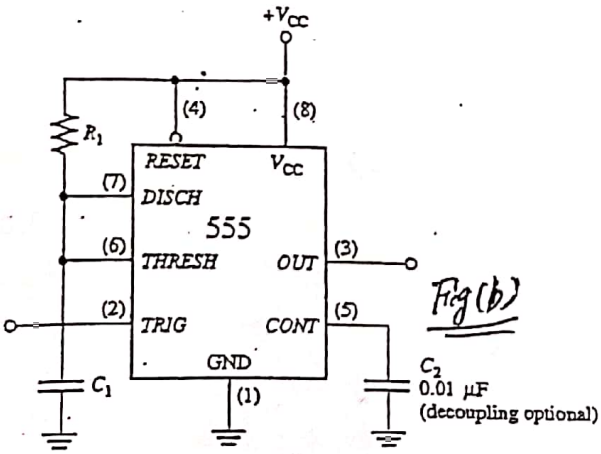
For all of the following design problems, you MUST show the design procedures in details, otherwise no score will be got.

1. How to design a T-type flip-flop by using a JK flip-flop and some gates. (10%)
2. What is the difference between frequency divisor and counter? Explain it with an example. (10%)
3. What is a counter decoder? Explain it with example. (10%)
4. Design a module-5 asynchronous counter. (10%)
5. Use JK flip-flops to design a 3-bit up/down synchronous counter. (20%)
6. Design a sequential circuit with an input binary sequence x and an output z. The output z=1 after it receives **exact** two continuum bits of 1 each time. You must consider the asynchronous initialization signal. (20%)
7. Fig (a) shows the internal functional diagram of 555 IC chip. For the Fig. (b) and (c), explain the functions and the detail operation principles, respectively. (20%)



Fig(a)

J	K	F_h	F_{h+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



Fig(b)

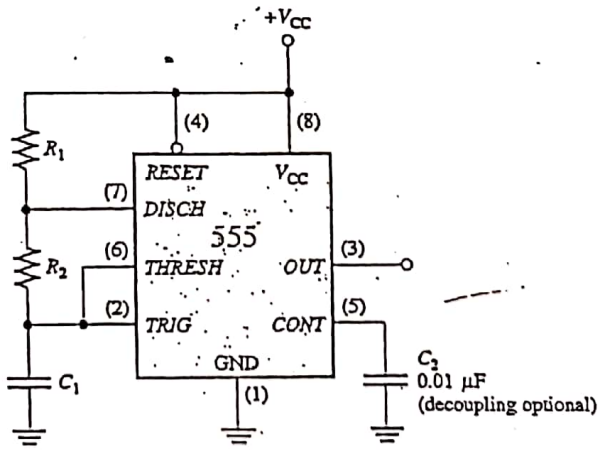


Fig (c)

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Exam II

1. Implement a full-adder circuit with a decoder and two OR gates. (10%)

2. Implement the following function with a multiplexer: (10%)

$$F(A,B,C,D)=\Sigma(0,1,3,4,8,9,15)$$

3. Design a BCD-to-excess-3 code converter with a BCD-to-decimal decoder and four OR gates. (10%)

4. Design a 4-line to 2-line priority encoder. Include an output E to indicate that at least one input is a 1. (10%)

5. Design a combinational circuit that generates the 9's complement of a BCD digit. (15%)

6. What size ROM would it take to implement: (a) A *BCD* adder / subtractor with a control input to select between the addition and subtraction. (b) Dual 4-line to 1-line multiplexers with common selection inputs. (c) A binary multiplier that multiplier two 4-bit numbers. (15%)

7. Construct a 5x32 decoder with four 3x8 decoder/de-multiplexers and a 2x4 decoder. (15%)

8. Design a four-bit-nibble control system that perform the bit manipulation defined in the control table as follow: (15%)

Control input		Output			
A	B	O_3	O_2	O_1	O_0
0	0	0	0	0	0
0	1	1	1	1	1
1	0	C_3'	C_2'	C_1'	C_0'
1	1	C_3	C_2	C_1	C_0

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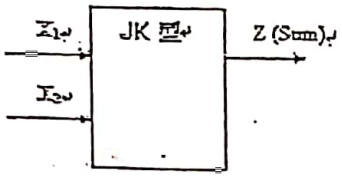
邏輯設計期末考

注意事項:State diagram、State table、電路圖(IC標示要清楚)

1. Design a serial adder (串列加法器) with a JK Flip-Flops and NOT /OR / AND gates. (20%)

   Hint: ($Z=X_1 \oplus X_2 \oplus Y$ Carry: $Y^+=X_1X_2+X_1Y+X_2Y$)

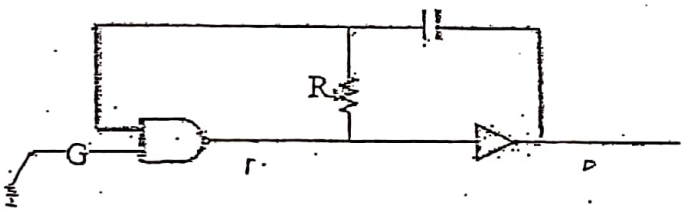


   EX: 101111 → (1+0+1+1+1+1) Y^+ Y^+

2. Design a synchronous counter which can giving the counting order *0, 3, 5, 1, 4, 6, 2*. Please use JK Flip-Flops. (15%)

3. Design a modulus-6 Johnson Counter. Please give the detail procedure and using D Flip-Flops. (15%)

4. For the circuit shown below is a clock generator. Please give the operation procedure and derive the clock's period. (20%)



5. Design a frequency divider which can provide a modul-7 divider. Please using D Flip-Flops. (15%)

6. Design an asynchronous counter which can provide the *0, 2, 4, 1, 3, 5* counting sequence. (15%)

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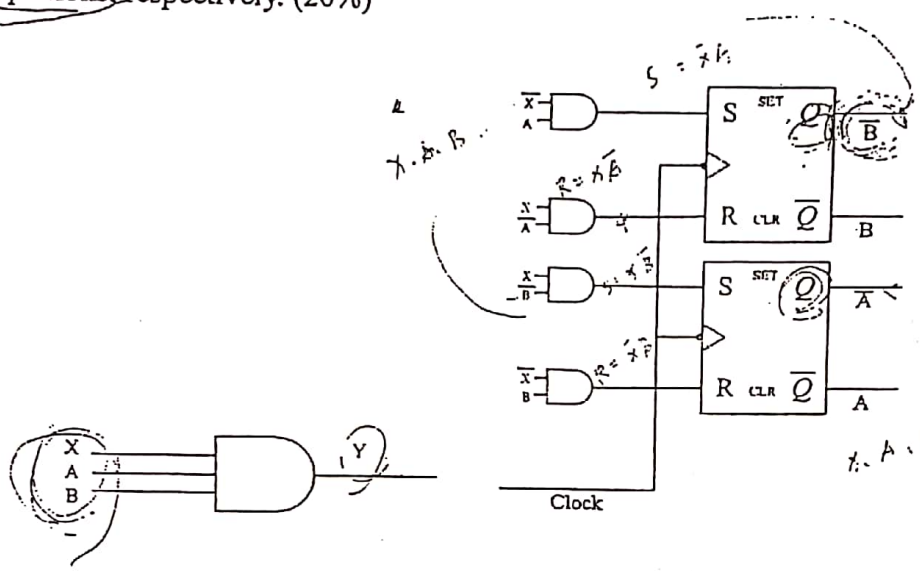
期末考 (9:00 ~ 11:00 Open Book)

1. Design the D flip-flop and T flip-flop by using JK flip-flop, respectively. Given the detail procedures you used. (需列出設計過程) (10%)

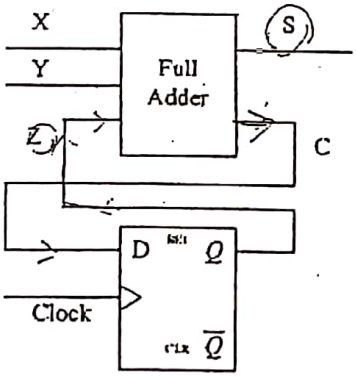
2. What is the difference between frequency division and binary counter? Give an example and explain your answer. (10%)

3. User 555 timers to implement 4 sec and 20 sec one-shotts, respectively. (10%)

4. Following is a clocked sequential circuit; Show its state table, the state diagram, and the next state equations, respectively. (20%)



5. The full adder of following circuit receives two external inputs x and y; the third input z comes from the output of a D flip-flop. The carry output is transferred to the flip-flop every clock pulse. The external S output gives the sum of x, y and z. Obtain the state table and state diagram of the sequential circuit. (20%)



6. Use J-K flip-flop to design a 3-bit asynchronous counter which can count the sequence of 0 to 5. (15%)

7. Use J-K flip-flop to design a counter that has a repeated sequence of six states 0→1→2→4→5→6. (15%)

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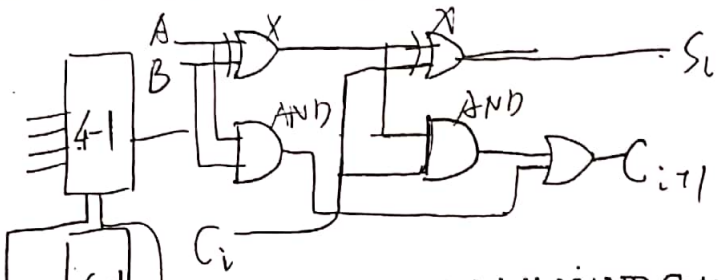
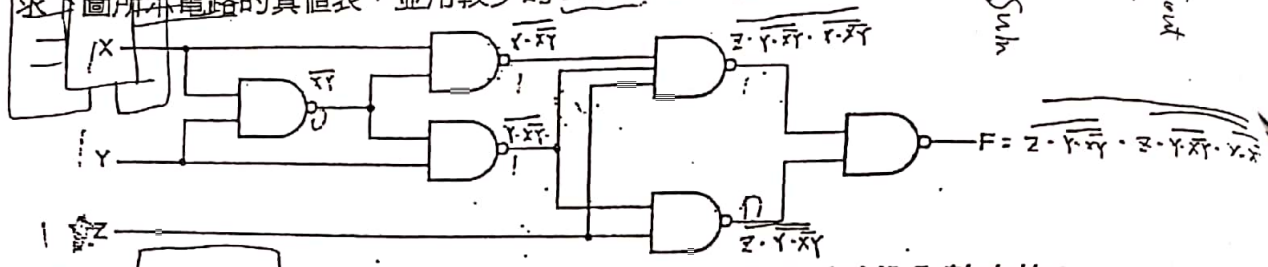


考試時間為 120 分鐘

1. 求下圖所示電路的真值表，並用較少的 NAND Gate 畫出等價電路。(10%)



2. 試設計一組合電路，使其輸入為一四位元數字，而其輸出為該輸入數字的 2 的補數。(5%)

3. 試設計兩個超三碼表示之十進位數字加法器。下列所示的為將兩個數字用一個四位元的二進位加完後所需要的修正：(15%)
   A. 進位輸出等於二進位加法器的進位。
   B. 若進位輸出=1，則加上 0011
   C. 若進位輸出=0，則加上 1101

4. 下列有三個布林函數定義出一個組合電路，試使用一個解碼器與額外的邏輯閘來設計此電路。(10%)

$$F_1 = \bar{X}\bar{Y} + XY\bar{Z}$$

$$F_2 = \bar{X} + Y$$

$$F_3 = XY + \bar{X}\bar{Y}$$

5. 試只用 NOR 閘繪製一個 2 對 4 線解碼的邏輯圖，並標出其致能輸入。(10%)

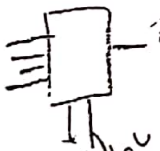
6. 試使用兩個 8 對 1 線多工器與一個 2 對 1 線多工器組成一個 16 對 1 線多工器，並使用標準的方塊圖符號。(10%)

7. 用一個雙重(Dual)4 對 1 線多工器製作一個全加器。(10%)

8. 用一個多工器製作下列布林函數。(10%)

$$F(A,B,C,D) = \sum m(0,3,5,6,8,9,14,15)$$

9. 試說明什麼是 PLD、GAL、PROM、PAL、PLA。(20%)



programmable Logic Device

Programmable Array Logic

Programmable Logic Device

AND array

OR array

$S_i = a_i \oplus b_i \oplus C_i$

$C = \cancel{abC_i}$

$ab + aC + bC$

$\bar{a}b + a(\bar{b}+b)C + (a+\bar{a})bC$

$\bar{a}b(0) + a\bar{b}(C) + \bar{a}bC + abC + (1+C)$

$\bar{a}b(0) + a\bar{b}(C) + \bar{a}bC + ab(1)$

$V_T = 2V_H e^{-t_1/RC}$

$= 2V_H e^{-\tau_1/RC}$

$\tau_1 = RC \ln 2V_H/V_T$

The second mid-examination of the Logic Design course

9:20~10:50 AM, 2006-05-15

1. Implement the following Boolean function with an 8-to-1-line multiplexer and a single inverter: $F(A,B,C,D)=\sum m(2,3,5,6,8,9,12,14)$

2. Design a combinational circuit that detects an error in the representation of a decimal digit in BCD. In other words, obtain a logic diagram whose output is equal to 1 when the inputs contain any one of the six unused bit combinations in the BCD code.

3. A majority function is generated in a combinational circuit when the output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority function.

4. Design a combinational circuit that accepts a 2-bit number and generates a 4-bit binary number output equal to the square of the input number.

5. Design a binary multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders.

(20 points for each problem)

9:10~11:00

1. 假設某一循序電路有兩個 JK 正反器 A 與 B、兩個輸入 X 與 Y 以及一個輸出 Z，下列爲正反器的輸入方程式與輸出方程式：(20%)

$J_A = BX + \bar{B}\bar{Y}$ $\qquad$ $K_A = \bar{B}X\bar{Y}$

$J_B = A + X\bar{Y}$ $\qquad$ $K_B = A + X\bar{Y}$

$Z = AXY + \bar{B}\bar{X}\bar{Y}$

(a) 試繪此電路的邏輯圖。

(b) 試求其狀態表與狀態圖。

2. 試設計一個有兩個 JK 正反器 A 與 B 以及兩個輸入 E 與 X。若 E=0，無論 X 的值爲何，電路維持原來狀態。當 E=1 且 X=1，則此電路產生由 00 到 01 到 10 到 11 再到 00 的一連串狀態改變，且一直重覆。當 E=1 且 X=0 時，此電路產生由 00 到 11 到 10 到 01 再到 00 的一連串狀態改變，且一直重覆。(20%)

(a) 試求其狀態表與狀態圖。

(b) 試繪此電路的邏輯圖。

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(b) 試繪此電路的邏輯圖。

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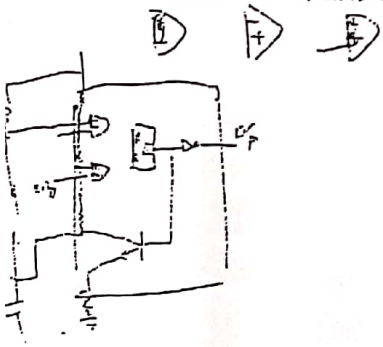
5. 請使用 JK 型正反器設計出 D 型與 T 型正反器，並詳細說明狀態變化與激勵表(Excitation Table)。(10%)

6. 請繪 555 單諧與多諧震盪電路，並說明其工作原理。(15%)



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Time: 9:15 to 11:00 AM

1. Implement a binary full adder with a dual 4-to-1 line multiplexer and a single inverter.. (10%)
2. Design an excess-3 to Gray code converter, requiring that all invalid input combinations give 0000 as the output code. (15%)
3. Design a combinational circuit that accepts a 2-bit number and generates a 4-bit binary number output equal to the square of the input number. (15%)
4. Construct a 4-to-16 lines decoder with an enable input using five 2-to-4 lines decoders with enable inputs. (15%)
5. Design one **pentad** (五) digit adder. It means that the adder has two 3-bit inputs, each to represent 0 to 7, and one bit of carry input, the output with 3-bit of sum and one bit of carry. (20%)
6. Design a 3-bit binary comparator. (15%)
7. Show that all of the digital circuits can be implemented by using NAND gates only. (10%)

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Time: 9:10~11:00 AM

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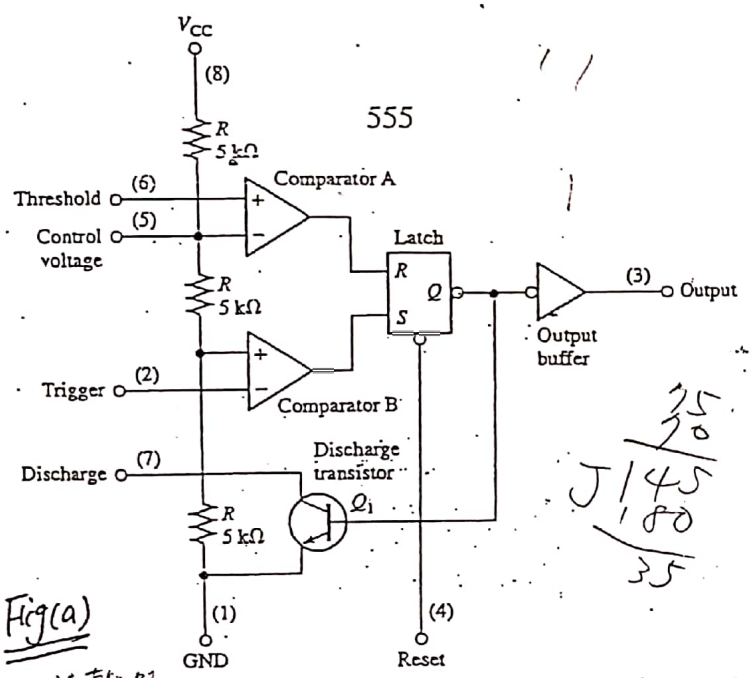
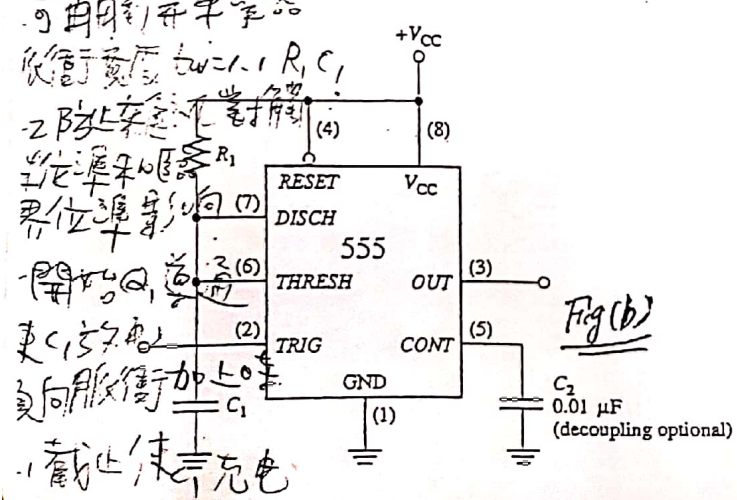
6. Design a sequential circuit with an input binary sequence x and an output z. The output z=1 after it receives **exact** two continuum bits of 1 each time. You must consider the asynchronous initialization signal. (20%)
7. Fig (a) shows the internal functional diagram of 555 IC chip. For the Fig. (b) and (c), explain the functions and the detail operation principles, respectively. (20%)



Fig(a)

J	K	F_n	F_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

35
20
J 145
180
35



Fig(b)

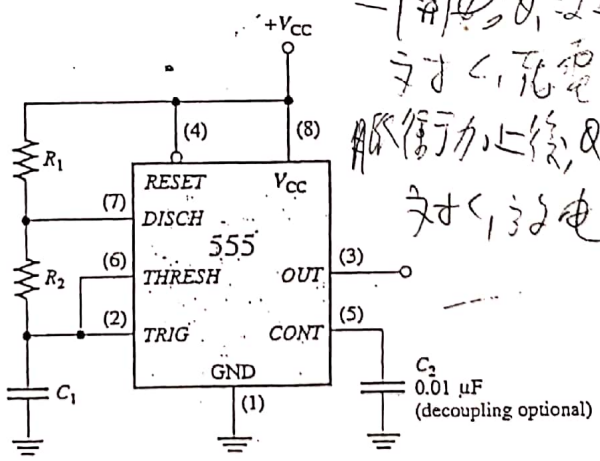


Fig (c)

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Exam II

1. Implement a full-adder circuit with a decoder and two OR gates. (10%)

2. Implement the following function with a multiplexer: (10%)

$$F(A,B,C,D)=\Sigma(0,1,3,4,8,9,15)$$

3. Design a BCD-to-excess-3 code converter with a BCD-to-decimal decoder and four OR gates. (10%)

4. Design a 4-line to 2-line priority encoder. Include an output E to indicate that at least one input is a 1. (10%)

5. Design a combinational circuit that generates the 9's complement of a BCD digit. (15%)

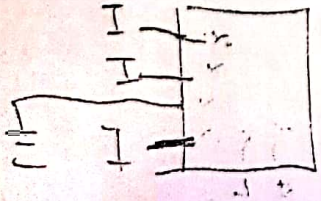
6. What size ROM would it take to implement: (a) A *BCD* adder / subtractor with a control input to select between the addition and subtraction. (b) Dual 4-line to 1-line multiplexers with common selection inputs. (c) A binary multiplier that multiplier two 4-bit numbers. (15%)

7. Construct a 5x32 decoder with four 3x8 decoder/de-multiplexers and a 2x4 decoder. (15%)

8. Design a four-bit-nibble control system that perform the bit manipulation defined in the control table as follow: (15%)

Control input		Output			
A	B	O_3	O_2	O_1	O_0
0	0	0	0	0	0
0	1	1	1	1	1
1	0	C_3'	C_2'	C_1'	C_0'
1	1	C_3	C_2	C_1	C_0

$S = ABI + \bar{A}B'I + \bar{A}\bar{B}\bar{I}$



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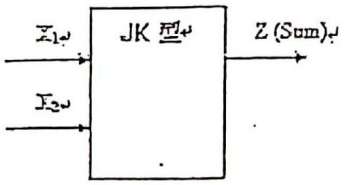
邏輯設計期末考

注意事項:State diagram、State table、電路圖(IC標示要清楚)

1. Design a serial adder (串列加法器) with a JK Flip-Flops and NOT /OR / AND gates. (20%)

   Hint: ($Z=X_1 \oplus X_2 \oplus Y$ Carry: $Y^+=X_1X_2+X_1Y+X_2Y$)

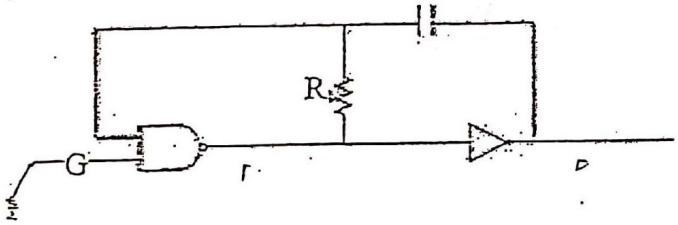


   EX: 101111 → 1+0 1+1 1+1

2. Design a synchronous counter which can giving the counting order *0, 3, 5, 1, 4, 6, 2*. Please use JK Flip-Flops. (15%)

3. Design a modulus-6 Johnson Counter. Please give the detail procedure and using D Flip-Flops. (15%)

4. For the circuit shown below is a clock generator. Please give the operation procedure and derive the clock's period. (20%)



5. Design a frequency divider which can provide a modul-7 divider. Please using D Flip-Flops. (15%)

6. Design an asynchronous counter which can provide the *0, 2, 4, 1, 3, 5* counting sequence. (15%)

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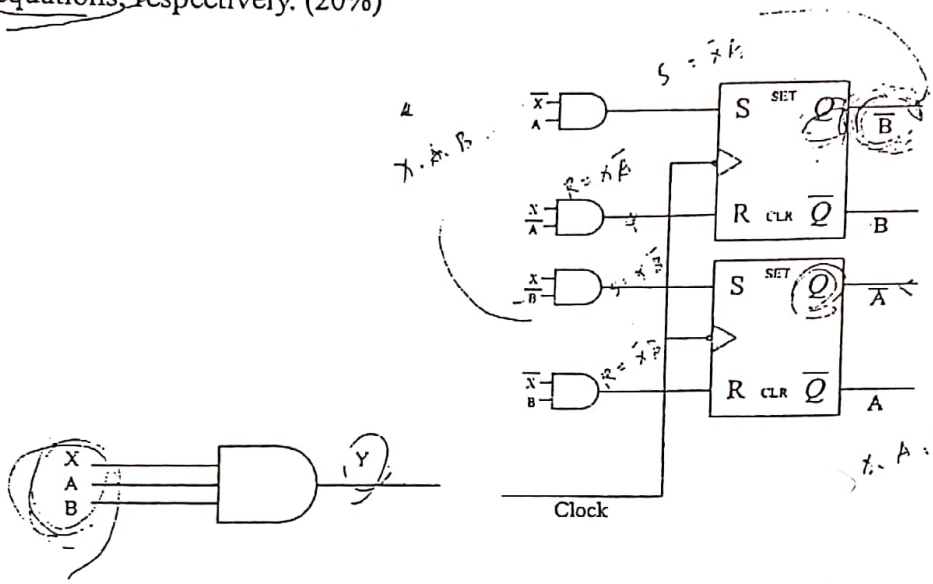
期末考 (9:00 ~ 11:00 Open Book)

1. Design the D flip-flop and T flip-flop by using JK flip-flop, respectively. Given the detail procedures you used. (需列出設計過程) (10%)

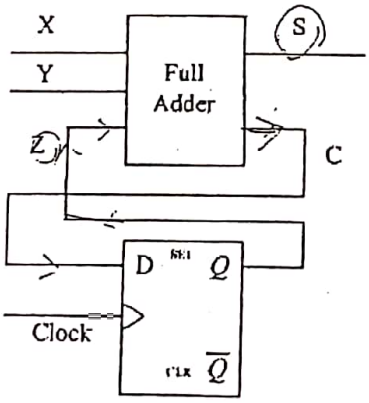
2. What is the difference between frequency division and binary counter? Give an example and explain your answer. (10%)

3. User 555 timers to implement 4 sec and 20 sec one-shots, respectively. (10%)

4. Following is a clocked sequential circuit; Show its state table, the state diagram, and the next state equations, respectively. (20%)



5. The full adder of following circuit receives two external inputs x and y; the third input z comes from the output of a D flip-flop. The carry output is transferred to the flip-flop every clock pulse. The external S output gives the sum of x, y and z. Obtain the state table and state diagram of the sequential circuit. (20%)



6. Use J-K flip-flop to design a 3-bit asynchronous counter which can count the sequence of 0 to 5. (15%)

7. Use J-K flip-flop to design a counter that has a repeated sequence of six states 0→1→2→4→5→6. (15%)

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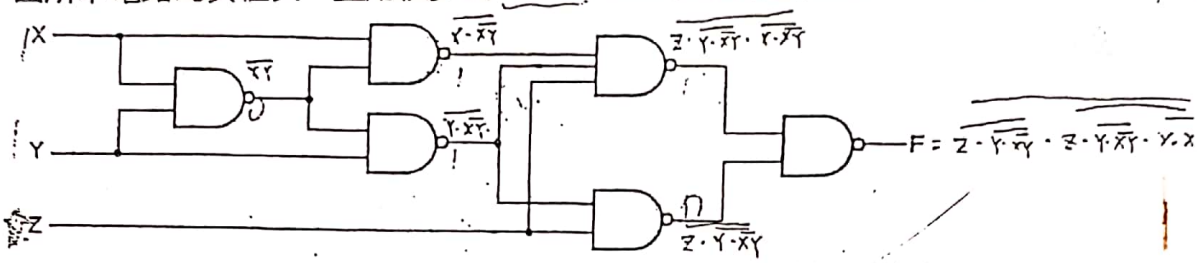
考試時間爲 120 分鐘

1. 求下圖所示電路的真值表，並用較少的 NAND Gate 畫出等價電路。(10%)



2. 試設計一組合電路，使其輸入爲一四位元數字，而其輸出爲該輸入數字的 2 的補數。(5%)

3. 試設計兩個超三碼表示之十進位數字加法器。下列所示的爲將兩個數字用一個四位元的二進位加完後所需要的修正：(15%)
   A. 進位輸出等於二進位加法器的進位。
   B. 若進位輸出=1，則加上 0011
   C. 若進位輸出=0，則加上 1101

4. 下列有三個布林函數定義出一個組合電路，試使用一個解碼器與額外的邏輯閘來設計此電路。(10%)

$$F_1 = \bar{X}\bar{Y} + XY\bar{Z}$$
$$F_2 = \bar{X} + Y$$
$$F_3 = XY + \bar{X}\bar{Y}$$

5. 試只用 NOR 閘繪製一個 2 對 4 線解碼的邏輯圖，並標出其致能輸入。(10%)

6. 試使用兩個 8 對 1 線多工器與一個 2 對 1 線多工器組成一個 16 對 1 線多工器，並使用標準的方塊圖符號。(10%)

7. 用一個雙重(Dual)4 對 1 線多工器製作一個全加器。(10%)

8. 用一個多工器製作下列布林函數。(10%)

$$F(A,B,C,D) = \sum m(0,3,5,6,8,9,14,15)$$

9. 試說明什麼是 PLD、GAL、PROM、PAL、PLA。(20%)