# Specification:

## Inputs:

A 3 digit binary input, X, Y, and Z with X is the most significant bit and Z is the least significant bit.

## Output:

A 7 digit binary output A, B, C, D, E, F, and G for 7 segment display correspondent to the input.

## Internal Operation:

A circuit to do the conversion in combinational logic.

# Formulation:

Out of 8, there are 6 possible inputs which are valid for displaying “ECE231-3-3”. So two combinations can be treated as don’t cares.

## Truth Table:

|  |  |  |
| --- | --- | --- |
| Display | X Y Z | A B C D E F G |
| 1 | 0 0 0 | 0 1 1 0 0 0 0 |
| 2 | 0 0 1 | 1 1 0 1 1 0 1 |
| 3 | 0 1 0 | 1 1 1 1 0 0 1 |
| C | 0 1 1 | 1 0 0 1 1 1 0 |
| E | 1 0 0 | 1 0 0 1 1 1 1 |
| - | 1 0 1 | 0 0 0 0 0 0 1 |
| X | 1 1 0 | X |
| X | 1 1 1 | X |

## K map:

For A

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | Y | |
| 0 | 1 | 1 | 1 |
| X | 1 | 0 | x | x |
|  | Z | |  |

A = X’Z + X’Y + XZ’

= X’Y + (XZ)

For B

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | Y | |
| 1 | 1 | 0 | 1 |
| X | 0 | 0 | x | x |
|  | Z | |  |

B = X’Y’ + X’Z’

= X’(Y’+Z’)

For C

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | Y | |
| 1 | 0 | 0 | 1 |
| X | 0 | 0 | x | x |
|  | Z | |  |

C = X’Z’

For D

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | Y | |
| 0 | 1 | 0 | 1 |
| X | 1 | 0 | x | x |
|  | Z | |  |

D = X’Z + X’Y + XZ’

= X’Y + (XZ)

For E

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | Y | |
| 0 | 1 | 1 | 0 |
| X | 1 | 0 | x | x |
|  | Z | |  |

E = X’Z + XZ’

= XZ

For F

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | Y | |
| 0 | 0 | 1 | 0 |
| X | 1 | 0 | x | x |
|  | Z | |  |

F = YZ + XZ’

For G

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | | Y | |
| 0 | 1 | 0 | 1 |
| X | 1 | 1 | x | x |
|  | Z | |  |

G = XY’ + Y’Z + YZ’

= XY’ + (YZ)

## Equations:

A = X’Y + (XZ)

B = X’(Y’+Z’)

C = X’Z’

D = X’Y + (XZ)

E = XZ

F = YZ + XZ’

G = XY’ + (YZ)

# Circuit Design:

