



# Arm® BSA Architecture Compliance Bare-metal

Version v1.2.0

## User Guide

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# Arm® BSA Architecture Compliance Bare-metal User Guide

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# 1. Overview to BSA ACS

This chapter provides an overview on Arm BSA ACS, the ACS design, and steps to customize the bare-metal code.

## 1.1 Abbreviations

The following table lists the abbreviations used in this document.

**Table 1-1: Abbreviations and expansions**

Abbreviation	Expansion
ACS	Architecture Compliance Suite
BSA	Base System Architecture
DMA	Direct Memory Access
ECAM	Enhanced Configuration Access Mechanism
GIC	Generic Interrupt Controller
IORT	Input Output Remapping Table
IOVIRT	Input Output Virtualization
ITS	Interrupt Translation Service
MMU	Memory Management Unit
MPIDR	Multiprocessor ID Register
MSI	Message-Signaled Interrupt
PAL	Platform Abstraction Layer
PCIe	Peripheral Component Interconnect Express
PE	Processing Element
PMU	Performance Monitoring Unit
RC	Root Complex
RP	Root Port
SoC	System on Chip
SMC	Secure Monitor Call
SMMU	System Memory Management Unit
UART	Universal Asynchronous Receiver and Transmitter
UEFI	Unified Extensible Firmware Interface
VAL	Validation Abstraction Layer

## 1.2 BSA ACS

Arm specifies a hardware system architecture which is based on Arm 64-bit architecture that server system software such as operating systems, hypervisors, and firmware can rely on. This ensures

standard system architecture to enable a suitably built single OS image to run on all the hardware compliant with this specification.

Arm provides the BSA Architecture Compliance Suite (ACS) which contains self-checking portable C-based test cases to verify the compliance of hardware platforms to Base System Architecture (BSA).

For more information on Arm BSA ACS, see the [README](#).

## 1.3 ACS design

The ACS is designed in a layered architecture that consists of the following components:

- Platform Abstraction Layer (PAL) is a C-based, Arm-defined API that you can implement. It abstracts features whose implementation varies from one target system to another. Each test platform requires a PAL implementation of its own. PAL APIs are meant for the compliance test to reach or use other abstractions in the test platform such as the UEFI infrastructure and bare-metal abstraction.
  - For each component, PAL implementation must populate a data structure which involves supplying SoC-specific information such as base addresses, IRQ numbers, capabilities of PE, PCIe, RC, SMMU, DMA, and others.
  - PAL also uses client drivers underneath to retrieve certain device-specific information and to configure the devices.
- Validation Abstraction Layer (VAL) provides an abstraction over PAL and does not change based on the platform. This layer uses PAL layer to achieve a certain functionality. The following example achieves read memory functionality.

```
val_PCIE_read_cfg -> pal_PCIE_read_cfg
```

- Test pool is a layer which contains a list of test cases implemented for each component.
- Application is the top-level layer which allocates memory for component-specific tables and executes the test cases for each component.

The ACS test components are classified as follows:

- PE
- GIC
- PCIe
- Exerciser
- I/O virtualization
- SMMU
- Timer
- Watchdog
- Power-wake semantics

- Peripherals
- Memory

## 1.4 Boot framework

The bootwrapper is a simple implementation of a boot loader to boot up the system and transition to the ACS where specific set of tests are run.

The bootwrapper initializes the hardware and loads the ACS into the memory, allowing the system to start up, independent of UEFI and execute ACS tests automatically. This further reduces porting complexity for the partners and provides them with off-the-shelf system Init code.

### 1.4.1 Boot process and boot flow

The boot process is the sequence of operations that occurs when a computer system is powered-on or restarted, allowing it to transition from a power-off state to an operational state, where the operating system can run.

A boot loader, also known as a boot manager, is a piece of software responsible for initiating the boot process and loading the operating system into memory. Boot loader is located in firmware or a dedicated boot partition and is executed when the system is powered-on or restarted.

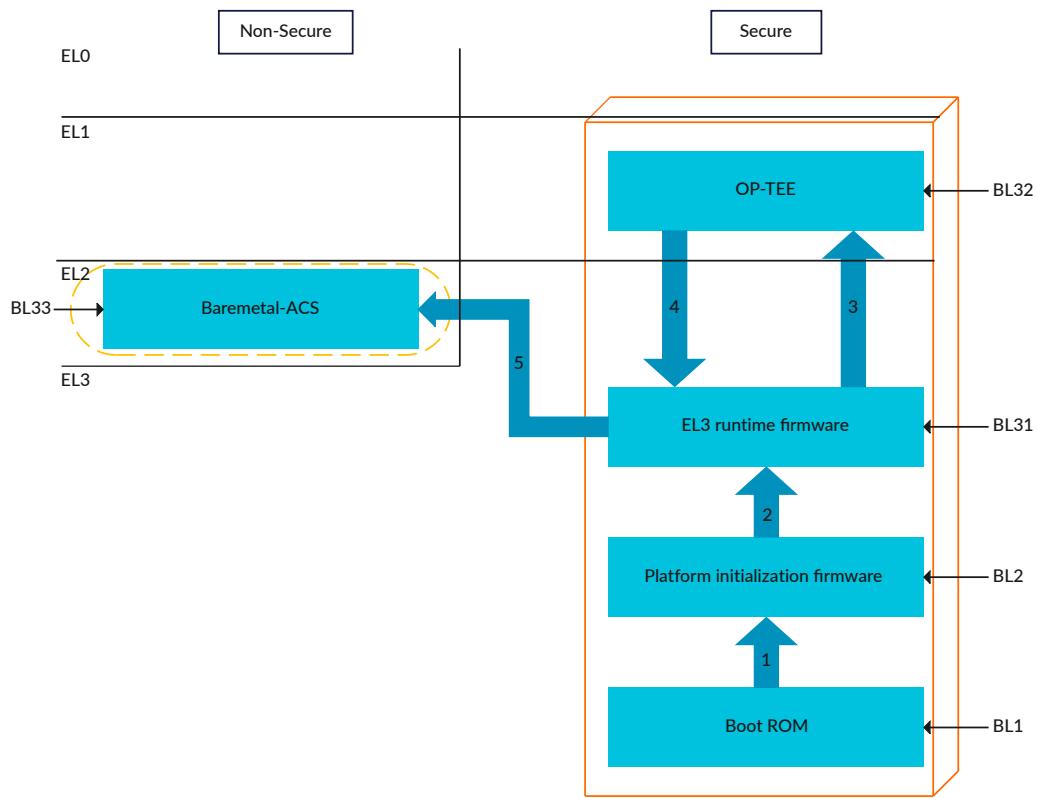
The cold boot path in this implementation of TF-A depends on the execution state. For AArch64, it is divided into five steps (in the order of execution):

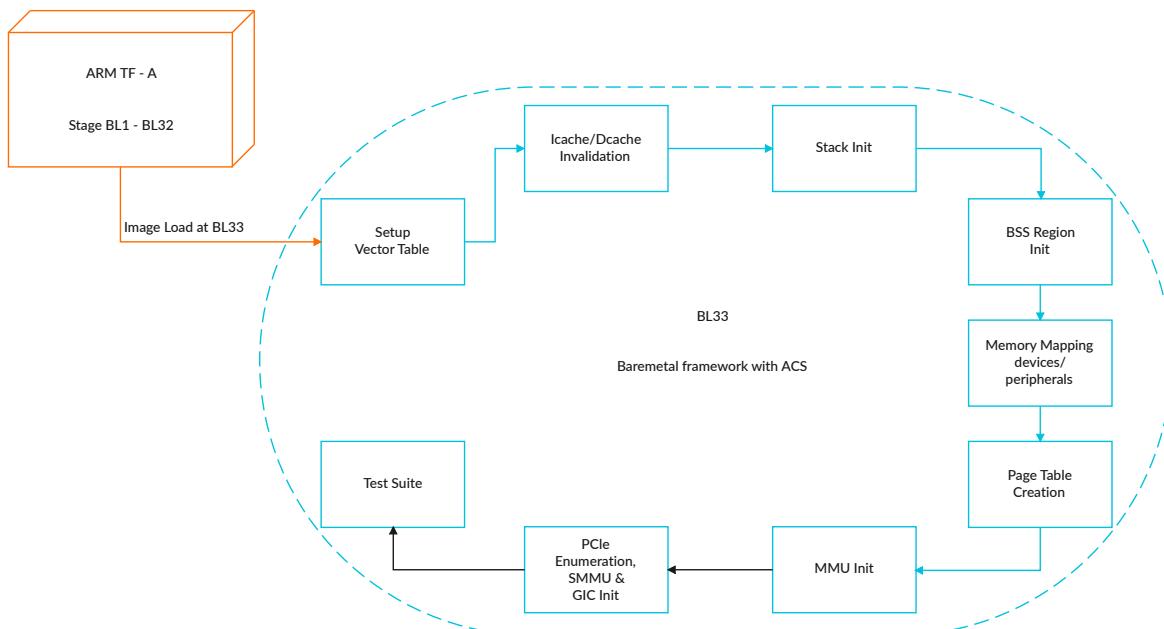
- Boot Loader stage 1 (BL1) - AP Trusted ROM
- Boot Loader stage 2 (BL2) - Trusted Boot Firmware
- Boot Loader stage 3-1 (BL31) - EL3 Run time Software
- Boot Loader stage 3-2 (BL32) - Secure-EL1 Payload (optional)
- Boot Loader stage 3-3 (BL33) - Non-trusted Firmware

### 1.4.2 Boot framework for Bare-metal

With the introduction of bootwrapper, the UEFI layer is bypassed in the ACS boot flow. BSA ACS with bootwrapper runs as non-trusted firmware at BL33.

The following figures show the overview of System boot flow and ACS boot flow in a system environment.

**Figure 1-1: System boot flow**

**Figure 1-2: ACS Boot framework flow**

## 1.5 Steps to customize bare-metal

The following are the steps to customize the bare-metal code for different platforms.



The `pal_baremetal` reference code is located in [baremetal](#).

**Note**

1. Run the command `./generate.py <platform_name>`.
2. Running the command creates the folder with the platform name and the PAL APIs under `target/<platform_name>/src/pal_bsa.c` to be filled.
3. Port all the required APIs. For more details on the list of APIs, see the [Porting requirements](#).
4. Modify the files `target/<platform_name>/include/platform_override_fvp.h` and `target/<platform_name>/include/platform_image_def.h` with platform-specific information. For more details on sample implementation, see the [Execution of BSA ACS](#).

## 1.5.1 Test suites

The following table lists the bare-metal test suites for each test implementation.

**Table 1-2: Bare-metal components**

Test suites	Files
PE	pal_pe.c
GIC	pal_gic.c
PCIe	pal_pcie.c, pal_pcie_enumeration.c
Exerciser	pal_exerciser.c
IOVIRT	pal_iovirt.c
SMMU	pal_smmu.c
Timer and Watchdog	pal_timer_wd.c
Peripherals (UART and Memory)	pal_peripherals.c
DMA	pal_dma.c
Miscellaneous	pal_misc.c



PAL implementation requires porting when the underlying platform design changes.

Note

## 2. Execution of BSA ACS

This chapter provides information on the execution of the BSA ACS on a full-chip SoC emulation environment.

### 2.1 SoC emulation environment

Executing BSA ACS on a full-chip emulation environment requires implementation of PAL. This involves providing a collection of SoC-specific information such as capabilities, base addresses, IRQ numbers to the test logic.

In Unified Extensible Firmware Interface (UEFI) base systems, all the static information is present in UEFI tables and in U-Boot base systems, all the static information is present in Device Tree. The PAL implementation which is based on UEFI and U-Boot, uses the generated header file for populating data structures. For a bare-metal system, this information must be supplied in a tabular format which becomes easy for PAL API implementation.

#### 2.1.1 PE

This section provides information on the number of PEs in the system.

##### PE-specific information

Tests contain comparison of Multiprocessor ID Register (MPIDR) values with actual values read from register. Such interrupts are generated for the Performance Monitoring Unit (PMU) lines and tested.

##### PLATFORM\_OVERRIDE\_PEx\_MPIDR:

MPIDR register value represents the xth PE hierarchy (cluster, core).

##### PLATFORM\_OVERRIDE\_PEx\_INDEX:

Represents the xth PE.

##### PLATFORM\_OVERRIDE\_PEx\_PMU\_GSIV:

PMU interrupt number for xth PE.

A platform with eight PEs is populated as follows:

```
#define PLATFORM_OVERRIDE_PE_CNT          0x8  
  
#define PLATFORM_OVERRIDE_PEO_INDEX        0x0  
#define PLATFORM_OVERRIDE_PEO_MPIDR        0x0  
#define PLATFORM_OVERRIDE_PEO_PMU_GSIV      0x17  
  
#define PLATFORM_OVERRIDE_PE1_INDEX        0x1  
#define PLATFORM_OVERRIDE_PE1_MPIDR        0x100  
#define PLATFORM_OVERRIDE_PE1_PMU_GSIV      0x17  
  
#define PLATFORM_OVERRIDE_PE2_INDEX        0x2
```

```
#define PLATFORM_OVERRIDE_PE2_MPIDR 0x200
#define PLATFORM_OVERRIDE_PE2_PMU_GSIV 0x17

#define PLATFORM_OVERRIDE_PE3_INDEX 0x3
#define PLATFORM_OVERRIDE_PE3_MPIDR 0x300
#define PLATFORM_OVERRIDE_PE3_PMU_GSIV 0x17

#define PLATFORM_OVERRIDE_PE4_INDEX 0x4
#define PLATFORM_OVERRIDE_PE4_MPIDR 0x10000
#define PLATFORM_OVERRIDE_PE4_PMU_GSIV 0x17

#define PLATFORM_OVERRIDE_PE5_INDEX 0x5
#define PLATFORM_OVERRIDE_PE5_MPIDR 0x10100
#define PLATFORM_OVERRIDE_PE5_PMU_GSIV 0x17

#define PLATFORM_OVERRIDE_PE6_INDEX 0x6
#define PLATFORM_OVERRIDE_PE6_MPIDR 0x10200
#define PLATFORM_OVERRIDE_PE6_PMU_GSIV 0x17

#define PLATFORM_OVERRIDE_PE7_INDEX 0x7
#define PLATFORM_OVERRIDE_PE7_MPIDR 0x10300
#define PLATFORM_OVERRIDE_PE7_PMU_GSIV 0x17
```

Header file representation:

```
typedef struct {
    uint32_t num_of_pe;
} PE_INFO_HDR;

/**
@brief structure instance for PE entry
**/

typedef struct {
    uint32_t pe_num;                                /* PE Index */
    uint32_t attr;                                  /* PE attributes */
    uint64_t mpidr;                                 /* PE MPIDR */
    uint32_t pmu_gsiv;                             /* PMU Interrupt */
    uint32_t gmain_gsiv;                           /* GIC Maintenance Interrupt */
    uint32_t acpi_proc_uid;                         /* ACPI Processor UID */
    uint32_t level_1_res[MAX_L1_CACHE_RES];        /* index of level 1 cache(s) in
    cache_info_table */
    uint32_t trbe_interrupt;                        /* TRBE Interrupt */
} PE_INFO_ENTRY;

typedef struct {
    PE_INFO_HDR header;
    PE_INFO_ENTRY pe_info[];
} PE_INFO_TABLE;
```

## SMBIOS-specific information

The parameters required for SMBIOS with reference values are as follows:

```
#define PLATFORM_OVERRIDE_SMBIOS_SLOT_COUNT 0x1
#define PLATFROM_OVERRIDE_SMBIOS_SLOT0_FAMILY 0x102
#define PLATFROM_OVERRIDE_SMBIOS_SLOT0_CORE_COUNT 16
```

Header file representation:

```
typedef struct {
    uint16_t processor_family;
    uint16_t core_count;
```

```

} PE_SMBIOS_TYPE4_INFO;

typedef struct {
    uint32_t slot_count;
    PE_SMBIOS_TYPE4_INFO type4_info[];
} PE_SMBIOS_PROCESSOR_INFO_TABLE;

```

### 2.1.1.1 MMU Configuration

This section provides information on the MMU for the PE MMU.

The parameters required for the PE MMU are populated as follows:

```

#define PLATFORM_PAGE_SIZE      0x1000
#define PLATFORM_OVERRIDE_MMU_PGT_IAS   48
#define PLATFORM_OVERRIDE_MMU_PGT_OAS   48

```

### 2.1.2 PCIe

This section provides information on the number of Peripheral Component Interconnect express (PCIe) root ports and the information required for PCIe enumeration.

```

#define PLATFORM_OVERRIDE_PCIE_ECAM0_HB_COUNT 1
#define PLATFORM_OVERRIDE_PCIE_ECAM0_SEG_NUM      0x0
#define PLATFORM_OVERRIDE_PCIE_ECAM0_START_BUS_NUM 0x0
#define PLATFORM_OVERRIDE_PCIE_ECAM0_END_BUS_NUM   0x8
#define PLATFORM_OVERRIDE_PCIE_ECAM0_EP_BAR64     0x4000100000
#define PLATFORM_OVERRIDE_PCIE_ECAM0_RP_BAR64     0x4000000000
#define PLATFORM_OVERRIDE_PCIE_ECAM0_EP_NPBAR32   0x60000000
#define PLATFORM_OVERRIDE_PCIE_ECAM0_EP_PBAR32    0x60600000
#define PLATFORM_OVERRIDE_PCIE_ECAM0_RP_BAR32    0x60850000

```

#### **PLATFORM\_OVERRIDE\_PCIE\_ECAMx\_EP\_BAR64:**

The address required for 64-bit Prefetchable Memory Base for an PCIe End Point.

#### **PLATFORM\_OVERRIDE\_PCIE\_ECAMx\_RP\_BAR64:**

The address required for 64-bit Prefetchable Memory Base for PCIe Type 1 devices.

#### **PLATFORM\_OVERRIDE\_PCIE\_ECAMx\_EP\_NPBAR32:**

The address required for 32-bit Non-Prefetchable Memory Base for an PCIe End Point.

#### **PLATFORM\_OVERRIDE\_PCIE\_ECAMx\_EP\_PBAR32:**

The address required for 32-bit Prefetchable Memory Base for an PCIe End Point.

#### **PLATFORM\_OVERRIDE\_PCIE\_ECAMx\_RP\_BAR32:**

The address required for 32-bit Memory Base for a PCIe Type 1 devices.

Parameters required for the PCIe enumeration for a platform is populated as follows:

#### **PLATFORM\_OVERRIDE\_NUM\_ECAM:**

Represents the number of Enhanced Configuration Access Mechanism (ECAM) regions in the system.

**PLATFORM\_MAX\_HB\_COUNT:**

Represents the maximum number of Host bridges in the system..

**PLATFORM\_OVERRIDE\_PCIE\_ECAM\_BASE\_ADDR\_x:**

ECAM base address: ECAM maps PCIe configuration space to a memory address. The memory address to the current configuration space must be provided here.

**PLATFORM\_OVERRIDE\_PCIE\_SEGMENT\_GRP\_NUM\_x:**

Segment number of the xth ECAM region.

**PLATFORM\_OVERRIDE\_PCIE\_START\_BUS\_NUM\_x:**

Starting bus number of the xth ECAM region.

**PLATFORM\_OVERRIDE\_PCIE\_END\_BUS\_NUM\_x:**

Ending bus number of the xth ECAM region.

A platform with one ECAM region is populated as follows:

```
/* PCIE platform config parameters */
#define PLATFORM_OVERRIDE_NUM_ECAM 1

/* Platform config parameters for ECAM_0 */
#define PLATFORM_OVERRIDE_PCIE_ECAM_BASE_ADDR_0 0x60000000
#define PLATFORM_OVERRIDE_PCIE_SEGMENT_GRP_NUM_0 0x0
#define PLATFORM_OVERRIDE_PCIE_START_BUS_NUM_0 0x0
#define PLATFORM_OVERRIDE_PCIE_END_BUS_NUM_0 0xFF
```

Header file representation:

```
typedef struct {
    uint64_t ecam_base; // ECAM Base address
    uint32_t segment_num; // Segment number of this ECAM
    uint32_t start_bus_num; // Start Bus number for this ecam space
    uint32_t end_bus_num; // Last Bus number
} PCIE_INFO_BLOCK;

typedef struct {
    uint32_t num_entries;
    PCIE_INFO_BLOCK block[];
} PCIE_INFO_TABLE;
```

### 2.1.2.1 PCIe device hierarchy table

This hierarchy table is used to obtain platform-specific support such as DMA, P2P and so on.

Parameters to be populated for each PCIe device is as follows:

PLATFORM_PCIE_DEVx_CLASSCODE	0x6040000
PLATFORM_PCIE_DEVx_VENDOR_ID	0x13B5
PLATFORM_PCIE_DEVx_DEV_ID	0xDEF
PLATFORM_PCIE_DEVx_BUS_NUM	0
PLATFORM_PCIE_DEVx_DEV_NUM	1
PLATFORM_PCIE_DEVx_FUNC_NUM	0
PLATFORM_PCIE_DEVx_SEG_NUM	0
PLATFORM_PCIE_DEVx_DMA_SUPPORT	0
PLATFORM_PCIE_DEVx_DMA_COHERENT	0

```
PLATFORM_PCIE_DEVx_P2P_SUPPORT    1
PLATFORM_PCIE_DEVx_DMA_64BIT      0
PLATFORM_PCIE_DEVx_BEHIND_SMMU     1
PLATFORM_PCIE_DEVx_ATC_SUPPORT    0
```

Header file representation:

```
typedef struct {
    uint64_t class_code;
    uint32_t device_id;
    uint32_t vendor_id;
    uint32_t bus;
    uint32_t dev;
    uint32_t func;
    uint32_t seg;
    uint32_t dma_support;
    uint32_t dma_coherent;
    uint32_t p2p_support;
    uint32_t dma_64bit;
    uint32_t behind_smmu;
    uint32_t atc_present;
    PERIPHERAL_IRQ_MAP irq_map;
} PCIE_READ_BLOCK;
```

## 2.1.3 DMA

This section provides the configuration options for Direct Memory Access (DMA) controller-based tests. Additionally, it describes the parameters for the number of DMA bus Requesters, and DMA Requester attributes that can be customized.

### 2.1.3.1 Number of DMA controllers

Header file representation:

```
#define PLATFORM_OVERRIDE_DMA_CNT 0
```

#### **PLATFORM\_OVERRIDE\_DMA\_CNT:**

Represents the number of DMA controllers in the system.

### 2.1.3.2 DMA Requester attributes

Header file representation:

```
typedef struct {
    DMA_INFO_TYPE_e type;
    void           *target;
    void           *port;
    void           *host;
    uint32_t        flags;
} DMA_INFO_BLOCK;
```

The actual information stored in the above pointers are implementation-specific.

## 2.1.4 SMMU and device tests

This section provides an overview on SMMU and the device tests. It also provides information on the number of IOVIRT nodes, SMMUs, RC, Named component, PMCG, ITS blocks, I/O virtualization node-specific information, SMMU node-specific information, RC-specific information, and I/O virtual address mapping.

### 2.1.4.1 Number of IOVIRT Nodes

Parameters to be filled are:

```
#define IORT_NODE_COUNT 0x13
```

#### IORT\_NODE\_COUNT:

Represents the total number of Root Complex (RC), SMMU, ITS, PMCG, and other nodes represented in IORT structure.

### 2.1.4.2 Number of SMMUs

Parameters to be filled are:

```
#define IOVIRT_SMMUV3_COUNT 5
```

```
#define IOVIRT_SMMUV2_COUNT 0
```

#### SMMU\_COUNT:

Represents the number of SMMUs in the system.

### 2.1.4.3 Number of RCs

Parameters to be filled are:

```
#define RC_COUNT 0x1
```

#### RC\_COUNT:

Represents the number of RCs present in the system.

#### 2.1.4.4 Number of PMCGs

Parameters to be filled are:

```
#define PMCG_COUNT 0x1
```

**PMCG\_COUNT:**

Represents the number of Performance Monitor Counter Groups (PMCGs) present in the system.

#### 2.1.4.5 Number of ITS blocks

Parameters to be filled are:

```
#define IOVIRT_ITS_COUNT 0x1
```

**IOVIRT\_ITS\_COUNT:**

Represents the number of Interrupt Translation Service (ITS) nodes in the system.

#### 2.1.4.6 I/O virtualization node-specific information

Header file representation:

```
typedef struct {
    uint32_t type;
    uint32_t num_data_map;
    NODE_DATA data;
    uint32_t flags;
    NODE_DATA_MAP data_map[];
} IOVIRT_BLOCK;

typedef union {
    char name[MAX_NAMED_COMP_LENGTH];
    IOVIRT_RC_INFO_BLOCK rc;
    IOVIRT_PMCG_INFO_BLOCK pmcg;
    uint32_t its_count;
    SMMU_INFO_BLOCK smmu;
} NODE_DATA;
```

#### 2.1.4.7 SMMU node-specific information

Header file representation:

```
typedef struct {
    uint32_t arch_major_rev;    ///< Version 1 or 2 or 3
    uint64_t base;             ///< SMMU controller base address
} SMMU_INFO_BLOCK;
```

**IOVIRT\_SMMUV3\_BASE\_ADDRESS:**

Represents the SMMU base address in the system.

### 2.1.4.8 Root Complex node specific information

Header file representation:

```
typedef struct {
    uint32_t segment;
    uint32_t ats_attr;
    uint32_t cca;           //Cache Coherency Attribute
    uint64_t smmu_base;
} IOVIRT_RC_INFO_BLOCK;
```

### 2.1.4.9 PMCG node-specific information

Header file representation:

```
typedef struct {
    uint64_t base;
    uint32_t overflow_gsiv;
    uint32_t node_ref;
} IOVIRT_PMCG_INFO_BLOCK;
```

### 2.1.4.10 I/O virtual address mapping

Header file representation:

```
typedef struct {
    uint32_t input_base;
    uint32_t id_count;
    uint32_t output_base;
    uint32_t output_ref;
} ID_MAP;
```

## 2.1.5 GIC

This section provides the parameters for Generic Interrupt Controller (GIC) specific test.

### GIC-specific tests

Parameters to be filled are:

```
#define PLATFORM_OVERRIDE_GICD_COUNT      0x1
#define PLATFORM_OVERRIDE_GICRD_COUNT       0x1
#define PLATFORM_OVERRIDE_GICITS_COUNT     0x1
#define PLATFORM_OVERRIDE_GICH_COUNT       0x1
#define PLATFORM_OVERRIDE_GICMSIFRAME_COUNT 0x0
#define PLATFORM_OVERRIDE_GICC_TYPE        0x1000
#define PLATFORM_OVERRIDE_GICD_TYPE        0x1001
#define PLATFORM_OVERRIDE_GICC_GICRD_TYPE   0x1002
#define PLATFORM_OVERRIDE_GICR_GICRD_TYPE   0x1003
#define PLATFORM_OVERRIDE_GICITS_TYPE      0x1004
#define PLATFORM_OVERRIDE_GICMSIFRAME_TYPE  0x1005
#define PLATFORM_OVERRIDE_GICH_TYPE        0x1006
#define PLATFORM_OVERRIDE_GICC_BASE        0x30000000
#define PLATFORM_OVERRIDE_GICD_BASE        0x30000000
```

```
#define PLATFORM_OVERRIDE_GICRD_BASE 0x300C0000
#define PLATFORM_OVERRIDE_GICITS_BASE 0x30040000
#define PLATFORM_OVERRIDE_GICH_BASE 0x2C010000
#define PLATFORM_OVERRIDE_GICITS_ID 0
#define PLATFORM_OVERRIDE_GICIRD_LENGTH (0x20000*8)
```

Header file representation:

```
typedef struct {
    uint32_t gic_version;
    uint32_t num_gicc;
    uint32_t num_gicd;
    uint32_t num_gicrd;
    uint32_t num_gicits;
    uint32_t num_gich;
    uint32_t num_msiframes;
    uint32_t gicc_type;
    uint32_t gicd_type;
    uint32_t gicrd_type;
    uint32_t gicrd_length;
    uint32_t gicits_type;
    uint64_t gicc_base[PLATFORM_OVERRIDE_GICC_COUNT];
    uint64_t gicd_base[PLATFORM_OVERRIDE_GICD_COUNT];
    uint64_t gicrd_base[PLATFORM_OVERRIDE_GICRD_COUNT];
    uint64_t gicits_base[PLATFORM_OVERRIDE_GICITS_COUNT];
    uint64_t gicits_id[PLATFORM_OVERRIDE_GICITS_COUNT];
    uint64_t gich_base[PLATFORM_OVERRIDE_GICH_COUNT];
    uint64_t gicmsiframe_base[PLATFORM_OVERRIDE_GICMSIFRAME_COUNT];
    uint64_t gicmsiframe_id[PLATFORM_OVERRIDE_GICMSIFRAME_COUNT];
    uint32_t gicmsiframe_flags[PLATFORM_OVERRIDE_GICMSIFRAME_COUNT];
    uint32_t gicmsiframe_spi_count[PLATFORM_OVERRIDE_GICMSIFRAME_COUNT];
    uint32_t gicmsiframe_spi_base[PLATFORM_OVERRIDE_GICMSIFRAME_COUNT];
} PLATFORM_OVERRIDE_GIC_INFO_TABLE;
```

## 2.1.6 Timer

This section provides the parameters for timer-specific tests.

### 2.1.6.1 Timer information

Parameters to be filled are:

```
#define PLATFORM_OVERRIDE_PLATFORM_TIMER_COUNT 0x2
#define PLATFORM_OVERRIDE_S_EL1_TIMER_GSIV 0x1D
#define PLATFORM_OVERRIDE_NS_EL1_TIMER_GSIV 0x1E
#define PLATFORM_OVERRIDE_NS_EL2_TIMER_GSIV 0x1A
#define PLATFORM_OVERRIDE_VIRTUAL_TIMER_GSIV 0x1B
#define PLATFORM_OVERRIDE_EL2_VIR_TIMER_GSIV 28
```

Header file representation:

```
typedef struct {
    uint32_t s_el1_timer_flag;
    uint32_t ns_el1_timer_flag;
    uint32_t el2_timer_flag;
    uint32_t el2_virt_timer_flag;
    uint32_t s_el1_timer_gsiv;
    uint32_t ns_el1_timer_gsiv;
```

```

uint32_t el2_timer_gsiv;
uint32_t virtual_timer_flag;
uint32_t virtual_timer_gsiv;
uint32_t el2_virt_timer_gsiv;
uint32_t num_platform_timer;
uint32_t num_watchdog;
uint32_t sys_timer_status;
}TIMER_INFO_HDR;

typedef struct {
uint32_t type;
uint32_t timer_count;
uint64_t block_cntl_base;
uint8_t frame_num[8];
uint64_t GtCntBase[8];
uint64_t GtCntEl0Base[8];
uint32_t gsiv[8];
uint32_t virt_gsiv[8];
uint32_t flags[8];
}TIMER_INFO_GTBLOCK;

typedef struct {
TIMER_INFO_HDR header;
TIMER_INFO_GTBLOCK gt_info[];
}TIMER_INFO_TABLE;

```

## 2.1.7 Watchdog timer

This section provides the parameters for the number of watchdog timer tests and watchdog information.

Parameters to be filled are:

```
#define PLATFORM_OVERRIDE_WD_TIMER_COUNT 2
```

### 2.1.7.1 Watchdog information

The following is the list of watchdog timers present in the system:

- Watchdog timer number
- Control base
- Refresh base
- Interrupt number
- Flags

Header file representation:

```

typedef struct {
uint64_t wd_ctrl_base;    ///< Watchdog Control Register Frame
uint64_t wd_refresh_base; // Watchdog Refresh Register Frame
uint32_t wd_gsiv;        ///< Watchdog Interrupt ID
uint32_t wd_flags;
}WD_INFO_BLOCK;

```

## 2.1.8 Memory

This section provides information on the memory map in the system.

### **PLATFORM\_OVERRIDE\_MEMORY\_ENTRY\_COUNT:**

Represents the number of memory range entries.

### **PLATFORM\_OVERRIDE\_MEMORY\_ENTRYx\_PHY\_ADDR:**

Represents the physical address of the xth memory entry.

### **PLATFORM\_OVERRIDE\_MEMORY\_ENTRYx\_VIRT\_ADDR:**

Represents the virtual address of the xth memory entry.

### **PLATFORM\_OVERRIDE\_MEMORY\_ENTRYx\_SIZE:**

Represents the size of the xth memory entry.

### **PLATFORM\_OVERRIDE\_MEMORY\_ENTRYx\_TYPE:**

Represents the type of the xth memory entry.

The following is an example for memory map.

#define PLATFORM_OVERRIDE_MEMORY_ENTRY_COUNT	0x4
#define PLATFORM_OVERRIDE_MEMORY_ENTRY0_PHY_ADDR	0xC000000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY0_VIRT_ADDR	0xC000000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY0_SIZE	0x4000000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY0_TYPE	MEMORY_TYPE_DEVICE
#define PLATFORM_OVERRIDE_MEMORY_ENTRY1_PHY_ADDR	0x10000000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY1_VIRT_ADDR	0x10000000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY1_SIZE	0xC170000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY1_TYPE	MEMORY_TYPE_NOT_POPULATED
#define PLATFORM_OVERRIDE_MEMORY_ENTRY2_PHY_ADDR	0xFF600000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY2_VIRT_ADDR	0xFF600000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY2_SIZE	0x10000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY2_TYPE	MEMORY_TYPE_RESERVED
#define PLATFORM_OVERRIDE_MEMORY_ENTRY3_PHY_ADDR	0x80000000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY3_VIRT_ADDR	0x80000000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY3_SIZE	0x7F000000
#define PLATFORM_OVERRIDE_MEMORY_ENTRY3_TYPE	MEMORY_TYPE_NORMAL

Header file representation:

```
typedef struct {
    MEM_INFO_TYPE_e type;
    uint64_t phy_addr;
    uint64_t virt_addr;
    uint64_t size;
    uint64_t flags; //To Indicate Cacheability etc..
}MEM_INFO_BLOCK;
```

## 2.1.9 Peripherals

This section provides information on the peripherals in the system.

Parameters to be filled are:

```
#define PLATFORM_OVERRIDE_PERIPHERAL_COUNT 3 //UART + USB + SATA
#define UART_ADDRESS 0xF98DFE18
#define BASE_ADDRESS_ADDRESS_SPACE_ID 0x0
#define BASE_ADDRESS_REGISTER_BIT_WIDTH 0x20
#define BASE_ADDRESS_REGISTER_BIT_OFFSET 0x0
#define BASE_ADDRESS_ADDRESS_SIZE 0x3
#define BASE_ADDRESS_ADDRESS 0x2A400000
#define UART_BAUD_RATE 0x7
#define UART_BAUD_RATE_BPS 115200
#define UART_CLK_RATE_HZ 48000000
#define UART_INTERRUPT_TYPE 8
#define UART_IRQ 0
#define UART_GLOBAL_SYSTEM_INTERRUPT 0x70
#define UART_PCI_DEVICE_ID 0xFFFF
#define UART_PCI_VENDOR_ID 0xFFFF
#define UART_PCI_BUS_NUMBER 0x0
#define UART_PCI_DEV_NUMBER 0x0
#define UART_PCI_FUNC_NUMBER 0x0
#define UART_PCI_FLAGS 0x0
#define UART_PCI_SEGMENT 0x0
```



**Note** Ensure that the BASE\_ADDRESS\_ADDRESS, UART\_BAUD\_RATE\_BPS, and UART\_CLK\_RATE\_HZ are configured properly to get PL011 UART prints on the console.

## 2.2 Bare-metal Boot

This section provides information on the Bare-metal boot requirements of the system.

The following system-specific definitions must be filled to load bootable image.

Parameters to be filled are:

```
#define PLATFORM_OVERRIDE_WORLD_IMAGE_SIZE 0x4000000
#define PLATFORM_MEMORY_POOL_SIZE (250 * 100000)
#define PLATFORM_SHARED_MEMORY_REGION 0x100000
#define PLATFORM_NORMAL_WORLD_IMAGE_BASE 0xE0000000
```

For more information on how to run BSA ACS with bootwrapper code, see the [README](#).



**Note** PLATFORM\_NORMAL\_WORLD\_IMAGE\_BASE is the entry point to BL33.

# 3. Porting requirements

This chapter provides information on different PAL APIs in PE, GIC, timer, IOVIRT, PCIe, SMMU, peripheral, DMA, exerciser, and other miscellaneous APIs.

## 3.1 PAL implementation

PAL is a C-based, Arm-defined API that you can implement. Each test platform requires a PAL implementation of its own.

The bare-metal reference code provides a reference implementation for a subset of APIs. Additional code must be implemented to match the target SoC implementation under the tests.

---

There are two implementation types for the PAL APIs and are classified in the following tables:



- Yes: indicates that the implementation of this API is already present. Since the values are platform-specific, it must be taken from the platform configuration file.
  - Platform-specific: you must implement all the APIs that are marked as platform-specific.
- 

### 3.1.1 PE

The following table lists the different types of APIs in PE.

**Table 3-1: PE APIs and their details**

API name	Function prototype	Implementation
create_info_table	<code>void pal_pe_create_info_table(PE_INFO_TABLE *PeTable);</code>	Yes
call_smc	<code>void pal_pe_call_smc(ARM_SMC_ARGS *args);</code>	Yes
execute_payload	<code>void pal_pe_execute_payload(ARM_SMC_ARGS *args);</code>	Yes
update_elr	<code>void pal_pe_update_elr(void *context, uint64_t offset);</code>	Platform-specific
get_esr	<code>uint64_t pal_pe_get_esr(void *context);</code>	Platform-specific
data_cache_ops_by_va	<code>void pal_pe_data_cache_ops_by_va(uint64_t addr, uint32_t type);</code>	Yes
get_far	<code>uint64_t pal_pe_get_far(void *context);</code>	Platform-specific
install_esr	<code>uint32_t pal_pe_install_esr(uint32_t exception_type, void(*esr)(uint64_t, void *));</code>	Platform-specific
get_num	<code>uint32_t pal_pe_get_num();</code>	Yes

API name	Function prototype	Implementation
create_info_table	void pal_smbios_create_info_table(PE_SMBIOS_PROCESSOR_INFO_TABLE *SmbiosTable)	Yes
psci_get_conduit	uint32_t pal_psci_get_conduit(void)	Platform-specific

### 3.1.2 GIC

The following table lists the different types of APIs in GIC.

**Table 3-2: GIC APIs and their details**

API name	Function prototype	Implementation
create_info_table	void pal_gic_create_info_table(GIC_INFO_TABLE* gic_info_table);	Yes
install_isr	uint32_t pal_gic_install_isr(uint32_t int_id, void(*isr)(void));	Platform-specific
end_of_interrupt	uint32_t pal_gic_end_of_interrupt(uint32_t int_id);	Platform-specific
request_irq	uint32_t pal_gic_request_irq(unsigned int irq_num, unsigned int mapped_irq_num, void *isr);	Platform-specific
free_irq	void pal_gic_free_irq(unsigned int irq_num, unsigned int mapped_irq_num);	Platform-specific
set_intr_trigger	uint32_t pal_gic_set_intr_trigger(uint32_t int_id, INTR_TRIGGER_INFO_TYPE etrigger_type);	Platform-specific
get_num_nongic_ctrl	uint32_t pal_get_num_nongic_ctrl(void);	Platform-specific

### 3.1.3 Timer

The following table lists the different types of APIs in timer.

**Table 3-3: Timer APIs and their details**

API name	Function prototype	Implementation
create_info_table	void pal_timer_create_info_table(TIMER_INFO_TABLE *timer_info_table);	Yes
wd_create_info_table	void pal_wd_create_info_table(WD_INFO_TABLE *wd_table);	Yes
get_counter_frequency	uint64_t pal_timer_get_counter_frequency(void);	Yes

### 3.1.4 IOVIRT

The following table lists the different types of APIs in IOVIRT.

**Table 3-4: IOVIRT APIs and their details**

API name	Function prototype	Implementation
create_info_table	void pal iovirt create info table( IOVIRT_INFO_TABLE *iovirt);	Yes
unique_rid_strid_map	uint32_t pal iovirt unique rid_strid_map(uint64_t rc_block);	Yes
check_unique_ctx_initd	uint32_t pal iovirt check unique ctx_intid(uint64_t smmu_block);	Yes
get_rc_smmu_base	uint64_t pal iovirt get_rc_smmu_base( IOVIRT_INFO_TABLE *iovirt, uint32_t rc_seg_num, uint32_t rid);	Yes

### 3.1.5 PCIe

The following table lists the different types APIs in PCIe.

**Table 3-5: PCIe APIs and their details**

API name	Function prototype	Implementation
create_info_table	void pal_pc当地 create_info_table (PCIE_INFO_TABLE *PcieTable);	Yes
read_cfg	uint32_t pal_pc当地 read_cfg(uint32_t bdf, uint32_t offset, uint32_t *data);	Yes
get_msi_vectors	uint32_t pal_get_msi_vectors(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn, PERIPHERAL_VECTOR_LIST**mvector);	Platform-specific
get_pc当地_type	uint32_t pal_pc当地 get_pc当地_type(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Yes
p2p_support	uint32_t pal_pc当地 p2p_support(void);	Yes
read_ext_cap_word	void pal_pc当地 read_ext_cap_word(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn, uint32_t ext_cap_id, uint8_t offset, uint16_t *val);	Yes
get_bdf_wrapper	uint32_t pal_pc当地 get_bdf_wrapper (uint32_t class_code, uint32_t start_bdf);	Yes
bdf_to_dev	void *pal_pc当地 bdf_to_dev(uint32_t bdf);	Yes
pal_pc当地_ecam_base	uint64_t pal_pc当地 ecam_base(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t tfunc)	Yes
pci_cfg_read	uint32_t pal_pc当地 cfg_read(uint32_t bus, uint32_t dev, uint32_t func, uint32_t offset, uint32_t *value)	Yes
pci_cfg_write	void pal_pc当地 cfg_write(uint32_t bus, uint32_t dev, uint32_t func, uint32_t offset, uint32_t data)	Yes
program_bar_reg	void pal_pc当地 program_bar_reg(uint32_t bus, uint32_t dev, uint32_t func)	Yes
enumerate_device	uint32_t pal_pc当地 enumerate_device(uint32_t bus, uint32_t sec_bus)	Yes
enumerate	void pal_pc当地 enumerate(void);	Yes
get_bdf	uint32_t pal_pc当地 get_bdf(uint32_t ClassCode, uint32_t StartBdf)	Yes

API name	Function prototype	Implementation
increment_bus_dev	uint32_t pal_increment_bus_dev(uint32_t StartBdf)	Yes
get_base	uint64_t pal_pcic_get_base(uint32_t bdf, uint32_t bar_index)	Yes
io_read_cfg	uint32_t pal_pcic_io_read_cfg(uint32_t bdf, uint32_t offset, uint32_t *data) ;	Yes
io_write_cfg	void pal_pcic_io_write_cfg(uint32_t bdf, uint32_t offset, uint32_t data);	Yes
get_snoop_bit	uint32_t pal_pcic_get_snoop_bit(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Yes
is_device_behind_smmu	uint32_t pal_pcic_is_device_behind_smmu(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Yes
get_dma_support	uint32_t pal_pcic_get_dma_support(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Yes
get_dma_coherent	uint32_t pal_pcic_get_dma_coherent(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Yes
Is_devideddma_64bit	uint32_t pal_pcic_is_devideddma_64bit(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Yes
get_legacy_irq_map	uint32_t pal_pcic_get_legacy_irq_map(uint32_t Seg, uint32_t Bus, uint32_t Dev, uint32_t Fn, PERIPHERAL_IRQ_MAP *IrqMap);	Platform-specific
get_root_port_bdf	uint32_t pal_pcic_get_root_port_bdf(uint32_t *Seg, uint32_t *Bus, uint32_t *Dev, uint32_t *Func);	Yes
dev_p2p_support	uint32_t pal_pcic_dev_p2p_support(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Yes
is_cache_present	uint32_t pal_pcic_is_cache_present(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Yes
is_onchip_peripheral	uint32_t pal_pcic_is_onchip_peripheral(uint32_t bdf);	Platform-specific
check_device_list	uint32_t pal_pcic_check_device_list(void);	Yes
get_rp_transaction_frwd_support	uint32_t pal_pcic_get_rp_transaction_frwd_support(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn)	Platform-specific
check_device_valid	uint32_t pal_pcic_check_device_valid(uint32_t bdf);	Platform-specific
mem_get_offset	uint32_t pal_pcic_mem_get_offset(uint32_t bdf, PCIE_MEM_TYPE_INFO_emem_type);	Platform-specific
device_driver_present	uint32_t pal_pcic_device_driver_present(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Platform-specific
bar_mem_read	uint32_t pal_pcic_bar_mem_read(uint32_t Bdf, uint64_t address, uint32_t *data);	Yes
bar_mem_write	uint32_t pal_pcic_bar_mem_write(uint32_t Bdf, uint64_t address, uint32_t data);	Yes

## 3.1.6 SMMU

The following table lists the different types of APIs in SMMU.

**Table 3-6: SMMU APIs and their details**

API name	Function prototype	Implementation
check_device_iova	uint32_t pal_smmu_check_device_iova(void *port, uint64_t dma_addr);	Platform-specific
device_start_monitor_iova	void pal_smmu_device_start_monitor_iova(void *port);	Platform-specific
device_stop_monitor_iova	void pal_smmu_device_stop_monitor_iova(void *port);	Platform-specific
pa2iova	uint64_t pal_smmu_pa2iova(uint64_t smmu_base, unit64_t pa);	Platform-specific
smmu_disable	uint32_t pal_smmu_disable(uint64_t smmu_base);	Platform-specific
create_pasid_entry	uint32_t pal_smmu_create_pasid_entry(uint64_t smmu_base, uint32_t pasid);	Platform-specific
get_device_path	uint32_t pal_get_device_path(const char *hid, char hid_path[] [MAX_NAMED_COMP_LENGTH]);	Yes
is_etr_behind_catu	uint32_t pal_smmu_is_etr_behind_catu(char *etr_path);	Platform-specific

## 3.1.7 Peripheral

The following table lists the different types of APIs in peripheral.

**Table 3-7: Peripheral APIs and their details**

API name	Function prototype	Implementation
create_info_table	void pal_peripheral_create_info_table(PERIPHERAL_INFO_TABLE *per_info_table);	Yes
is_PCIE	uint32_t pal_peripheral_is_PCIE(uint32_t seg, uint32_t bus, uint32_t dev, uint32_t fn);	Yes
memory_create_info_table	void pal_memory_create_info_table(MEMORY_INFO_TABLE *memoryInfoTable);	Platform-specific
memory_ioremap	uint64_t pal_memory_ioremap(void *addr, uint32_t size, uint32_t attr);	Platform-specific
memory_unmap	void pal_memory_unmap(void *addr);	Platform-specific
memory_get_unpopulated_addr	uint64_t pal_memory_get_unpopulated_addr(uint64_t *addr, uint32_t instance)	Platform-specific

### 3.1.8 DMA

The following table lists the different types of APIs in DMA.

**Table 3-8: DMA APIs and their details**

API name	Function prototype	Implementation
create_info_table	void pal_dma_create_info_table(DMA_INFO_TABLE *dma_info_table);	Yes
start_from_device	uint32_t pal_dma_start_from_device(void *dma_target_buf, uint32_t length, void *host, void *dev);	Platform-specific
start_to_device	uint32_t pal_dma_start_to_device(void *dma_source_buf, uint32_t length, void *host, void *target, uint32_t timeout);	Platform-specific
mem_alloc	uint64_t pal_dma_mem_alloc(void *buffer, uint32_t length, void *dev, uint32_t flags);	Platform-specific
scsi_get_dma_addr	void pal_dma_scsi_get_dma_addr(void *port, void *dma_addr, uint32_t *dma_len);	Platform-specific
mem_getAttrs	int pal_dma_mem_getAttrs(void *buf, uint32_t *attr, uint32_t *sh)	Platform-specific
dma_mem_free	void pal_dma_mem_free(void *buffer, addr_tmem_dma, unsigned int length, void *port, unsigned int flags);	Platform-specific

### 3.1.9 Exerciser

The following table lists the different types of APIs in exerciser.

**Table 3-9: Exerciser APIs and their details**

API name	Function prototype	Implementation
get_ecsr_base	uint64_t pal_exerciser_get_ecsr_base(uint32_t Bdf, uint32_t BarIndex)	Platform-specific
get_pcie_config_offset	uint64_t pal_exerciser_get_pcie_config_offset(uint32_t Bdf)	Platform-specific
start_dma_direction	uint32_t pal_exerciser_start_dma_direction(uint64_t Base, EXERCISER_DMA_ATTRDirection)	Platform-specific
find_pcie_capability	uint32_t pal_exerciser_find_pcie_capability(uint32_t ID, uint32_t Bdf, uint32_t Value, uint32_t *Offset)	Platform-specific
set_param	uint32_t pal_exerciser_set_param(EXERCISER_PARAM_TYPE type, uint64_t value1, uint64_t value2, uint32_t bdf);	Platform-specific
get_param	uint32_t pal_exerciser_get_param(EXERCISER_PARAM_TYPE type, uint64_t *value1, uint64_t *value2, uint32_t bdf);	Platform-specific
set_state	uint32_t pal_exerciser_set_state(EXERCISER_STATE state, uint64_t *value, uint32_t bdf);	Platform-specific
get_state	uint32_t pal_exerciser_get_state(EXERCISER_STATE *state, uint32_t bdf);	Platform-specific
ops	uint32_t pal_exerciser_ops(EXERCISER_OPS ops, uint64_t param, uint32_t instance);	Platform-specific
get_data	uint32_t pal_exerciser_get_data(EXERCISER_DATA_TYPE type, exerciser_data_t *data, uint32_t tbdf, uint64_t ecam);	Platform-specific

API name	Function prototype	Implementation
is_bdf_exerciser	uint32_t pal_is_bdf_exerciser(uint32_t bdf)	Platform-specific

### 3.1.10 Memory map

The following table lists the different types of APIs required for Memory Map.

**Table 3-10: Memory map APIs and their details**

API name	Function prototype	Implementation
add_mmap	void pal_mmu_add_mmap(void);	Platform-specific
get_mmap_list	void *pal_mmu_get_mmap_list(void);	Platform-specific
get_mapping_count	uint32_t pal_mmu_get_mapping_count(void);	Platform-specific

### 3.1.11 Miscellaneous

The following table lists the different types of miscellaneous PAL APIs.

**Table 3-11: Miscellaneous APIs and their details**

API name	Function prototype	Implementation
mmio_read8	uint8_t pal_mmio_read8(uint64_t addr);	Yes
mmio_read16	uint16_t pal_mmio_read16(uint64_t addr);	Yes
mmio_read	uint32_t pal_mmio_read(uint64_t addr);	Yes
mmio_read64	uint64_t pal_mmio_read64(uint64_t addr);	Yes
mmio_write8	void pal_mmio_write8(uint64_t addr, uint8_t data);	Yes
mmio_write16	void pal_mmio_write16(uint64_t addr, uint16_t data);	Yes
mmio_write	void pal_mmio_write(uint64_t addr, uint32_t data);	Yes
mmio_write64	void pal_mmio_write64(uint64_t addr, uint64_t data);	Yes
print	void pal_print(char8_t *string, uint64_t data);	Platform-specific
uart_print	void pal_uart_print(int log, const char *fmt, ...);	Yes
print_raw	void pal_print_raw(uint64_t addr, char *string, uint64_t data)	Yes
mem_free	void pal_mem_free(void *buffer);	Platform-specific
mem_compare	int pal_mem_compare(void *src, void *dest, uint32_t len);	Yes
mem_set	void pal_mem_set(void *buf, uint32_t size, uint8_t value);	Yes
mem_allocate_shared	void pal_mem_allocate_shared(uint32_t num_pe, uint32_t sizeofentry);	Yes
mem_get_shared_addr	uint64_t pal_mem_get_shared_addr(void);	Yes
mem_free_shared	void pal_mem_free_shared(void);	Yes
mem_alloc	void *pal_mem_alloc(uint32_t size);	Yes
mem_virt_to_phys	void *pal_mem_virt_to_phys(void *va);	Platform-specific

API name	Function prototype	Implementation
mem_alloc_cacheable	void *pal_mem_alloc_cacheable(uint32_t Bdf, uint32_t Size, void **Pa);	Platform-specific
mem_free_cacheable	void pal_mem_free_cacheable(uint32_t Bdf, uint32_t Size, void *Va, void *Pa);	Platform-specific
mem_phys_to_virt	void *pal_mem_phys_to_virt ( uint64_t Pa);	Platform-specific
strncmp	uint32_t pal_strncmp(const char8_t *str1, const char8_t *str2, uint32_t len);	Yes
memcpy	void *pal_memcpy(void *DestinationBuffer, const void *SourceBuffer, uint32_t Length);	Yes
time_delay_ms	uint64_t pal_time_delay_ms(uint64_t time_ms);	Platform-specific
page_size	uint32_t pal_mem_page_size();	Platform-specific
alloc_pages	void *pal_mem_alloc_pages (uint32 NumPages);	Platform-specific
free_pages	void pal_mem_free_pages (void *PageBase, uint32_t NumPages);	Platform-specific
mem_calloc	void *pal_mem_calloc(uint32_t num, uint32_t Size);	Yes
aligned_alloc	void *pal_aligned_alloc( uint32_t alignment, uint32_t size );	Yes
target_is_bm	uint32_t pal_target_is_bm()	Yes
mem_free_aligned	void pal_mem_free_aligned(void *buffer);	Platform-specific
strncpy	void *pal_strncpy(void *DestinationStr, const void *SourceStr, uint32_t Length);	Yes
uart_pl011_putc	void pal_driver_uart_pl011_putc(int c);	Yes

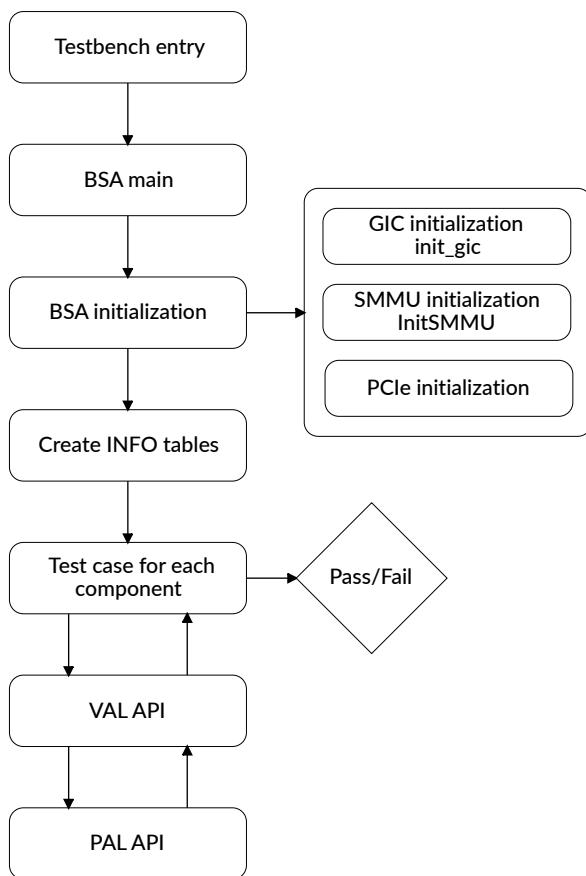
# 4. BSA ACS flow

This chapter provides the BSA ACS flow diagram and BSA test example flow.

## 4.1 BSA ACS flow diagram

The following flow diagram shows the sequence of events from initialization of devices, initialization of BSA test data structures, and test case execution.

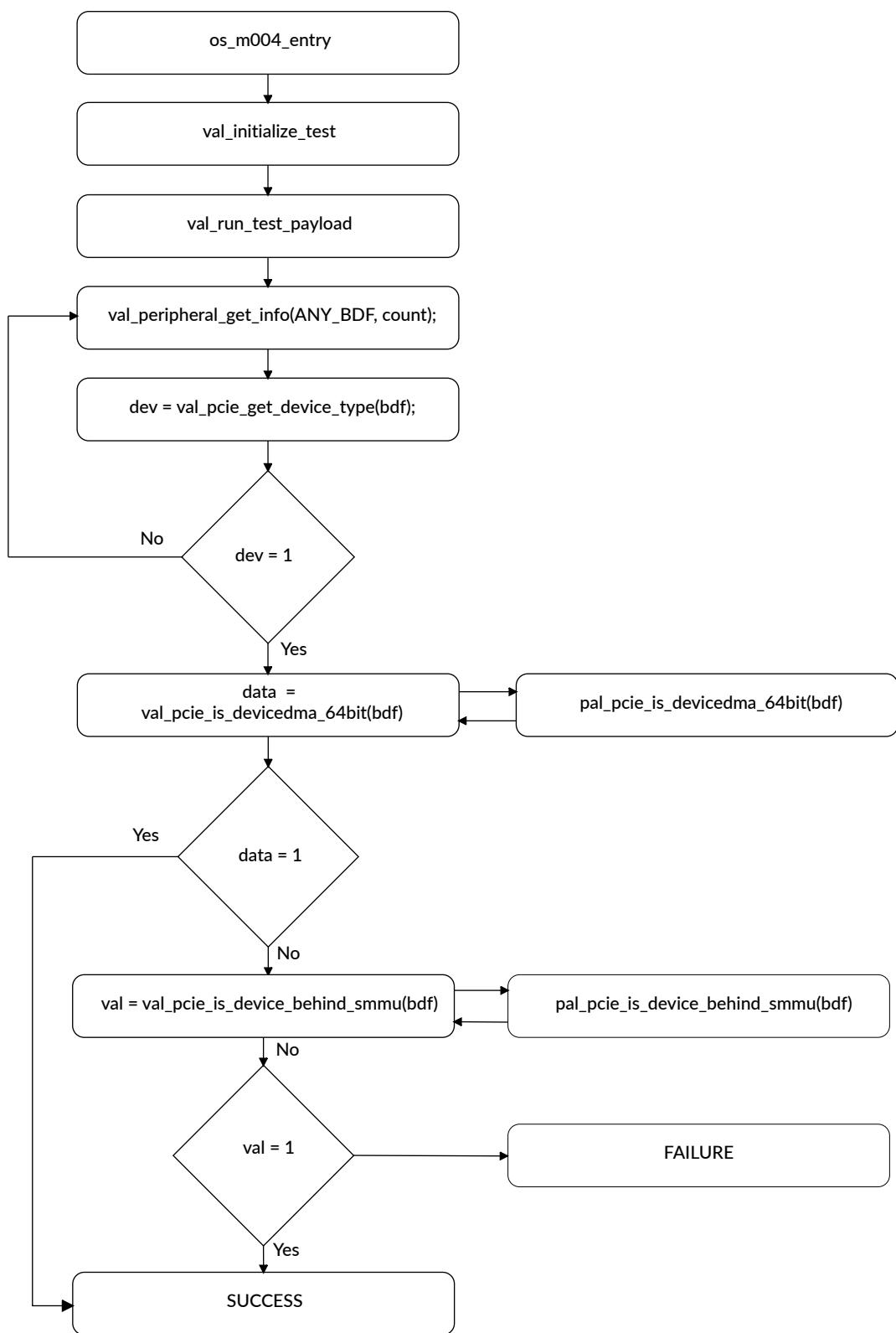
**Figure 4-1: BSA flow diagram**



## 4.2 BSA test example flow

If the device is Message-Signaled Interrupt (MSI) enabled, then the flag is set to MSI\_ENABLED by the PAL layer. The test checks whether the device is of type endpoint and then checks if the flags are set to MSI\_ENABLED.

The following flowchart shows the test that checks MSI support in a PCIe device.

**Figure 4-2: BSA example flow diagram**

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# Product and document information

Read the information in these sections to understand the release status of the product and documentation, and the conventions used in the Arm documents.

## Product status

All products and Services provided by Arm require deliverables to be prepared and made available at different levels of completeness. The information in this document indicates the appropriate level of completeness for the associated deliverables.

### Product completeness status

The information in this document is for a Beta product, that is a product under development.

## Revision history

These sections can help you understand how the document has changed over time.

### Document release information

The Document history table gives the issue number and the released date for each released issue of this document.

#### Document history

Issue	Date	Confidentiality	Change
0102-01	10 December 2025	Non-Confidential	REL v1.2.0
0100-07	28 May 2025	Non-Confidential	REL v1.1.1
0100-06	25 March 2025	Non-Confidential	REL v1.1.0
0100-05	29 March 2024	Non-Confidential	REL v1.0.8
0100-04	19 December 2023	Non-Confidential	REL v1.0.7
0100-03	7 November 2023	Non-Confidential	REL v1.0.6
0100-02	28 September 2023	Non-Confidential	REL v1.0.6
0100-01	28 March 2023	Non-Confidential	REL v1.0.4

The Change history tables describe the technical changes between released issues of this document in reverse order. Issue numbers match the revision history in [Document release information](#) on page 36.

**Table 2: Issue 0100-01**

Change	Location
First release.	-

**Table 3: Differences between Issue 0100-01 to 0100-02**

Change	Location
Updated the steps to customize the bare-metal code.	See, <a href="#">1.5 Steps to customize bare-metal</a> on page 9.
Updated the PCIe APIs and their details table.	See, <a href="#">3.1.5 PCIe</a> on page 25.
Updated SMMU APIs and their details table.	See, <a href="#">3.1.6 SMMU</a> on page 26.
Updated BSA test example flow diagram	See, <a href="#">4.2 BSA test example flow</a> on page 31.

**Table 4: Differences between Issue 0100-02 to 0100-03**

Change	Location
Added a new section for MMU configuration.	See, <a href="#">2.1.1.1 MMU Configuration</a> on page 13.
Added new sections, Boot framework, Boot process and boot flow and Boot framework for Bare-metal.	See, <a href="#">1.4 Boot framework</a> on page 7, <a href="#">1.4.1 Boot process and boot flow</a> on page 7, and <a href="#">1.4.2 Boot framework for Bare-metal</a> on page 7
Added a new section Peripherals.	See, <a href="#">2.1.9 Peripherals</a> on page 21.
Added a new section Bare-metal Boot.	See, <a href="#">2.2 Bare-metal Boot</a> on page 22.
Updated the information required for PCIe enumeration.	See, <a href="#">2.1.2 PCIe</a> on page 13.
Added MMU in abbreviation.	See, <a href="#">1.1 Abbreviations</a> on page 5.
Added new APIs in Miscellaneous APIs and their details table and updated the Function prototype.	See, <a href="#">3.1.11 Miscellaneous</a> on page 29.

**Table 5: Differences between Issue 0100-03 to 0100-04**

Change	Location
Added a new section for Memory map.	See, <a href="#">3.1.10 Memory map</a> on page 29.
Updated the Miscellaneous APIs and their details table.	See, <a href="#">3.1.11 Miscellaneous</a> on page 29.
Updated the PCIe APIs and their details table.	See, <a href="#">3.1.5 PCIe</a> on page 25.
Removed the API <code>get_legacy_irq_map</code> from the Exerciser APIs and their details table.	See, <a href="#">3.1.9 Exerciser</a> on page 28.

**Table 6: Differences between Issue 0100-04 to 0100-05**

Change	Location
Updated the folder details.	See, <a href="#">1.5 Steps to customize bare-metal</a> on page 9 .
Updated the PCIe root ports and parameters.	See, <a href="#">2.1.2 PCIe</a> on page 13.

**Table 7: Differences between Issue 0100-05 to 0100-06**

Change	Location
Added API <code>get_num_nongic_ctrl</code> in the GIC APIs table.	See, <a href="#">3.1.2 GIC</a> on page 24
Added API <code>create_info_table</code> in the PE APIs table.	See, <a href="#">3.1.1 PE</a> on page 23

Change	Location
Added SMBIOS-specific information in PE.	See, <a href="#">2.1.1 PE</a> on page 11

**Table 8: Differences between Issue 0100-06 to 0100-07**

Change	Location
Updated the steps to customize the bare-metal code.	See, <a href="#">1.5 Steps to customize bare-metal</a> on page 9

**Table 9: Differences between Issue 0100-07 to 0102-01**

Change	Location
No technical changes.	-

## Conventions

The following subsections describe conventions used in Arm documents.

### Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: [developer.arm.com/glossary](https://developer.arm.com/glossary).

### Typographic conventions

Arm documentation uses typographical conventions to convey specific meaning.

Convention	Use
italic	Citations.
<b>bold</b>	Interface elements, such as menu names.  Terms in descriptive lists, where appropriate.
monospace	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
monospace <u>underline</u>	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments.  For example:  <code>MRC p15, 0, &lt;Rd&gt;, &lt;CRn&gt;, &lt;CRm&gt;, &lt;Opcode_2&gt;</code>
<b>SMALL CAPITALS</b>	Terms that have specific technical meanings as defined in the <i>Arm® Glossary</i> . For example, <b>IMPLEMENTATION DEFINED</b> , <b>IMPLEMENTATION SPECIFIC</b> , <b>UNKNOWN</b> , and <b>UNPREDICTABLE</b> .

**Caution**

We recommend the following. If you do not follow these recommendations your system might not work.

**Warning**

Your system requires the following. If you do not follow these requirements your system will not work.

**Danger**

You are at risk of causing permanent damage to your system or your equipment, or of harming yourself.

**Note**

This information is important and needs your attention.

**Tip**

This information might help you perform a task in an easier, better, or faster way.

**Remember**

This information reminds you of something important relating to the current content.

# Useful resources

This document contains information that is specific to this product. See the following resources for other useful information.

Arm documents are available on [developer.arm.com/documentation](https://developer.arm.com/documentation).

Confidential documents are only available to licensees, when logged in. Each document link in the following tables provides direct access to the online version of the document.

Arm product resources	Document ID	Confidentiality
Arm® BSA Architecture Compliance User Guide	102504	Non-Confidential
Arm® BSA Architecture Compliance Validation Methodology	102503	Non-Confidential