CMOS VLSI DESIGN PROJECT REPORT
ECE 3005

Implementation of a 1-Bit Full Adder and Edge-Triggered D Flip-Flop in 90nm

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ABSTRACT :

- This project is to design a 1-bit full adder and a D flip-flop using Cadence virtuoso or ngspice. Then inputs of full adder are given using the D flip flop with the clock. The designs in this project are implemented using 90nm technology in Cadence Virtuoso.

OBJECTIVE :

- Design and stimulate the full adder, D flip flop and integrate the both for the final design.
- To ensure low power consumption, less delay and correct output waveforms.

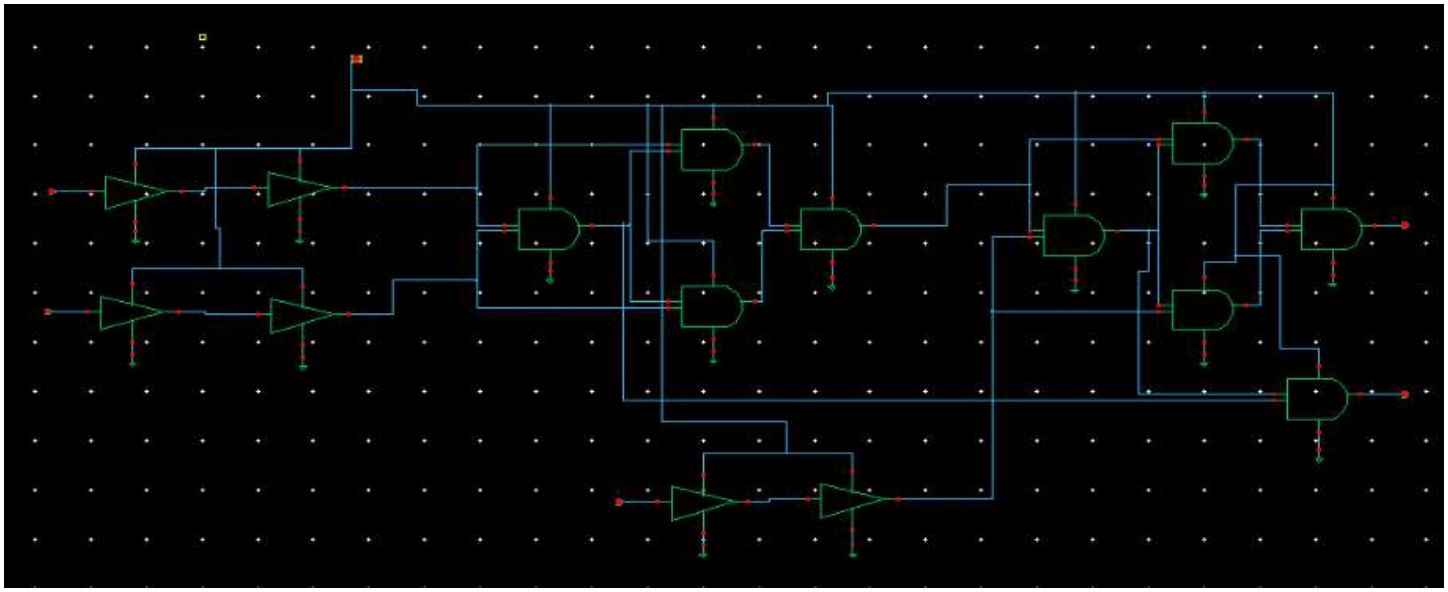
SETUP:

- The project uses gpdk 90nm technology in Cadence Virtuoso.
- Buffers are added at the input side and 1.5V is given as Vdd.
- For each circuit(Inverter, full adder, D FF), symbol is created and then used for further designing.

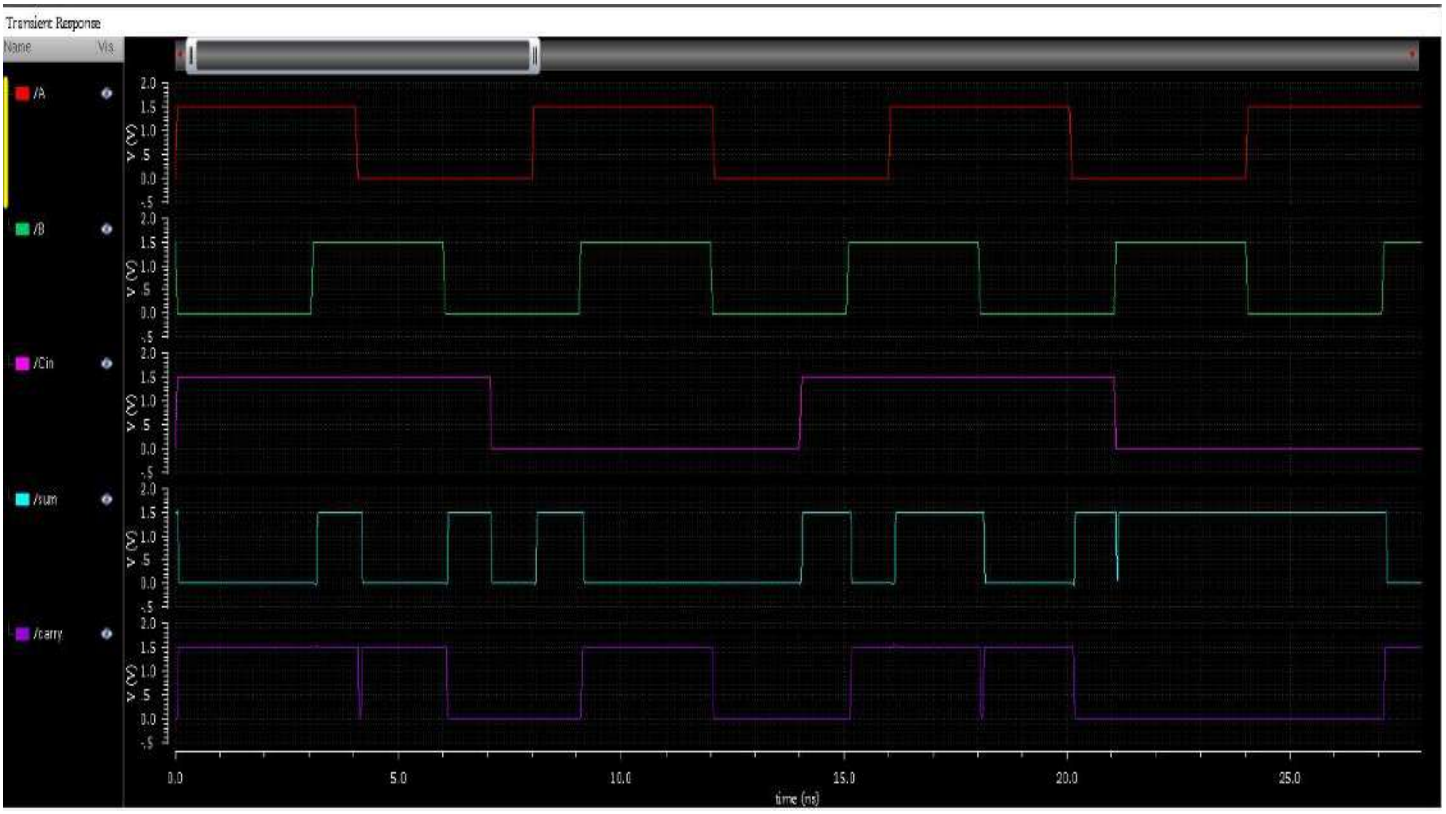
OUTCOME:

- The outcome of the project is to get proper working of the final integrated circuit and finding the minimum clock Tmin and maximum frequency.

ONE-BIT FULL ADDER SCHEMATIC :



OUTPUT WAVEFORM :



POWER OF FULL ADDER :

DELAYS OF FULL ADDER :

Combination-1 000

delay = 50ps

Combination-2 001

delay = 46ps

Combination-3 010

delay = 50ps

Combination-4 011

delay: 77ps

Combination-5 100

delay = 81ps

Combination-6 101

delay=77ps

Combination-7 110

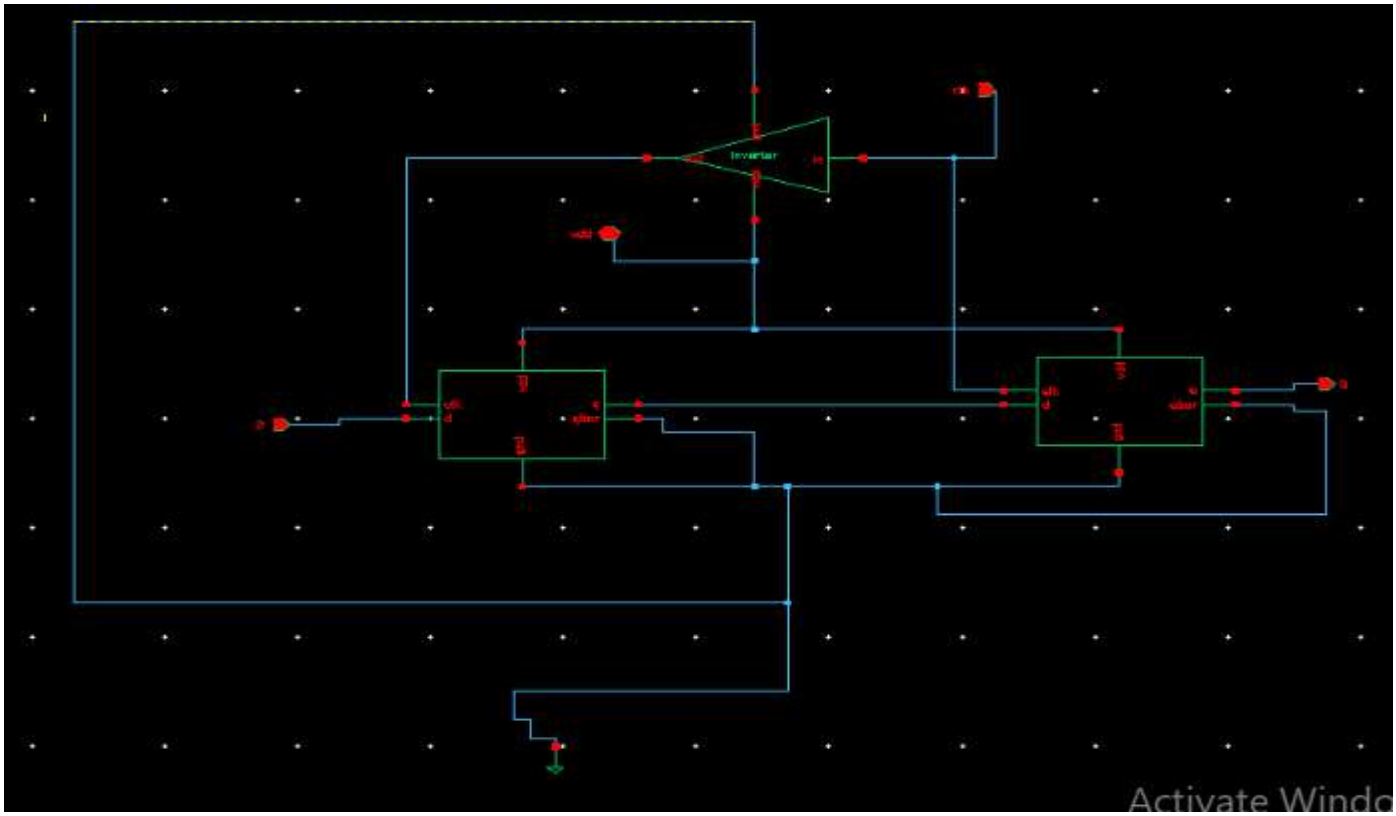
delay=56ps

Combination-8 111

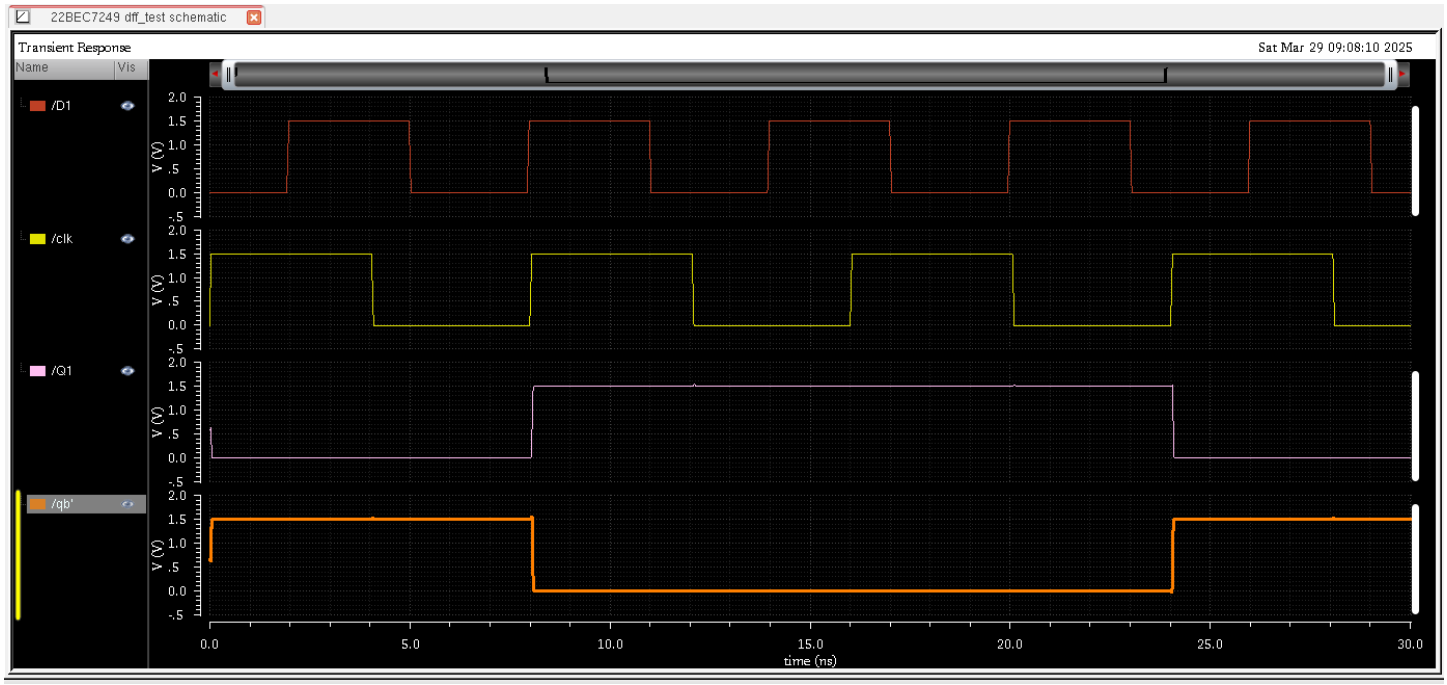
delay=46PS

overall delay of full adder = 81ps

D FLIPFLOP:



OUTPUT WAVEFORM OF D FLIP FLOP :



POWER OF D_FLIPFLOP:

Timing Analaysis Methodology:

Begin by identifying the relevant clock transition—typically the rising edge for a D flip-flop—where data is expected to be latched. Examine the behavior of the D input signal immediately before and after this transition to determine the timing relationship.

Setup Time:

To find the setup time, locate the last moment at which the data input (D) remains stable *prior* to the active clock edge. Measure the time interval between this stable point and the clock edge—this gives the setup time.
The setup time must satisfy the condition:
Tclk ≥ Tclk-q + Tcomb + Tsetup

Tsetup=33ps

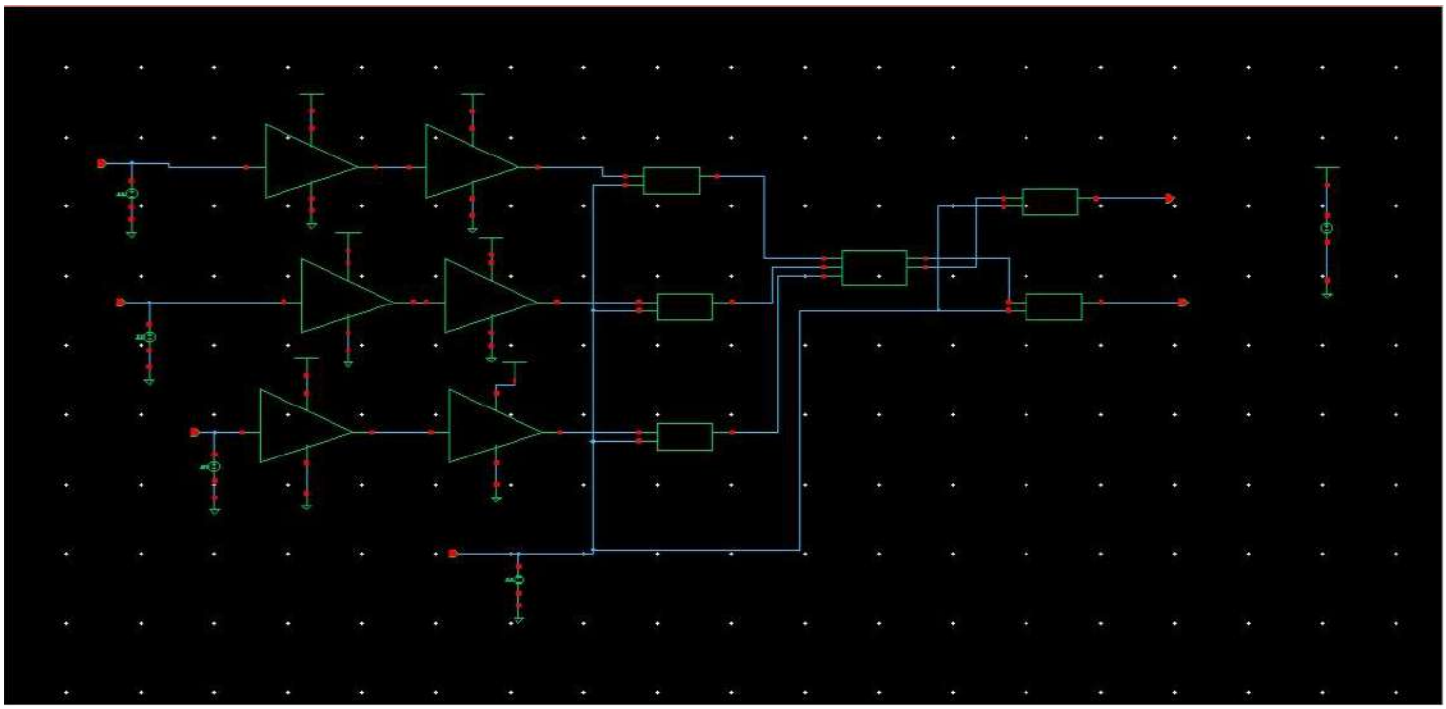
Hold Time:

To determine hold time, observe the first point at which the D input changes *after* the clock edge. Measure the duration from the clock edge to this transition. This value represents the hold time.
The condition to satisfy is:
Thold ≤ Tclk-q + Tcomb

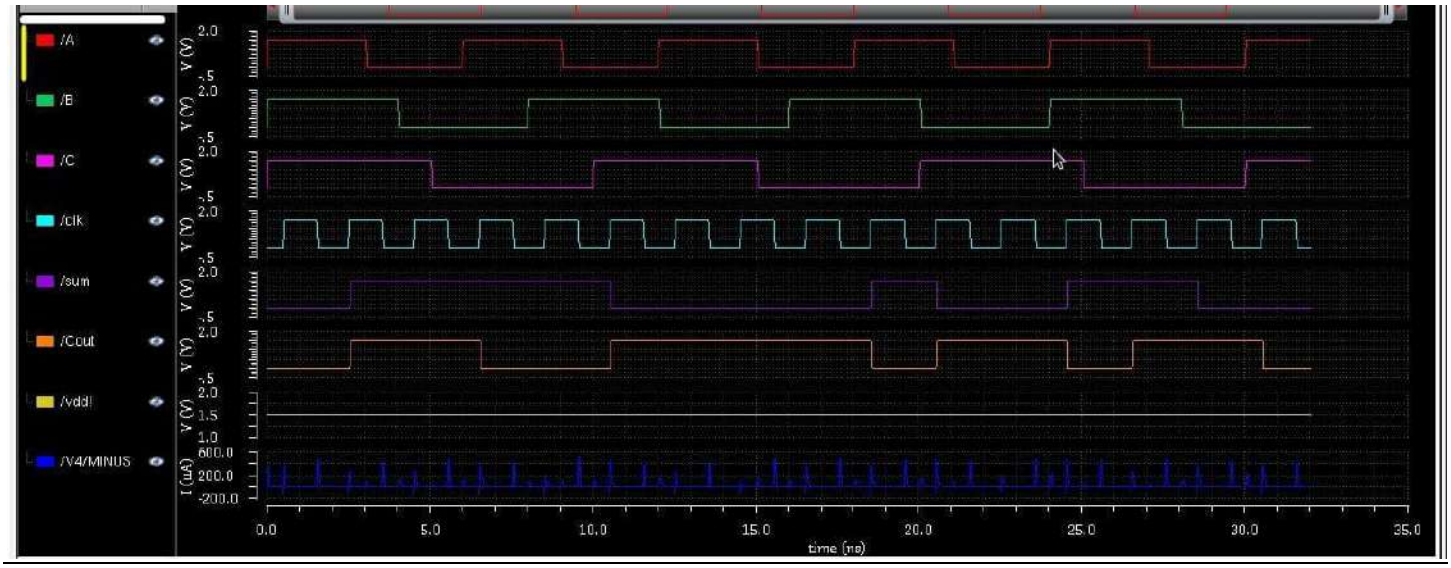
Thold=0ps

Ensure the output (Q) reflects the correct value of D after the clock edge to validate timing

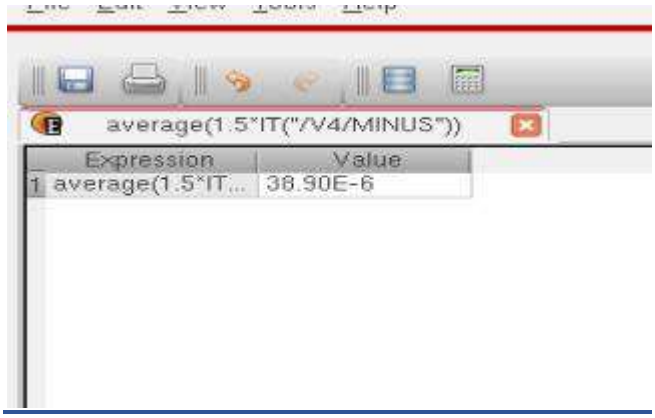
INTEGRATED CIRCUIT SCHEMATIC :



OUTPUT WAVEFORM :



POWER OF INTEGRATED CIRCUIT:



TABULAR RESULT :

Sl. No.	Design	No. TXs	Total Area	Max Delay (m)	Avg. Power (Watt)	PDP (Power Delay Product)(m^2)
1	FA	48	576*10^(-15) m^2	81P	36.62u	29.16 * 10^(-16)
2	FF	38	456*10^(-15) m^2	43p	36u	15.48*10^(-16)
3	Integrated	150	1800*10^(-15) m^2	157p	38.9u	61.07*10^(-16)
4	At max clk speed	150	1800*10^(-15) m^2	296.53p	52.62u	15.603*10^(-15)

Min. TClock period - 157p , Max. Clock Freq. - 6.369GHZ

From the formula,

Tclk(min) = Tclk-q + Tsetup + Tcmob

= 43ps +33ps+ 81ps

= 157ps

Max frequency = 1/(Tclk(min))
= 1/157p
= 6.369GHZ

CONCLUSION:

In conclusion, the project effectively demonstrated the principles and practices of CMOS VLSI design through the implementation and integration of a 1-bit full adder and a D edge-triggered flip-flop using 90nm technology. By focusing on performance metrics such as power efficiency, timing accuracy, and area optimization, the design adhered to modern standards in digital circuit design. The use of hierarchical and modular design approaches facilitated clearer development and validation workflows. Moreover, the hands-on experience with professional simulation tools like NGSPICE and Cadence Virtuoso provided valuable insight into the real-world VLSI design process. This project not only achieved its technical objectives but also served as a solid foundation for advancing toward more sophisticated and scalable digital systems.