Twangilizer Theory of Operation

Description:

The Twangilizer is a Eurorack module that fits in a 3U x 20HP format. It is an “additive synthesis” module that generates four sine waves that are harmonically related to a given input signal.

Using the 8-position rotary switches the user can select from 8 harmonics (1f – 8f). The resulting signals can be used as-is or can be halved in frequency by the toggle switches. This gives the user many interesting options when creating a sound.

The levels of the resulting harmonics can be adjusted using the front panel potentiometers or via the CV inputs. An indicator LED displays the level of the adjustment.

Inputs:

1. Clock input. Accepts signals > .1VRMS. 20 – 20KHz. An LED indicates CLK present.
2. CV1 – CV4. Control the level of the harmonics sent to analog out. 0-10V range.

Outputs:

1. Analog Out. Sum of all four harmonics.
2. CLK Outputs 1-4. Digital outputs of the four harmonics. For syncing other modules.

Several circuit blocks are used to implement the Twangilizer:

1. Power Supply
2. Clock capture
3. Harmonic generators
4. Waveform generators
5. Tracking Filters
6. Signal reconstruction
7. VCAs
8. Digital Outputs
9. Analog Output

Power Supply

The power connector is “Either Way” but should be tested with a diode tester to make sure the diodes have been installed correctly. 1N5819 SCHOTTKY diodes are used. While not the lowest possible forward voltage, they are available from JLCPCB, so they have been used extensively in the circuitry.

The resulting voltage after the diode drops are approx.: +11.5V and -11.6V given +/-12V inputs.

All the remaining voltages are derived from these supplies.

Even though many Eurorack systems contain +5V rails, not all of them do. For this reason, +5V is generated locally. An AMS1117-5.0 is used for this purpose. It has a 1A capacity so should be plenty for this application.

The harmonic and waveform generators use +9V and -9V. These functions require good regulation to achieve a stable waveform. The LM317 used for the +9V requires a certain amount of headroom, or else +10V would have been chosen, as the PLLs work best with higher supply voltages. However, 9V is good enough. The -9V rail requires less than 200uA, so an op amp regulator is ideal here.

The symmetry of the waveform depends on the absolute value of the -9V rail being close to the +9V rail. For this reason, .1% resistors were chosen.

Also, the bias point for the VCO pickoff circuits is set by the -9V. This is a sensitive parameter, so it needs to be accurate. A 500ohm trimpot adjusts the +9V rail. With components at their nominal values, an adjustment range of 8.61V – 9.62V is achieved. The nominal adjustment range is skewed so that the worst case range is adequate and as symmetrical about the 9V value as possible. The results of this are:

1. Set RV1 to 200ohms for 9.01V when all components are nominal.
2. Worst case lower value is 8.76V
3. Worst case upper value is 9.21V

Refer to lm317.xlsx for the calculations used in this discussion.

Tests

1. D1 – D4 correctly installed
2. +12 > 11.4
3. -12 > -11.5
4. +5V between 4.9V and 5.1V
5. Adjust +9V between 8.95V and 9.05V
6. -9V within .5% of +9V magnitude.

Clock Capture

The clock capture circuit supplies the signal to the harmonic generators. It is spec'd for a signal greater than .1VRMS in amplitude and works in the range of 20Hz – 20KHz. We test at .05VRMS. The input clock signal is AC coupled and then low-pass filtered. The 3dB point of the low-pass filter is at 30KHz.

The signal is then given a gain of 51 and passed to a comparator and then finally to a transistor circuit that translates the voltage to a 9V signal compatible with the harmonic and waveform generators.

Another transistor circuit drives a “Clock Present” indicator LED.

Tests

1. CLK waveform good at 20Hz .05VRMS sine wave
2. CLK waveform good at 20KHz .05VRMS sine wave

3. No CLK at 70KHz .05VRMS sine wave
4. CLK present indicator OFF when no clock is present
5. CLK present indicator ON when clock is present

Harmonic Generators

The harmonics are generated using phase locked loops with down counters whose outputs are routed to the reset input via the 8 position rotary switches. This arrangement creates a frequency multiplier of 1f – 8f depending on the position of the switch. The signal can be further modified by the toggle switches that follow. These are either connected to the signal or to a flip-flop that divides the frequency in half. When the frequency divider position is chosen, you get the resulting frequencies: 1/2f, 1f, 3/2f, 2f, 5/2f, 3f, 7/2f, 4f.

There is a foible in the circuit when in 1f mode. A race condition exists that results in the output signal oscillating at around 110KHz. This is fixed by the slight delay added to the 1f position via the 1K resistor and 10pF capacitor.

Waveform Generators

The outputs of the Harmonic Generators are fed to the Waveform Generators which create the sinewave approximations. These 10-step waveforms are created by CD4046/CD4017 combinations similar to the Harmonic Generators.

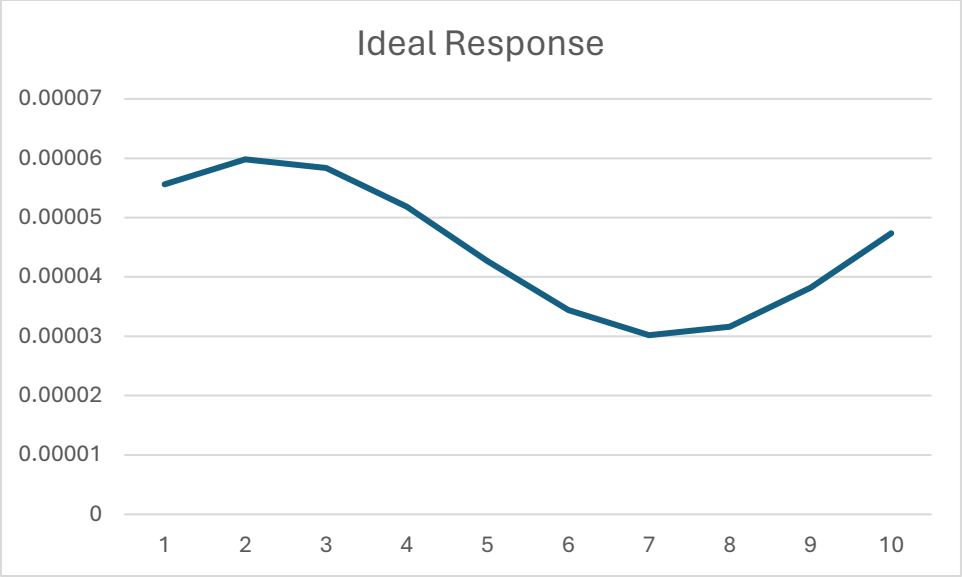
But instead of selectable ratios, these circuits are all set to multiply by 10. Each output of the CD4017 is sent through a resistor to a summing amplifier. The gain of this amp is set to produce a signal compatible with the next stage. The resulting signal from the Waveform Generators is -3dBm @600 or .547VRMS.

Here is the Excel calculation for the ideal resistor values:

F	G	H
0	5.56066E-05	161851.2
0.1	5.98153E-05	150463.1
0.2	5.83651E-05	154201.8
0.3	5.18098E-05	173712.4
0.4	4.26534E-05	211003.3
0.5	3.43933E-05	261678.9
0.6	3.01846E-05	298164.8
0.7	3.1635E-05	284495.2
0.8	3.81903E-05	235661.8
0.9	4.73467E-05	190087

G =0.000015*SIN((F?+.125)*6.2832)+0.000045 *defines current through resistor*

H =9/G? *defines ideal resistor value*



Real resistor values have been substituted in the following table and graph:

I	J	K
162000	1.06E-05	-0.55206
1.50E+05	0.000015	-0.7845
1.54E+05	1.34E-05	-0.70299
1.74E+05	6.72E-06	-0.35167
2.10E+05	-2.1E-06	0.112071
2.61E+05	-1.1E-05	0.550052
3.00E+05	-1.5E-05	0.7845
2.87E+05	-1.4E-05	0.71343
2.37E+05	-7E-06	0.367424
1.91E+05	2.12E-06	-0.1109
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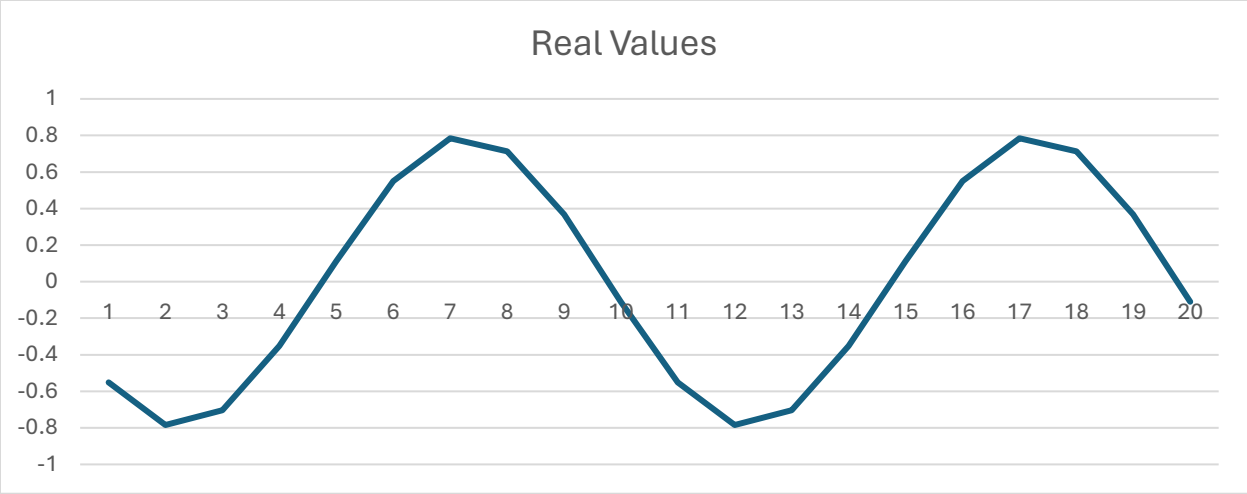
2.37E+05	-7E-06	0.367424
1.91E+05	2.12E-06	-0.1109

J =9/I?-0.000045

K =-52300*J?



Equation K shows the 52.3K resistor that sets the gain of the summing amplifier.

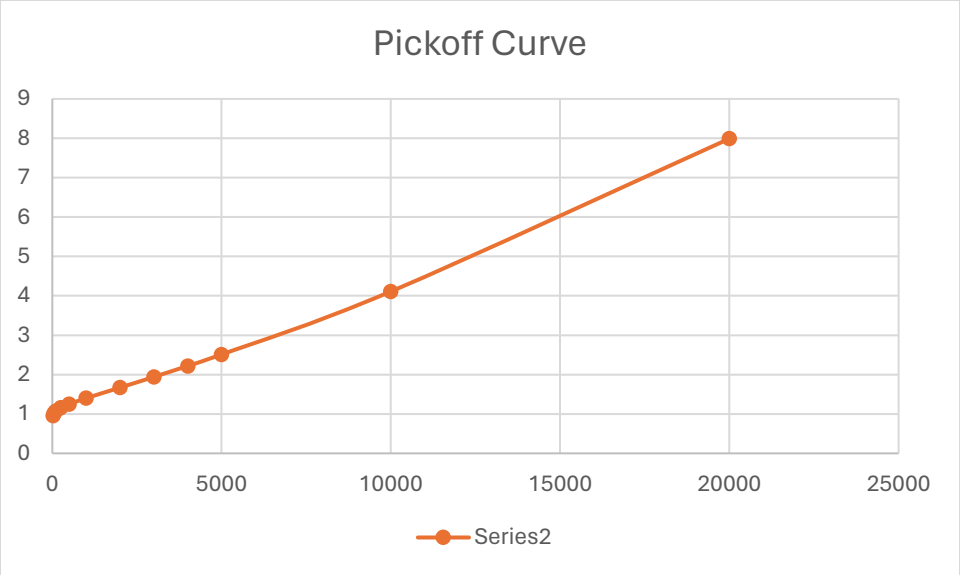
Dividing the peak value of .7845V by the square root of two results in .555VRMS. The 100pF cap in the feedback filters the high frequency components (-3dB @30KHz) of the signal and reduces the amplitude to near the desired .547VRMS.

Tracking Filters

The job of the tracking filters is to produce sine waves from the approximate waveforms formed by the Waveform Generators described above. The tracking filters use the VCO in of the PLL chips to sense the frequency and set the corner frequency of the filters as required.

The CD4046 phase locked loop IC has a capture range defined by the RC combination of the cap that appears between pins 6 and 7 and the resistor chain that is connected to pin 11. With a resistor that has a nominal value of 35K (10K plus half the 50K of the trimpot) and a capacitor of 300pF, you get a center frequency around 100KHz when the circuit is configured as a 10f multiplier. See fig. 5 in the data sheet.

Increasing RC reduces the upper capture point and increases the slope of the pickoff curve.

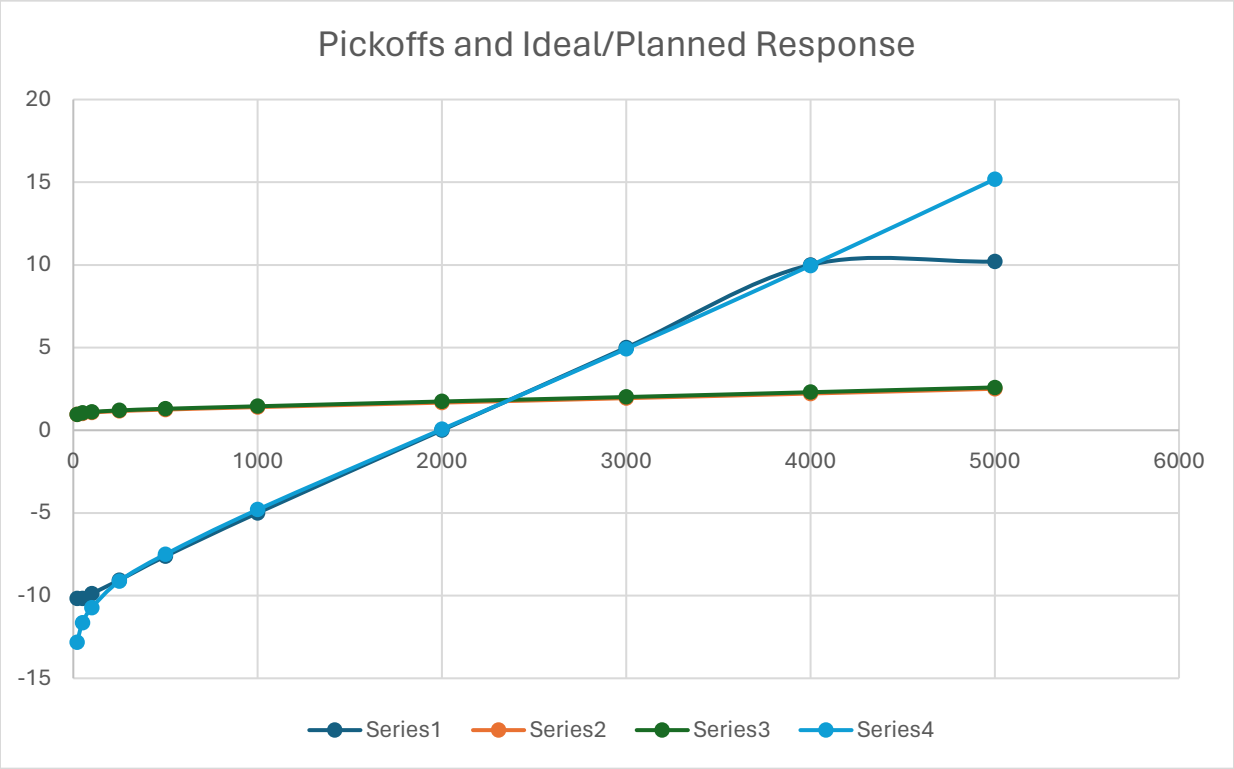


The filters use a signal that ranges from -10VDC to +10VDC to set the corner frequency. The table shows the Ideal curve which was empirically derived. It also shows the results measured from a v0.0 Twangilizer and a circuit on the PBJ protoboard. Finally, it shows the computed curve.

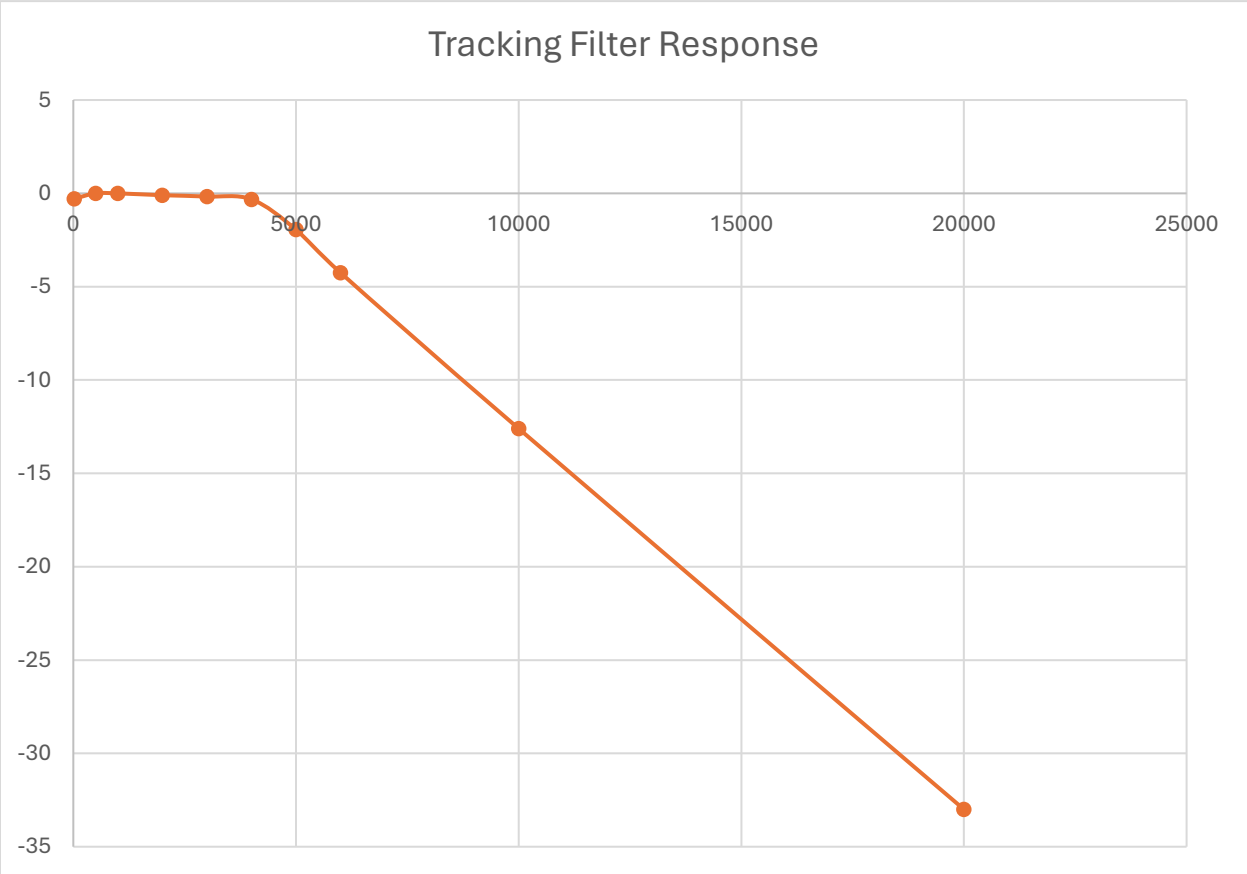
Refer to VCO Pickoff Meas.xlsx for the following data.

Freq	Ideal	Twang Pickoff	PBJ Pickoff	Computed
5000	10.2	2.51	2.59	15.18
4000	10	2.22	2.3	9.96
3000	5	1.94	2.01	4.92
2000	0	1.67	1.74	0.06
1000	-5	1.4	1.45	-4.8
500	-7.62	1.25	1.3	-7.5
250	-9.06	1.16	1.2	-9.12
100	-9.88	1.07	1.11	-10.74
50	-10.17	1.02	1.05	-11.64
20	-10.17	0.954	0.962	-12.828

Planned =(Pickoff*17)-28



The resulting curve for the tracking filters looks something like the following measured trace:



The signal from the VCO is not a pure DC signal. It contains pulses that continually correct the output frequency. These pulses must be filtered lest they affect the output signal. A single stage filter with a cutoff frequency of 6.8KHz accomplishes this task. The 499K pickoff resistor and a 47pF cap is used.

A spreadsheet that was used to select resistor values is found here: VCO Pickoff Plan.xlsx

Signal Reconstruction

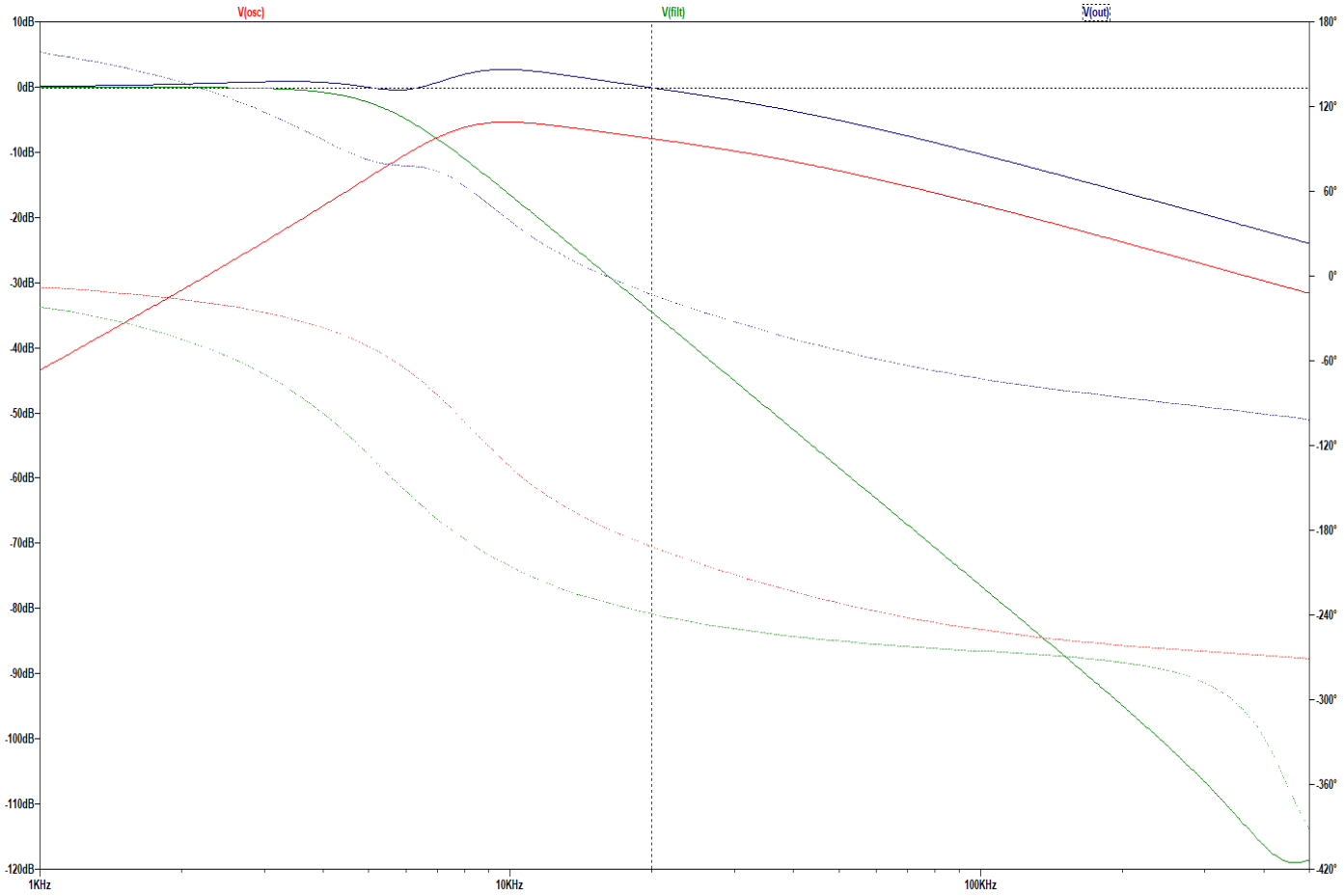
Because the requirement is for an output signal that spans 20Hz through 20KHz and the tracking filters produce a signal that is truncated above 5KHz, a method to handle the higher frequencies must be found.

The output of a high pass filter sourced by the Waveform Generators can be summed with the tracking filter output to accomplish this. The hi pass filter was designed to produce the flattest possible response when summed with the output of the tracking filters. Because the tracking filters have an approximate 7dB gain, the sum of the two filters must be weighted appropriately to get the best response.

The parameters of this filter are as follows: *High-Pass; 2nd order Chebyshev 2.4dB*

-3dB @6KHz -24dB @ 2KHz

The plot below shows the LT Spice simulation: (from spice\VCF model.asc)



Tests

Measure at TP12 – TP19

1. 1f waveform good at 20Hz CLK
2. 1f waveform good at 20KHz CLK
3. Measure 50Hz at 100Hz CLK for 1f/2
4. 2f waveform good at 20Hz CLK
5. 2f waveform good at 10KHz CLK
6. 3f waveform good at 20Hz CLK
7. 3f waveform good at 6.67KHz CLK
8. 4f waveform good at 20Hz CLK
9. 4f waveform good at 5KHz CLK
10. 5f waveform good at 20Hz CLK
11. 5f waveform good at 4KHz CLK
12. 6f waveform good at 20Hz CLK
13. 6f waveform good at 3.33KHz CLK
14. 7f waveform good at 20Hz CLK
15. 7f waveform good at 2.86KHz CLK
16. 8f waveform good at 20Hz CLK
17. 8f waveform good at 2.5KHz CLK

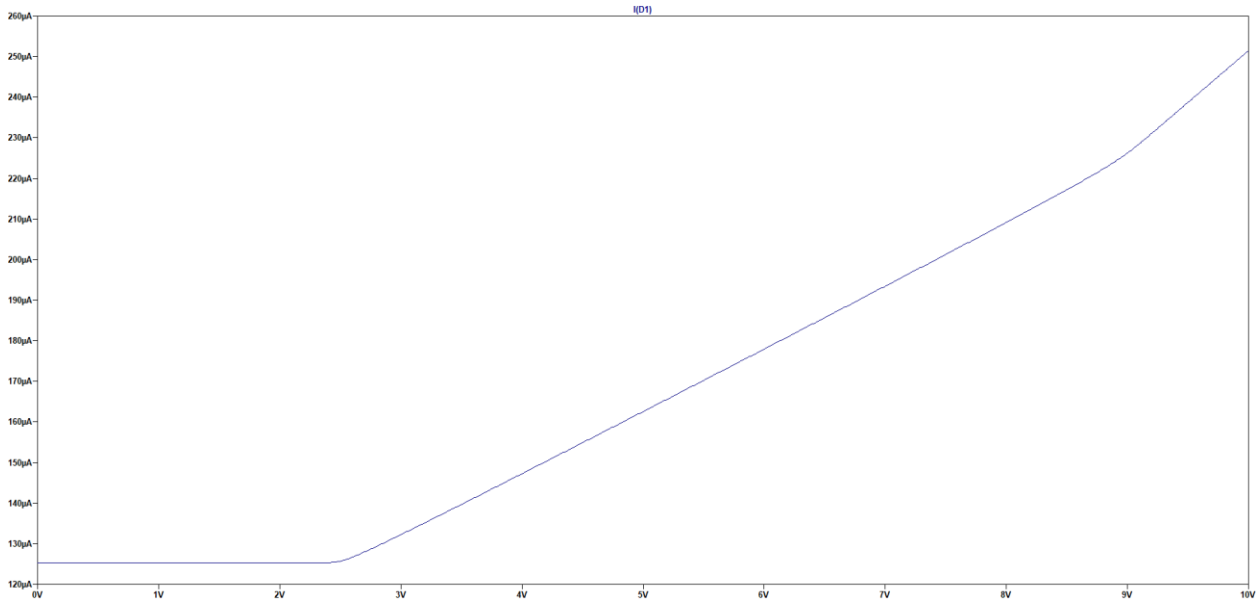
VCAs

Now that the frequency of the harmonic has been set and the tracking filter has turned the output of the waveform generator into a sine wave, the level must be set. This is accomplished using a voltage-controlled amplifier.

There are two control inputs to the VCA, one from the CV input jack which is protected in the usual way with a 510ohm resistor and 1N5819s, and one set by the CV bias potentiometer. The 510ohms is small enough in resistance to be insignificant to the 200K input. Since the bias pot uses +9V as its reference, the voltage divider is adjusted to match the range of the CV input by the 180K resistor. In either case, this sets the full-scale voltage value at the non-inverting input of the op amp to be 5V. This implies 5V at the inverting input which sets a current of 250uA. (5V / 20K)

When the CV bias pot is used in conjunction with the CV input, the bias sets a current level that is increased by the CV input when it exceeds the voltage level of the CV bias. A transfer function curve of CV input vs LED current best illustrates this. The bias pot is set to 50% in this example.

See spice\VCA.asc



Here we see the current at 125uA until the CV input is greater than 2.5V. This is because diode D4 does not conduct until the CV input exceeds 2.5V. The current then increases with CV until the maximum of 250uA is reached.

With the CV bias set to 100%, the base current will be 250uA. In this case the CV input will increase the current to a maximum of 330uA with the increase starting when the CV input equals 5V.

In the above example, the slight upturn when CV input is greater than 9V occurs when D3 is no longer conducting.

The VCA circuit uses a vactrol as the controlled element. The NSL-32SR3 has a nominal resistance of 600 ohms with an LED current of 250uA. The output of the Signal Reconstruction element is approximately 3.5Vp-p. This must be raised to the specified output level of 10Vp-p. This implies a gain of 2.86 which is realized by the 1.21K in series with the 1K trimpot at 50% divided by 600 ohms.

An indicator LED is put in series with the vactrol LED as an indication of the control voltage level.

Tests

Measure at Analog Output, CLK input 1000Hz.

1. 0V CV, bias adjustment off. Measure < .1VRMS.

Digital Outputs

The digital outputs are +5V square waves generated from the outputs of the Harmonic Generators which outputs are 9V square waves and must be level-shifted to the required 5V. Open collector drivers are used for this purpose. They are pulled up by a 510ohm resistor and the outputs are protected by another 510ohm resistor and the usual 1N5819 diodes. A 100nF cap decouples the outputs to provide a clean square wave.

Analog Output

The analog output is the sum of the four VCA outputs. It is followed by a 4th order Butterworth 20KHz low pass filter. The output is protected by the usual 510ohm/1N5819 circuit.

The curve of the filter is modeled in the file: spice\final_output.asc