Twangilizer Theory of Operation

## Description:

The Twangilizer is a Eurorack module that fits in a 3U x 20HP format. It is an “additive synthesis” module that generates four sine waves that are harmonically related to a given input signal.

Using the 8-position rotary switches, the user can select from 8 harmonics (1f – 8f). The resulting signals can be used as-is or can be halved in frequency by the toggle switches. This gives the user many interesting options when creating a sound.

The levels of the resulting harmonics can be adjusted using the front panel potentiometers and/or via the CV inputs. An indicator LED displays the level of the adjustment.

## Inputs:

1. Clock input. Accepts signals > .1V peak-to-peak. 20 – 20KHz. An LED indicates CLK present.
2. CV1 – CV4. Control the level of the harmonics sent to Analog Out. 0-8V range.

## Outputs:

1. Analog Out. Sum of all four harmonics.
2. CLK Outputs 1-4. Digital outputs of the four harmonics. For syncing other modules.

## Several circuit blocks are used to implement the Twangilizer:

1. Power Supply
2. Clock capture
3. Harmonic generators
4. Waveform generators
5. Tracking Filters
6. Signal reconstruction
7. VCAs
8. Digital Outputs
9. Analog Output

## Power Supply

The power connector is “Either Way” but should be tested with a diode tester to make sure the diodes have been installed correctly. BAT54 SCHOTTKY diodes are used. They are rated at 200mA. The +12V rail pulls 100mA max and the -12V rail much less than that. Assuming a total current of 150mA through the package with a worst-case 1V drop, we get a power dissipation of only 150mW. According to the datasheet, derating occurs at 50C, so overheating under normal operating conditions shouldn’t be an issue.

The resulting voltages after the diode drops are typically +11.5V and -11.6V given +/-12V inputs. This leaves enough headroom for the op amps that may need to deal with +/-10V signals.

The +9V rail is derived from the +12V supply. The -9V rail is derived from +9V.

The harmonic and waveform generators use +9V and -9V. These functions require good regulation to achieve a stable waveform. The LM317 used for the +9V requires a certain amount of headroom (see further discussion at end of this document), or else +10V would have been chosen, as the PLLs work best with higher supply voltages. However, 9V is good enough. The -9V rail requires less than 200uA, so an op amp regulator is ideal here.

The symmetry of the waveform depends on the absolute value of the -9V rail being close to the +9V rail. For this reason, .1% resistors were chosen.

Also, the bias point for the VCO pickoff circuits is set by the -9V. This is a sensitive parameter, so it needs to be accurate. A 500ohm trimpot adjusts the +9V rail. With components at their nominal values, an adjustment range of 8.61V – 9.62V is achieved. The nominal adjustment range is skewed so that the worst-case range is adequate and as symmetrical about the 9V value as possible. The results of this are:

1. Set RV1 to 200ohms for 9.01V when all components are nominal.
2. Worst case lower value is 8.76V
3. Worst case upper value is 9.21V

Refer to <lm317.xlsx> for the calculations used in this discussion.

### Tests

1. D1 – D4 correctly installed
2. +12 > 11.4
3. -12 > -11.5
4. Adjust +9V between 8.95V and 9.05V
5. -9V within .5% of +9V magnitude.

## Clock Capture

The clock capture circuit supplies the signal to the harmonic generators. It is spec'd for a signal greater than .1Vpp in amplitude and works in the range of 20Hz – 20KHz.

Refer to [spice\CLK Pickoff.asc](spice/CLK%20Pickoff.asc) for the following discussion.

The input signal is AC coupled and then low-pass filtered. The signal is then given a gain of 46.2 which forms a band pass filter whose characteristics are shown in the graph below.

A blue lines on a white background

Description automatically generated

The -3dB points are approximately 6.6Hz and 50KHz.

This signal is passed to a comparator which has a hysteresis of .94V. The comparator’s trip point is skewed slightly positive from 0V. This prevents the Clock Present LED from lighting when no signal is present due to offset voltage errors inherent in the op amp.

Finally, the signal is sent to a transistor circuit that level-shifts it to a 9V digital wave compatible with the harmonic and waveform generators.

Another transistor circuit drives a “Clock Present” indicator LED.

All tests are performed with a .25Vpp sine wave input.

### Tests

1. CLK waveform good at 20Hz
2. CLK waveform good at 20KHz
3. No CLK at 10Hz
4. No CLK at 30KHz
5. CLK present indicator OFF when no clock is present
6. CLK present indicator ON when clock is present

## Harmonic Generators

The harmonics are generated using phase locked loops with down counters whose outputs are routed to the reset input via the 8 position rotary switches. This arrangement creates a frequency multiplier of 1f – 8f depending on the position of the switch. The signal can be further modified by the toggle switches that follow. These are either connected to the signal or to a flip-flop that divides the frequency in half. When the frequency divider position is chosen, you get the resulting frequencies: 1/2f, 1f, 3/2f, 2f, 5/2f, 3f, 7/2f, 4f.

There is a foible in the circuit when in 1f mode. A race condition exists that sometimes results in the output signal oscillating at around 110KHz. This is fixed by the slight delay added to the 1f position via a 1K resistor and 10pF capacitor.

No testing is needed here unless subsequent stages fail.

If testing is required, the signal can be measured at the center pin of the divide-by-two toggle switches. A 1KHz clock signal is adequate for the following tests.

### Tests

1. CLK signal correct for all 8 rotary switch settings
2. CLK signal correct for both toggle switch settings

## Waveform Generators

The outputs of the Harmonic Generators are fed to the Waveform Generators which create the sinewave approximations. These 10-step waveforms are created by CD4046/CD4017 combinations that are similar to the Harmonic Generators.

But instead of selectable ratios, these circuits are set to multiply by 10. Each output of the CD4017 is sent through a resistor to a summing amplifier. The gain of this amp is set to produce a signal compatible with the next stage. The resulting signal from the Waveform Generators is -3dBm @600 or .547VRMS.

The peak value of the current going into the summing junction is set at 15uA. So, the current will vary from -15uA to +15uA to create a bipolar signal at the output. But, since only positive currents are available from the +9V powered CD4017, a -45uA offset is added using -9V through a 200K resistor. This offset must be accounted for in the resistor calculation.

In the equation below, we see 15uA as the peak current times the sine of the sum of 0-.9 and a phase offset of .125 (to improve wave shape) times 2π. The 45uA offset is added to this value.

Note that the sine calculation is in Radians.

Refer to <wavegen.xlsx> for the following discussion.

Here is the Excel calculation for the ideal resistor values: (see below table)

G =0.000015\*SIN((F?+.125)\*6.2832)+0.000045 *defines current through the resistor*

H =9/G? *defines ideal resistor value*

|  |  |  |
| --- | --- | --- |
| F | G | H |
| 0 | 5.56066E-05 | 161851.2 |
| 0.1 | 5.98153E-05 | 150463.1 |
| 0.2 | 5.83651E-05 | 154201.8 |
| 0.3 | 5.18098E-05 | 173712.4 |
| 0.4 | 4.26534E-05 | 211003.3 |
| 0.5 | 3.43933E-05 | 261678.9 |
| 0.6 | 3.01846E-05 | 298164.8 |
| 0.7 | 3.1635E-05 | 284495.2 |
| 0.8 | 3.81903E-05 | 235661.8 |
| 0.9 | 4.73467E-05 | 190087 |

Real resistor values have been substituted in the following table and graph:

|  |  |  |
| --- | --- | --- |
| I | J | K |
| 162000 | 1.06E-05 | -0.55206 |
| 1.50E+05 | 0.000015 | -0.7845 |
| 1.54E+05 | 1.34E-05 | -0.70299 |
| 1.74E+05 | 6.72E-06 | -0.35167 |
| 2.10E+05 | -2.1E-06 | 0.112071 |
| 2.61E+05 | -1.1E-05 | 0.550052 |
| 3.00E+05 | -1.5E-05 | 0.7845 |
| 2.87E+05 | -1.4E-05 | 0.71343 |
| 2.37E+05 | -7E-06 | 0.367424 |
| 1.91E+05 | 2.12E-06 | -0.1109 |
| 162000 | 1.06E-05 | -0.55206 |
| 1.50E+05 | 0.000015 | -0.7845 |
| 1.54E+05 | 1.34E-05 | -0.70299 |
| 1.74E+05 | 6.72E-06 | -0.35167 |
| 2.10E+05 | -2.1E-06 | 0.112071 |
| 2.61E+05 | -1.1E-05 | 0.550052 |
| 3.00E+05 | -1.5E-05 | 0.7845 |
| 2.87E+05 | -1.4E-05 | 0.71343 |
| 2.37E+05 | -7E-06 | 0.367424 |
| 1.91E+05 | 2.12E-06 | -0.1109 |

J =9/I?-0.000045

K =-52300\*J?

Equation K shows the 52.3K resistor that sets the gain of the summing amplifier.

Dividing the peak value of .7845V by the square root of two results in .555VRMS. The 100pF cap in the feedback filters the high frequency components (-3dB @30KHz) of the signal and reduces the amplitude to near the desired .547VRMS.

The Tracking Filters in the next section take their input from the VCO pins of the CD4046s. The response of the PLLs must be adjusted to work with the Tracking Filters. Set the input clock frequency to 1KHz and adjust the pot until a voltage of -4.2V is measured at the VCO pickoff test points. (TP8 – TP11).

### Tests (measured at TP4 – TP7)

1. OSC waveform good at 20Hz
2. OSC waveform good at 20KHz

## Tracking Filters

The job of the tracking filters is to produce sine waves from the approximate waveforms formed by the Waveform Generators described above. The tracking filters use the VCO in of the PLL chips to sense the frequency and set the corner frequency of the filters as required.

The CD4046 phase locked loop IC has a capture range defined by the RC combination of the cap that appears between pins 6 and 7 and the resistor chain that is connected to pin 11. With a resistor that has a nominal value of 35K (10K plus half the 50K of the trimpot) and a capacitor of 300pF, you get a center frequency around 100KHz when the circuit is configured as a 10f multiplier. See fig. 5 in the data sheet.

Increasing RC reduces the upper capture point and increases the slope of the pickoff curve.

The graph below shows the pickoff level vs. the input clock frequency.

The filters use a signal that ranges from -10VDC to +10VDC to set their cutoff frequency. The table below shows the Ideal curve which was empirically derived. It also shows the results measured from a v0.0 Twangilizer and a circuit on the PBJ protoboard. Finally, it shows the computed curve.

Refer to [VCO Pickoff Meas.xlsx](VCO%20Pickoff%20Meas.xlsx) for the following data.

|  |  |  |  |
| --- | --- | --- | --- |
| Freq | Ideal | VCO Pickoff | Computed |
| 5000 | 10.2 | 2.51 | 15.18 |
| 4000 | 10 | 2.22 | 9.96 |
| 3000 | 5 | 1.94 | 4.92 |
| 2000 | 0 | 1.67 | 0.06 |
| 1000 | -5 | 1.4 | -4.8 |
| 500 | -7.62 | 1.25 | -7.5 |
| 250 | -9.06 | 1.16 | -9.12 |
| 100 | -9.88 | 1.07 | -10.74 |
| 50 | -10.17 | 1.02 | -11.64 |
| 20 | -10.17 | 0.954 | -12.828 |

Planned =(Pickoff\*17)-28The resulting curve for the tracking filters looks something like the following measured trace:

The signal from the VCO is not a pure DC signal. It contains pulses that continually correct the output frequency. These pulses must be filtered lest they affect the output signal. A single stage filter with a cutoff frequency of 6.8KHz accomplishes this task. The 499K pickoff resistor and a 47pF cap is used.

A spreadsheet that was used to select resistor values is found here: [VCO Pickoff Plan.xlsx](VCO%20Pickoff%20Plan.xlsx)

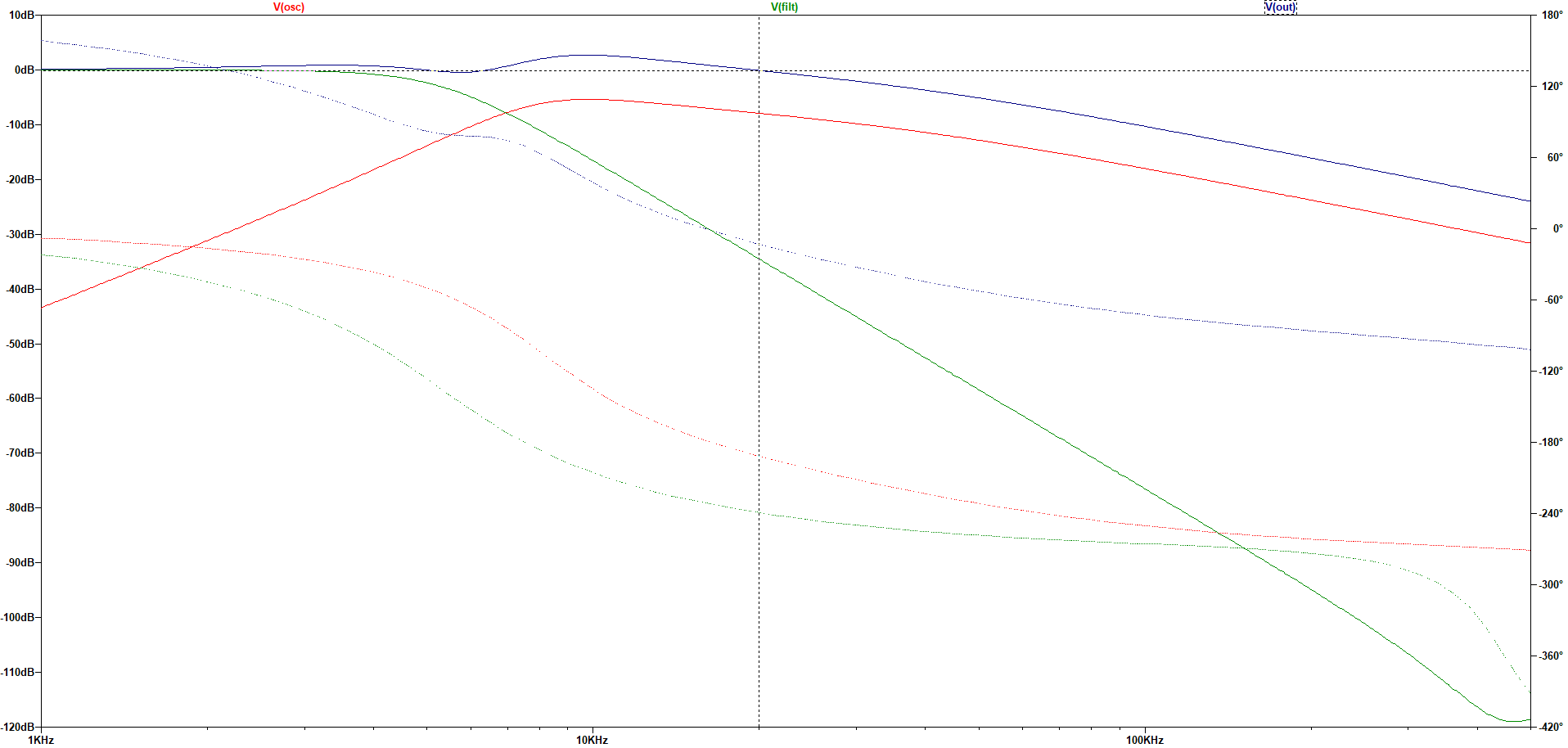
## Signal Reconstruction

Because the requirement is for an output signal that spans 20Hz through 20KHz and the tracking filters produce a signal that is truncated above 5KHz, a method to handle the higher frequencies must be found.

The output of a high pass filter sourced by the Waveform Generators can be summed with the tracking filter output to accomplish this. The hi pass filter was designed to produce the flattest possible response when summed with the output of the tracking filters. Because the tracking filters have an approximate 7dB gain, the sum of the two filters must be weighted appropriately to get the best response.

The parameters of this filter are as follows: *High-Pass; 2nd order Chebyshev 2.4dB*

*-3dB @6KHz -24dB @ 2KHz*

The plot below shows the LT Spice simulation: (from [spice\VCF model.asc](spice/VCF%20model.asc))

### Tests

Measure at TP12 – TP19

1. 1f waveform good at 20Hz CLK
2. 1f waveform good at 20KHz CLK
3. Measure 50Hz at 100Hz CLK for 1f/2
4. 2f waveform good at 20Hz CLK
5. 2f waveform good at 10KHz CLK
6. 3f waveform good at 20Hz CLK
7. 3f waveform good at 6.67KHz CLK
8. 4f waveform good at 20Hz CLK
9. 4f waveform good at 5KHz CLK
10. 5f waveform good at 20Hz CLK
11. 5f waveform good at 4KHz CLK
12. 6f waveform good at 20Hz CLK
13. 6f waveform good at 3.33KHz CLK
14. 7f waveform good at 20Hz CLK
15. 7f waveform good at 2.86KHz CLK
16. 8f waveform good at 20Hz CLK
17. 8f waveform good at 2.5KHz CLK

### VCAs

Now that the frequency of the harmonic has been set and the tracking filter has turned the output of the waveform generator into a sine wave, the level must be set. This is accomplished using a voltage-controlled amplifier.

See [spice\VCA.asc](spice/VCA.asc)

There are two control inputs to the VCA, one from the CV input jack which is protected in the usual way with a 510ohm resistor and a BAT54S; and one set by the CV bias potentiometer. The 510ohms is small enough in resistance to be insignificant to the 120K input.

Since the bias pot uses +9V as its reference, the voltage divider is adjusted to match the range of the CV input by the 150K resistor. In either case, this sets the full-scale voltage value at the non-inverting input of the op amp to be 5V. This implies 5V at the inverting input which sets an LED current of 250uA. (5V / 20K)

When the CV bias pot is used in conjunction with the CV input, the bias sets a current level that is increased by the CV input only when it exceeds the voltage level of the CV bias. A transfer function curve of CV input vs LED current best illustrates this. The bias pot is set to 50% in this example.

A graph with a line

Description automatically generated

Here we see the LED current at 125uA until the CV input is greater than 2.5V. This is because diode D4 does not conduct until the CV input exceeds 2.5V. The current then increases with CV until the maximum of 250uA is reached.

With the CV bias set to 100%, the base current will be 250uA. In this case the CV input will increase the current to a maximum of 330uA with the increase starting when the CV input exceeds 5V.

In the above example, the slight upturn when CV input is greater than 7V occurs when D3 becomes reverse biased.

BAT54 Schottky diodes are placed in series with the sense resistors to minimize interaction due to resistive loading. According to the manual, the maximum leakage current of a BAT54 at 25V is 2uA. The worst-case condition in this circuit is 10V. The manual indicates the typical leakage at 10V is .1uA. The manual also states that, for the current this circuit will experience, the diodes will have a forward voltage drop of only .12V. Conveniently, these are the values that are used by the Spice simulator.

The VCA circuit uses a vactrol as the controlled element. The NSL-32SR3 has a nominal resistance of 600 ohms with an LED current of 250uA. The output of the Signal Reconstruction element is approximately 3.5Vp-p. This must be raised to the specified output level of 10Vp-p. This implies a gain of 2.86 which is realized by the 1K in series with the 2K trimpot at 50% divided by the 600 ohms of the full-scale resistance of the vactrol.

This also gives a transfer function of roughly 1V at CVin equals 1Vpp at Analog Out.

An indicator LED is put in series with the vactrol LED as an indication of the control voltage level.

### Tests

Measure at Analog Output, CLK input 1000Hz.

1. 0V CV, bias adjustment off. Measure < .1VRMS.
2. 1V CV, bias adjustment off. Measure 1Vpp +/-2%
3. 8V CV, bias adjustment off. Measure 8Vpp +/-2%
4. 0V CV, bias adjustment 50%. Measure 5Vpp +/-5%
5. 0V CV, bias adjustment 100%. Measure 10Vpp +/-5%

### Digital Outputs

The digital outputs are +5V square waves generated from the outputs of the Harmonic Generators. These outputs are 9V square waves and must be level-shifted to the required 5V. The 9V signal is reduced to 4.9V by a resistive divider formed by 10K and 12K resistors. This is fed into the non-inverting input of an op amp.

A 20pF capacitor from the non-inverting input to ground limits the slew rate of the input signal which minimizes ringing at the output.

The output is protected by the usual 510 ohm/BAT54S combination.

### Analog Output

The analog output is the sum of the four VCA outputs. It is followed by a 4th order Butterworth 20KHz low pass filter. The output is protected by the usual 510ohm/BAT54 circuit.

The curve of the filter is modeled in the file: [spice\final\_output.asc](spice/final_output.asc)

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Description automatically generated

### Further Discussion

1. The LM317 manual states that 3V of headroom is recommended to maintain maximum current without overheating. However, the 9V circuitry of the Twangilizer draws very little current. The manual also states that the part requires greater than 1.25V headroom. Giving the part 1.5V of headroom at minimum means that the +12V rail (after the reverse protection diode) has to be at least 10.5V. This translates to an input of 11V or greater, which is easily realizable in Eurorack systems.