



SOROTI UNIVERSITY

SCHOOL OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING
MAY 2024 SEMESTER FINAL EXAMINATIONS

COURSE UNIT: CONTROL SYSTEMS ENGINEERING

COURSE CODE: EEE3205

SEMESTER: II

DATE: Thursday, 16th May 2024

TIME: 09:00am - 12:00pm

GENERAL INSTRUCTIONS:

1. Fill in the required information on your answer booklet (Student ID No, date, etc.)
2. The paper consists of FIVE questions.
3. Answer ANY FOUR questions.
4. Each question carries 25 marks.
5. A formula sheet is attached.
6. A semi-log paper and graph paper are provided.
7. All plots must be carefully drawn with axes labelled.
8. You may use an electronic calculator if it has neither a facility for textual storage nor graphical display.

QUESTION ONE

(a) Define the following.

- i. Control system. [1]
- ii. Signal flow graph. [1]

(b) Compare an open-loop and closed-loop system. [4]

(c) State the advantage of Mason's gain rule over block diagram reduction technique. [2]

(d) A control system is shown in Fig. Q1(d).

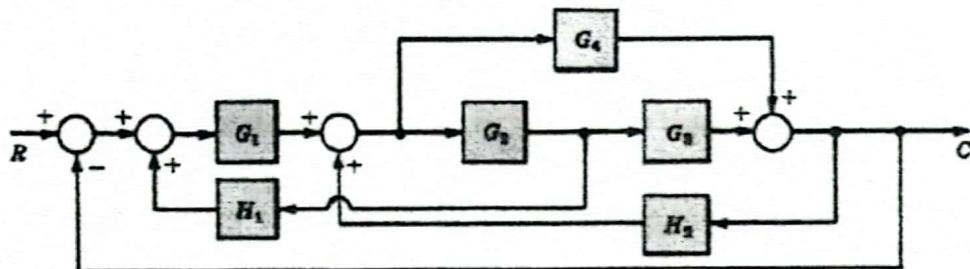


Fig. Q1(d)

- i. Draw the corresponding signal flow graph. [2]

- ii. Determine the transfer function $\frac{C(s)}{R(s)}$ using Masons' gain rule. [5]

(e) Derive the transfer function, $G(s) = \frac{x_1(s)}{F(s)}$ of the translational mechanical system shown in

Fig. Q1(e). Draw all the necessary free body diagrams [10]

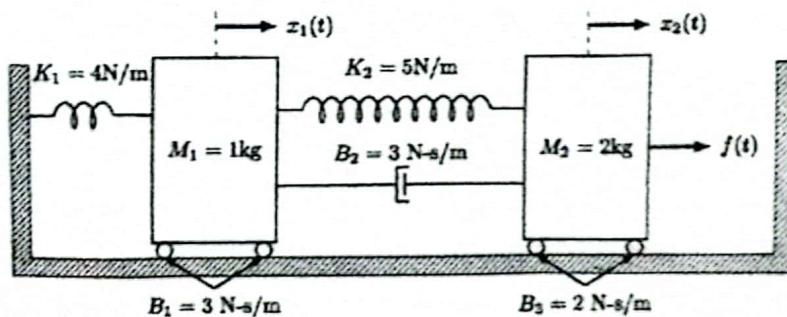


Fig. Q1(e)

QUESTION TWO

(a) Define the following.

- i. Transient response. [1]
- ii. Steady-state response. [1]
- iii. Percentage maximum overshoot. [1]
- iv. Settling time. [1]

(b) The block diagram of a first order system is given in Fig. Q2(b). Suppose a unit step input is applied at the input, $R(s)$.

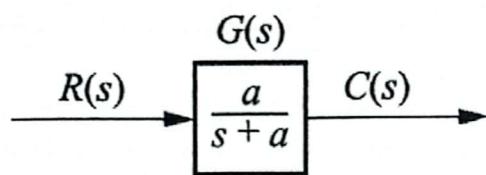


Fig. Q2(b)

- i. Find the Laplace Transform and the inverse Laplace transform of its step response. [2]
 - ii. Formulate the time constant of the system. [3]
- (c) Sketch a graph showing the following parameters associated with the underdamped response of a second order system. [3]
- i. Rise time
 - ii. Peak time
 - iii. Settling time

(d) Consider the system shown in Fig. Q2(d)1. To improve the performance of the system, feedback is added to the system, which results in Fig. Q2(d)2.

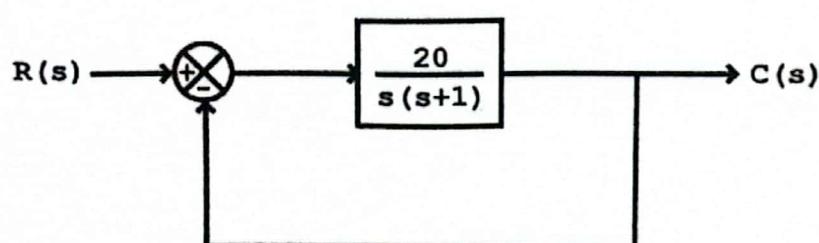


Fig. Q2(d)1

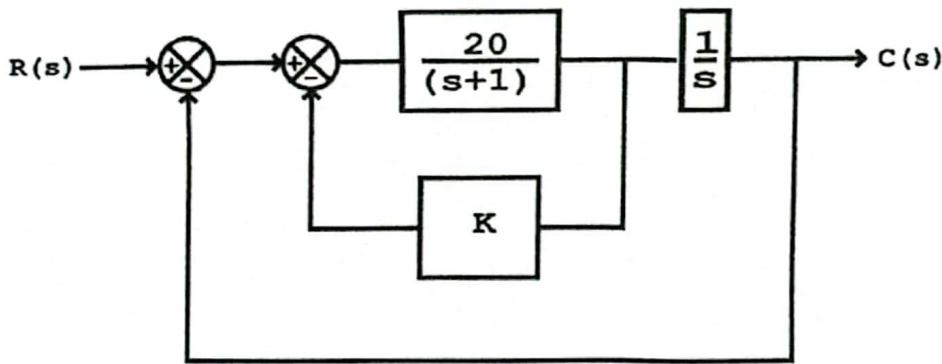


Fig. Q2(d)2

- Determine the value of K such that the damping ratio of the new system is 0.4. [3]
- Compare the overshoot, rise time, peak time and settling time of the two systems.

[10]

QUESTION THREE

- (a) Define a root locus. [1]
- (b) Give two advantages of the root locus method. [2]
- (c) A unity feedback system is characterized by the open-loop transfer function,

$$G(s) = \frac{k}{(s+2)(s^3 + 10s^2 + 49s + 100)}$$

- i. Using Routh's stability criterion, calculate the range of values of K for the system to be stable. [4]
- ii. Determine the value of K , which will cause sustained oscillations in the closed-loop system. [1]
- iii. Compute the frequency of sustained oscillations. [2]

(d) A block diagram of the bank angle controller for an airplane is given in Fig. Q3(d).

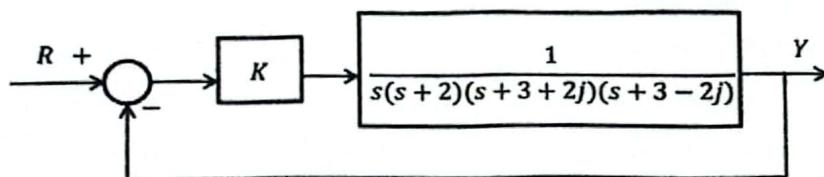


Fig. Q3(d)

- i. Sketch the root locus of the system, showing all your working. [10]
- ii. Define the range of values of K that causes the system to be unstable. [1]
- iii. Calculate the angles of departure of the complex poles. [2]
- iv. Write a simple MATLAB code to obtain the root locus of the system. [2]

QUESTION FOUR

(a) Define the following.

- i. Frequency response. [1]
- ii. Decibel. [1]
- iii. Gain margin. [1]

(b) A transfer function is given below.

$$G(s) = \frac{100(s + 10)}{s(s + 20)(s^2 + 4s + 16)}$$

- i. Using the semi log paper provided, sketch the Bode plot of the transfer function. [8+7]
- ii. Obtain the:
 - a. Gain cross-over frequency. [1]
 - b. Phase cross-over frequency. [1]
 - c. Gain margin [1]
 - d. Phase margin [1]
- iii. Using the values obtained in Q4 (b)(ii), comment on the stability of the system. [1]
- iv. Write a MATLAB code to obtain the Bode plot of the system. [2]

QUESTION FIVE

- (a) State one advantage and one disadvantage of a proportional controller. [2]
- (b) Using suitable equations and block diagrams, explain the following types of controllers employed in control systems.
- PD controller. *in time domain* [3]
 - PID controller. ** forward ** [3]
- (c) State the significance of the following in a PID controller.
- Proportional controller. [1]
 - Integral controller. [1]

- (d) A control system is represented by a block diagram shown in Fig. Q5(d), where a PID controller is used to control the system. The PID controller has the transfer function of

$$G_c(s) = K_p \left(1 + \frac{1}{T_i s} + T_d s \right)$$

To design a PID controller, the second method of Ziegler-Nichols is used for the determination of the values of parameters, $K_p = 0.6K_{cr}$; $T_i = 0.5P_{cr}$ and $T_d = 0.125P_{cr}$.

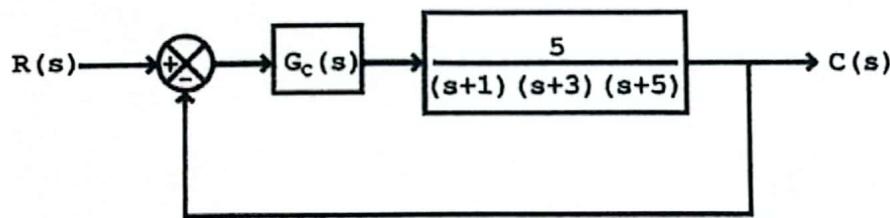


Fig. Q5(d)

- Solve for K_p , T_i and T_d *standard form* [9]
- Reconstruct the block diagram with the new $G_c(s)$ [2]
- Evaluate the transfer function $\frac{C(s)}{R(s)}$ [4]

ATTACHMENT: COMMONLY USED FORMULAS

Mason's gain rule	$G(s) = \frac{C(s)}{R(s)} = \frac{1}{\Delta} \sum_{k=1}^n P_k \Delta_k$ <p>where:</p> <p>P_k = kth forward path gain $\Delta = 1 - \sum$ individual loop gains + \sum nontouching loop gains taken two at a time - \sum nontouching loop gains taken three at a time $\Delta_k = 1 - \sum$ loop gains which don't touch the forward path</p>		
Laplace transform	1	\xleftrightarrow{LT}	$\frac{1}{s}$
	$e^{-at}u(t)$	\xleftrightarrow{LT}	$\frac{1}{s+a}$
Transfer function of a second order system	$G(s) = \frac{\omega_n^2}{s^2 + 2\varepsilon\omega_n + \omega_n^2}$		
Transient response specifications of a second order system	<p>Rise time:</p> $T_r = \frac{\pi - \theta}{\omega_n \sqrt{1 - \xi^2}}; \quad \theta = \tan^{-1} \left(\frac{\omega_n \sqrt{1 - \xi^2}}{\xi \omega_n} \right)$ <p>Peak time:</p> $T_p = \frac{\pi}{\omega_n \sqrt{1 - \xi^2}}$ <p>Percentage maximum overshoot:</p> $\%OS = e^{-\left(\frac{\pi\xi}{\sqrt{1-\xi^2}}\right)} \times 100\%$ <p>Settling time:</p> $T_s = \frac{4}{\xi \omega_n}$		



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**SCHOOL OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING
2023/2024 SEMESTER TWO TEST NO.1**

COURSE UNIT: CONTROL SYSTEMS ENGINEERING

COURSE CODE: EEE3205

SEMESTER: II

DATE: Wednesday, 12th March 2024

TIME: 08:20am - 09:50am

LECTURER: Mr. Ivan Tim Oloya

INSTRUCTIONS:

1. *Fill in the required information on your answer booklet (Student ID No, date, etc.)*
2. *Answer all the questions.*
3. *You may use an electronic calculator if it has neither a facility for textual storage nor graphical display.*

[Question]

(a) Define the following, citing a suitable example.

- i. Open-loop system [2]
- ii. Closed-loop system [2]

(b) Draw a rough sketch of the above two systems, with clear labels of all the parts. [4] *not*

(c) Reduce the block in Fig. 1c to a single transfer function. *(using Mason's rule)* [9]

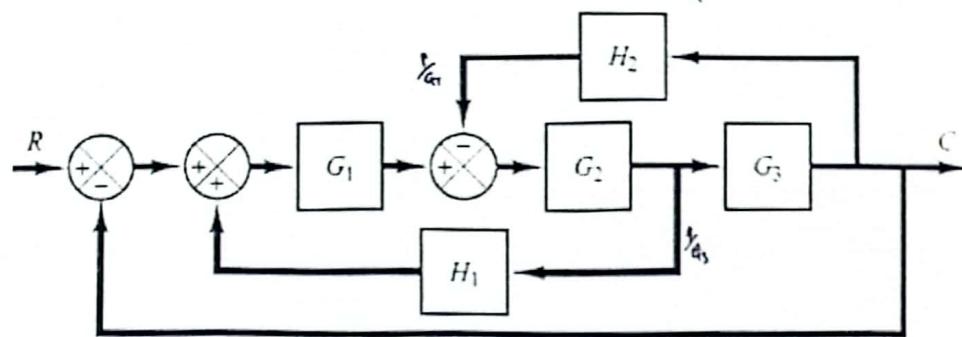


Fig. 1c

(d) Convert the block diagram in Fig. 1c to a signal-flow graph. [4]

(e) Using Mason's rule, obtain the Transfer function for the signal-flow graph obtained in question 1(d). $\frac{1}{\Delta} \sum P_a Q_a$ [4]

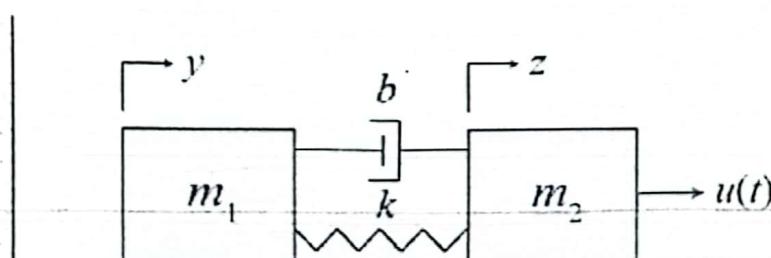
[Question Two]

(f) State one advantage and one disadvantage of the following.

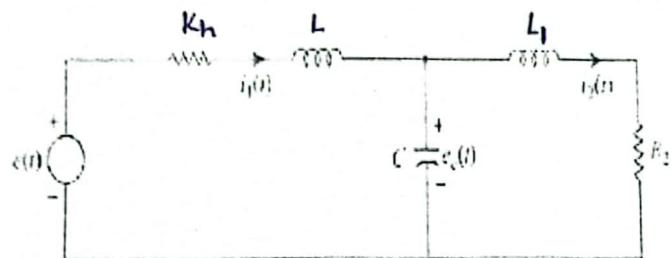
- i. Frequency-domain modelling *- easy to deal with* [2]
- ii. Time-domain modelling *- complex* [2]

Design a state space equation for the following systems:

- i. [6]



- ii. [5]



[Question Three]

- (a) For the block diagram shown in Fig. 3a. Determine the value of gain K and velocity-feedback constant K_h so that the maximum percentage overshoot in the unit step response is 0.1 and the peak time is 0.5s. With these values of K and K_h , obtain the rise time and settling time. Assume $J = 1 \text{ kg} - \text{m}^2$ and $B = 1 \text{ Nms/rad}$

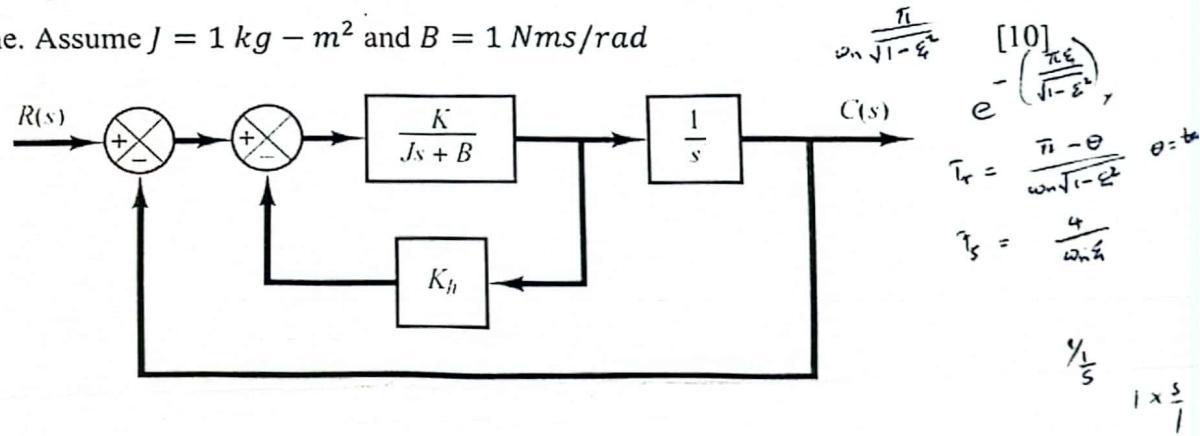


Fig. 3a



SOROTI UNIVERSITY

SCHOOL OF ENGINEERING AND TECHNOLOGY DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING 2023/2024 SEMESTER TWO TEST NO.2

COURSE UNIT: CONTROL SYSTEMS ENGINEERING

COURSE CODE: EEE3205

SEMESTER: II

DATE: Wednesday, 24th April 2024

TIME: 2.00pm – 3:30pm

LECTURER: Mr. Ivan Tim Oloya

INSTRUCTIONS:

1. Fill in the required information on your answer booklet (Student ID No, date, etc.)
2. Answer all the questions.
3. You may use an electronic calculator if it has neither a facility for textual storage nor graphical display.

[Question One]

(a) Consider the following system.

$$G(s) = \frac{K}{s(s+1)(s^2 + 4s + 5)} \quad H(s) = 1, K \geq 0$$

- i. Draw the root locus of the system, showing all your work. [10]
- ii. Are there complex poles? If yes, what are the angles of departure. [2]
- iii. What are the range of values of K to ensure stability of the system. [1]
- iv. Write a simple MATLAB code to obtain the root locus of the system. [2]

[Question Two]

(a) Define the following.

- i. Gain cross-over frequency. [1]
- ii. Phase margin [1]

(b) A transfer function given below.

$$G(s) = \frac{4}{s(s+1)(s+2)}$$

- i. Using the semi-log paper provide, sketch the Bode plot of the transfer function. [8]

(c) Obtain the following.

- i. Gain cross-over frequency. [1]
- ii. Phase cross-over frequency. [1]

(d) Using the values obtained in (b) i, comment on the stability of the system. [1]

(e) Write a simple MATLAB code to obtain the bode plot of the system

[Question Three]

(a) A PID controller is used to control the system below.

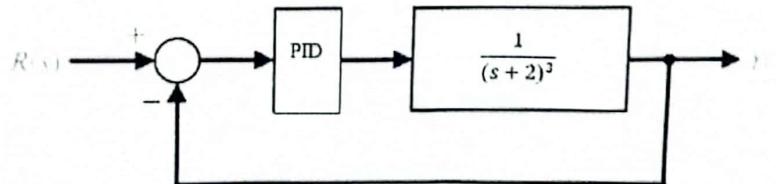


Fig. 3a

Fig.

0.015

$$T_i = \frac{k_p}{k_i} \quad T_d = \frac{k_d}{k_p}$$

- i. Using Ziegler-Nichols tuning rule, determine the values of the parameters K_p, T_d, T_i . [8]
- ii. Obtain the transfer function of the PID controller. [2]
- iii. What are the locations of the poles and zeros? [1]

Formulae:

Type of Controller	K_p	T_i	T_d
P	$0.5K_{cr}$	∞	0
PI	$0.45K_{cr}$	$\frac{1}{1.2}P_{cr}$	0
PID	$0.6K_{cr}$	$0.5P_{cr}$	$0.125P_{cr}$

$$G_c(s) = 0.075k_{cr}p_{cr} \left(\frac{s + \frac{4}{p_{cr}}}{s} \right)^2$$

$$\rho_{cr} = \frac{2\pi}{\omega_{cr}}$$

$$\gamma_m = \frac{\Sigma \text{poles} - \Sigma \text{zeros}}{n-m}$$

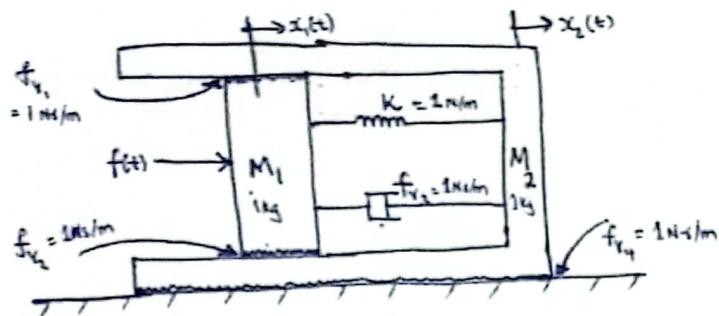
$$\theta_m = \frac{(2k+1)180}{n-m}$$

$$\theta_{pole} = 180 - \sum \text{other pole angles} + \sum \text{other zero angles}$$



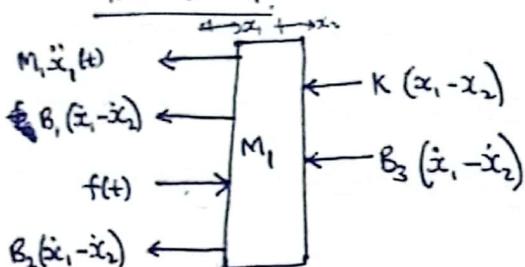
$$C_p = K_p e^{j\theta_m}$$

$$K_p = \frac{C_p}{e^{j\theta_m}}$$



$$\text{let } f_{v_1} = B_1, f_{v_2} = B_2, f_{v_3} = B_3, f_{v_4} = B_4$$

Forces on M_1 :



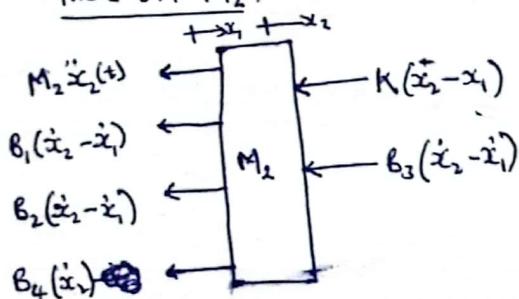
$$f(t) = M_1 \ddot{x}_1(t) + B_1 [\dot{x}_1(t) - \dot{x}_2(t)] + B_2 [\dot{x}_1(t) - \dot{x}_2(t)] + B_3 [\dot{x}_1(t) - \dot{x}_2(t)] + K [x_1(t) - x_2(t)]$$

$$F(s) = M_1 s^2 X_1(s) + B_1 s X_1(s) - B_1 s X_2(s) + B_2 s X_1(s) - B_2 s X_2(s) + B_3 s X_1(s) - B_3 s X_2(s) + K X_1(s) - K X_2(s)$$

$$F(s) = [M_1 s^2 + B_1 s + B_2 s + B_3 s + K] X_1(s) - [B_1 s + B_2 s + B_3 s + K] X_2(s)$$

$$F(s) = [s^2 + 3s + 1] X_1(s) - [3s + 1] X_2(s) \quad \text{--- (1)}$$

Forces on M_2 :



$$M_2 \ddot{x}_2(t) + B_1 [\dot{x}_2(t) - \dot{x}_1(t)] + B_2 [\dot{x}_2(t) - \dot{x}_1(t)] + B_3 [\dot{x}_2(t) - \dot{x}_1(t)] + B_4 [\dot{x}_2(t)] + K [x_2(t) - x_1(t)] = 0$$

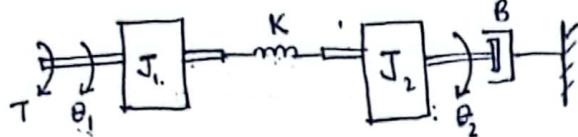
$$[M_2 s^2 + B_1 s + B_2 s + B_3 s + B_4 s + K] X_2(s) - [B_1 s + B_2 s + B_3 s + B_4 s + K] X_1(s) = 0$$

$$X_1(s) = \frac{[s^2 + 3s + 1] X_2(s)}{[3s + 1]} \quad \text{--- (2)}$$

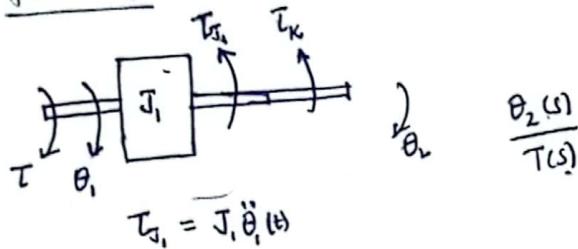
Sub X_1 in (1)

$$\frac{F(s)}{X_2(s)} = \frac{(s^2 + 3s + 1)(s^2 + 4s + 1) - (3s + 1)(3s + 1)}{3s + 1} = \frac{(s^4 + 7s^3 + 14s^2 + 7s + 1) - (9s^2 + 6s + 1)}{3s + 1}$$

$$\frac{X_2(s)}{F(s)} = \frac{3s + 1}{s^4 + 7s^3 + 5s^2 + s} = \frac{3s + 1}{s(s^3 + 7s^2 + 5s + 1)}$$



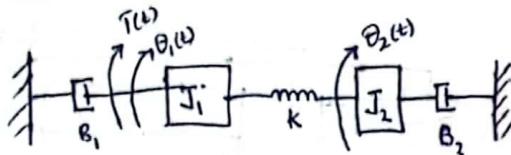
free body:



$$T_{J_1} = J_1 \ddot{\theta}_1(t)$$

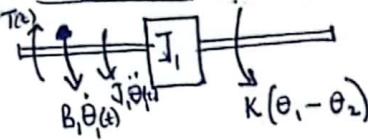
$$T_K = K[\theta_1(t) - \theta_2(t)]$$

$$\frac{\theta_2(s)}{T(s)}$$



freebody:

Torque on J1:



$$T(t) = J_1 \ddot{\theta}_1(t) + B_1 \dot{\theta}_1(t) + K(\theta_1 - \theta_2)$$

$$T(s) = J_1 s^2 \theta_1(s) + B_1 s \theta_1(s) + K \theta_1(s) - K \theta_2(s)$$

$$T(s) = [J_1 s^2 + B_1 s + K] \theta_1(s) - K \theta_2(s) \quad \text{--- (1)}$$

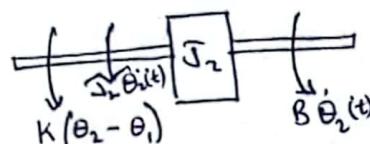
$$T(t) = T_{J_1} + T_K$$

$$T(t) = J_1 \ddot{\theta}_1(t) + K[\theta_1 - \theta_2]$$

$$T(s) = J_1 s^2 \theta_1(s) + K[\theta_1(s) - \theta_2(s)]$$

$$T(s) = [J_1 s^2 + K] \theta_1(s) - K \theta_2(s) \quad \text{--- (1)}$$

Torque on J2:



$$[J_1 \ddot{\theta}_1(t) + B_1 \dot{\theta}_1(t) + K[\theta_1 - \theta_2]] = 0$$

$$[J_1 s^2 \theta_1(s) + B_1 s \theta_1(s) + K \theta_1(s) - K \theta_2(s)] = 0$$

$$[J_1 s^2 \theta_1(s) + B_1 s \theta_1(s) - K \theta_1(s)] = 0$$

$$\theta_1(s) = \frac{[B_1 s + K]}{J_1 s^2 + B_1 s} \theta_2(s)$$

$$\frac{T(s)}{\theta_2(s)} = \frac{[J_1 s^2 + B_1 s + K]}{K} \frac{[B_2 s + K]}{[J_1 s^2 + B_1 s + K]} - K^2$$

$$\frac{\theta_2(s)}{T(s)} = \frac{K}{[J_1 s^2 + B_1 s + K] [B_2 s + K] - K^2}$$

$$\frac{\theta_2(s)}{T(s)} = \frac{K}{[J_1 s^2 + B_1 s + K] [J_2 s^2 + B_2 s + K] - K^2}$$

$$\theta_1(s) = \frac{[J_2 s^2 + B_2 s + K]}{K} \theta_2(s)$$

Sub $\theta_1(s)$ in (1)

$$\frac{T(s)}{\theta_2(s)} = \frac{[J_1 s^2 + K] [J_2 s^2 + B_2 s + K] - K^2}{K}$$

CSE

$$\frac{\theta_2(s)}{T(s)} = \frac{K}{[J_1 s^2 + B_1 s + K] [J_2 s^2 + B_2 s + K] - K^2}$$

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SOROTI UNIVERSITY

COHORT 2020

TEST I FOR

33
BONGO JOSHUA
2001600003

BACHELOR OF ENGINEERING IN ELECTRONICS AND COMPUTER ENGINEERING

DATE:	THURSDAY 4 TH APRIL 2024
TIME:	02:00 p.m. to 03:00 p.m (1 Hour)
YEAR OF STUDY: III	SEMESTER: II
COURSE CODE:	CPE3204
COURSE TITLE:	COMPUTER ARHITECTURE AND ORGANIZATION

INSTRUCTIONS

1. This paper comprises of 2 (Two) sections A and B. Attempt ALL questions in both sections.
2. Circle the correct alternative in section A. Answers to section B must be written in the answer sheets provided.
3. Neat Work is a MUST

SECTION A (Circle the correct alternative) – 20 Marks

1. What is computer architecture?
 A. set of categories and methods that specify the functioning, organisation, and implementation of computer systems

B. set of principles and methods that specify the functioning, organisation, and implementation of computer systems

C. set of functions and methods that specify the functioning, organisation, and implementation of computer systems

D. None of the mentioned behaviour of function modes

2. What is computer organization?

A. structure and behaviour of a computer system as observed by the user

B. structure of a computer system as observed by the developer

C. structure and behaviour of a computer system as observed by the developer

D. All of the mentioned

3. Which of the following is a type of architecture used in the computers nowadays?
 A. Microarchitecture B. Harvard Architecture
 C. Von-Neumann Architecture D. System Design
4. Which of the following is the subcategories of computer architecture?
 A. Microarchitecture B. Instruction set architecture
 C. Systems design D. All of the mentioned
5. Which of the architecture is power efficient?
 A. RISC B. ISA C. IANA D. CISC
6. The circuit used to store one bit of data is known as _____
 Register B. Encoder C. Decoder D. Flip Flop
7. $(2FAOC)_{16}$ is equivalent to _____
 A. $(195\ 084)_{10}$ B. $(00101111010\ 0000\ 1100)_2$
 C. Both A and B D. None of these
8. The average time required to reach a storage location in memory and obtain its contents is called
 A. seek time B. turnaround time C. access time D. transfer time
9. Which of the following is lowest in memory hierarchy?
 A. Cache memory B. Secondary memory C. Registers D. RAM
 E. None of the above
10. A three input NOR gate gives logic high output only when all inputs are low
 A. one input is high B. one input is low
 C. two inputs are low D. all inputs are high
11. _____ register keeps tracks of the instructions stored in program stored in memory.
 Address Register B. Index Register C. Program Counter D. Accumulator
12. Logic gates with a set of input and outputs is arrangement of _____
 A. Combinational circuit B. Logic circuit C. Design circuits D. Register
13. A group of bits that tell the computer to perform a specific operation is known as
 A. Instruction code B. Micro-operation C. Accumulator D. Register
14. A microprogram sequencer _____
 A. generates the address of next micro instruction to be executed.
 B. generates the control signals to execute a microinstruction.
 C. sequentially averages all microinstructions in the control memory.
 D. enables the efficient handling of a micro program subroutine.

15. A flip-flop is a binary cell capable of storing information of _____
 A. One bit B. Byte C. Zero bit D. Eight bit
16. An interface that provides a method for transferring binary information between internal storage and external devices is called....
 A. I/O interface B. Input interface C. Output interface D. I/O bus
17. Status bit is also called _____
 A. Binary bit B. Flag bit C. Signed bit D. Unsigned bit
18. An address in main memory is called _____
 A. Physical address B. Logical address C. Memory address D. Word address
19. The 2s compliment form (Use 6-bit word) of the number 1010 is _____
 A. 111100. B. 110110. C. 110111. D. 1011.
$$\begin{array}{r} 0001010 \\ 1110101 \\ + \quad 1 \\ \hline 0110 \end{array}$$
20. What is the content of Stack Pointer (SP)?
 A. Address of the current instruction
 B. Address of the next instruction
 C. Address of the top element of the stack
 D. Size of the stack.

SECTION B (Answer in the answer sheets provided) – 20 marks

21. (a) Explain the four major components of the computer structure, highlighting their functions. [8 marks]
- (b) Briefly explain the process a character typed on the keyboard goes through to be displayed on the computer monitor [2 marks]
22. (a) Convert the following arithmetic expression into postfix form:
 $A+B-C*E/F+B*D$ [5 marks]
- (b) Evaluate the post fix expression: [5 marks]

8 2 3 ^ / 2 3 * + 5 1 * -

END OF QUESTION PAPER

SECTION B

- 21 : (b) - When a character on a keyboard is pressed, electronic signal is transmitted to the system unit of the computer.
- The electronic signal is then converted in ASCII codes, and then stored in memory for processing.
- After processing, the ASCII code is converted in an image.
- The image is then outputted and displayed on the computer's monitor.

10

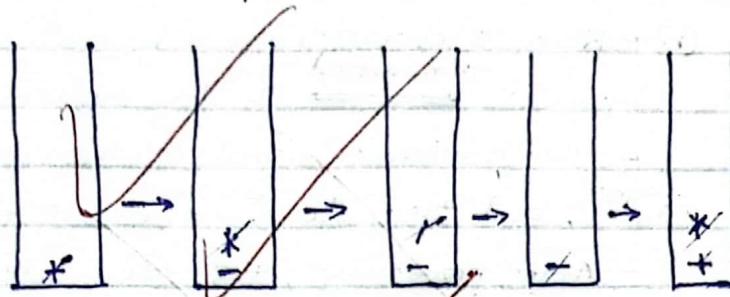
- (a) ① CPU (Central processing unit): This is the main component that controls the execution and operation of instructions and operation of other components of the computer.
- It executes instructions and performs computations and comparisons.
- ② Primary memory: This is also known as the main memory. It is a storage medium that can be used to temporarily store information that is being used by the computer, this kind is called RAM (Random Access Memory).
ROM is also a primary memory used to store info permanently to store information that is used during the running of the computer.
- ③ Secondary memory: This is a mass storage medium that is used to store data or information permanently. This may be data that is not currently in use. It is slower than the main memory components. It stores large ^{size} amount of data, and can be used for backup.
- ④ System Bus: This is a set of connecting conductors that connects the CPU (processor) with other components of the computer. This can be used to convey information such as memory address, control signal, and data.

"importance/
significance/
why we need
RAID system".

22 : (a)

RAID (Redundant Array of Independent Drives)

$$A + B - C * E / F + B * D$$



$$= AB + CE * F / - BD * +$$

0

(b)

$$823 \uparrow 23 * + 51 * -$$

$$= 8(2^3) / (2 * 3) + (5 * 1) -$$

$$= 88 / 6 + 5 -$$

$$= (8/8).6 + 5 -$$

$$= 16 + 5 -$$

$$= (1+6) 5 -$$

$$= 7 5 -$$

$$= 7 - 5$$

$$= 2$$



SOROTI UNIVERSITY
SCHOOL OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING

MAY 2024 SEMESTER EXAMINATIONS FOR
BACHELOR OF ENGINEERING IN ELECTRONICS AND
COMPUTER ENGINEERING (BENG ECE)
COHORT 2020

DATE: FRIDAY 17TH MAY 2024
TIME: 09:00 a.m. to 12:00 noon. (3 Hours)
YEAR OF STUDY: III **SEMESTER:** II
COURSE CODE: CPE 3204
COURSE TITLE: COMPUTER ARCHITECTURE AND ORGANIZATION

INSTRUCTIONS

1. This paper comprises of **SIX (6)** questions.
2. Answer **ANY FIVE (5)** questions of your choice.
3. All your answers **MUST** be written in the answer book provided.
4. Neat Work is a **MUST**.

**THIS PAPER MUST NOT BE OPENED UNTIL PERMISSION HAS BEEN
GIVEN BY THE INVIGILATOR**

✓ QUESTION 1 (20 Marks)

Binary numbers are useful in computer systems, where each binary digit (*bit*) can be represented by one state of a “binary switch” that is either on or off. However, binary numbers are hard to read, partly because of their great length, so we explore other ways in which numbers can be represented.

Required:

- (a) Showing all the steps involved, convert the binary number $(\underline{101} \underline{010} \underline{101} \underline{11})_2$ to:
- (i) Octal. [3 marks]
 - (ii) Decimal. [3 marks]
 - (iii) Hexadecimal. [3 marks]
- (b) Showing all the steps involved, express the hexadecimal number $(4FB2)_{16}$ in:
- (i) Binary. [3 marks]
 - (ii) Decimal format. [3 marks]
- (c) Form the two's complement of the binary number $(111011101110)_2$. [3 marks]
- (d) Find the 8421BCD format representation of the decimal number 25.48. [2 marks]

✓ QUESTION 2 (20 Marks)

- (a) What is an instruction format? [2 marks]
- (b) Describe the most common fields of instruction formats. add more [6 marks]
- (c) With examples, discuss different types of instruction formats. [12 marks]

✓ QUESTION 3 (20 Marks)

Computers are complex machines powered by various components working together. Understanding these vital elements and their functions is key to comprehending how computers operate.

- (a) Write notes about the following computer components, highlighting their functions:

- | | |
|-------------------|-----------|
| (i) Main memory | [3 marks] |
| (ii) Control Unit | [3 marks] |
| (iii) Registers | [3 marks] |
| (iv) System Bus | [3 marks] |

- (b) Draw a block diagram illustrating how the Central Processing Units interact with other components of the computer structure [4 marks]
- (c) How is a single-bus/ processor architecture different from a Multiprocessing System architecture? [2 marks]
- (d) Explain the difference between data lines different from address lines with respect to their roles. [2 marks]

QUESTION 4 (20 Marks)

- (a) Explain what is meant by the term addressing modes? [2 marks]
- (b) With examples explain the different types of addressing modes used in the design of an instruction set architecture. [18 marks]

QUESTION 5 (20 Marks)

(a) Infix, prefix, and postfix notations are utilized to represent mathematical expressions for computational processing. Briefly explain each of the following notations. Give an example in each case.

- (i) Infix. [3 marks]
(ii) Prefix. [3 marks]

(b) During computational processing, different operators are assigned varying priorities. Arrange the following operators in descending order of priority (starting with one of the highest priority and ending with one of the lowest.) [5 marks]

/, ^, -, *, +

(c) A stack is the commonly used data structure for evaluating postfix expression.

- (i) Define a stack. [2 marks]
(ii) Convert the expression $((3+14)*2)/7$ to Postfix format. [3 marks]

(d) Evaluate the following postfix expressions:

623+-382/+*2^3+ [4 marks]

QUESTION 6 (20 Marks)

- (a) (i) Explain the term memory hierarchy. [2 marks]
such that access time is reduced.
(ii) Using an illustration describe the memory hierarchy design. [4 marks]
(iii) Explain the major features of memory hierarchy. [8 marks]
- (b) (i) Define assembly language. [2 marks]
low-level language used to communicate with hardware.
(ii) Describe the syntax of assembly language statements. [4 marks]
syntax [label] [mnemonic] [operands], [comment]. speed

END OF EXAMINATION PAPER



SOROTI UNIVERSITY

SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING

MAY 2024 SEMESTER FINAL EXAMINATIONS

COURSE UNIT: VLSI SYSTEMS DESIGN

COURSE CODE: EEE3201

SEMESTER: II YEAR: 3

DATE: WEDNESDAY, 29TH MAY, 2024

TIME: 9:00 a.m - 12:00 noon

GENERAL INSTRUCTIONS:

1. *The paper consists of FIVE (5) questions.*
2. *Answer ANY FOUR (4) questions.*
3. *Each question carries 25 marks.*
4. *A sheet of formulas some of which you may need is attached at the end.*
5. *All diagrams where required must be carefully drawn appropriate labelling.*
6. *You may use an electronic calculator with 4 significant accuracy in calculations.*

**THIS PAPER MUST NOT BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY
THE INVIGILATOR**

QUESTION ONE (25 MARKS)

- a) Briefly mention 5 impacts that VLSI technologies have had on electronic products. (5 marks)
- b) Derive Miller's Theorem and explain its application in study of dynamic behaviour of IC signals. (7 marks)
- c) (i) Show that the average dynamic power dissipation of a switched CMOS gate loaded with an effective output capacitance, C_{eff} is given by
- $$P_{dyn} = C_{eff}V_{DD}^2f$$
- where V_{DD} is the power supply voltage and f is the signal switching frequency. (6 marks)
- (ii) If a CMOS gate feeds to 100 other gates, $V_{DD} = 3.3\text{ V}$, node capacitance is 15 fF, and switching frequency is 1 GHz, find the average dynamic power dissipated. (4 marks)
- d) What techniques are used to minimize power dissipation in VLSI circuits? Name three of them. (3 marks)

QUESTION TWO (25 MARKS)

- * a) How can VLSI circuits be classified according to the type of signals they handle? (4 marks)
- * b) What do you understand by each of the following terms as used in semiconductor theory?
- (i) Relative mobility (2 marks)
 - (ii) Fermi Energy (2 marks)
 - (iii) Inversion layer (2 marks)
- c) Write a short code to implement a 3-input NAND gate in Verilog HDL. (4 marks)
- d) Implement the following combinational circuit modules using CMOS gate logic:
- (i) $Y = \overline{ABC + D}$ (5 marks)
 - (ii) $Y = \bar{A} \bar{B}(\bar{C} + \bar{D})$ (6 marks)

QUESTION THREE (25 MARKS)

Q

* a) Name 4 classifications of digital IC technologies according to their complexity. (2 marks)

b) Draw a diagram of a 6-transistor (6T) memory cell and briefly explain how it works.

(6 marks)

a)

i)

j)

✓ c) (i) What is meant by a well in VLSI fabrication? (2 marks)

(ii) Draw a clearly labelled diagram of the cross-section of a CMOS logic inverter fabricated using a well. (4 marks)

d) An n-channel MOSFET is fabricated with the following parameters:

$$t_{ox} = 0.15 \mu\text{m}$$

$$\epsilon_{ox} = 3.8\epsilon_0, \text{ F/m}$$

$$\mu_n = 780, \text{ cm}^2/\text{V-s}$$

$$V_{TH} = 0.7 \text{ V}$$

$$W = 80 \mu\text{m}, L = 20 \mu\text{m}$$

$$\lambda = 0.02$$

*1 cm = 100 mm
1 mm = 10,000 micrometers*

(i) What is the gate to substrate-capacitance of the device? (1 mark)

(ii) What is its transconductance parameter k ? (2 marks)

(iii) If the gate-to-source voltage is 2 V, what is i_D for $v_{DS} = 1.5 \text{ V}$. (4 marks)

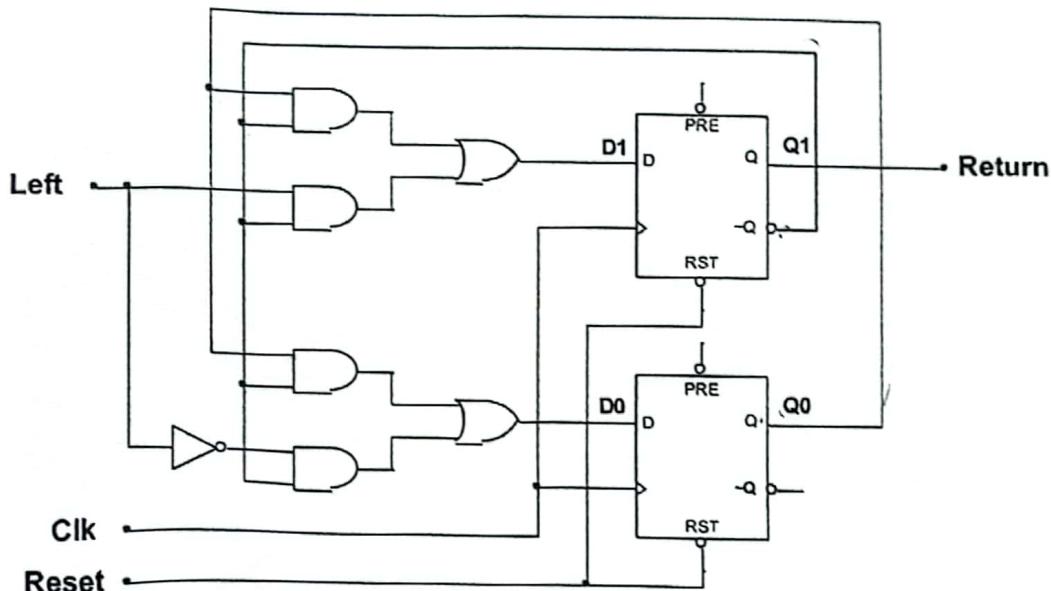
e) The n-channel MOSFET in (d) is used in a VLSI module to implement a **variable resistance** with its gate connected to the drain and with the source connected to the substrate.

(i) Explain why the device will operate either in the cut-off mode or saturated mode, but cannot operate in the linear mode. (2 marks)

(ii) What is its effective resistance when $V_{DS} = 2.0 \text{ V}$? (2 marks)

QUESTION FOUR (25 MARKS)

- a) A flash memory cell uses a special MOSFET with two gates.
- Explain, with the aid of an illustration, why this transistor uses two gates. (3 marks)
 - Explain briefly, with the aid of an illustration, how data may be written into this memory cell and potentially stored for many years. (3 marks)
- b) A module of a Finite State Machine realization circuit is shown in Fig. Q4.c. Assume that the circuit is initially RESET. In the circuit $\sim Q$ means \bar{Q} and PRESETS are not used.



- Determine its next state equations. (4 marks)
- Derive its state transition table (8 marks)
- Draw the finite state diagram (4 marks)
- Given that
 - For Flip Flop: $t_{\text{setup}} = 2 \text{ ns}$, $t_{\text{hold}} = 1 \text{ ns}$, $t_{\text{CQ}} = 2 \text{ ns}$
 - For Gates: $t_{\text{INV}} = t_{\text{OR}} = t_{\text{AND}} = 0.5 \text{ ns}$
 - Interconnections: $t_{\text{int}} = 0.5 \text{ ns}$ all paths
 - Margin: 10%

Determine the maximum switching frequency that can be used. (3 marks)

QUESTION FIVE (25 MARKS)

- a) VLSI chips may be generally classified according to their functions and uses. Name 4 of these classifications. *RF, Analog, Digital and SoC* (4 marks)
- b) A block diagram of a Finite State Machine (FSM) is shown in Fig. Q5.1 and its state diagram is shown in Fig. Q5.2.

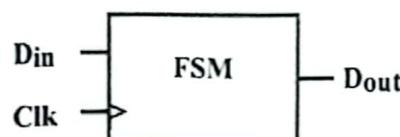


Fig.Q5.1

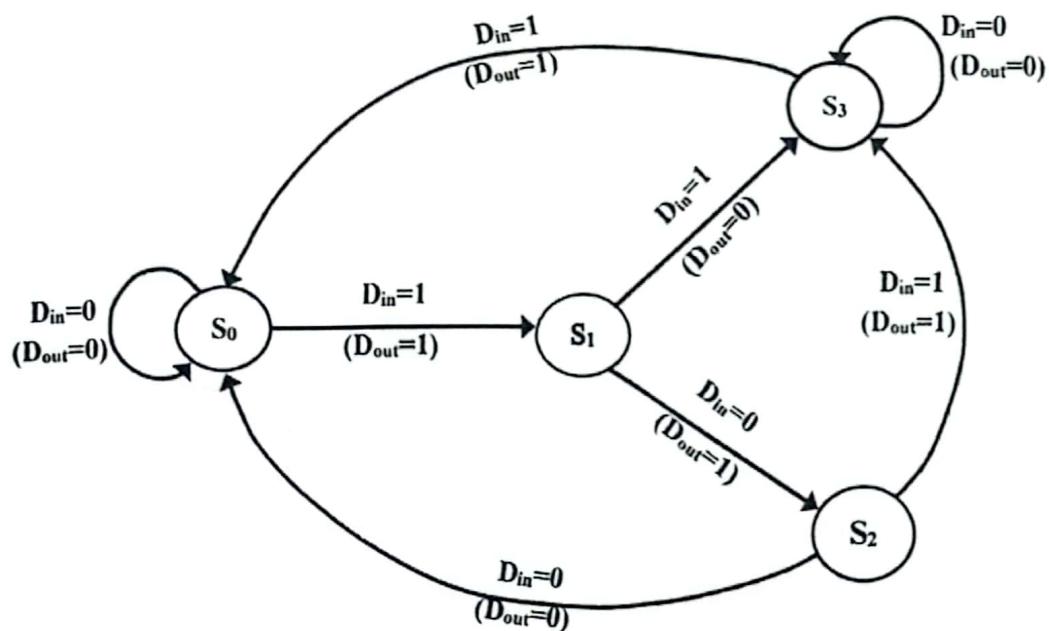


Fig.Q5.2

You are required to design the FSM using the following code :

$$S_0 = "00", S_1 = "01", S_2 = "10", S_3 = "11"$$

- (i) Derive the state transition table. [8 Marks]
- (ii) Derive the next state logic and output logic expressions. [6 Marks]
- (iii) Implement/synthesize this machine using gates and flip flops. [7 marks]

MOSFET OPERATION MODES

SYMBOLS and UNITS:

t_{ox} = oxide thickness, m

ϵ_{ox} = permittivity of oxide , F/m

μ_n = surface mobility of free electrons, m²/V-s

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ F/m²

V_{TH} = threshold voltage, V

$k = \frac{\mu_n C_{ox} W}{L}$, A/V²

In SPICE:

$$k' = KP = \mu_n C_{ox} = \mu_n \frac{\epsilon_{ox}}{t_{ox}}, \text{ and } k = k' \frac{W}{L}, \text{ A/V}^2$$

1. CUT-OFF MODE

$v_{GS} < V_{TH}$ and $v_{DS} > 0$, but small then $i_D = 0$

2. LINEAR (TRIODE) MODE

For

$v_{GS} > V_{TH}$ and $0 < v_{DS} < (v_{GS} - V_{TH})$,

We derived

$$i_D = k[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2]$$

For small v_{DS} ,

$$i_D \approx k(v_{GS} - V_{TH})v_{DS}$$

or drain current is linear with drain to source voltage for given gate to source voltage

3. SATURATION MODE

For

$v_{GS} \geq V_{TH}$ and $v_{DS} > (v_{GS} - V_{TH})$,

We can show that

$$i_D = \frac{k}{2}(v_{GS} - V_{TH})^2$$

Allowing for channel width modulation.

$$i_D = \frac{k}{2}(v_{GS} - V_{TH})^2(1 - \lambda v_{DS}) \quad \text{for saturation region}$$

$$i_D = k[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2](1 - \lambda v_{DS}) \quad \text{for linear region, to avoid discontinuity at transition from linear to saturation}$$

DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING
EEE3202 VLSI SYSTEMS DESIGN

CONTINUOUS ASSESSMENT TEST I 2PM-4PM - 18TH MARCH, 2024

ANSWER ALL QUESTIONS. Questions do not carry equal marks

$$\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$$

- Q.1** (a) Explain why semiconductors are doped. *+/- free electrons and holes*
 (b) Name three materials which can be used as semiconductors. Which property of these materials makes them suitable for this use? *Si GaAs Ge bonds with each other form valence electrons*
 (c) Explain how a p-channel MOSFET can be biased to operate in each of the following modes: cut-off mode, linear (triode) mode, and saturation mode.

$$V_{DS} > V_{GS} + V_{TP} \quad V_{DS} \in V_{GS} + V_{TP} \quad \geq$$

- Q.2** An n-channel MOSFET is fabricated with the following parameters:

$$t_{ox} = 0.1 \mu\text{m},$$

$$\epsilon_{ox} = 3.8\epsilon_0 \text{ F/m}$$

$$\mu_n = 790 \text{ cm}^2/\text{V-s}$$

$$V_{TH} = 1.5 \text{ V}$$

$$W = 55 \mu\text{m}, L = 20 \mu\text{m}$$

The source and substrate of the device are connected, and a gate-to-source voltage of 4 V is applied. Determine:

- the transconductance parameter, k_n of the device?
- the value of v_{DS} that results in a pinch-off condition?
- the value of i_D for the pinch-off condition?
- The value of i_D for v_{DS} greater by 1 V than the potential corresponding to pinch-off?
- The value of i_D for v_{DS} less by 1 V than the potential corresponding to pinch-off?

- Q.3** In MOSFET Integrated circuits, MOSFET devices are generally used in place of resistors.

- Show that a variable resistance can be realized by connecting the drain and gate of an n-channel MOSFET, and its source and substrate (body).
- Obtain an expression for the equivalent resistance of the circuit in (a).
- If an n-channel MOSFET device has:

$$V_{TH} = 1.0 \text{ V}, \quad t_{ox} = 0.1 \mu\text{m}, \quad \epsilon_{ox} = 3.8\epsilon_0 \text{ F/m}$$

$$W = 75 \mu\text{m}, \quad L = 20 \mu\text{m}, \quad \mu_n = 800 \text{ cm}^2/\text{V-s}$$

- What is the equivalent resistance for $v_{DS} = 3 \text{ V}$.
- What width W could be used to obtain an equivalent resistance of $10 \text{ k}\Omega$, assuming that other parameters remain unchanged?

- Q.4** Obtain and sketch a realization of the following Boolean expressions using CMOS logic:

$$a) \bar{Y} = A + \bar{B}\bar{C}$$

$$b) Y = C(B + \bar{A})$$

$$R_{on} = \frac{1}{k_n(V_{GS} - V_{TH})} \quad C_p = \frac{V_{DS}}{R_o}$$

$\frac{1}{k_n(V_{GS} - V_{TH})}$

$R_{on} = \frac{V_{DS}}{\frac{1}{k_n(V_{GS} - V_{TH})}}$



cutoff saturation

$$R_{on} = \frac{V_{DS}}{\frac{1}{k_n(V_{GS} - V_{TH})}}$$

DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING

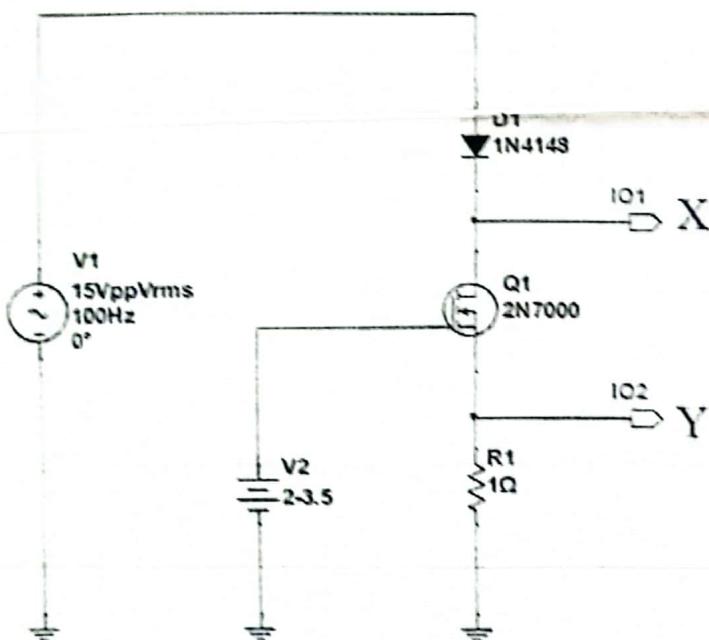
OUTPUT CHARACTERISTICS OF A MOSFET

OBJECTIVE

To display the output characteristic of an n-channel MOSFET and identify the two regions of operation of a MOSFET – Linear region and saturation region.

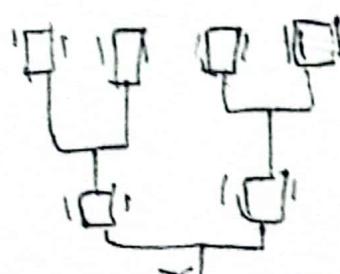
PROCEDURE

1. Connect the circuit shown in the diagram.
2. Monitor the voltage V_{DS} on Ch1 of the scope and the current I_D (as voltage across the 1 Ohm resistor) on Ch 2. The Voltage V_{GS} is from a fixed dc power source, while the Supply to the drain is a sinusoidal a.c. supply from a signal generator.
3. Set the voltage V_{GS} to be 2.3 V and set the scope to X-Y display. This displays Ch2 against Ch1. You may need to adjust Ch1 and Ch2 position and range knobs to get a good output characteristic display. When ok save the trace on a flash drive.
4. Repeat 3 to get another trace for $V_{GS} = 2.7$ and then for 3.0 V
5. Identify the regions of operation of the device from each of your traces.



CONCLUSIONS

Make observations and deduce conclusions from your results.



SOROTI UNIVERSITY
DEPT OF ELECTRONICS AND COMPUTER ENGINEERING

STATIC (DC) SWITCHING CHARACTERISTICS OF A MOSFET

1. INTRODUCTION

The 2N7000 is an N-Channel MOSFET. The aim of this Lab exercise is to examine the switching characteristics of this MOSFET when used as a switch. We will do this by measuring and plotting the transfer characteristics V_{DS} vs V_{GS}

2. PROCEDURE

- a) Connect a common source circuit of the MOSFET with a resistor of $1\text{ k}\Omega$ drain to V_{DD} resistor. The MOSFET is a 3-terminal device (Drain, Gate and Source). *Draw this circuit.*
- b) Apply 15 V fixed supply voltage V_{DD} from Ch1 of the triple output DC supply between the free end of the drain resistor to source (ground). Apply a variable DC voltage V_{GS} (Ch2 of the Triple output DC supply) between gate and source.
- c) Connect a voltmeter between drain and source to measure V_{DS} .
- d) Starting from $V_{GS}=0\text{ V}$, take readings of V_{DS} and V_{GS} in small steps up to $V_{GS}=+5\text{ V}$
Remember to take closer readings where the voltages are changing fast!
- *e) Plot V_{DS} vs V_{GS} , and V_{DS} vs I_D . You will need to calculate I_D from your readings
- f) Repeat (d) – (e) with drain resistors of $2.2\text{ k}\Omega$, and $4.7\text{ k}\Omega$.

3. QUESTIONS AND CONCLUSIONS

- a) From your plots discuss the switching properties and voltages of the MOSFET.
- b) Estimate the switch on input threshold voltage and the resistance $R_{DS(on)}$ when the device is fully on.

MOSFET OPERATION MODES

SYMBOLS and UNITS:

t_{ox} = oxide thickness, m

ϵ_{ox} = permittivity of oxide, F/m

μ_n = surface mobility of free electrons, m²/V-s

C_{ox} = gate capacitance, = $\frac{\epsilon_{ox}}{t_{ox}}$ F/m²

V_{TH} = threshold voltage, V

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In SPICE:

$$k' = KP = \mu_n C_{ox} = \mu_n \frac{\epsilon_{ox}}{t_{ox}}, \text{ and } k = k' \frac{W}{L}, \text{ A/V}^2$$

1. CUT-OFF MODE

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2. LINEAR (TRIODE) MODE

For

$v_{GS} > V_{TH}$ and $0 < v_{DS} < (v_{GS} - V_{TH})$,

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$$i_D = k[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2]$$

For small v_{DS} ,

$$i_D \approx k(v_{GS} - V_{TH})v_{DS}$$

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3. SATURATION MODE

For

$v_{GS} \geq V_{TH}$ and $v_{DS} > (v_{GS} - V_{TH})$,

We can show that

$$i_D = \frac{k}{2}(v_{GS} - V_{TH})^2$$

Allowing for channel width modulation.

$$i_D = \frac{k}{2}(v_{GS} - V_{TH})^2(1 - \lambda v_{DS}) \quad \text{for saturation region}$$

$$i_D = k[(v_{GS} - V_{TH})v_{DS} - \frac{1}{2}v_{DS}^2](1 - \lambda v_{DS}) \quad \text{for linear region, to avoid discontinuity at transition from linear to saturation}$$



SOROTI UNIVERSITY
SCHOOL OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING

**MAY 2024 SEMESTER EXAMINATIONS FOR THE BACHELOR OF
ELECTRONICS AND COMPUTER ENGINEERING**

COHORT 2020

COURSE CODE:	CPE3203	
COURSE NAME:	INTELLIGENT SYSTEMS	
YEAR:	3	SEMESTER : 2
DATE:	TUESDAY, 28 TH MAY, 2024	
TIME:	2:00 P.M. TO 5:00 P.M.	

Instructions:

1. There are **SEVEN (7)** questions in this paper.
2. Attempt **ANY FIVE (5)** questions of your choice.
3. Each question carries 20 marks.
4. Begin each question on a new page.
5. The paper has a Case Study at the beginning which you should use to answer any questions or part questions referring to it.

**THIS PAPER IS NOT TO BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE
INVIGILATOR**

CASE STUDY

A clan is a family consisting of all children, descendants and spouses of a recognised ancestor in a given tribe. The ABEINIKA clan is planning to choose their clan chairperson and clan committee members, from a pool of one hundred and eighty-eight clan members. Previously, they would select them through elections, but there have been concerns that the elections are not free and fair and voter bribing or threatening / intimidation is prevalent. This time round, they want to engage the services of an expert system that will select the eligible candidates for the committee members and then ultimately, the most suitable of them for the position of clan chairperson.

* QUESTION 1:

One of the key players of an AI system are the experts or knowledge providers. However, sometimes challenges are encountered when dealing with information provided by experts.

- a. With relevant examples, discuss four challenges faced with raw unprocessed expert information. (8 marks)
- b. Suggest one way each of the identified challenges in (a) can be solved. (8 marks)
- c. Refer to the Case Study and suggest four questions you shall require the experts to answer which will be input into the expert system. (4 marks)

✓ QUESTION 2:

- a. Define Artificial Intelligence (AI). (5 marks)
- * b. AI is based on re-representation of knowledge using mathematical concepts. Discuss five of these concepts. - fuzzy - rules - neural networks - logic - constraint propagation - search algorithms (5 marks)
- c. Discuss three differences between monotonic and non-monotonic reasoning. (4 marks)
- d. Propose three facts and three rules for the Case study narrated. (6 marks)

x **QUESTION 3:**

- a. Discuss any four bad behaviours software engineers may show during the development of intelligent systems. (8 marks)
- b. Discuss the major techniques that can be applied to mitigate the bad behaviours identified in (a). (8 marks)
- c. Assume you are approached by a stakeholder of the clan in the Case Study and asked to do something in the system to ensure that a particular person comes up as the best contender. However, this goes against the professional code of conduct. How will you solve this dilemma? (4 marks)

QUESTION 4:

Data is a critical component of intelligent systems, and data gathering and processing is one of the core activities of an AI engineer.

- ✓ a. Suggest at least three sources of data about the clan members in the Case Study that you will consider while building the AI engine. (5 marks)
- ✓ b. Discuss five data pre-processing techniques that can be applied after the data has been obtained. (5 marks)
- ✓ c. Narrate how you intend to proceed after the data cleaning up to the final determination of the clan committee members. (10 marks)

QUESTION 5:

- a. Discuss logic programming and its three applications. (4 marks)
- b. Define the following concepts in logic programming:
 - i. Predicate
 - ✓ ii. Backtracking
 - iii. Rules
 - iv. Queries
 - v. Conjunctions
 - vi. Tree
 - ✓ vii. Tokenisation
 - , viii. The Parsing problem
- c. Drawing from the Case Study and using the proper syntax, provide a relevant example of the concepts in (b). (8 marks)

QUESTION 6:

With the aid of diagrams, explain each of the following concepts

- a. k-means clustering (5 marks)
- b. classification ^{k-nearest} (5 marks)
- c. Agglomerative hierarchical approach (5 marks)
- d. Divisive hierarchical approach (5 marks)

QUESTION 7:

- ✓ a. What are the three laws of Robotics? (6 marks)
- ✓ b. If you all the powers to create a 4th Law of Robotics, what would it be? (2 marks)
- ✓ c. Suggest three areas you can deploy a robot(s) to improve the committee selection process in the Case Study. (6 marks)
- ✓ d. Discuss three challenges in Robotics generally. (6 marks)

TEST 1 CPE3203: INTELLIGENT SYSTEMS

Date: 01/05/2024

INSTRUCTIONS

Attempt both questions

Use the SLEEP.CSV dataset to answer the questions

Question 1: 50 marks

- a) Visualise the data 10
- b) Compute the Accuracy of the data using
 - a. KNN 10
 - b. Naïve Bayesian 10
 - c. Decision trees 10
 - d. Neural network 10

Question 2: 50 marks

Assume you are a sleep expert who has been contracted to develop a sleep expert system in prolog

- a. Analyse the data and suggest any five prolog rules 10
- b. Show screenshots of any of your choice but derived from the data:
 - a. Fact 10
 - b. A Query 10
 - c. Function 10
 - d. Structure 10
 - e. list

*sleep quality >= 7
Disorder != "none"
PhysicalActivity >= 30
BloodPressure = "Normal"*



SOROTI UNIVERSITY
SCHOOL OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING

**MAY 2024 EXAMINATIONS FOR
BACHELOR OF ENGINEERING IN ELECTRONICS AND COMPUTER
ENGINEERING (BEng.ECE)**

2020 COHORT

COURSE CODE:	EEE3207
COURSE TITLE:	OPTOELECTRONICS
YEAR OF STUDY:	THREE
SEMESTER:	TWO
EXAM DATE:	MONDAY 27 TH MAY 2024
TIME	2:00 P.M. TO 5:00 P.M.

INSTRUCTIONS TO ALL CANDIDATES

- *This Examination Paper contains SIX (6) questions*
- *Attempt any FOUR (4) questions*
- *All questions carry equal marks of 25%.*
- *Begin each question on a fresh page and do not write on the margins.*
- *All rough work should be done within the official answer booklet.*
- *Adhere to the instructions as outlined on the answer booklet*

**DO NOT OPEN THIS PAPER UNTIL PERMISSION HAS BEEN GIVEN BY THE
INVIGILATOR**

QUESTION ONE (25 marks)

- a. Explain the differences between Optoelectronics, Electro-Optics, and Photonics. [9 marks]
- b. Discuss each of the following optoelectronics devices giving three applications for each case.
- i. Photodiodes [3 marks]
 - ii. Photovoltaics (or solar cells) [3 marks]
 - iii. Photoresistors [3 marks]
- c. Discuss the law of total internal reflection in optoelectronics and illustrate it with a real life application. [7 marks]

QUESTION TWO (25 Marks)

- a. Draw a detailed block diagram of an optical fibre communication system:
- i. Label each block appropriately. [8 marks]
 - ii. Describe the function of each block [9 marks]
- b. Discuss the phenomenon of interference in optoelectronics and give one real life application. [8 marks]

QUESTION THREE (25 Marks)

- a. What do you understand by “link budget” calculation? What is the purpose of such a calculation in the design and analysis of an optical communication system. [6 marks]
- b. Define and explain the key components and steps involved in optical fiber link budget calculation. [7 marks]
- c. An optical communication link is designed to transmit data over a (single-mode) optical fiber of 100 km, with fiber loss of 0.2 dB/km, six splices with 0.05 dB per splice loss, and two connectors with 0.2 dB loss per connector. The receiver sensitivity is $20 \mu\text{W}$.
- i. What is the loss budget of the system? [4 marks]
 - ii. What is the minimum transmitter power? [4 marks]
 - iii. If the fiber is to be tapped at half-way point (i.e 50 km) and a 50 km optical fiber cable used to take the signals to another destination, what changes would you propose to make in the communication link? [4 marks]

QUESTION FOUR

- a. Discuss the following critical performance parameters of an optical communications link: [10 marks]
- (i) Quantum efficiency
 - (ii) Responsivity
 - (iii) Cut off wavelength
 - (iv) Speed of response
- b. Describe the optical amplifiers used in an optical communication link [5 marks]
- c. Discuss what is meant by fronthaul and backhaul in wireless networks [5 marks]
- d. Discuss what a data centre network is, using concepts of its topologies [5 marks]

QUESTION FIVE (25 Marks)

- a. Briefly explain what photodetectors are, giving their different classifications and applications. [10 marks]
- b. Explain an optical modulator and briefly describe the two main categories giving their applications in real life. [5 marks]
- c. Discuss the aspects of emission and absorption of light. [5 marks]
- d. Describe the working principle of absorption spectroscopy. [5 marks]

NAME
YAH
CFA

✓QUESTION SIX (25 Marks)

- a. Explain polarisation in optoelectronics. [5 marks]
- b. Discuss the working principle of an optoelectronic device that uses the phenomenon of polarization, giving a real life application. [8 marks]
- c. Consider what happens when two neighboring coherent sources are examined through an imaging system with an aperture of diameter D. The two sources have an angular separation of $\Delta\theta$ at the aperture. The aperture produces a diffraction pattern of the sources S₁ and S₂ as shown in Fig. Q6c. As the sources get closer, their angular separation becomes narrower and the diffraction patterns overlap more. According to the Rayleigh criterion, the spots are just resolvable when the principal maximum of one diffraction pattern coincides with the minimum of the other, which is given by the condition,

$$\sin(\Delta\theta_{min}) = 1.22 \frac{\lambda}{D}$$

The human eye has a pupil diameter of about 2 mm. What would be the minimum angular separation of the two points under a green light of 550nm and their minimum separation if the two objects are 30 cm from the eye? The refractive index n = 1.33 (water) in the eye.

[8 marks]

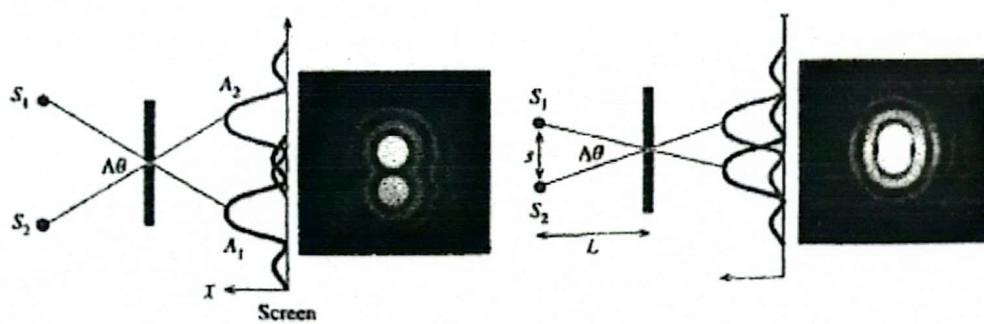
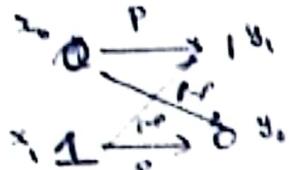


Figure Q6c: Diffraction Pattern

- d. Discuss the access networks-lastmile networks (passive optical networks) [4 marks]

$$\begin{aligned}
 P(Y_1|X_1) &= 1 - P \quad P(Y_1) = (1-P)p(x_1) + Pp(x_1) \\
 P(Y_1|X_0) &= P \quad P(Y_1) = P(Y_1|X_1)p(x_1) + P(Y_1|X_0)p(x_0) \\
 P(Y_0|X_1) &= P \quad P(Y_1) = Pp(x_1) + (1-P)p(x_1)
 \end{aligned}$$

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$\frac{P}{1-P}$

EEE3201 VLSI SYSTEMS

$$\sum_{i=1}^{n-1} P(Y_i|x_i)p(x_i) = P(Y_n)$$

CONTINUOUS ASSESSMENT TEST 2 - 2-4 p.m. - 22ND APRIL, 2024

$P(a_1|x_1) P(a_2|x_2)$

ANSWER ALL QUESTIONS. - QUESTIONS DO NOT CARRY EQUAL MARKS

- Q.1 (a) Explain what is meant by "Noise Margin" of logic gate.
 (b) Give two equations which define noise margins of a logic gate.

- Q.2 (a) Define the power-delay product of a logic gate.
 (b) Explain how can the power delay product of a logic system be

~~Reduced noise~~ — Voltage swing
~~switching~~ — Switching Activity

- Q.3 Write a short code to implement a 3-input NOR gate in Verilog HDL.

Fr. 3

module nor(A,B,C,Y);
 input(A,B,C);
 output(Y);
 assign Y = ~ (A|B|C);

- Q.4 (a) What is a floating gate NMOS transistor.
 (b) How is a floating gate used in VLSI circuit design?

- Q.5 A logic Inverter is constructed using an NMOS transistor with a resistive load of $20\text{ k}\Omega$.

The inverter has an effective load capacitance of 15 fF .

- a) Calculate the expected delay time of the inverter. $t_{pd} = RC$
 b) Estimate the rise-time of the inverter. $t_r = 2.2R_{eff}C$
 c) Estimate the maximum switching frequency the inverter can be subjected to.

$$f_{max} = \frac{1}{2t_r} = \frac{1}{2t_{pd}} = \frac{1}{2RC}$$

- Q.6 A 64-Mbit memory chip is partitioned into blocks, with each block having 4096 rows and 256 columns.

- (a) How many blocks are required?
 (b) Give the number of bits required for the row address, column address, and block address.
 (c) Give a sketch showing the partitioning and decoding arrangements of the chip.

- Q.7 Give a sketch of an SRAM storage cell and explain how it works.

$$\frac{1024}{X} = 32$$

power dissipation formula