Mechatronics (ROB-GY 5103 Section A)

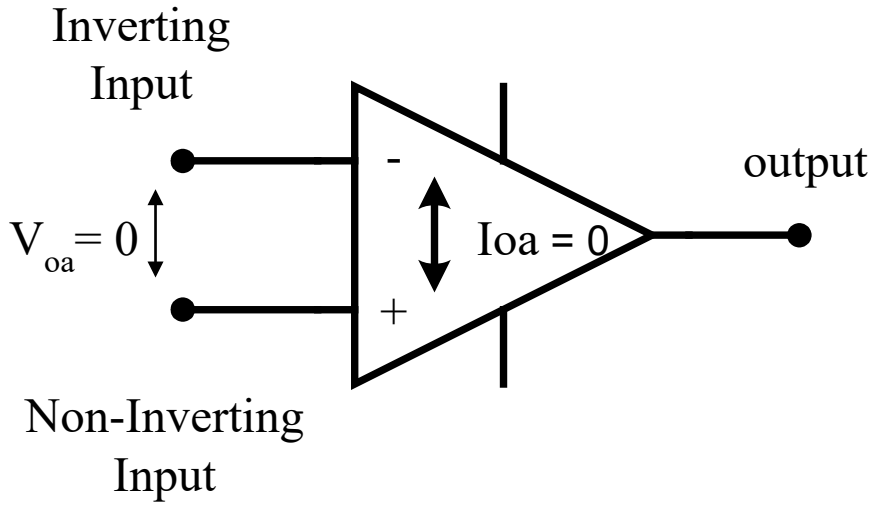
- **Today's lecture:**
  - Analog to Digital conversion
  - Quick intro to op-amps
- (See Topics #4 and #7 from Main Text for details)

Note on Term Project

555 Timer Review

Operational Amplifier (Op-Amp)

- Looks like a comparator, but designed for analog output (amplifying analog input) rather than digital output (high/low)



Operational Amplifier (Op-Amp)

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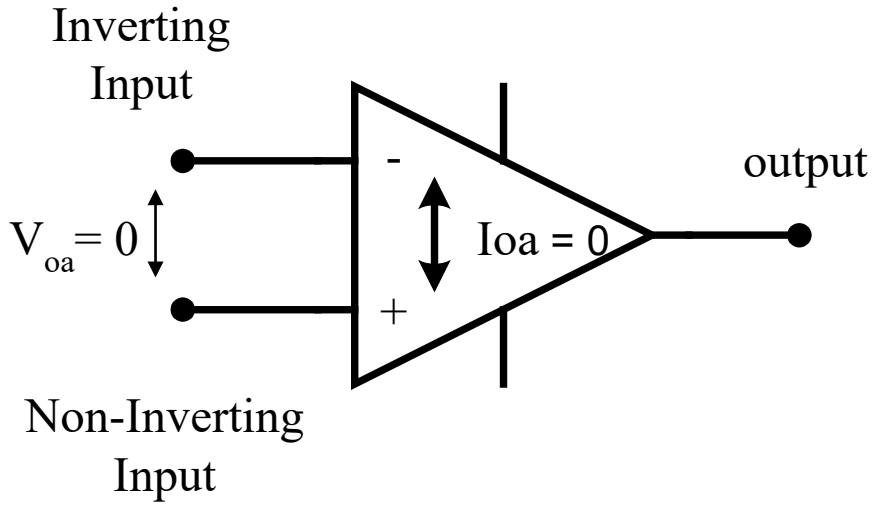
- Op-amp input terminals (inverting and non-inverting terminals) have very high input impedance.
- **Two rules:**
  - No current flows through the input terminals ($I_{oa} = 0$).
  - Voltage drop across the input terminals is zero ($V_{oa} = 0$).



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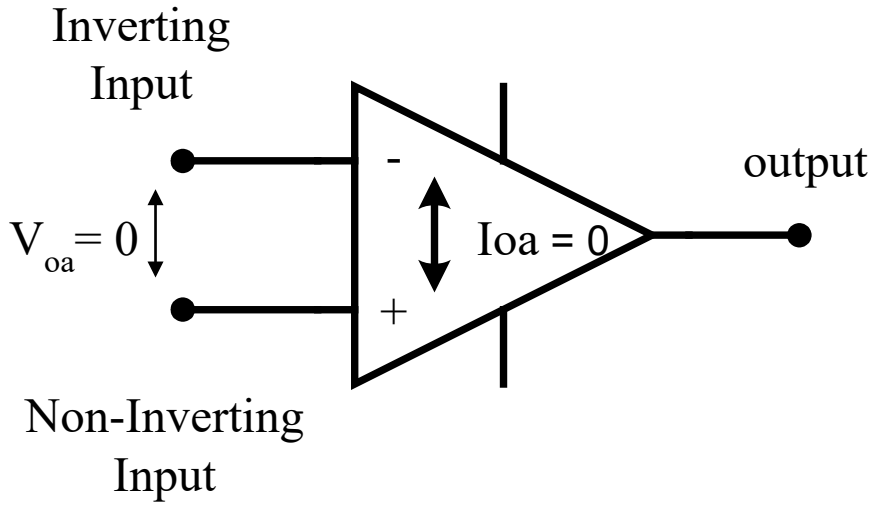


Output terminal will do whatever it takes to enforce these rules! High-gain amplification

Op-Amp Configurations

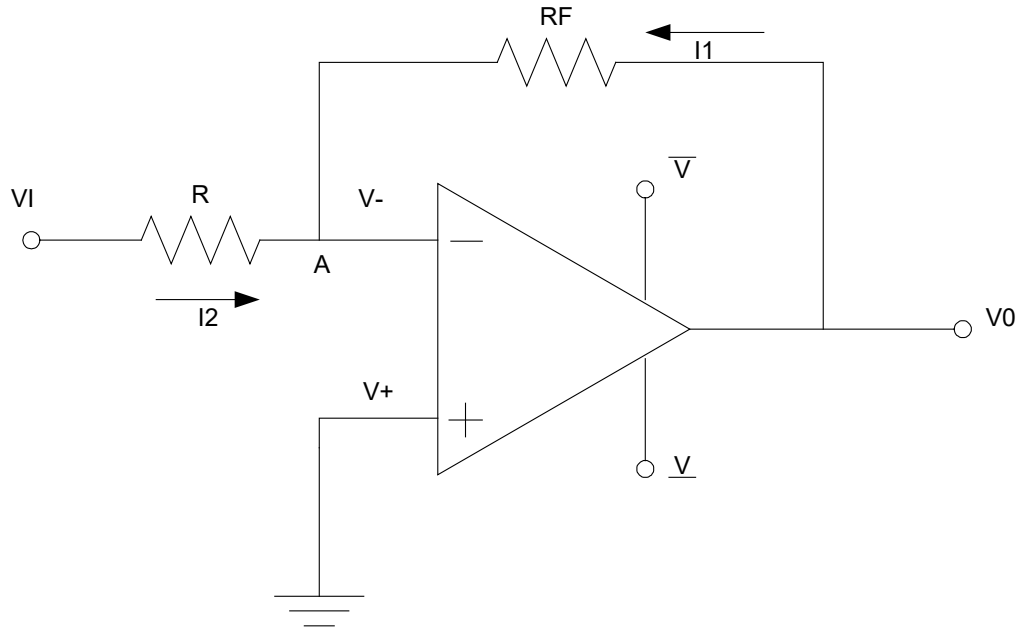
- **Inverting Amplifier**
- **Non-Inverting Amplifier**
- **Summing Amplifier**
- Difference Amplifier
- Integrator Amplifier
- Differentiator Amplifier
- Active Filters

Inverting Op-Amp—I

- Condition:

$$I_- = I_+ = 0 \quad \text{and } V_- = V_+ \Rightarrow V_- = 0 \text{ since } V_+ = 0$$

$$I_1 = \frac{V_0 - V_-}{R_F} = \frac{V_0}{R_F} \qquad I_2 = \frac{V_I - V_-}{R} = \frac{V_I}{R}$$



Inverting Op-Amp—II

- Since $I_{\_} = 0$, using KCL at **A**, we obtain:

$$I_1 + I_2 - I_{\_} = 0 \quad \Rightarrow \quad I_1 + I_2 = 0$$

$$\Rightarrow I_2 = -I_1 \Rightarrow \frac{V_I}{R} = -\frac{V_0}{R_F}$$

- So

$$V_0 = -\left(\frac{R_F}{R}\right) V_I$$

- If R and R_F are replaced by impedances Z and Z_F, respectively and V_I and V_0 are replaced by their respective phasors, then

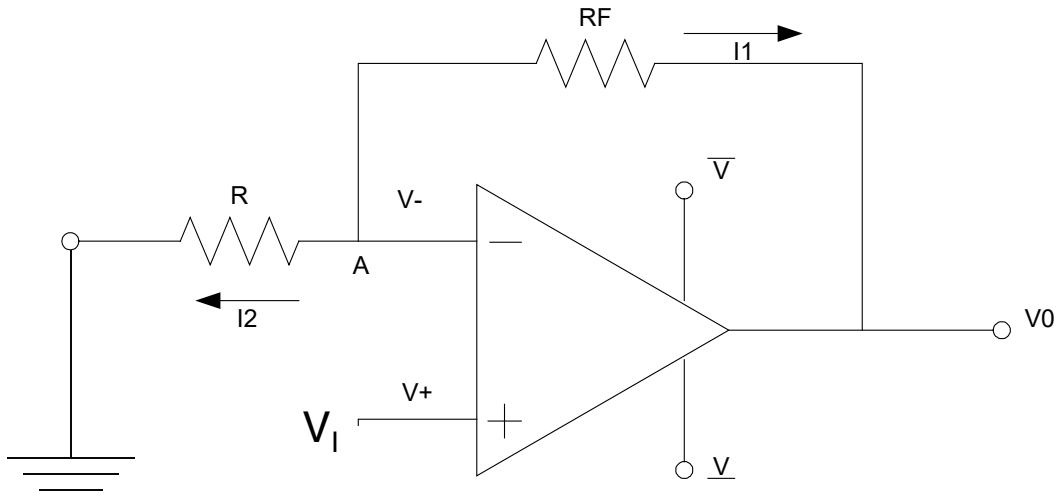
$$\frac{\overline{V_0}}{\overline{V_I}} = -\frac{Z_F}{Z}$$

$$\text{where } \overline{V_0} : P[V_0], \overline{V_I} = P[V_I]$$

Non-Inverting Op-Amp—I

$$I_- = I_+ = 0 \quad \text{and } V_- = V_+ \Rightarrow V_- = V_I \text{ since } V_+ = V_I$$

$$I_1 = \frac{V_0 - V_I}{R_F} \qquad I_2 = \frac{V_I}{R}$$



Non-Inverting Op-Amp—II

- Since $I_{-}=0$, by applying KCL at **A** we obtain:

$$I_1 - I_2 - I_{-} = 0 \quad \Rightarrow \quad I_1 - I_2 = 0 \quad \Rightarrow \quad I_1 = I_2$$

$$\Rightarrow \frac{V_I}{R} = \frac{V_0 - V_I}{R_F} \Rightarrow \frac{V_0}{R_F} = \frac{V_I}{R} + \frac{V_I}{R_F}$$

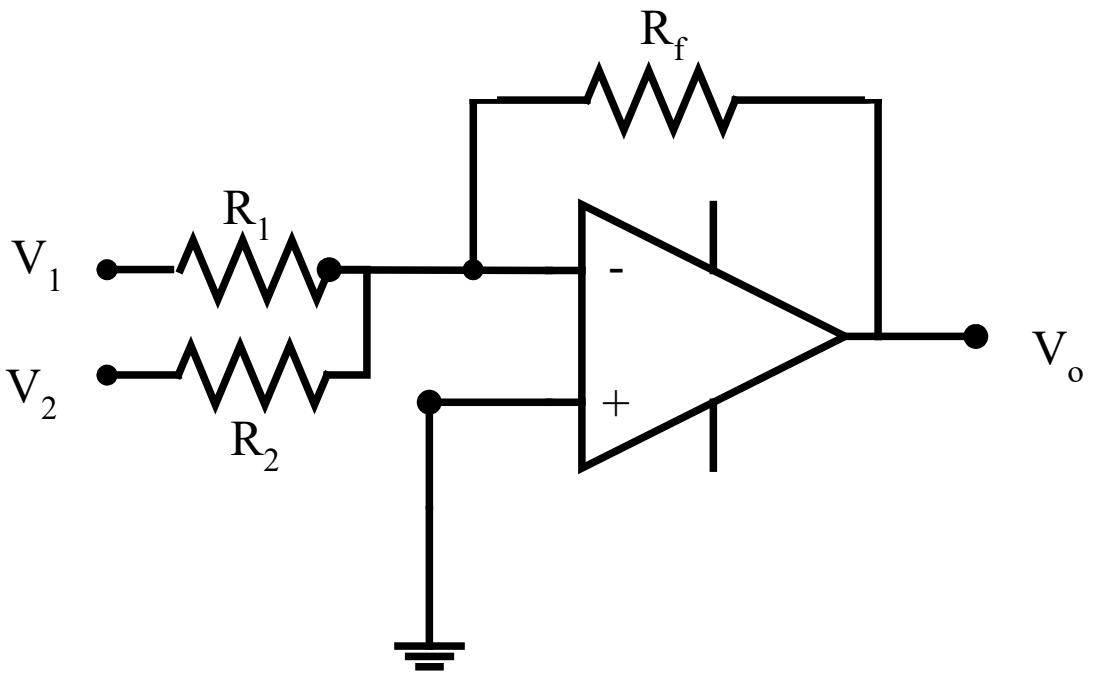
- So

$$V_0 = \left(1 + \frac{R_F}{R}\right) V_I$$

- Once again, if AC inputs and outputs are involved and if R and R_F are replaced by Z and Z_F, respectively, then

$$\frac{\overline{V_0}}{\overline{V_I}} = \left(1 + \frac{Z_F}{Z}\right)$$

Summing Amplifier



$$V_o = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$$

Analog vs. Digital

Analog vs. Digital

- Continuous vs. Discrete

Analog vs. Digital

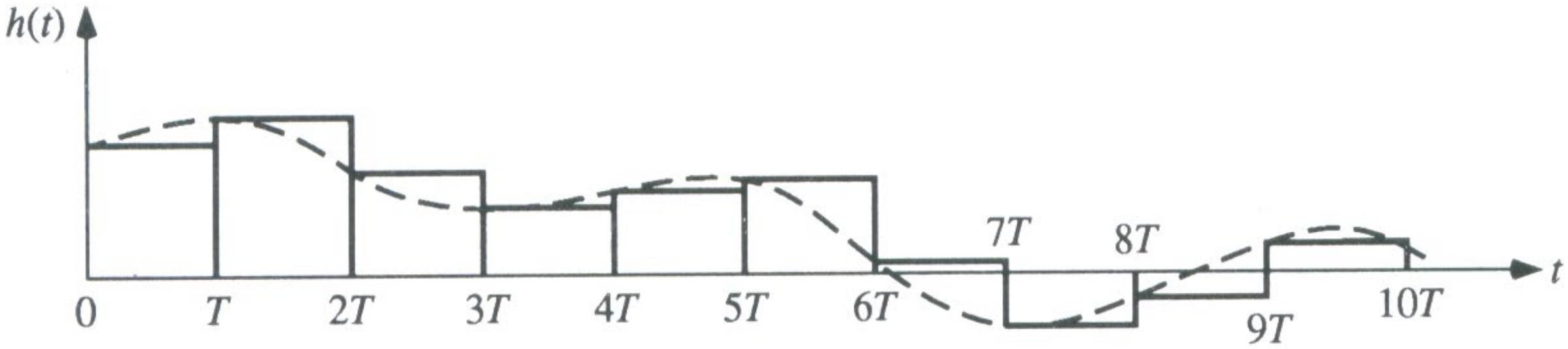
- Continuous vs. Discrete
- Signal Processing
  - Signal Conditioning
  - Applications
    - Data Acquisition
    - Anomaly detection

Analog to Digital (A2D) Conversion

- Process of representing an analog signal digitally.
- Three step procedure:
  - **Sampling**
  - **Quantization**
  - **Coding**

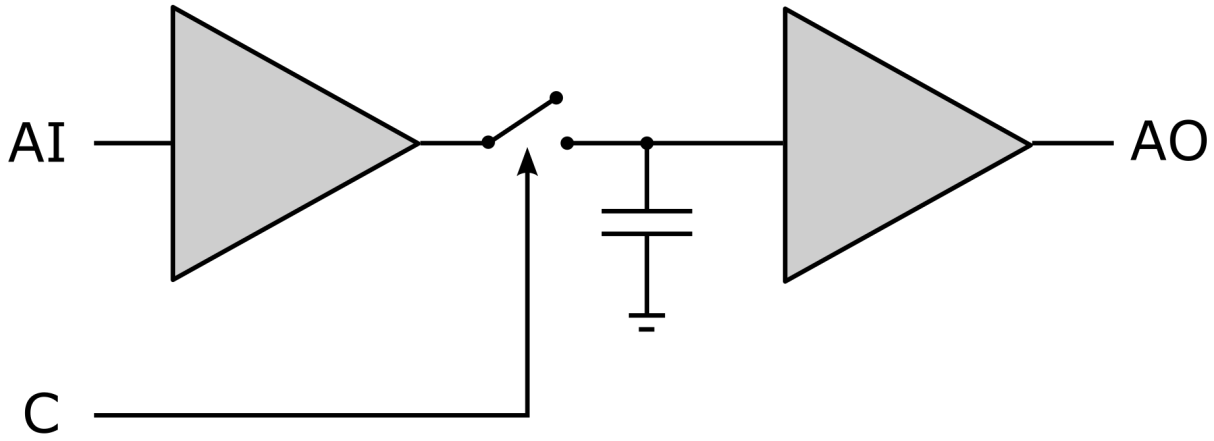
A2D: Sampling

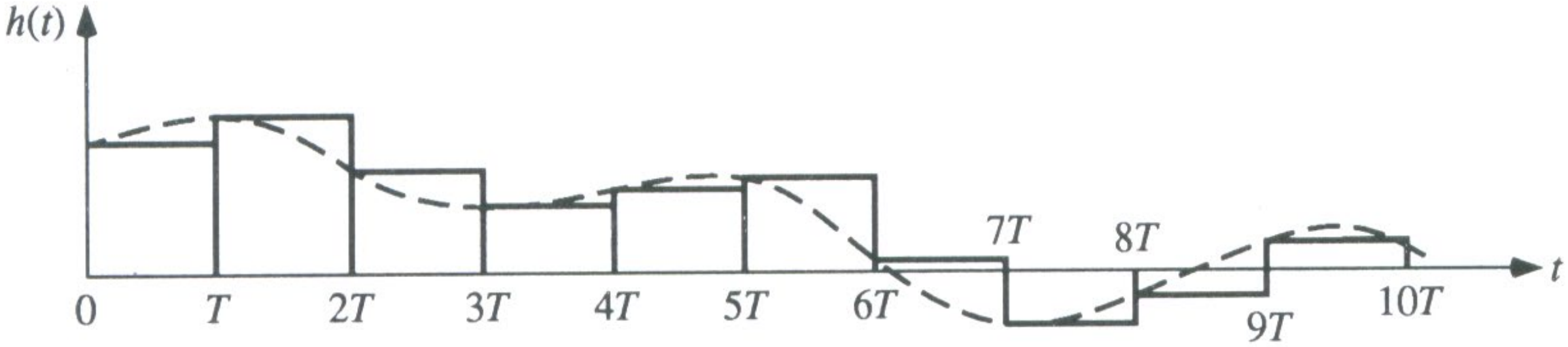
- The process of sampling refers to obtaining the analog signal measurement at discrete instants (sampling instants)
- **Sample and hold:** sampled value of signal is held constant until next sampling instant
- **Nyquist Theorem:** minimum sampling rate is double the highest frequency



A2D: Sample and Hold Implementation

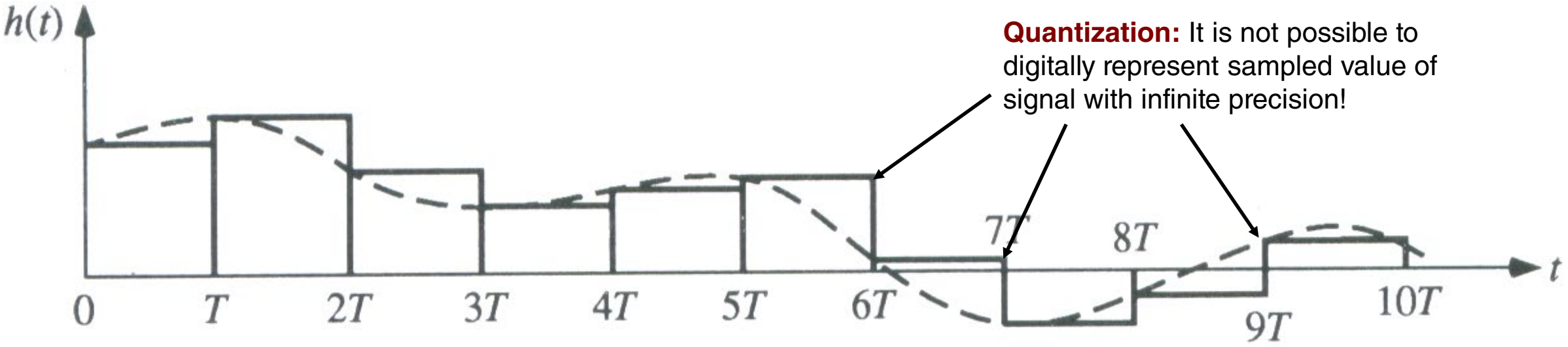
- Hardware implementation





A2D: Quantization

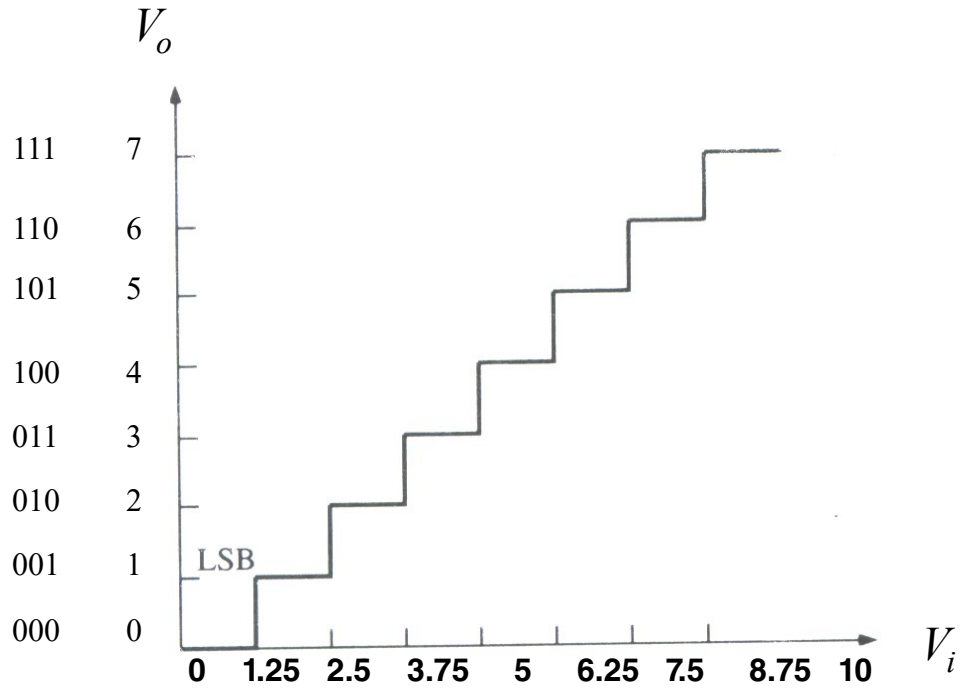
- Represent sampled signal magnitude at **allowable discrete levels**.
- Use of a finite number of bits to store data allows only a finite resolution A2D.
- Analog number is rounded/truncated in the quantization process.
  - Only a finite number of levels with finite bit representation.



A2D: Quantization

- Let us assume $0V \le V_i \le 10V$
- Let us assume 3 bits are used to store V_i. Note that using 3 bits we can get at most 8 different states (2^3). Then, V_i can be subdivided into 8 levels.

$$\frac{10}{8} = \underbrace{1.25V}_{\text{Quantization level resolution}}$$



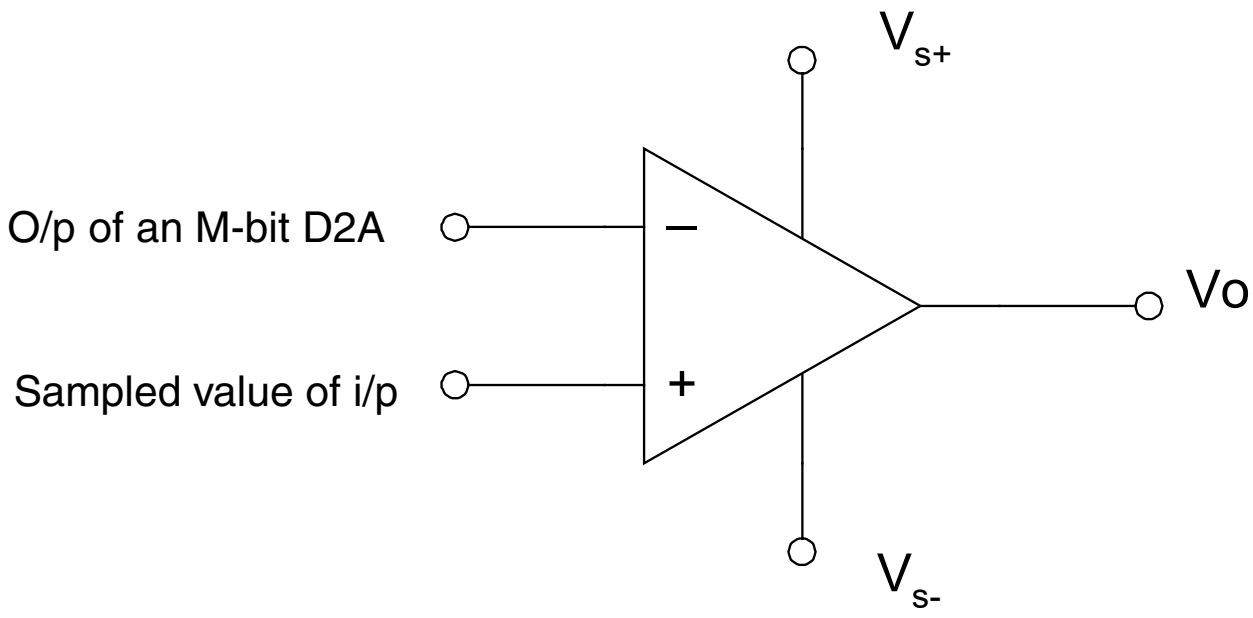
0 V – 10 V

- In general, let us say $V_{\min} \le V_i \le V_{\max}$
- Let us say n bits are used, then, the quantization level (size) is:

$$Q = \frac{V_{\max} - V_{\min}}{2^n}$$

Successive Approximation A2D Converter

- Input voltage sampled at a time instant t_0.
- **D2A converter**
  - Provides an equivalent analog voltage signal to represent contents of an M-bit register.
- **Comparator**
  - Compares input voltage to the output of D2A converter and successively turns the bits of an M-bit register on/off to approximate input voltage.



Successive Approximation A2D Converter

- 0-15V range, 4-bit successive approximation A2D converter

$$\text{Step size: } \frac{15\text{ V}}{2^4} = 0.9375\text{ V}$$

Initial status	Register (Level)	Equivalent Voltage	Input Voltage	Comparator
All bits off	0000 (0)	0	10.1	High
Turn MSB to 1	1000 (8)	7.5	10.1	High
Leave MSB at 1, turn next bit to 1	1100 (12)	11.25	10.1	Low
Leave MSB at 1, turn next to MSB to 0, and the one following that to 1	1010 (10)	9.375	10.1	High
Keep previous ones and turn LSB to 1	1011 (11)	10.3125	10.1	Low
Turn the LSB to 0	1010 (10)	9.375	10.1	High

- Input Voltage: 10.1 V
- Answer: 9.375 Quantized Value

A2D: Coding (or encoding)

- Converts the quantized signal to a binary signal

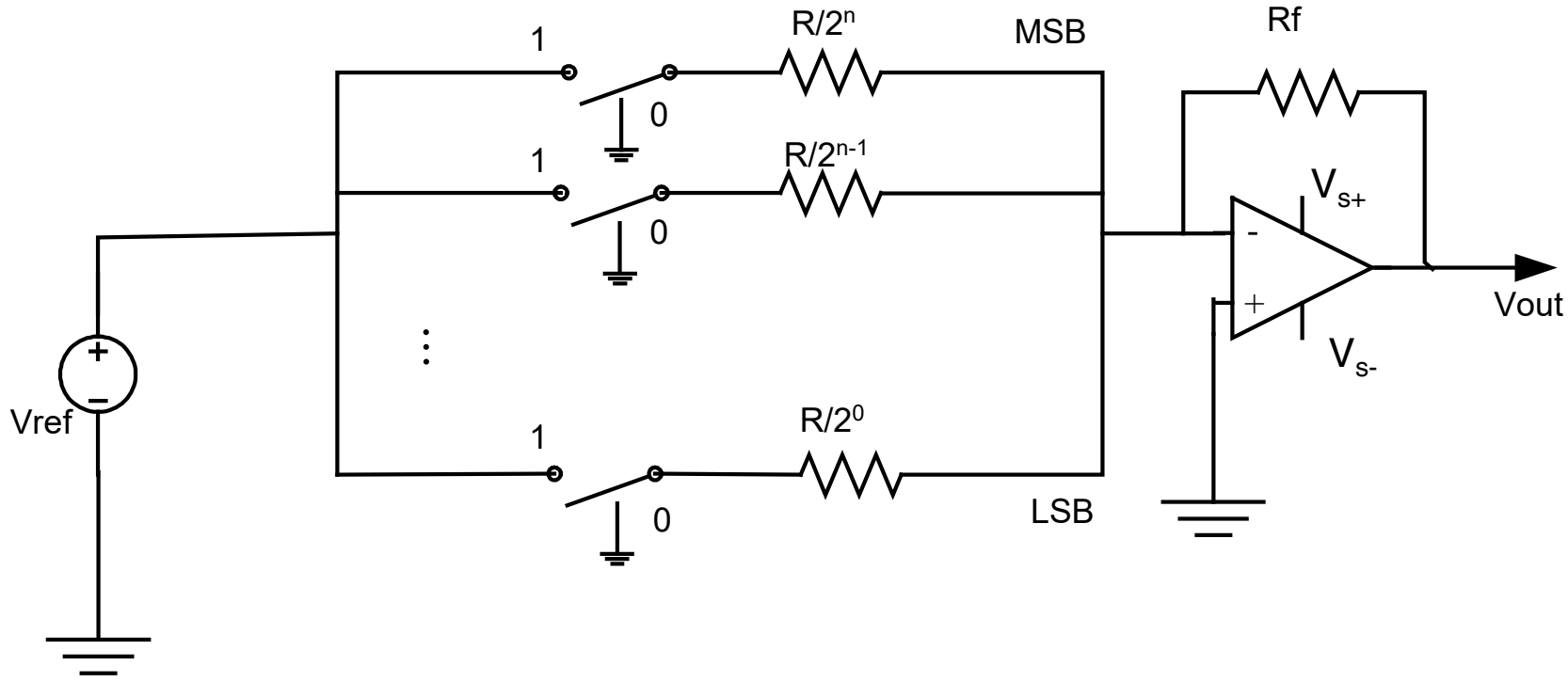
- Techniques to save memory by specifying **bit depth** (bits per sample)
- Aside:
  - Commercial A2D converters have 8,10,12, or 16 bit resolution which give quantization levels of 256,1024,4096, 65536, respectively.
  - Maximum sampling rate and resolution (# of bits) of A2D will dictate its accuracy and reliability.

Digital to Analog (D2A) Conversion

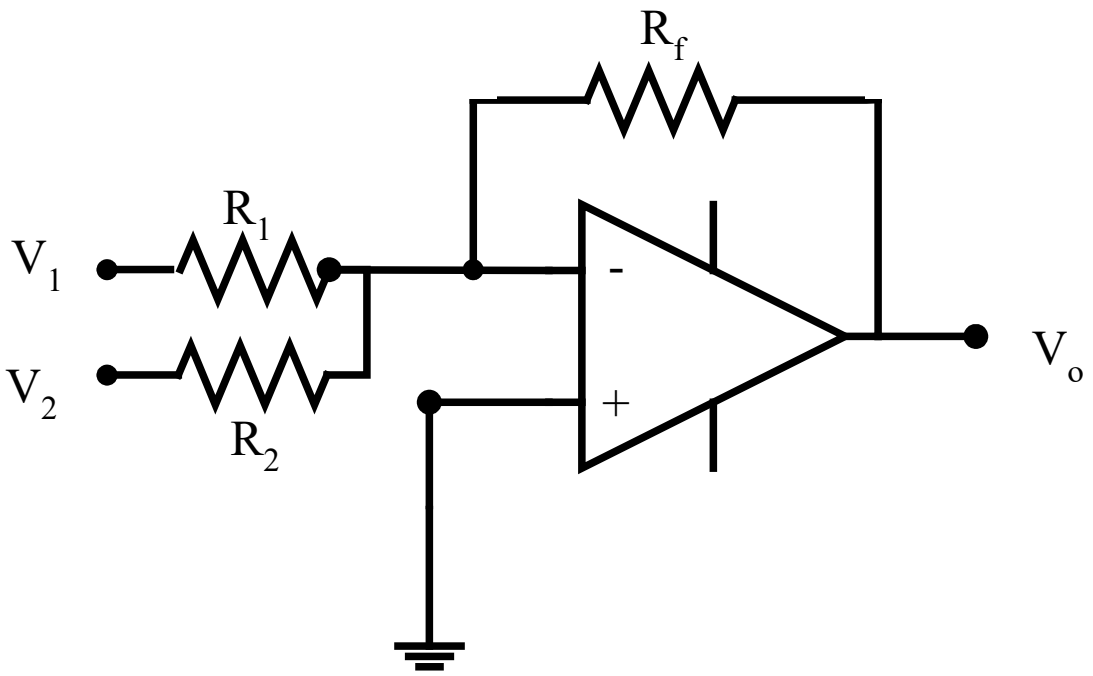
- Often a computer needs to provide a signal that actuates a motor/pump/electromagnet/etc.
  - Digital device actuates an analog device.
- D2A converter takes a data input in binary representation and provides its decimal representation. This is accomplished by implementing the following conversion equation.
  - Signal Reconstruction

$$(b_n b_{n-1} \cdots b_1 b_0)_2 = b_n 2^n + b_{n-1} 2^{n-1} + \cdots + b_1 2^1 + b_0 2^0$$

Op-Amp Circuit for D2A



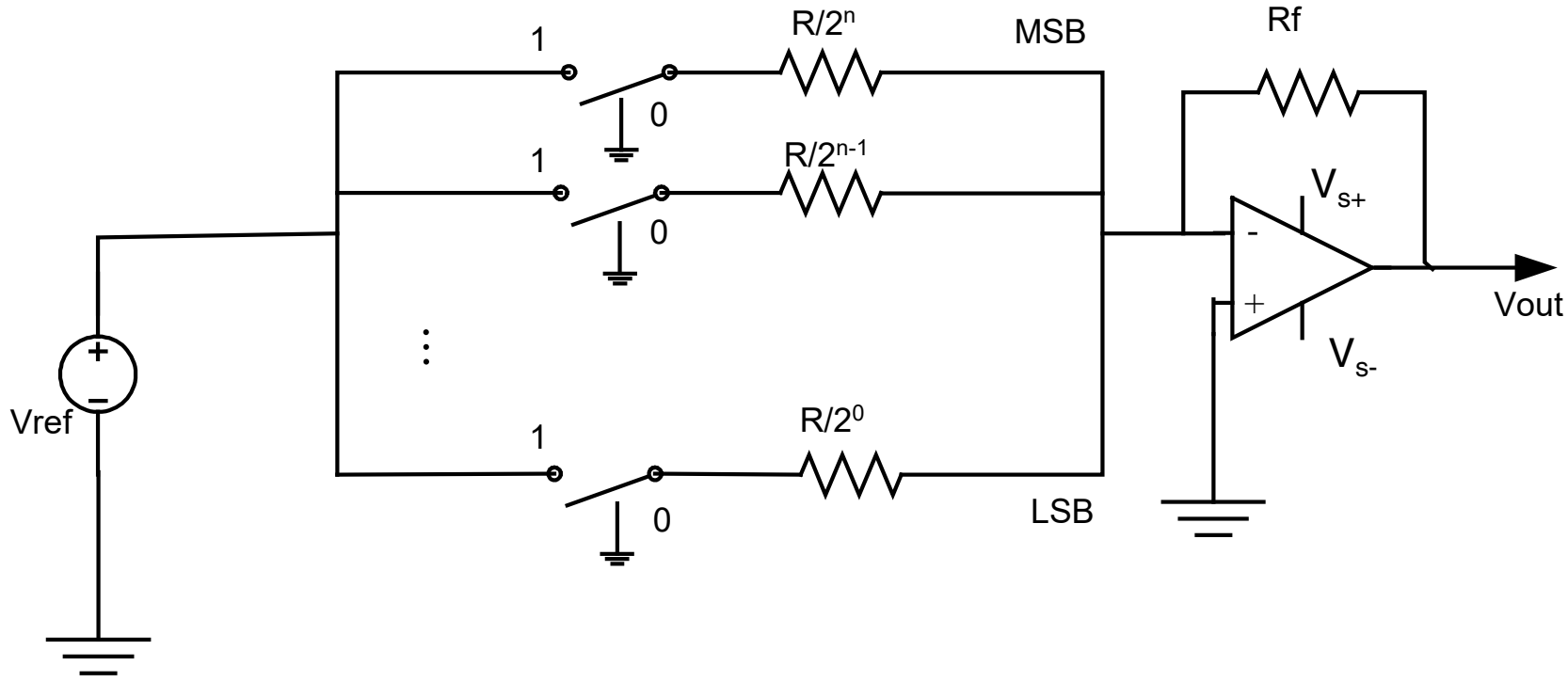
Summing Amplifier



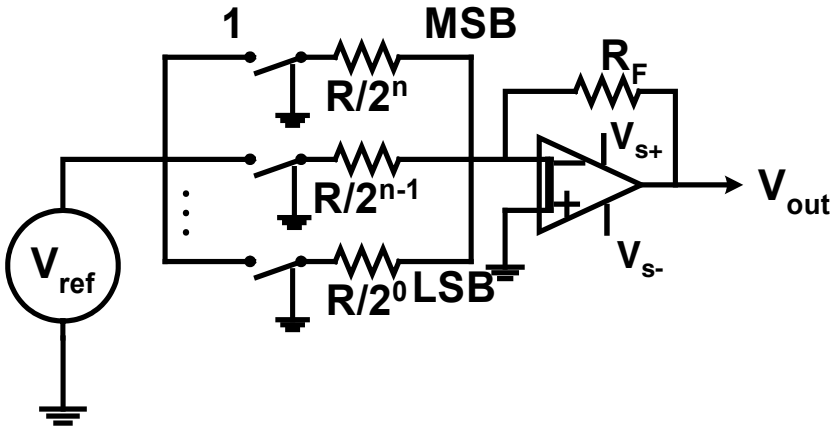
$$V_o = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$$

Op-Amp Circuit for D2A

- Finding such a large range of exact resistances is not easy



Op-Amp Circuit for D2A—II



- Each switch can be in either of two positions:
  - On → 1 (Connected to V_{ref})
  - Off → 0 (Connected to Ground)
- Using the result from summing amplifier:

$$V_{out} = -\frac{R_F}{R/2^n}V_n - \frac{R_F}{R/2^{n-1}}V_{n-1} - \cdots - \frac{R_F}{R/2^0}V_0$$

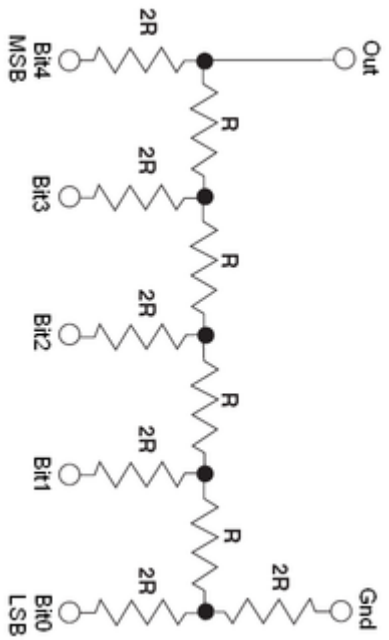
- $V_0, V_1, V_2, \ldots, V_{n-1}, V_n$ are voltages across $R/2^0, R/2^1, R/2^2, \ldots, R/2^{n-1}, R/2^n$, resistors, respectively.
- Note: $V_i = V_{ref} b_i$ where $b_i = 1$ or $0, i = 0,1,\ldots,n.$
- Then,

$$V_{out} = -\frac{R_F}{R}V_{ref}\left[b_n 2^n + b_{n-1}2^{n-1} + \cdots + b_0 2^0\right]$$

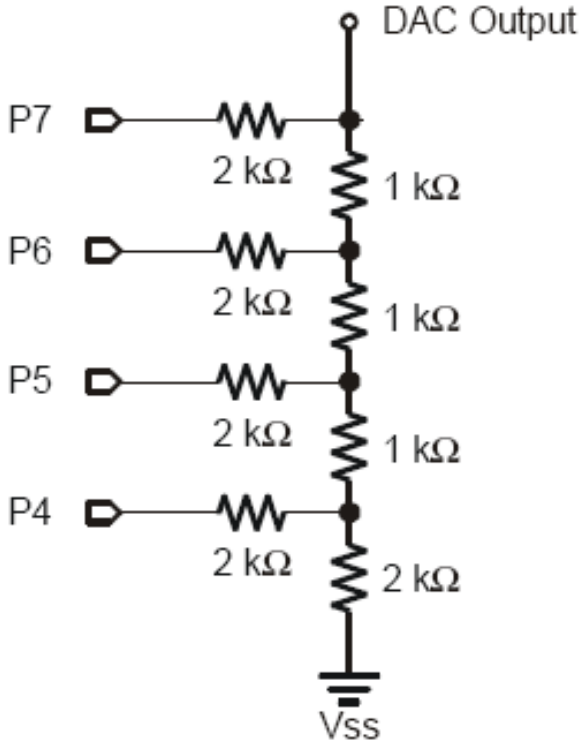
  - Output voltage is directly proportional to decimal equivalent of binary numbers.
- Note: getting resistors with exact values $R/2^i, i = 0,\ldots,n$ is not easy!

R-2R Resistive-Ladder D2A

- Use a resistor ladder with only two resistances, R and $2R$



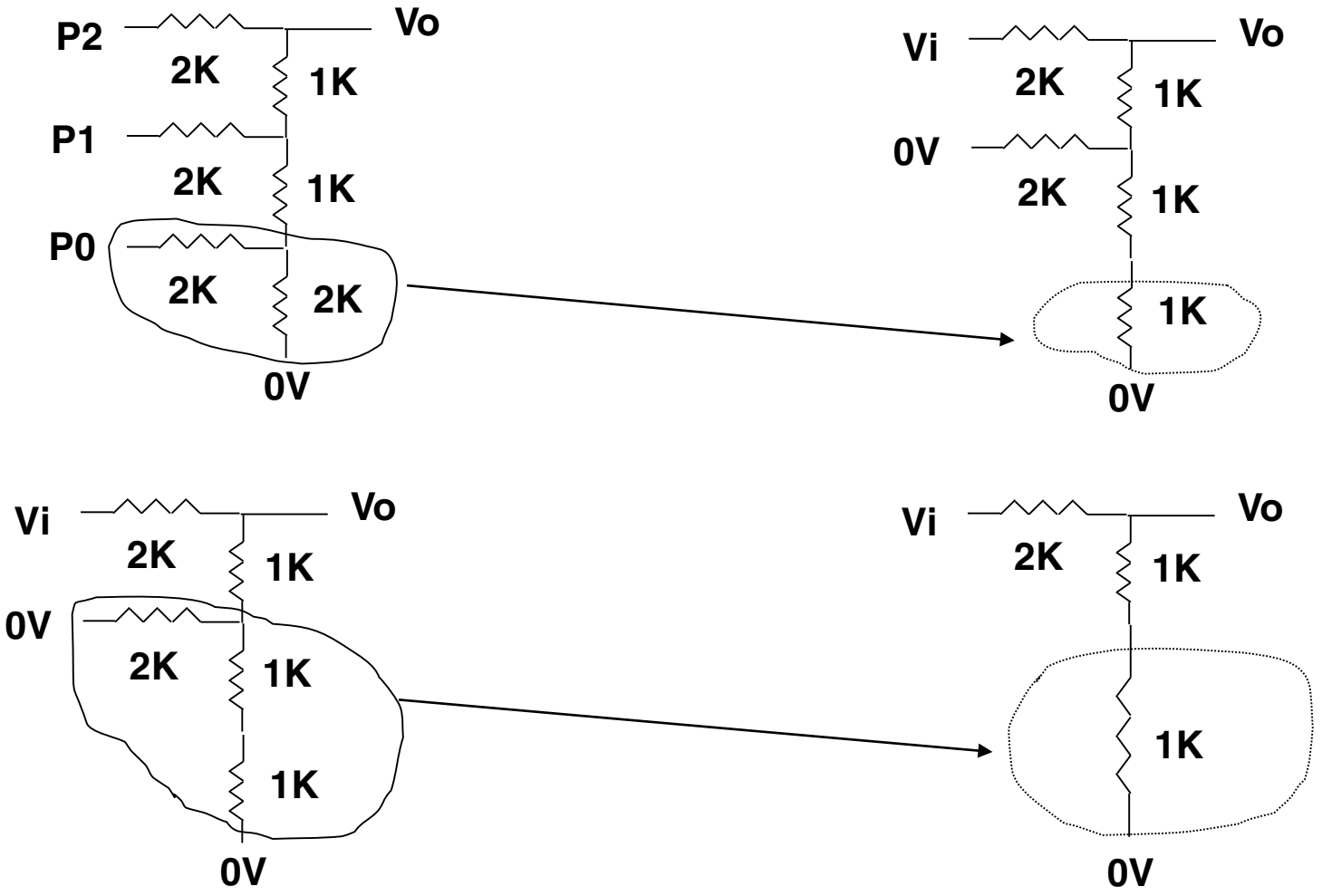
5-bit D2A



4-bit D2A

R-2R Resistive-Ladder D2A: 3Bit Example—I

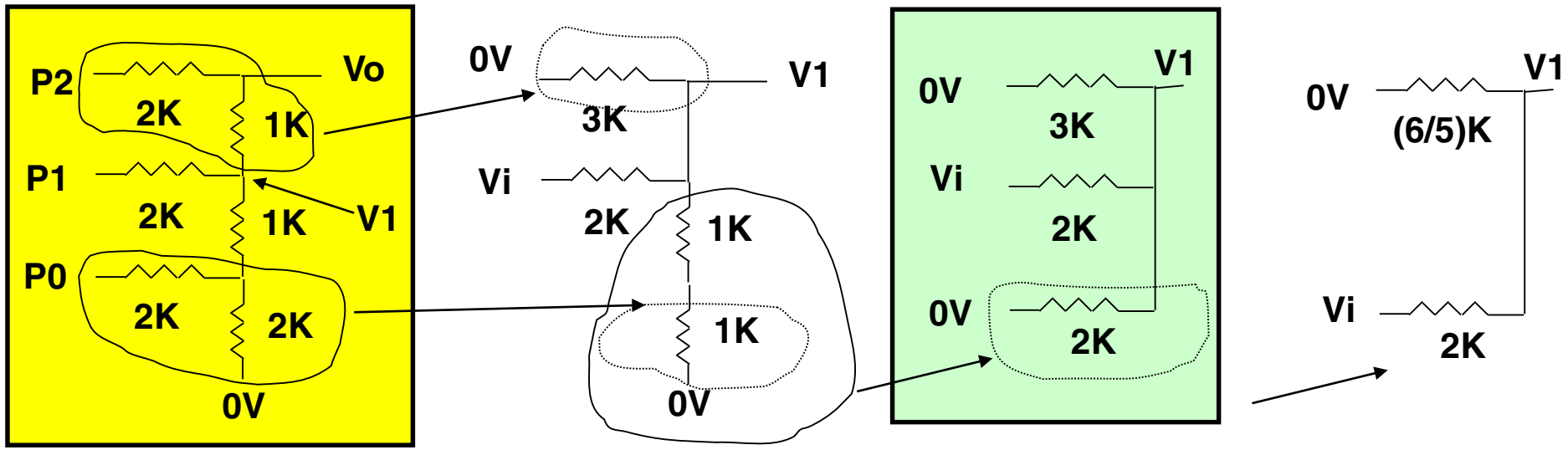
- Consider P0 = P1 = 0 and P2 = V_i = 5V



- So Vo=(1/2)Vi=2.5V

R-2R Resistive-Ladder D2A: 3Bit Example—II

- Consider P0=P2=0 and P1=Vi=5V

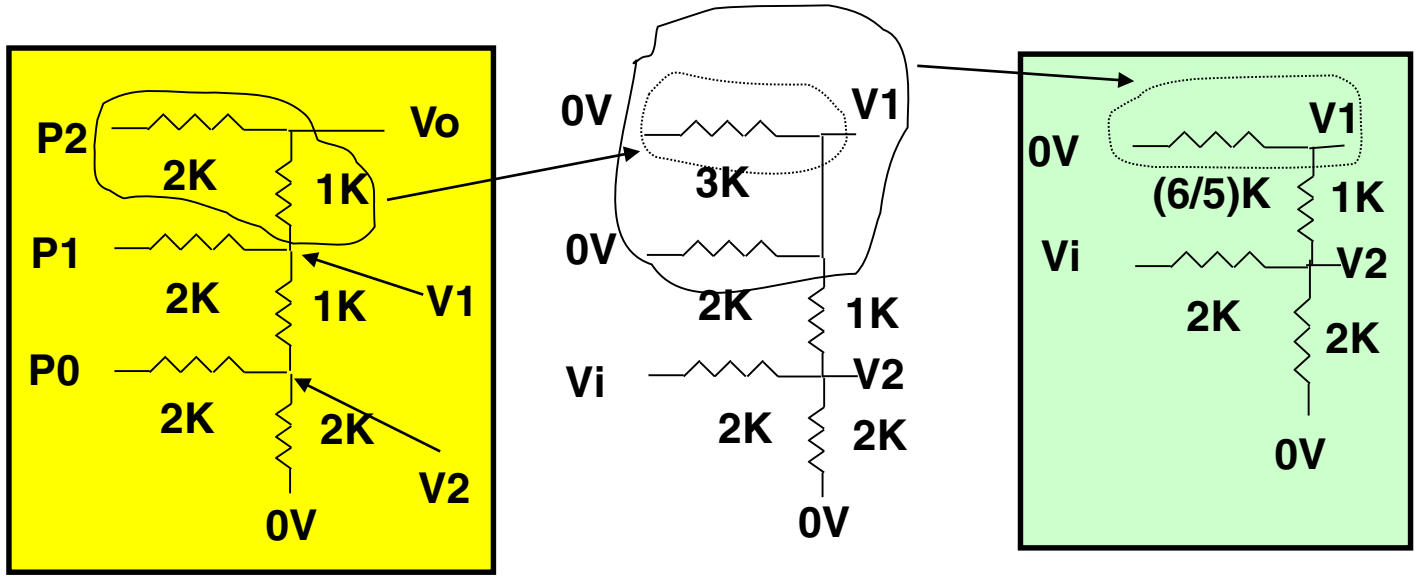


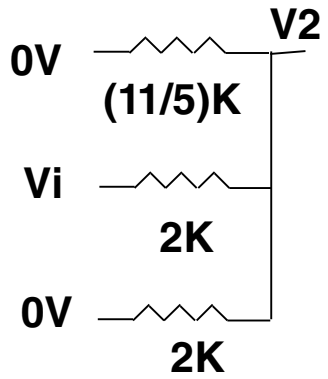
$$V1 = \frac{\frac{6}{5}}{\frac{6}{5}+2} Vi = \frac{6}{16} Vi$$

$$Vo = \frac{2}{3} V1 = \frac{2}{3} \times \frac{6}{16} Vi = \frac{1}{4} Vi = \frac{1}{4} \times (5V)$$

R-2R Resistive-Ladder D2A: 3Bit Example—III

- Consider P1=P2=0 and P0=Vi=5V



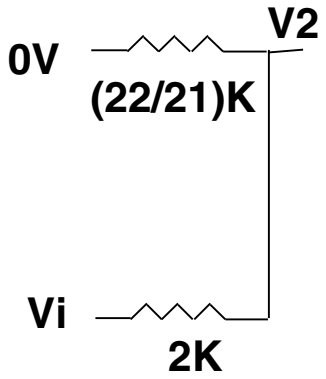


$$V2 = \frac{\frac{22}{21}}{\frac{22}{21}+2} Vi = \frac{22}{64} Vi$$

$$V1 = \frac{\frac{6}{5}}{\frac{6}{5}+1} Vi = \frac{6}{11} V2$$

$$Vo = \frac{2}{3} V1 = \frac{2}{3} \times \frac{6}{11} V2 = \frac{4}{11} V2$$

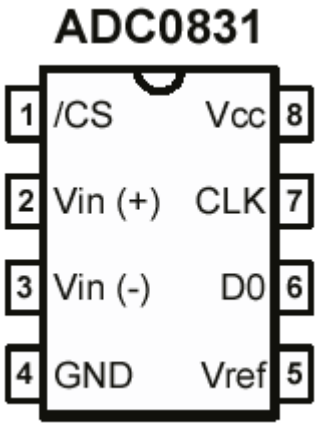
$$Vo = \frac{4}{11} \times \frac{22}{64} Vi = \frac{1}{8} Vi = \frac{1}{8}(5V)$$



AD0831

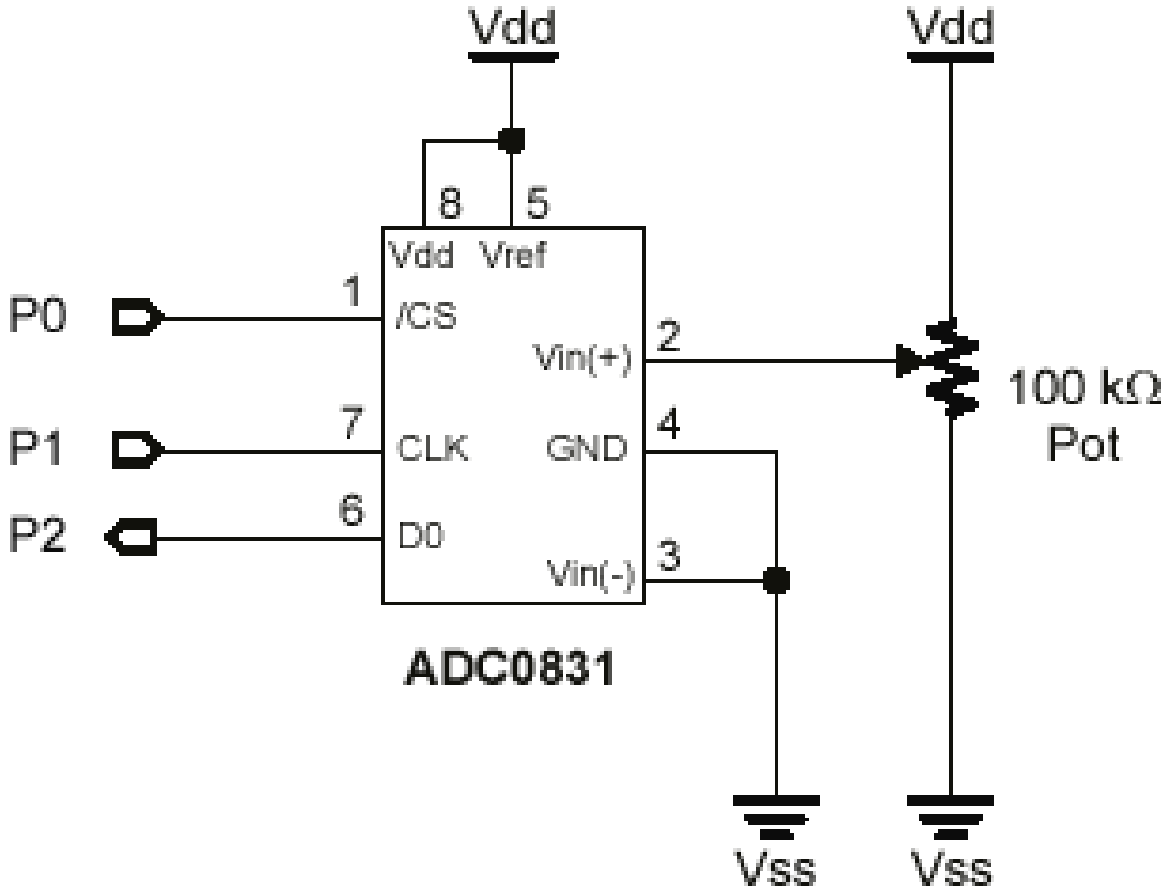
- 8-bit converter

Pins	Description
PIN1	Chip select pin: A2D is ready to do conversion when PIN1 is driven low
PIN2	0 to 5V analog input that needs to be digitized
PIN3	Zero offset adjustment
PIN4	Ground
PIN5	Span adjustment
PIN6	8 bit A2D output
PIN7	Clock signal from BS2
PIN8	Regulated 5V (Power supply)



A2D Circuit: AD0831

- In the A2D circuit shown here, we wish to measure a 0-5V analog signal.
  - The signal is generated using a potentiometer connected to a 5V source.
  - The zero offset is fixed at 0V by connecting PIN3 to 0V.
  - The span is set at 5V by connecting PIN5 to 5V.
  - This A2D has 8-bit resolution, thus the O/P is a number from 0 to 255.

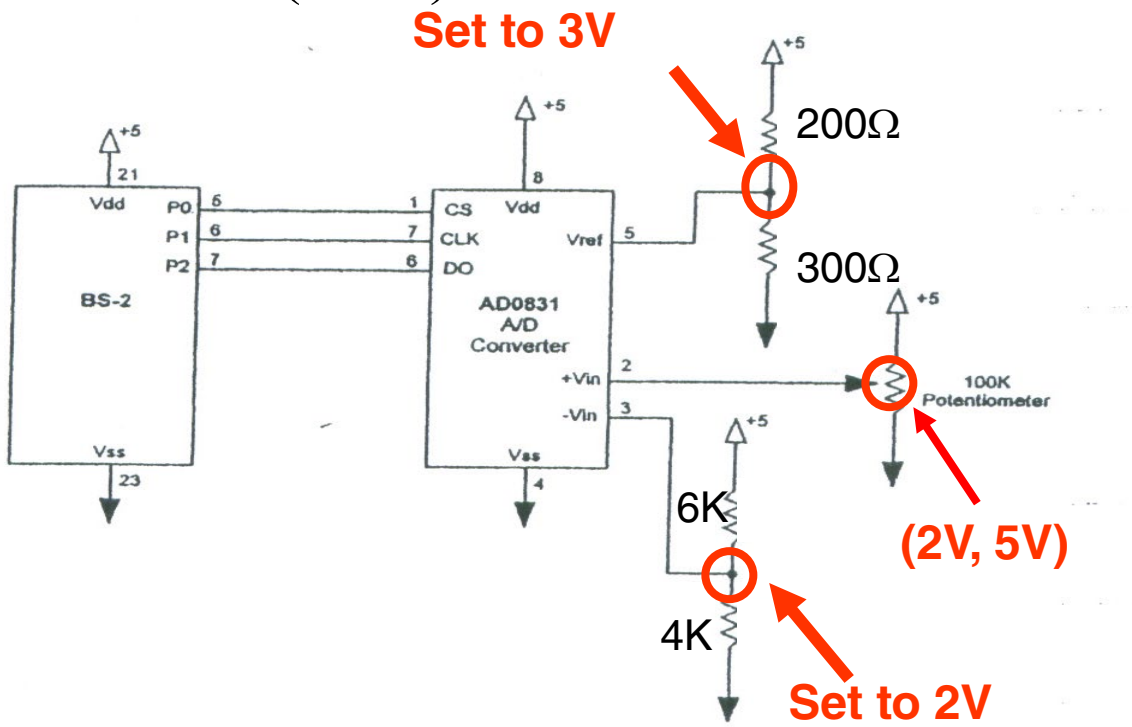


A2D Circuit: Offset Adjustment

- Using a 2V bias input on Pin3 of A2D, and 3V on Pin5, the analog signal from (2V, 5V) is digitized with full 8-bit resolution.

$$\frac{(2-2)V}{(5-2)V}\times 255 = 0$$

$$\frac{(5-2)V}{(5-2)V}\times 255 = 255$$



Hands-on Exercises: Digital Input

Basic Analog and Digital Basic Analog to Digital Conversion	Chapter 3
StampWorks Manual Experiment #28	pp. 156 – 161
Basic Analog and Digital Basic Digital to Analog Conversion	Chapter 4