AN1626/D

Noise Management in Motor Drives

Prepared by: Warren Schultz

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

During motor drive design and development, a lot of time is normally spent dealing with high noise levels that are present in these systems. A number of techniques are presented here that make the nuts and bolts of noise management easier, and therefore take a lot of re−design and debugging out of motor drive design. Many of these techniques trade some component cost for noise robustness. The benefits are reduced development cost, faster time to market, and a higher likelihood of trouble free operation in the field.

CIRCUIT TECHNIQUES

Circuit design can have a profound influence upon both the amount of noise produced and upon the susceptibility of motor drive circuits to the noisy environments in which they operate. The following discussion looks at N−Channel output stages, complementary output stages, and controllers.

N−Channel Output Stages:

For off−line motor drives that use N−Channel IGBT's, an illustration of noise robust circuit design is provided by comparing Figures 1 and 2. Figure 1 shows a minimal circuit topology for one Phase output. Figure 2 adds the components that it takes to make this topology noise robust.

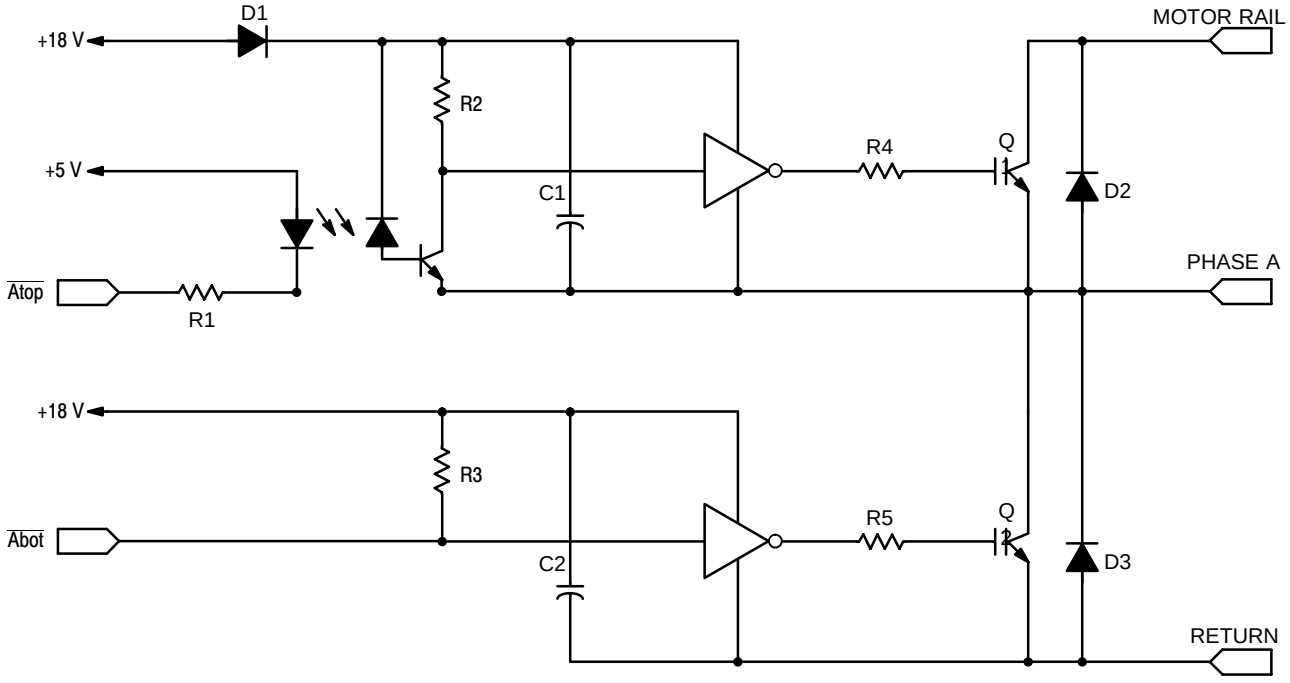

Figure 1. Minimal N−Channel IGBT Power Stage

March, 2007 − Rev. 1

Publication Order Number:
AN1626/D

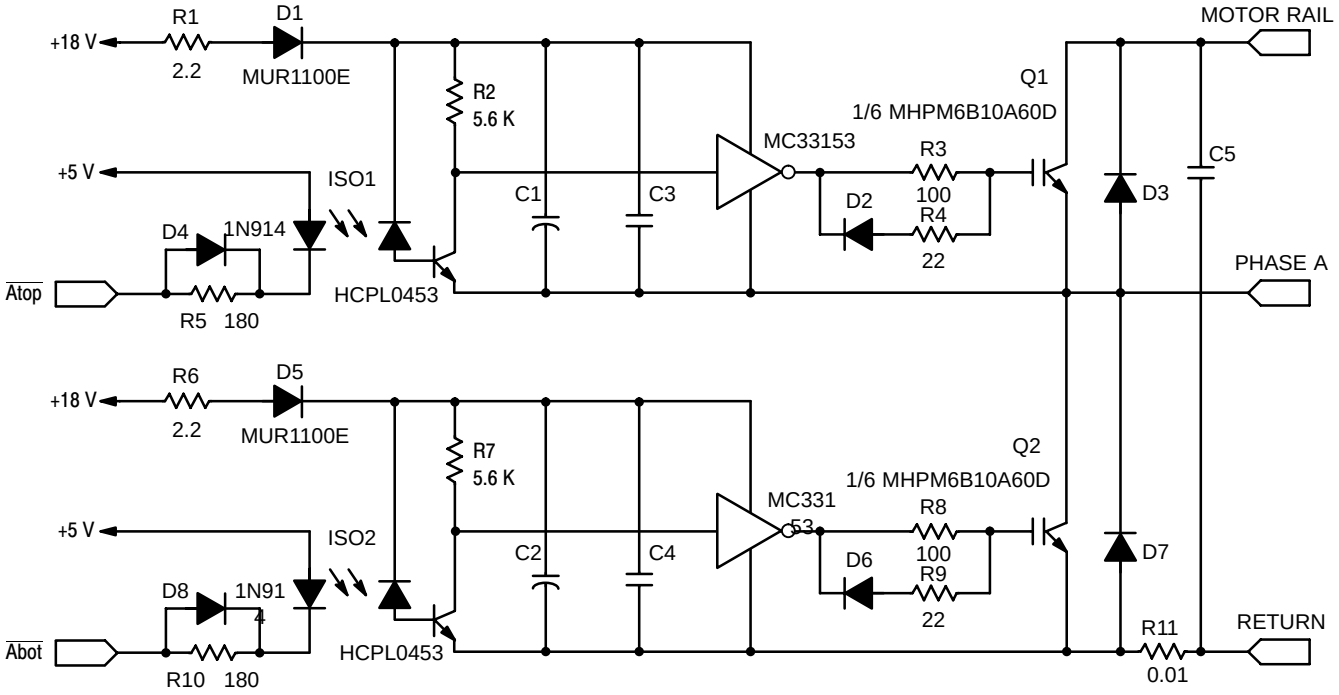

Figure 2. Robust N−Channel IGBT Power Stage

Perhaps the single biggest circuit design influence is the use of opto couplers. Opto's are widely used in upper half−bridge IGBT gate drives for level shifting. When used in the lower half−bridge gate drives as well, noise robustness is significantly improved.

Consider the robust design in Figure 2. Both Top and Bottom inputs are opto coupled to inverting gate drivers. This arrangement provides level shifting and also isolates the inputs from the high voltage power stage. The isolation provided by this circuit topology significantly improves noise immunity for two reasons. First, the opto's are very effective at keeping conducted noise away from microcontrollers. The noise isolation that they provide adds a degree of robustness that can make controller layout and debugging much simpler. Second, the use of opto's in the lower half bridge facilitates gate drive grounding, since the isolation allows each gate drive to be returned directly to the emitter of its corresponding IGBT. This is a significant issue with regard to power stage design, since ground noise effects on the gate drives is one of the more difficult issues.

To further illustrate this point, consider the schematic in Figure 3, where the lower half gate drives are not opto coupled. In this figure, all of the gate driver returns are first tied together, and then contact the power ground at only one point. The effects of this layout constraint are illustrated by showing parasitic ground inductance between phases as inductor Lp. When a switching transient occurs, the voltage drop across Lp shows up between the gate drivers and their respective IGBT's emitters. The result is unwanted gate−emitter voltage spikes that can cause turn−on or turn−off at inappropriate times. In contrast, use of opto couplers permits driver returns to be connected directly to their respective emitters, and eliminates the effects of phase to phase parasitic inductance.

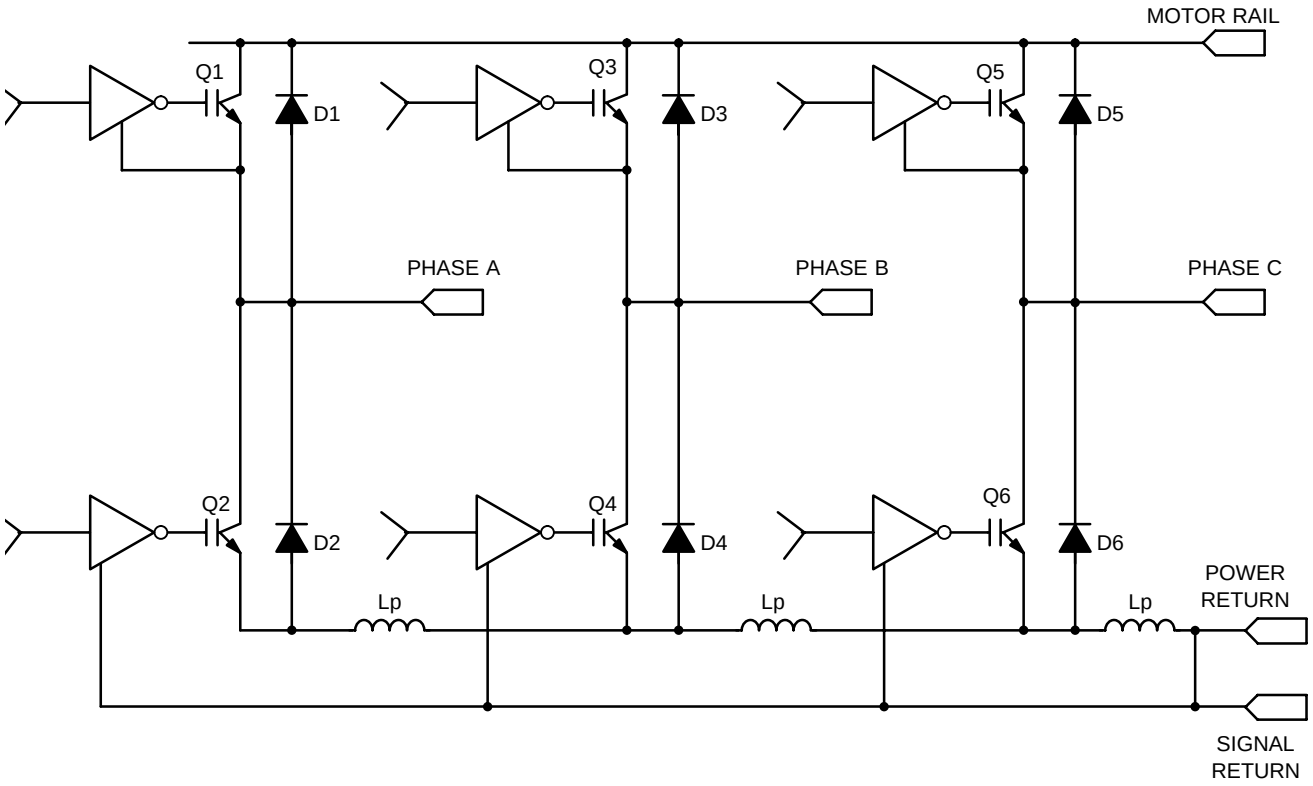

Figure 3. Ground Inductance

To put a rough order of magnitude on this issue, let's assume that 10 amps is switched in 25 nsec, and that Lp = 25 nH. The resulting voltage transient across Lp is then 25E−9(10/25E−9) = 10 volts. Since these transients occur between the gate driver outputs and IGBT gates, ten volt spikes can easily cause transitions to the wrong state. For drives that are less than 3 horsepower, careful layout can yield acceptable results. However, using opto couplers both top and bottom provides a much more noise robust design.

To help with gate transients, the MHPM6B10A60D IGBT's that are shown in Figure 2 have a 6 volt gate threshold, as opposed to the standard 3.5 volt threshold for MOS gated power devices. The higher threshold provides an additional 2.5 volts of noise margin with respect voltage spikes that will turn an IGBT on when it is supposed to be off. The MC33153 gate drivers that are also in this circuit have an under voltage lockout that is designed for the 6 volt threshold.

Referring again to Figure 2, diodes D4 and D8 reduce input impedance to the opto's when the inputs are high. The lower impedance provides higher noise immunity by insuring that the opto's remain off when they are supposed to be off, given an environment that includes high dv/dt. Resistors R1 and R6 protect the 18 volt gate drive supply from di/dt induced voltage transients. Without these resistors it is very difficult to get an all N−Channel power stage to work properly. They, in effect, act as shock absorbers, isolating the gate driver's bias voltage from L(di/dt) voltage spikes that are produced by switching the power devices. Although unnecessary for rectification, diode D5 serves the same function on the lower gate drive. C3 and C4 are ceramic capacitors that provide an improved high frequency return path for the gate drive during switching transients. A short high frequency return current path for the power devices is provided with C5. Polypropylene film capacitors, such as the WIMA MKP10 series, work well for this purpose.

Between the driver output and IGBT gates, two resistors and a diode are used instead of a single gate drive resistor. The additional components allow the IGBT's to turn on slower than they are turned off. Careful choice of turn−on time is important, since peak reverse recovery di/dt of the opposing transistor's freewheeling diode is dependent upon turn−on time. Since the most troublesome noise in a typical power stage is generated during reverse recovery, the two resistor topology and careful choice of values is an important part of the design.

Complementary Output Stages:

Complementary P−Channel / N−Channel MOSFET output stages are generally somewhat simpler than all N−Channel output stages, since voltages and power levels are lower. A typical circuit is illustrated in Figure 4. It shows a complementary output stage that is capable of operating at 5 amps and 48 volts. The design challenges in this type of circuit arise from the reverse recovery characteristics of the power MOSFETs' Drain−Source diodes. Unlike IGBT's with discrete diodes that are designed for softness, power

MOSFET drain−source diodes tend to be snappy during reverse recovery. Figure 5 illustrates this point. It shows a typical power MOSFET's drain−source diode recovery characteristics. After reaching a negative peak at turn−off, the diode's current returns very rapidly to zero. This behavior can produce di/dt's on the order of 1 amp per nsec.

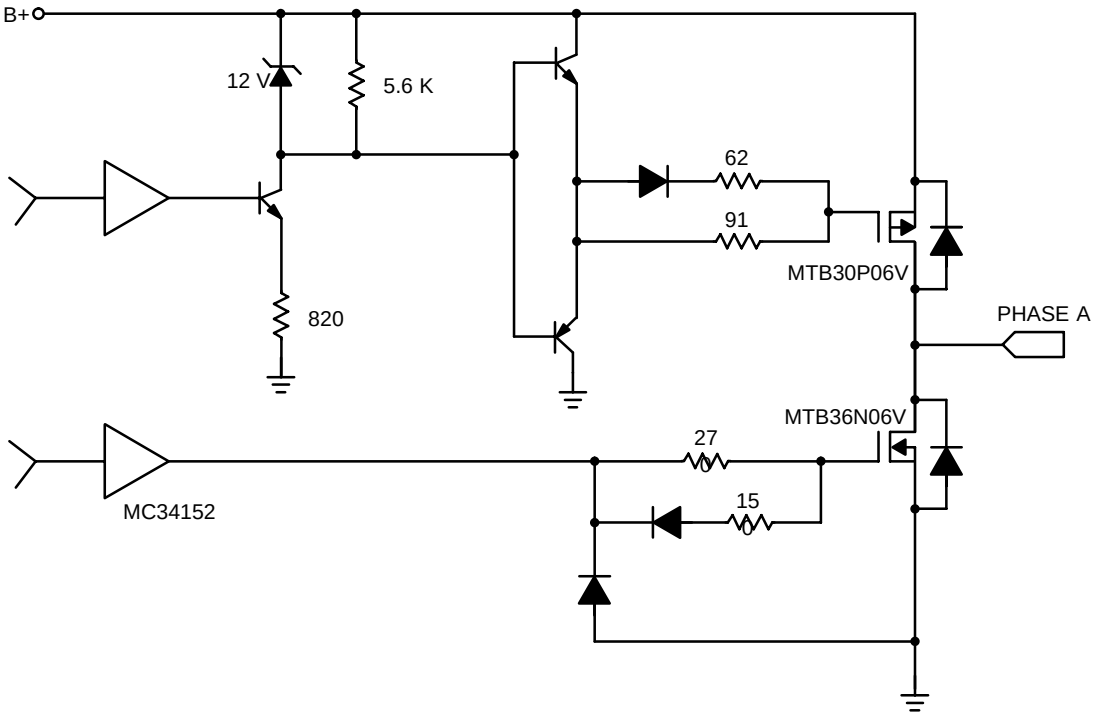

Figure 4. Complementary Power Stage

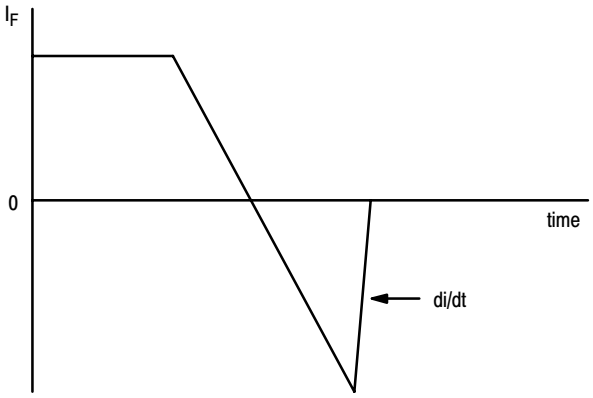

Figure 5. Drain−Source Diode Snap

At this rate, even 10 nH of parasitic inductance can produce troubling transients. Fortunately, diode snap can be slowed down somewhat with appropriate choice of gate drive resistors. Doing that requires different values for turn−on and turn−off. Figure 4 shows how, with two resistors and a diode for the gate of each MOSFET. In addition to using two values, the switching times that they target is very important. The values shown in Figure 4 produce rise and fall times of approximately 200 nsec. With 200 nsec switching times, the resulting gate drive impedances are high enough to permit a small amount of dv/dt induced shoot through current to flow, which considerably softens diode snap.

The way that this works is as follows. In addition to the reverse recovery current that you would normally expect, there is another current generated by switching transitions that can be called dv/dt induced shoot through current. When one transistor in the bridge turns on, its opposing transistor's drain is pulled rapidly to the opposite rail. dV/dt impressed at the drain causes a current to flow through the gate to drain capacitance and show up at the gate as input current. This current returns to the source potential through the gate drive's off−state impedance. It forward biases the gate by drive impedance times dV/dt current. If this voltage exceeds the off transistor's turn−on threshold, then dv/dt induced shoot through current is produced.

Although shoot through current is something that one normally strives to minimize, in this case a small amount is a good tradeoff for the resulting reductions in di/dt. During reverse recovery, dv/dt induced shoot through current adds to the diode's current waveform in a way that significantly reduces negative peak to zero di/dt. Correct choice of gate drive resistors can easily reduce peak di/dt by a factor of 3.

Brushless DC Motor Controllers:

Brushless DC motor controllers that use Hall Sensors pose noise immunity challenges related to the sensor inputs. The sensors are in an inherently noisy environment, since they are located in the motor close to PWM noise that is present in the windings. Given this situation, some motors do a much better job than others of presenting clean signals to the controller. For the general case, it is necessary to build some noise immunity into the way a Brushless controller receives Hall sensor inputs. An example of how this can be done is shown in Figure 6

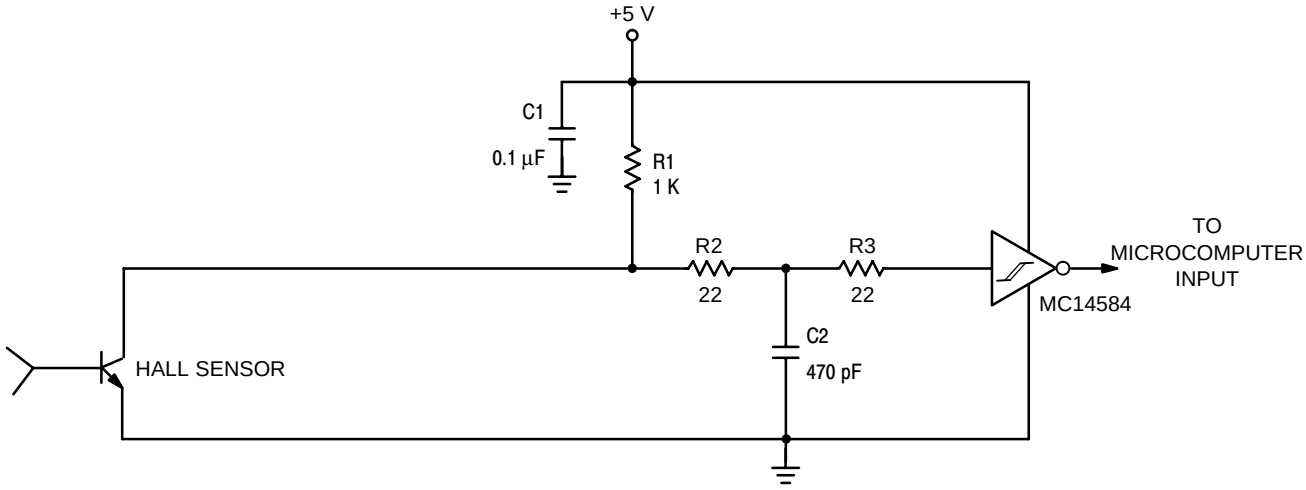

Figure 6. Hall Sensor Input

In this illustration, two techniques are used for isolating noise transmitted by Hall sensors. The first is a 100 nsec filter that is comprised of R2, C2, and R3. Since Hall sensor rise times are typically on the order of 500 nsec, the 100 nsec time constant does not significantly affect timing of the Hall signals, yet it is very effective at suppressing spikes that occur on Hall sensor lines. Once the signal is filtered, it is also a good idea to run it through a relatively slow 14000 series Schmidt trigger. The Schmidt trigger improves noise immunity by virtue of its hysteresis, and because 14000 series CMOS parts are inherently slower than most modern microcomputers. This is a case where it is very helpful not to use devices that are any faster than they need to be.

In addition to circuitry, the way that microcomputer code is written also has an important influence on noise robustness. Since the sequence of commutation is known, it is relatively easy to detect an out of sequence Hall sensor input. Generally speaking, when this occurs it is desirable to turn all the power transistors off until a valid Hall code is received. In other words, it is better to let the motor coast in the presence of an incorrect Hall input than to commutate to the wrong state.

LAYOUT

In a motor drive, layout is a critical part of the total design. Often, getting a system to work properly is actually more a matter of layout than circuit design. The following discussion covers some general layout principals, power stage layouts, and controller layouts.

General Principles:

There are several general layout principles that are important to motor drive design. They can be described as five rules:

Rule 1: Minimize Loop Areas. This is a general principle that applies to both power stages and noise sensitive inputs. Loops are antennas. At noise sensitive inputs, the area enclosed by an incoming signal path and its return is proportional to the amount of noise picked up by the input. At power stage outputs, the amount of noise that is radiated is also proportional to loop area.

Rule 2: Cancel fields by running equal currents that flow in opposite directions as close as possible to each other. If two equal currents flow in opposite directions, the resulting electromagnetic fields will cancel as the two currents are brought infinitely close together. In printed circuit board layout, this situation can be approximated by running signals and their returns along the same path but on different layers. Field cancelation is not perfect due to the finite physical separation, but is sufficient to warrant serious attention in motor drive layouts. Looked at from a different perspective, this is another way of looking at Rule #1, i.e., minimize loop areas.

Rule 3: On traces that carry high speed signals avoid 90 degree angles, including "T" connections. If you think of high speed signals in terms of wavefronts moving down a trace, the reason for avoiding 90 degree angles is straightforward. To a high speed wavefront, a 90 degree angle is a discontinuity that produces unwanted reflections. From a practical point of view, 90 degree turns on a single trace are easy to avoid by using two 45 degree angles or a curve. Where two traces come together to form a "T" connection, adding some material to cut across the right angles accomplishes the same thing.

Rule 4: Connect signal circuit grounds to power grounds at only one point. The reason for this constraint is that transient voltage drops along power grounds can be substantial, due to high values of di/dt flowing through finite inductance. If signal processing circuit returns are connected to power ground a multiple points, then these transients will show up as return voltage differences at different points in the signal processing circuitry. Since signal processing circuity seldom has the noise immunity to handle power ground transients, it is generally necessary to tie signal ground to power ground at only one point.

Rule 5: Use ground planes selectively. Although ground planes are highly beneficial when used with digital circuitry, in power control systems they are better used selectively. A single ground plane in a motor drive would violate Rule #4 by mixing power and signal grounds at multiple points. In addition, ground planes tend to make large antenna's for radiating noise. In motor drives, a good approach is to use ground planes for digital circuitry, and use ground traces in the power stages and for analog circuitry.

Power Stages:

There are two overriding objectives with regard to power stage layout. First, it is necessary to control noise at the gate drives so power devices are not turned on when they are supposed to be off or vice versa. Second, it is highly desirable to minimize radiated noise with layout, where tight loops and field cancellation can reduce the cost of filters and enclosures.

Looking first at gate drive, noise management is greatly facilitated by using the source or emitter connection for each power device as a miniature ground plane for that device's gate drive. This is particularly important for high side N−Channel gate drives, where the gate drivers have high dv/dt displacements with respect to power ground. If the power device's source or emitter connection is used like a ground plane, parasitic capacitive coupling back to power ground is minimized, thereby increasing the dv/dt immunity of the gate drive.

Consider the circuit that is shown in Figure 7. Further let's assume that the phase output swings 300 volts in 100 nsec, and that the parasitic capacitance to power ground, Cp, is only 1 pF. Then a simple i = C(dv/dt) calculation suggests that 3 mA of charging current will flow through Cp. This 3 mA into 5.6 K ohms of node impedance is much more than enough to cause false transitions. These numbers illustrate a very high sensitivity to parasitic coupling, which makes layout of this part of the circuit very important.

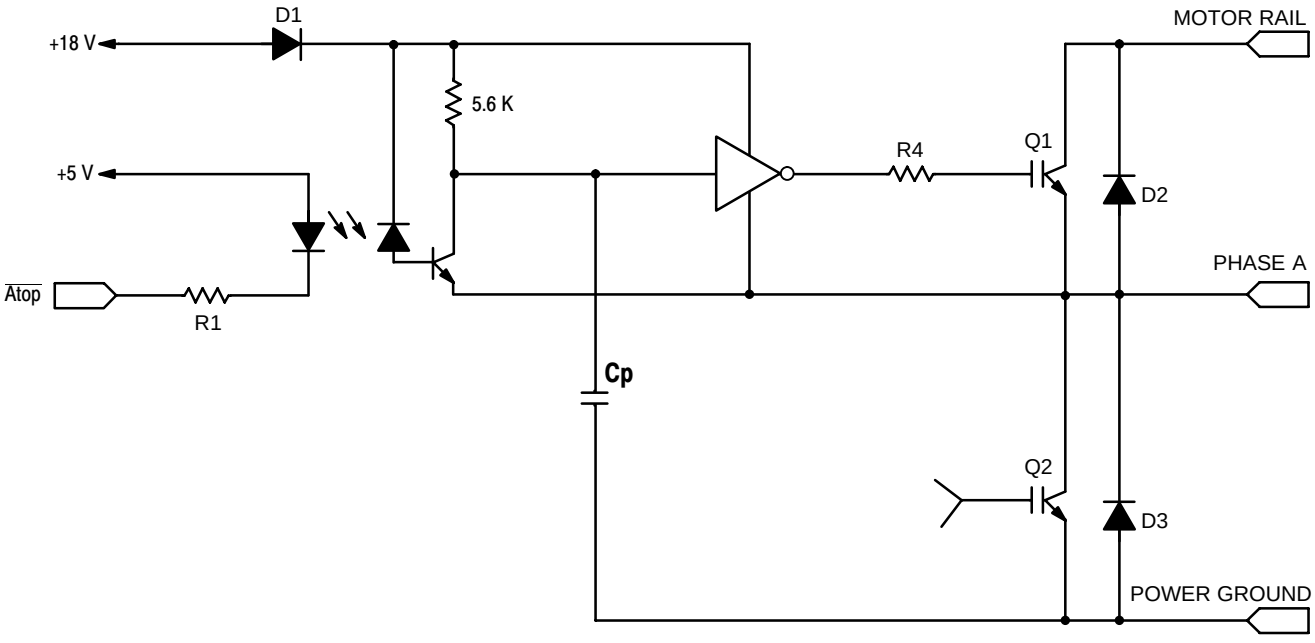

Figure 7. Parasitic Capacitance

In addition to viewing source or emitter connections as miniature ground planes, it is also important to keep any signals referenced to ground at least 1/8th inch away from high side gate driver inputs. Given this constraint, it is easy to see why use of use of a single ground plane in power stages is not usually good design practice.

Gate drive noise immunity is also facilitated by minimizing the loop area that contains the gate drive decoupling cap, gate driver, gate, and source or emitter of the power device. One way to do this is to route the gate drive signal either directly above or beneath its return. If the return is relatively wide (1/10th inch or greater) it forms the miniature ground plane that was previously discussed. The resulting minimum loop area minimizes capacitive coupling as well as antenna effects that inject noise at the input of the gate driver. In addition, relatively high peak gate drive currents get some field cancellation, which reduces radiated noise.

The other major source of gate drive noise that causes false transitions is non−zero voltage drops in power grounds. Using opto couplers and routing each gate drive return directly to the emitter of its corresponding power device is the cleanest way to provide noise immunity. For fractional horsepower drives where opto couplers are not practical, taking care to minimize the inductance between power device emitters or sources is a viable alternative.

In terms of reducing the amount of noise that is produced by power stages, minimizing loop areas is a key consideration. The most important is the loop that includes the upper half−bridge IGBT drain, lower half−bridge IGBT source, and high frequency bus decoupling cap. The idea here is to try to keep the high di/dt that is produced during diode reverse recovery in as small an area as possible. This is a part of the circuit where running traces that have equal but opposite currents directly over each other is a priority. Since the currents into and out of the decoupling cap are equal and opposite, running these two traces directly over each other provides field cancellation and minimum loop areas where they are needed most.

Figure 8 illustrates the difference between a loop that has been routed correctly and one that has not. In this figure, the solid circles represent pads, the schematic symbols show the components that are connected to the pads, and two routing layers are shown with cross−hatching that goes in opposite directions. Note that by routing the two traces one over the other that the critical loop area is minimized.

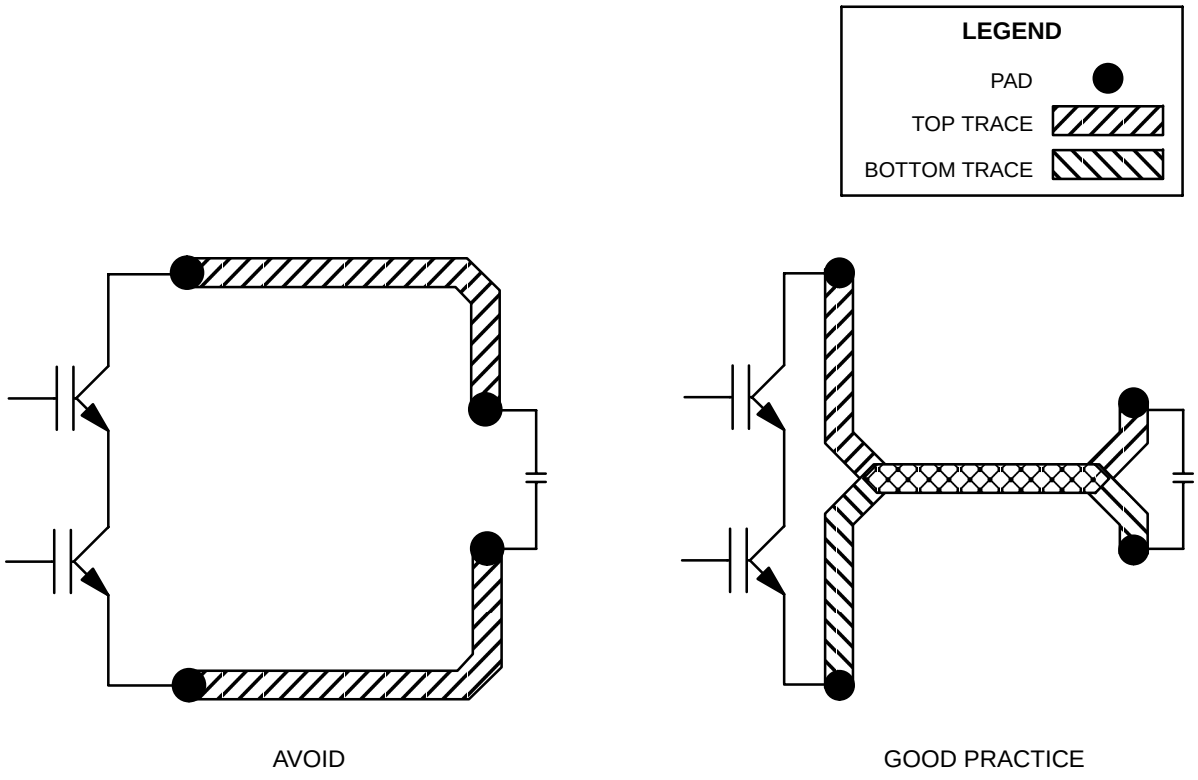

Figure 8. Minimizing Loop Areas

For similar reasons it is desirable to run power and return traces one directly on top of the other. In addition, if a current sampling resistor is used in the return, using a surface mount resistor is preferable due to its lower inductance. It also can be placed directly over the power trace, providing uninterrupted field cancellation from placing power and return traces over each other. Again for field cancellation, it is also desirable to run phase outputs parallel and as close as possible to each other.

The power stage is the place where avoiding right angles is most important. Single traces are easy, two forty five degree angles or a curve easily accomplish a 90 degree turn. It is just as important to avoid 90 degree angles in T connections. Figure 9 illustrates correct versus incorrect routing for both cases.

Figure 9. 90 Degree Angles

Controllers:

The primary layout issue with controllers is ground partitioning. A good place to start is with the architecture that is shown in Figure 10. This architecture has several key attributes. Analog ground and power ground are both separate and distinct from digital ground, and both contact digital ground at only one point. For analog ground it is preferable to make the one point as close as possible to the analog to digital converter's ground reference (VREFL). For power ground the connection should be as close as possible to the microcomputer's power supply return (VSS). Note also that the path from VREFL to VSS is isolated from the rest of digital ground until it approaches VSS.

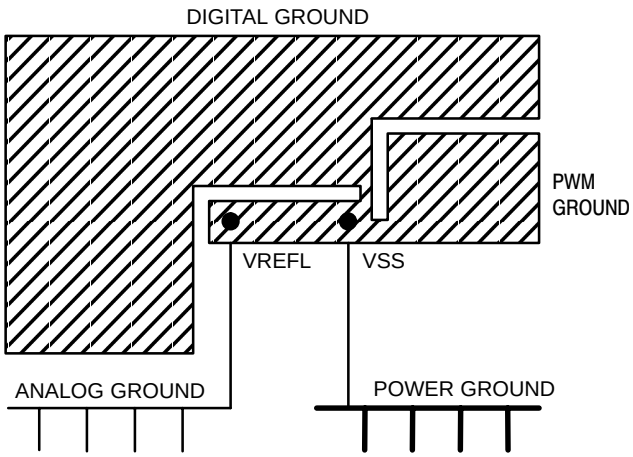

Figure 10. Ground Architecture

PWM ground is also isolated as a separate ground plane section until it approaches VSS. This is most important in systems that use opto couplers, since the current that flows through the PWM ground return will be higher than other digital return currents. If a two layer board is used, traces replace the ground planes that are shown in Figure 10. The partitioning, however, remains the same.

In addition to grounding, controllers benefit from attention to avoiding 90 degree angles, since there are generally a lot of high speed signals on the digital portion of the board. Routing with 45 degree angles or curves minimizes unwanted reflections, which increases noise immunity.

CONCLUSION

For the most part, the functional architecture of motor drives is much more straightforward than some of the techniques that are required to get them to work. The non−straightforward aspects arise from high levels of both di/dt and dv/dt that produce a lot of noise management design issues. These are systems in which a fraction of a picofarad of stray capacitance in the wrong place, a ground connection that is not carefully routed, or the absence of a functionally not so obvious component will all cause improper operation.

The most important design issues are careful attention to grounding, minimizing critical loop areas, use of series bootstrap resistors, careful attention to power transistor transition times, and filtering sensor inputs. Additional benefits are gained by avoiding 90 degree angles in board layout and cancelling fields by routing equal and opposite current flows as close as possible to each other. As expected, consideration given to these issues up front pays off when it comes to getting a design to work right the first time.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative