

# Neo: Real-Time On-Device 3D Gaussian Splatting with Reuse-and-Update Sorting Acceleration

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## Abstract

3D Gaussian Splatting (3DGS) rendering in real-time on resource-constrained devices is essential for delivering immersive augmented and virtual reality (AR/VR) experiences. However, existing solutions struggle to achieve high frame rates, especially for high-resolution rendering. Our analysis identifies the sorting stage in the 3DGS rendering pipeline as the major bottleneck due to its high memory bandwidth demand. This paper presents Neo, which introduces a reuse-and-update sorting algorithm that exploits temporal redundancy in Gaussian ordering across consecutive frames and devises a hardware accelerator optimized for this algorithm. By efficiently tracking and updating Gaussian depth ordering instead of re-sorting from scratch, Neo significantly reduces redundant computations and memory bandwidth pressure. Experimental results show that Neo achieves up to 10.0 $\times$  and 5.6 $\times$  higher throughput than state-of-the-art edge GPU and ASIC solution, respectively, while reducing DRAM traffic by 94.5% and 81.3%. These improvements make high-quality and low-latency on-device 3D rendering more practical.

**CCS Concepts:** • Computer systems organization → Architectures; • Computing methodologies → Rendering.

**Keywords:** Domain Specific Architecture (DSA), Accelerator, Neural Rendering, 3D Gaussian Splatting (3DGS)

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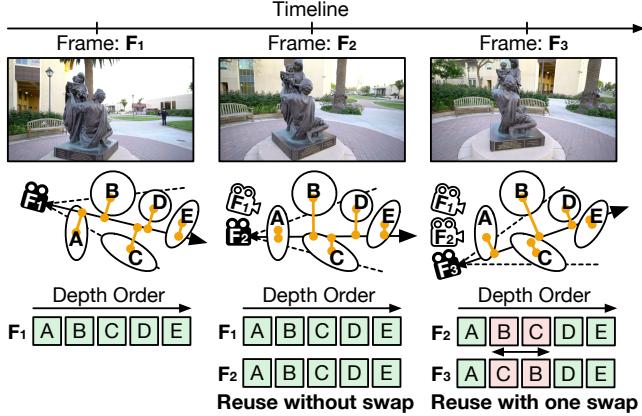
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## 1 Introduction

The success of Generative AI in text generation [1, 8, 12, 28, 46, 52, 60, 76, 77, 95, 106] has demonstrated its potential, paving the way for researchers to explore its next step: virtual world generation [4, 7, 15, 31, 32, 39, 43, 62, 84, 86]. Modern augmented and virtual reality (AR/VR) devices such as Apple Vision Pro [2], Meta Orion AR Glasses [67], and Meta Quest 3 [66] exemplify the growing demand for immersive environments, where human interactions unfold in dynamic, computer-generated worlds, necessitating high-fidelity content and scalable virtual world creation.

*View synthesis*, which creates new viewpoints of a scene from existing data, is crucial for enabling virtual experiences. Recently, 3D Gaussian Splatting (3DGS) has emerged as an effective technique that balances rendering quality and performance, while providing a low-cost solution for immersive applications. To ensure a smooth user experience [24, 101], such applications demand high-resolution rendering with ultra-low latency (e.g., 7–15ms[3]). While cloud processing may appear attractive, it introduces critical delays [5, 6], thereby necessitating on-device 3DGS rendering.

However, this on-device requirement creates tension with the high computational demands of real-time view synthesis. For instance, industry-leading automotive GPUs such as the Jetson Orin [37, 74] and even the state-of-the-art 3DGS-optimized accelerator [50] deliver only around 60 FPS at HD resolution, offering lower frame rates when targeting the per-eye high-resolution commonly used in AR/VR, such as 2K or 4K per eye [2, 33, 68, 82, 93, 97]. This performance gap underscores the need for more efficient on-device solutions.



**Figure 1.** Reuse opportunities in the sorting stage of 3D Gaussian Splatting (3DGS) inference. The figure illustrates how the Gaussian order across three consecutive frames ( $F_1$ ,  $F_2$ , and  $F_3$ ) exhibits significant temporal similarities.

To better understand the bottlenecks and opportunities, we first conduct a thorough performance characterization of an existing 3DGS accelerator, GSCore [50]. Our analyses suggest that GSCore effectively mitigates bottleneck in rasterization, leaving the sorting stage as a new and dominant bottleneck in the rendering pipeline. Unfortunately, sorting is a well-established operation in modern computing, making it inherently difficult to accelerate through conventional means. However, 3DGS renders frames sequentially over time, repeatedly performing sorting on largely similar Gaussian orders across consecutive frames. This temporal redundancy presents an opportunity to minimize redundant computations and improve efficiency.

Inspired by this insight, this paper proposes Neo by jointly designing (1) reuse-and-update sorting mechanism to exploit temporal redundancy in Gaussian ordering and (2) a hardware-accelerated sorting pipeline for on-device 3DGS rendering. Figure 1 depicts the reuse opportunities that form the basis of the proposed reuse-and-update sorting mechanism. In designing Neo, we identify the following challenges:

- **Challenge 1: High sorting overhead in rendering.** In general, sorting is performed occasionally and reused across iterations. However, sorting in 3DGS differs from general purpose sorting, as it requires reordering millions of Gaussians for every rendered frame. Existing sorting implementations rely on bandwidth-intensive memory accesses, making real-time on-device rendering impractical.
- **Challenge 2: Missed temporal redundancy in sorting.** Re-sorting Gaussians from scratch every frame overlooks the strong temporal locality inherent in 3DGS rendering. Since most Gaussians retain similar depth order across consecutive frames, treating each frame independently leads to redundant computations and excessive DRAM traffic, limiting scalability at high resolutions.

To address the aforementioned challenges, this paper makes the following contributions.

- **Reuse-and-update sorting for temporal redundancy exploitation.** Neo introduces a reuse-and-update sorting mechanism that leverages the temporal redundancy in 3D Gaussian Splatting (3DGS) rendering. Instead of sorting Gaussians from scratch for every frame, Neo efficiently tracks and updates the sorted Gaussian table across consecutive frames. By identifying minimal changes in Gaussian ordering over time, this mechanism significantly reduces redundant sorting computations and memory bandwidth overhead. Moreover, by selectively updating only designated segments of the table, Neo minimizes unnecessary operations, thereby improving overall processing efficiency. As a result, this optimization enables real-time sorting at AR/VR resolutions while maintaining rendering accuracy, even in scenes with frequent viewpoint changes.
- **Accelerating sorting stage for on-device rendering.** Neo implements a hardware-accelerated sorting pipeline optimized for efficient on-device 3DGS rendering. While existing accelerators focus primarily on optimizing rasterization, they overlook the inefficiencies of sorting, resulting in excessive DRAM traffic. Neo addresses this limitation by integrating dedicated sorting hardware that minimizes memory access overhead and accelerates depth-based Gaussian ordering within the rendering pipeline. This hardware adopts a hybrid sorting strategy that integrates both partial and global ordering, effectively performing Gaussian sorting with low computational overhead. By coupling this hardware support with a reuse-and-update sorting mechanism, Neo delivers significant improvements in both latency and throughput, making real-time, high-resolution AR/VR rendering practical.

To evaluate Neo, we implement a cycle-accurate simulator based on the 3DGS rendering pipeline and model the execution of sorting operation. Our evaluation uses a representative set of neural rendering workloads, including complex scenes to assess the impact of temporal redundancy. We synthesize Neo using Synopsys Design Compiler with ASAP 7nm library [98] and measure its performance and memory bandwidth usage against NVIDIA Orin AGX GPU [37] and the state-of-the-art accelerator GSCore [50]. Our results show that Neo achieves up to  $10.0\times$  and  $5.6\times$  higher throughput compared to the Orin AGX GPU and GSCore, respectively, while reducing sorting-induced memory traffic by 94.4% and 81.3%. Furthermore, Neo enables real-time 3DGS rendering at QHD resolutions, achieving the average throughput of 99.3 FPS required for smooth AR/VR experiences. These results demonstrate that Neo effectively overcomes the sorting bottleneck in real-time 3DGS rendering, advancing the realization of generative virtual worlds and enabling truly immersive on-device experiences.

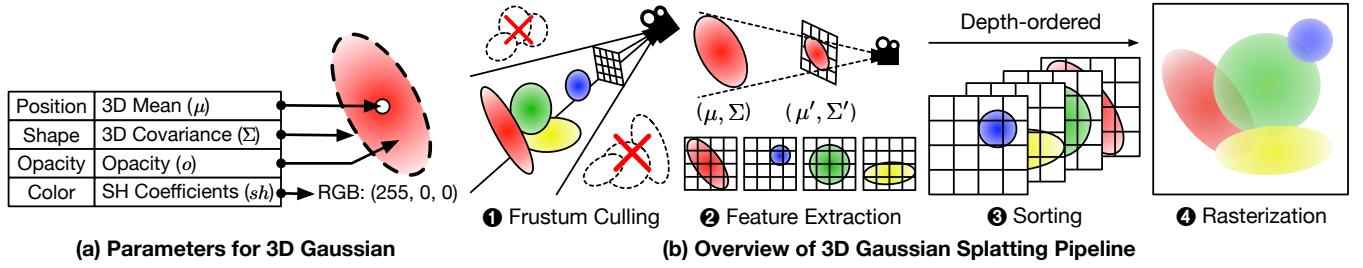


Figure 2. Brief overview of 3D Gaussian Splatting.

## 2 Background

### 2.1 Real-Time 3D Rendering in On-Device Systems

Recent advances in augmented and virtual reality (AR/VR) have driven the development of mobile devices and headsets [2, 34, 66, 81, 93] capable of rendering high-fidelity scenes. These on-device platforms support high frame rates and resolution, delivering immersive experiences. For instance, Apple Vision Pro [2] features a combined 23 million pixels, achieving 4K-level resolution. Meanwhile, Meta Quest 3 [66] provides a per-eye resolution of 2064×2208, with both devices supporting refresh rates of up to 90Hz. These stringent specifications are critical for delivering immersive experiences and ensuring user comfort [100, 101]. However, meeting these demands is challenging when rendering high-fidelity scenes given the limited computing resources of on-device systems. A straightforward approach is offloading rendering requests to cloud servers. However, this method suffers from frame drops due to network congestion, which is a critical issue in latency-sensitive rendering applications [5, 6]. These constraints highlight the necessity for on-device AR/VR platforms to integrate on-device rendering capabilities.

### 2.2 3D Gaussian Splatting (3DGS)

3DGS [38] has emerged as a promising rendering method for synthesizing complex real-world scenes while achieving real-time rendering performance. To render 3D scenes, 3DGS exploits millions of 3D Gaussians, modeled as anisotropic ellipsoids. As illustrated in Figure 2(a), each Gaussian is identified by a radial opacity  $\alpha$ , as shown in Equation 1:

$$\alpha(x) = o \cdot e^{-\frac{1}{2}(x-\mu)^T \Sigma^{-1} (x-\mu)} \quad (1)$$

where  $o$  is an opacity value,  $\mu$  is a mean vector,  $\Sigma$  is a 3D covariance matrix. In addition,  $sh$  refers to spherical harmonics coefficients, which enable rendering of view-dependent color [27]. These explicit 3D representations are learnable parameters, trained with differentiable rasterization and gradient-based optimization. Given a set of Gaussians, 3DGS employs a  $\alpha$ -blending process [83], akin to traditional rendering methods [9] that use explicit 3D representations to render scenes. This innovative approach incorporates the strengths of both traditional scene reconstruction methods [51, 99, 102] and prior neural rendering techniques [23, 69, 71, 85], delivering exceptional rendering quality and performance.

### 2.3 3D Gaussian Splatting Pipeline

Figure 2(b) denotes the 3DGS pipeline with four main stages: frustum culling, feature extraction, sorting, and rasterization.

**1 Frustum Culling.** First, the system discards Gaussians that are not visible from the current camera viewpoint and preserves only those required for subsequent stages. This initial filtering process reduces redundant computations for Gaussians outside the camera's field of view.

**2 Feature Extraction.** With the filtered 3D Gaussians, the system projects them onto the camera's image plane, extracting their view-dependent features in conjunction with the camera viewpoint. This includes 2D representations  $(\mu', \Sigma')$  transformed by 3D parameters  $(\mu, \Sigma)$  and color  $(c)$  calculated using the coefficients of spherical harmonics  $(sh)$  [27].

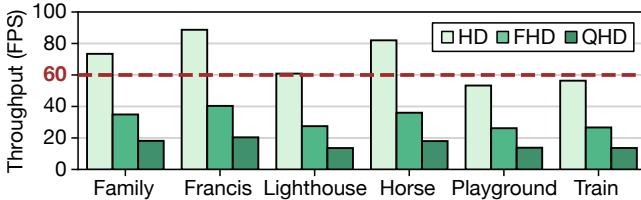
**3 Sorting.** After extracting features from 3D Gaussians, the projected 2D Gaussians overlap on the image plane. At this stage, the system sorts them by depth. This ordering is a crucial step for the subsequent rasterization stage, which leverages it to blend overlapping 2D Gaussians by accumulating their pixel colors in a depth-sorted manner.

**4 Rasterization.** At this stage, the system computes pixel colors by  $\alpha$ -blending [83] the depth-sorted Gaussians. Starting from the foremost Gaussian, each Gaussian contributes to the pixel color and accumulates opacity. When the cumulative opacity exceeds a predefined threshold, further processing for that pixel stops, as its color is considered finalized, thereby reducing unnecessary computation.

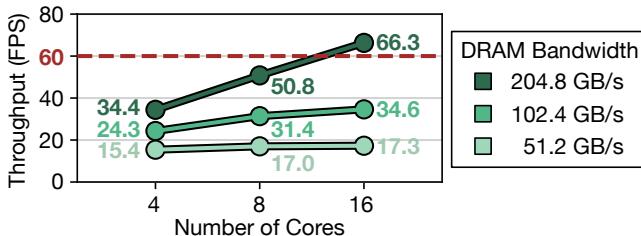
### 2.4 3D Gaussian Splatting Acceleration

**Tile-based parallelism.** For efficient rendering, the 3DGS system subdivides the image plane into a grid of smaller 2D regions (*tiles*). In the ③ sorting stage, it duplicates and distributes Gaussians to the intersected tiles, and in the ④ rasterization stage, it processes 2D Gaussians on a *per-tile* basis. This approach enables the system to process only the Gaussians within each tile's boundary, thereby reducing redundant computation. Furthermore, it leverages hardware threads to process multiple tiles in parallel, further improving overall rendering performance.

**GPU implementations.** To leverage this parallelism, 3DGS methods [38, 73, 78] employ GPUs for tile-based sorting and rasterization. They utilize NVIDIA CUB library [75] for sorting and implement custom CUDA kernels [44] to



**Figure 3.** Throughput comparison with different resolutions.



**Figure 4.** Throughput comparison across core counts and DRAM bandwidth when rendering at QHD resolution. Each colored label denotes the corresponding FPS performance.

support a cumulative  $\alpha$ -blending during rasterization. Although these GPU-driven approaches enhance rendering performance through extensive parallel processing, the cumulative  $\alpha$ -blending step remains a significant bottleneck, especially in on-device AR/VR environments.

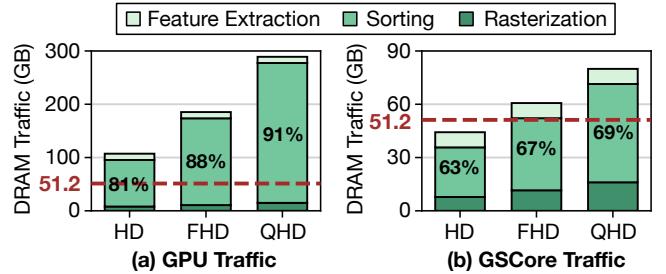
**ASIC acceleration: GSCore.** To address this challenge, recent work GSCore [50] introduces a pioneering ASIC-based acceleration solution for on-device 3DGS systems. By adopting hierarchical tile-based sorting and subtile-based rasterization, GSCore efficiently processes millions of Gaussians under tight resource constraints. While this specialized co-design significantly outperforms GPU-based solutions, the stringent on-device constraints continue to push resource demands beyond what GSCore approaches can readily handle. In the following section, we analyze how these constraints affect on-device 3DGS performance and define the key research challenge of this work.

### 3 Motivation

#### 3.1 Challenge in On-Device 3DGS Rendering

Despite GSCore’s efforts to accelerate 3DGS rendering, achieving real-time performance under the high frame rate and resolution requirements of modern AR/VR platforms (see Section 2.1) remains a significant challenge. To analyze these characteristics, we selected six scenes from the Tanks and Temples dataset [42]: Family, Francis, Horse, Lighthouse, Playground, and Train, which were captured in real-world outdoor environments and serve as representative benchmarks for evaluating the performance of 3DGS rendering.

**Rendering performance under constraints.** Figure 3 shows the throughput (FPS) performance of GSCore at three different resolutions: HD (1280×720), FHD (1920×1080), and QHD (2560×1440). Following the rationale described in the



**Figure 5.** DRAM traffic (GB) required for rendering 60 frames and breakdown of memory bandwidth consumption across 3DGS pipeline stages.

original paper [50], we configure the evaluation system with 4 computing cores and a DRAM bandwidth of 51.2 GB/s. This configuration enables a thorough assessment of GSCore’s FPS performance within the tight resource budgets typical of on-device AR/VR environments. The results show that GSCore achieves 66.7 FPS at HD (1280×720), exceeding the conservative service-level objective (SLO) requirement of 60 FPS. However, at higher resolutions GSCore experiences a significant FPS drop, achieving only 31.1 FPS and 15.8 FPS at FHD and QHD, respectively. These performance limitations underscore the need for a robust acceleration solution capable of delivering scalable and responsive 3DGS rendering within resource-constrained on-device systems.

#### 3.2 Performance Characterization of 3DGS

To better understand the throughput performance of 3DGS at high-resolution (QHD), we perform a bottleneck analysis of GSCore by varying two primary system knobs: the number of compute unit cores and available DRAM bandwidth. Figure 4 shows FPS performance against varying core counts (4, 8, and 16 cores) under three distinct DRAM bandwidth conditions (51.2 GB/s, 102.4 GB/s, and 204.8 GB/s).

**Implication from cores.** First, we focus on the scenario representative of typical edge devices, characterized by limited DRAM bandwidth around 51.2 GB/s, as provided by conventional GSCore setups. Under this bandwidth constraint, increasing the core count from 4 to 16 provides minimal performance improvements; specifically, even a fourfold increase in cores yields only about a 1.12× improvement in FPS, falling significantly short of the targeted 60 FPS SLO. This result indicates that computational scaling alone is insufficient when bandwidth constraints are tight.

**Implication from bandwidth.** Next, we examine the impact of DRAM bandwidth on the FPS performance of the 3DGS system. At the highest bandwidth (204.8 GB/s), which is a 4× increase over a typical on-device system (51.2 GB/s), the 3DGS system surpasses the 60 FPS SLO, achieving a 3.83× improvement in FPS. These results indicate that high-resolution 3DGS performance is constrained by DRAM bandwidth rather than computational power, identifying memory bandwidth as the primary bottleneck.

**Bandwidth breakdown.** To further investigate the sources of bandwidth usage, we perform an analysis of bandwidth consumption in high-resolution 3DGS. Figure 5 presents the DRAM traffic (GB) required to render 60 frames and its breakdown for the GPU-based 3DGS and GSCore across different resolutions. In both systems, the results show that the sorting stage dominates bandwidth consumption, accounting for up to 90.8% on the GPU and 69.3% on GSCore. GSCore achieves a noticeable reduction in memory requirements for 3DGS rendering. However, it still requires an average bandwidth of 60.7 GB/s and 80.0 GB/s in FHD and QHD resolutions, respectively. This high bandwidth demand limits the availability of high-resolution 3DGS rendering in on-device AR/VR systems, whose practical DRAM bandwidths range from 17.8 GB/s to 59.7 GB/s [22, 30, 48, 50, 53–55, 70]. These findings highlight the need to optimize the sorting stage, which is the major bandwidth bottleneck in the 3DGS pipeline, to realize high-resolution and low-latency on-device 3DGS systems.

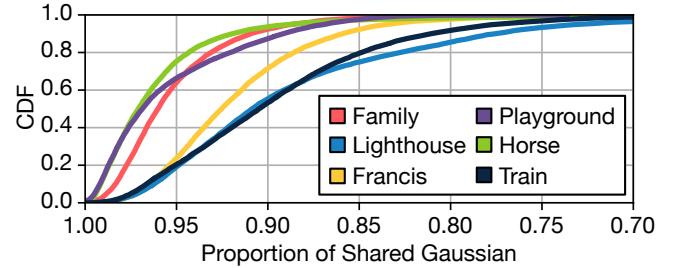
### 3.3 Opportunity to Reduce Computation in Sorting

To alleviate the bandwidth bottleneck caused by Gaussian sorting, we investigate the potential of temporally reusing Gaussians previously sorted in prior frames.

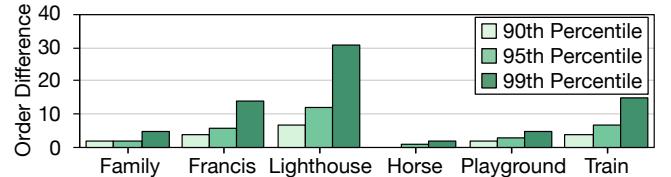
**Per-frame sorting in 3DGS.** In Gaussian sorting, each tile identifies the Gaussians that intersect it, determines their depth order for the subsequent rasterization stage, and stores this order in a Gaussian table. As the camera viewpoint changes, this table becomes outdated, so the system reprocesses the sorting stage from scratch for every frame. However, per-frame sorting overlooks the temporal similarity between consecutive frames, which arises from the gradual motion of Gaussians during camera movement and results in unnecessary memory bandwidth consumption.

**Temporal similarity analysis.** To quantify this temporal similarity, we first analyze the Gaussian retention between the Gaussian tables of consecutive frames. Figure 6 shows the cumulative distribution function (CDF) of the proportion of shared Gaussians across six real-world scenes. In all scenes, over 90% of tiles retain more than 78% of their Gaussians from the previous frame, highlighting the potential for reusing Gaussians from the previous frame’s table.

In a second experiment, we measure how the ordering of Gaussians within each tile changes between consecutive frames. Figure 7 illustrates the sorting order differences at the 90th, 95th, and 99th percentiles. Results show that 99% of the sorting order remains largely consistent across consecutive frames. Notably, at the 99th percentile, the Gaussian with the greatest shift moves only 31 positions from its original location, a negligible deviation given that each tile contains thousands of Gaussians. Extending from the Gaussian retention observed in Figure 6, this result further substantiates the opportunity to leverage temporal similarity between frames to mitigate redundant updates in the Gaussian table.



**Figure 6.** Temporal similarity of assigned Gaussian per tile.



**Figure 7.** Temporal similarity of sort order per tile.

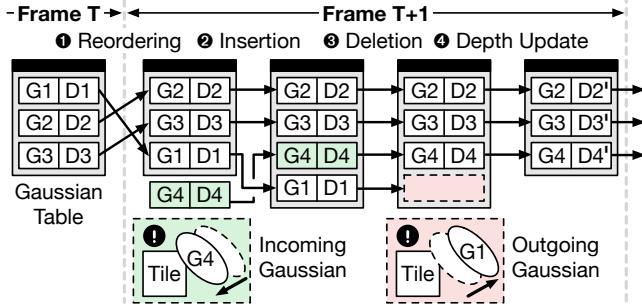
These findings indicate the need for a bandwidth-optimized sorting technique for on-device 3DGS systems. To address this, we propose Neo, a hardware-algorithm co-designed solution that enables efficient 3DGS rendering through memory-efficient sorting acceleration, leveraging temporal similarity in moving camera scenarios within AR/VR applications.

## 4 Neo’s Reuse-and-Update Sorting

This section introduces the software component of our Neo solution, designed to efficiently leverage temporal similarity between consecutive frames to facilitate high-resolution 3DGS rendering on edge devices. By intelligently reusing sorting information across frames, we significantly reduce bandwidth requirements and computational overhead.

### 4.1 Design Space Exploration and Considerations

**Design space exploration of sorting reuse methods.** When leveraging temporal similarity under moving camera, two conventional strategies are periodic sorting and background sorting. Periodic sorting intermittently recomputes the full sorting order while skipping sorting in intermediate frames, which reduces average latency but introduces occasional spikes. Moreover, errors accumulate between refresh intervals, leading to gradual degradation in rendering quality. In contrast, background sorting [45] continuously updates sorting results in parallel with rendering, and each frame uses the most recently prepared results. This approach mitigates latency spikes but introduces sustained memory traffic, which incurs memory contention and increases average latency. Moreover, discrepancies between the viewpoints of sorting and rendering frames degrade visual quality. To address these limitations, we propose an incremental update strategy that reuses the previous frame’s sorting results while applying fine-grained corrections. Even under abrupt



**Figure 8.** Overview of reuse-and-update sorting.

camera motion, this method recovers the correct ordering within a few frames, eliminating the need for full sorting.

**Considerations for incremental update.** In designing the incremental update strategy, we identify three primary sources of variability that the system must handle: (1) Change in camera viewpoint can alter Gaussian depths, invalidating the previous ordering. (2) New Gaussians can become visible in a specific tile. (3) Gaussians no longer relevant may disappear from the tile. Handling these factors is critical for robust incremental sorting, ensuring consistent accuracy under dynamic viewpoints and scene content.

## 4.2 Flow of Reuse-and-Update Sorting

Figure 8 shows the flow of the reuse-and-update sorting algorithm, consisting of four main operations.

**① Reordering.** We reuse the Gaussian table from the previous frame. However, when the viewpoint changes, the depth order of Gaussians changes, requiring reordering. To handle this efficiently, we employ *Dynamic Partial Sorting*, which performs partial sorting within on-chip memory and minimizes off-chip accesses. Section 4.3 provides further details.

**② Insertion.** We collect newly visible Gaussians entering a tile (i.e., incoming Gaussians) separately and insert them into the Gaussian table. Since the number of incoming Gaussians is typically small compared to the Gaussian table, this insertion incurs minimal computational overhead.

**③ Deletion.** We identify Gaussians that move out of a tile (i.e., outgoing Gaussians) due to camera motion and remove them from the Gaussian table at each iteration.

After completing the three steps above, we use the updated Gaussian table for rasterization. During rasterization, the system fetches necessary Gaussian features (e.g., position, depth, and color) to compute pixel values of the scene.

**④ Depth Update.** During rasterization, we update the depth values in the sorted Gaussian table. We exploit the availability of these values in this stage to enable on-the-fly depth refresh for subsequent frames. This design eliminates costly irregular accesses that would otherwise be required to fetch depth values. Section 4.4 provides further details.

After completing reordering, insertion, deletion, and depth update, the system passes the Gaussian table with updated depth values to the next frame's 3DGS rendering pipeline.

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## Algorithm 1: Dynamic Partial Sorting

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```

Input:  $I$ : Current Frame Iteration Number
 $G_{I-1}$ : Previous Sorted Gaussian Table of Tile
 $L$ : Size of Gaussian Table of Tile
 $C$ : Size of Chunk for Chunk Sorting
Output:  $G_I$ : Current Sorted Gaussian Table of Tile
// Interleaving Sorting Boundaries
1 if  $I \bmod 2 \equiv 1$  then
2    $\text{range} \leftarrow (\text{start} : 0, \text{end} : C)$  ;
3 else
4    $\text{range} \leftarrow (\text{start} : 0, \text{end} : \lfloor \frac{C}{2} \rfloor)$  ;
5 while true do
  // Chunk-based Partial Sorting
  6    $S \leftarrow \text{Slice}(G_{I-1}, \text{range})$  ;
  7    $S' \leftarrow \text{Sort}(S)$  ;
  8    $\text{Slice}(G_I, \text{range}) \leftarrow S'$  ;
  // Update Sorting Parameters
  9   if  $\text{range.start} + C \geq L$  then
    10     $\text{break}$  ;
  11    $\text{range.start} \leftarrow \text{range.start} + C$  ;
  12    $\text{range.end} \leftarrow \min(\text{range.end} + C, L)$  ;

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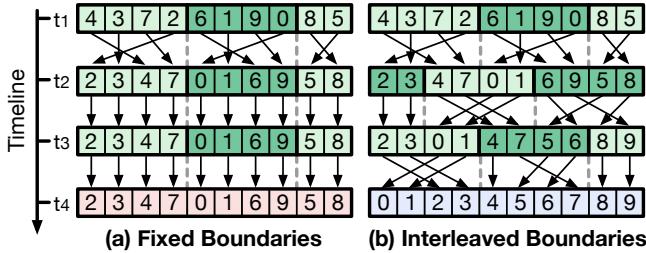
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## 4.3 Reordering the Reused Gaussian Table

In order to exploit the Gaussian tables carried over from previous frames, we devise a sorting algorithm that leverages temporal locality to make on-the-fly corrections. We refer to this algorithm as *Dynamic Partial Sorting*. Algorithm 1 outlines our *Dynamic Partial Sorting* approach, comprising two main strategies: chunk-based partial sorting and interleaving the sorting boundaries. By leveraging the sorted table from the previous frame, our method avoids a full global sort each time, reducing off-chip bandwidth usage while preserving accurate ordering over consecutive frames.

**Chunk-based partial sorting (lines 5–12)** We observe that the Gaussian sorting order within each tile remains largely consistent across adjacent frames. Based on this observation, our design partitions the Gaussian table into small chunks that fit within on-chip memory, and sorts each chunk independently. In our implementation, each chunk stores up to 256 Gaussians in on-chip memory. During each iteration, we read one chunk (line 6) from DRAM into on-chip memory, sort it in place (line 7), and write back the results (line 8). This local sorting approach significantly reduces bandwidth usage by retrieving and writing back each chunk only once, unlike conventional global sorting methods that make multiple passes over the entire table, repeatedly scanning and rewriting it. The algorithm continues chunk by chunk until the full table has been processed (lines 9–10).

**Interleaving sorting boundaries (lines 1–4).** Relying on a static partition can lead to inaccuracy if Gaussians need to cross chunk boundaries. Figure 9(a) illustrates the limitation of performing local sorting. Suppose at time  $t_1$ , the



**Figure 9.** Comparison of two different partial sorting.

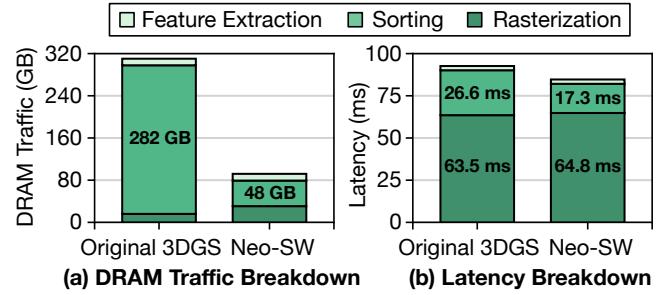
depths of Gaussians change due to camera viewpoint shifts, and requires reordering to depths 0 to 9. Because we only apply partial sorting within fixed chunks, Gaussians cannot cross these boundaries, even after multiple sorting iterations at subsequent times  $t_2$ ,  $t_3$ , and  $t_4$ . In contrast, Figure 9(b) demonstrates our strategy to interleave sorting boundaries. Initially, at time  $t_1$ , we perform the same local sorting as in the fixed-boundary approach. However, starting from the next iteration ( $t_2$ ), we interleave sorting boundaries, shifting chunk boundaries by half the chunk size. This staggered adjustment allows Gaussians to cross previous chunk boundaries, progressively reaching their correct positions. By repeating this process over subsequent iterations, Gaussians can freely move toward their correct sorting positions. As illustrated, by time  $t_4$ , all Gaussians have successfully reached their intended positions, highlighting the effectiveness of our interleaving sorting boundary method.

**Single off-chip sorting pass.** In our design, we retrieve each chunk from DRAM and write it back only once. While multiple sorting passes are possible, it introduces a trade-off between accuracy and memory traffic, depending on the number of off-chip passes. Increasing the number of passes guarantees more accurate Gaussian ordering, which improves rendering quality, but incurs memory traffic proportional to the number of passes. In practice, we observe that a single sorting pass introduces only negligible accuracy degradation (e.g., less than 0.1 dB). Because additional passes provide marginal benefit, we adopt a single off-chip sorting pass to minimize memory traffic.

**Accuracy restoration.** *Dynamic Partial Sorting* may require a few iterations to reestablish accurate ordering, potentially degrading accuracy. However, applying this technique reduces off-chip accesses and enhances sorting performance, leading to faster rendering. This creates a positive feedback loop: faster rendering enables more frequent sorting and updates, which, in turn, maintains accurate ordering during continuous camera movement. As a result, this technique leads to negligible accuracy degradation.

#### 4.4 Bandwidth-Efficient Depth Update

**Challenges in per-frame depth refresh.** To maintain an up-to-date sorted Gaussian table, we must update the depth values within the table. A naive approach would fetch each



**Figure 10.** Performance comparison between the original 3DGS and Neo-SW on Orin AGX, with DRAM traffic measured over 60 rendered frames.

Gaussian’s updated depth from the large off-chip feature table after rendering. However, this approach incurs substantial random DRAM accesses because it performs a per-Gaussian depth refresh of the Gaussian table for every tile. Since our design prioritizes minimizing off-chip bandwidth, such random accesses significantly degrade performance.

**Deferred depth update.** We observe that rasterization already fetches each Gaussian’s full feature information from the off-chip table. Hence, rather than incurring a second memory pass for depth updates, we piggyback on this access by directly overwriting the depth values in the sorted Gaussian table during rasterization, eliminating redundant memory operations. However, this design defers the depth update such that, for any given frame, sorting relies on depth values that are one frame stale. In practice, this one-frame delay introduces only negligible ordering error without degrading rendering quality. Furthermore, without this optimization, depth updates incur an additional memory access, doubling the memory traffic per tile. As a result, Neo without this strategy exhibits 33.2% higher memory traffic compared to the full Neo design. Likewise, this optimization significantly reduces random off-chip memory accesses.

#### 4.5 Performance Implication from Neo Algorithm

To evaluate the performance gains of a software-only version of Neo, we implement a custom CUDA kernel for sorting and modify the rasterization kernel. We enable *Dynamic Partial Sorting* in the ① reordering step by modifying existing sorting libraries from Meta [65] and NVIDIA [75]. We integrate the ② insertion and ③ deletion steps into a merge-sorting process that combines incoming Gaussians with the reused Gaussian table. Finally, we implement ④ deferred depth updates during rasterization. We evaluate this implementation on the NVIDIA Orin AGX platform.

**Limitation of software-only solution.** Figure 10 presents the latency and DRAM traffic of the software-only implementation of Neo, with DRAM traffic measured over 60 rendered frames. While the algorithm significantly reduces memory traffic, with 70.4% overall and 82.8% during the sorting stage as shown in Figure 10(a), its latency improvement remains

modest at only 1.1 $\times$ , as shown in Figure 10(b). This modest speedup results from two primary factors. First, the insertion and deletion operations in the sorting stage induce irregular memory access patterns, degrading spatial locality and limiting SIMD utilization. Consequently, despite the significant reduction in memory traffic, the sorting stage achieves only a 1.54 $\times$  speedup. Second, as prior work [49, 50, 104] highlights, rasterization remains the dominant bottleneck in GPU-based execution, accounting for 68.8% of total runtime. Since Neo specifically targets the sorting stage under the assumption that rasterization has already been accelerated, it delivers inherently limited end-to-end impact on GPU performance. These inefficiencies underscore the fundamental limitations of GPU-based execution. Addressing them requires a hardware-software co-designed architecture, which we introduce in the next section.

## 5 Neo Accelerator Architecture

This section presents the hardware architecture of Neo, which accelerates the 3DGS pipeline with reuse-and-update sorting. We first provide an overview of the data flow across the engines, followed by detailed descriptions of each engine.

### 5.1 Architecture Overview

Figure 11 illustrates the architecture of Neo. Our design consists of three main engines, Preprocessing Engine, Sorting Engine, and Rasterization Engine.

**Preprocessing Engine.** The Preprocessing Engine handles the first two stages of the 3DGS pipeline, namely frustum culling and feature extraction. For each Gaussian, it determines the tiles where the Gaussian has become newly visible and collects the per-Gaussian information required for rendering. These operations produce two types of tables: (1) a feature table, which stores Gaussian attributes required for rasterization, and (2) incoming Gaussian tables, which record the newly visible Gaussians for each tile.

**Sorting Engine.** Next, the Sorting Engine performs two types of sorting. First, it performs *Dynamic Partial Sorting* on the Gaussian tables from the previous frame that contain newly updated depth values. Second, it sorts the incoming Gaussian tables from the current frame provided by the Preprocessing Engine. To accelerate both reordering and sorting, the engine employs specialized parallel sorting units.

**Rasterization Engine.** Finally, the Rasterization Engine performs the last stage of the pipeline, rasterization, using both the sorted Gaussian tables and the feature table. To eliminate redundant computations, our design adopts subtiling [50], which applies  $\alpha$ -blending only to each subtile for the Gaussians intersecting it. The Rasterization Engine integrates dedicated hardware for on-the-fly subtiling-based rasterization and for deferred depth updates, which enable reuse-and-update sorting in subsequent frames.

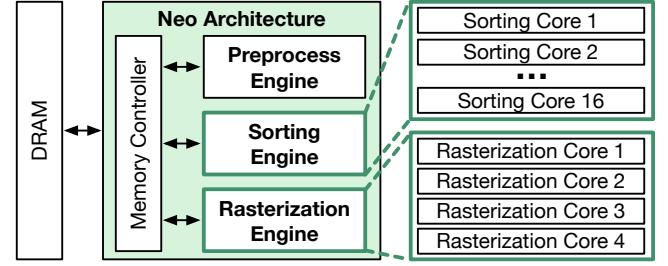


Figure 11. Overall of architecture of Neo.

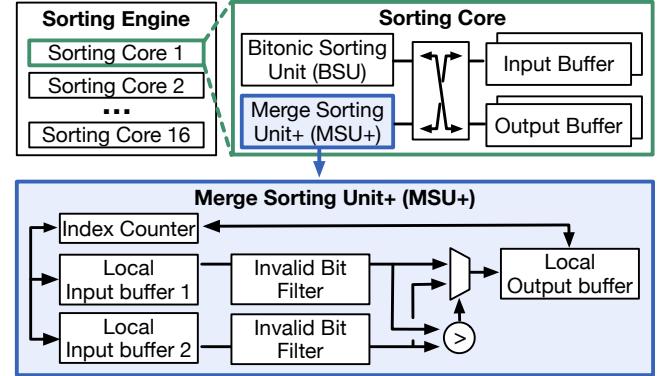


Figure 12. Microarchitecture of Sorting Engine.

### 5.2 Preprocessing Engine

The Preprocessing Engine consists of projection units and color calculation units for frustum culling and feature extraction, and incorporates duplication units to support the reuse-and-update sorting scheme.

**Conventional preprocessing.** The projection unit projects Gaussians onto the image plane and performs frustum culling to discard those outside the camera frustum. Next, the color calculation unit derives view-dependent color for each Gaussian using spherical harmonics. Together, these units generate a feature table that stores essential rasterization attributes, including color, mean, covariance matrix, opacity, and radius.

**Processing incoming Gaussians.** The duplication unit uses 2D Gaussian information to identify the tiles intersected by each Gaussian and generates the corresponding Gaussian tables. Our design adds a verification step that checks whether each Gaussian exists in the previous frame's Gaussian table. This step produces the incoming Gaussian tables by allowing the system to process only newly visible Gaussians, thereby enabling the reuse-and-update sorting scheme. As a result, the unit outputs per-tile Gaussian tables containing the IDs and depth values of newly incoming Gaussians.

### 5.3 Sorting Engine

Figure 12 shows the microarchitecture of our Sorting Engine, which comprises 16 parallel Sorting Cores. Each Sorting Core has a Bitonic Sorting Unit (BSU), a Merge Sorting

Unit+ (MSU+), and I/O buffers. Both input and output buffers employ double buffering to mask memory-access latency.

**Conventional sorting.** To perform conventional sorting of the Gaussian table from scratch, the Sorting Core follows standard merge-sort steps. Each core loads a 256-entry chunk into its input buffer and partitions it into smaller 16-entry sub-chunks that the BSU can process. The BSU sorts each sub-chunk, and the MSU+ merges the partially sorted results. The system then writes each fully sorted chunk back to DRAM, processes the remaining chunks, and finally performs a global merge across all sorted chunks.

**Dynamic Partial Sorting.** Beyond conventional sorting, the Sorting Engine supports *Dynamic Partial Sorting* to reuse the Gaussian table from the previous frame. Specifically, the engine loads a 256-entry chunk from the previous frame’s table and reorders it in the same manner as conventional sorting, using the BSU to sort sub-chunks followed by an MSU+ merge. Because no additional merges are required across chunks, the design avoids extra off-chip memory traffic.

**Inserting and deleting entries.** Alongside conventional sorting and *Dynamic Partial Sorting*, the MSU+ merges the sorted Gaussian table with the incoming Gaussian table and removes outgoing Gaussians from the table. Specifically, the Preprocessing Engine first generates the incoming Gaussian tables, and the Sorting Engine sorts them using a conventional algorithm before merging them with the sorted Gaussian table from the previous frame. At the same time, the MSU+ removes outgoing Gaussians based on their valid bits, which were marked as valid or invalid during the previous frame’s rasterization. This design stems from the observation that, although outgoing Gaussians can be excluded during rasterization using their valid-bit flag, immediately removing them would require costly shifting of subsequent entries. By deferring memory realignment to the merge step, the MSU+ efficiently deletes invalid entries without incurring the cost of shifting the entries. Furthermore, it inserts new entries simultaneously, thereby improving performance.

#### 5.4 Rasterization Engine

Figure 13 illustrates the microarchitecture of our Rasterization Engine, comprising four Rasterization Cores. Each core contains four Subtile Compute Units (SCU), four Intersection Test Units (ITU), and dedicated buffers for bitmaps, 2D Gaussian features, and pixel data.

**Intersection Test Unit (ITU).** Our design adopts subtile-based rasterization, inspired by GSCore [50], which subdivides each tile into multiple smaller subtiles. Since a Gaussian typically intersects only a subset of subtiles within a tile, this approach reduces redundant computations. To track Gaussian–subtile intersections, GSCore maintains lightweight subtile metadata in the form of a bitmap that indicates whether a Gaussian overlaps each subtile. However, 3DGS generates these bitmaps early in the pipeline and propagates them through all stages, even though they are only used during

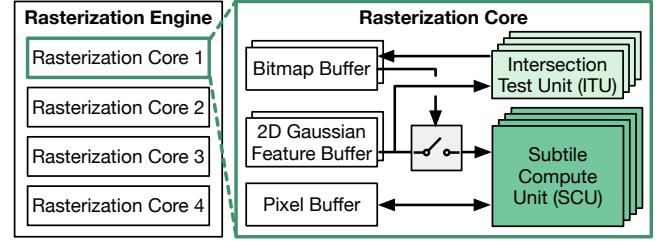


Figure 13. Microarchitecture of Rasterization Engine.

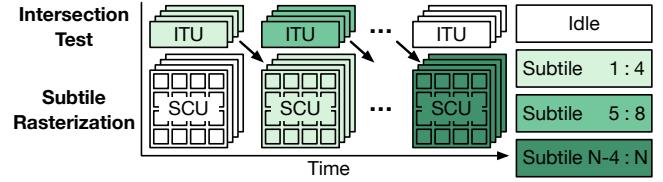


Figure 14. Execution timeline of Rasterization Engine. Intersection Test Unit (ITU) and Subtile Computation Unit (SCU) process subtiles in a pipelined manner.

rasterization, causing unnecessary memory traffic. To address this inefficiency, we integrate Intersection Test Units (ITUs) within the Rasterization Core to generate the required bitmaps on the fly. Specifically, each ITU uses the 2D parameters of a Gaussian to test intersection boundaries and store the resulting bitmap in a local buffer. Moreover, the ITU plays a key role in reuse-and-update sorting by detecting outgoing Gaussians through a cumulative OR operation. This operation accumulates intersection bitmaps across all subtiles to flag Gaussians with at least one intersection. By flipping this bit, the system identifies Gaussians with no intersections and eliminates them in the next sorting stage.

**Subtile Computation Unit (SCU).** Following the intersection tests, each SCU performs  $\alpha$ -blending to compute pixel values for its assigned subtile. The system filters Gaussians using the bitmaps generated by the ITUs and routes them only to SCUs whose subtiles intersect with the Gaussian. After rasterizing the 2D Gaussian feature buffer for a given group of subtiles, the system writes the intermediate pixel values to the pixel buffer and proceeds to the next group. To maximize efficiency, we pipeline intersection testing with rasterization. Figure 14 illustrates this pipelining scheme. While rasterization for the first group of four subtiles (1–4) must wait for its intersection tests to complete, subsequent subtiles benefit from overlapping execution as the ITUs process the next group of subtiles concurrently with the ongoing rasterization of the current one. This overlap effectively hides the latency of on-the-fly bitmap generation.

**Updating table for next frame.** After rasterizing all subtiles, the system extracts depth values from the 2D Gaussian feature buffer and retrieves valid bits from the bitmap buffer. It then updates the corresponding entries in the Gaussian table and forwards the updated table to the next frame.

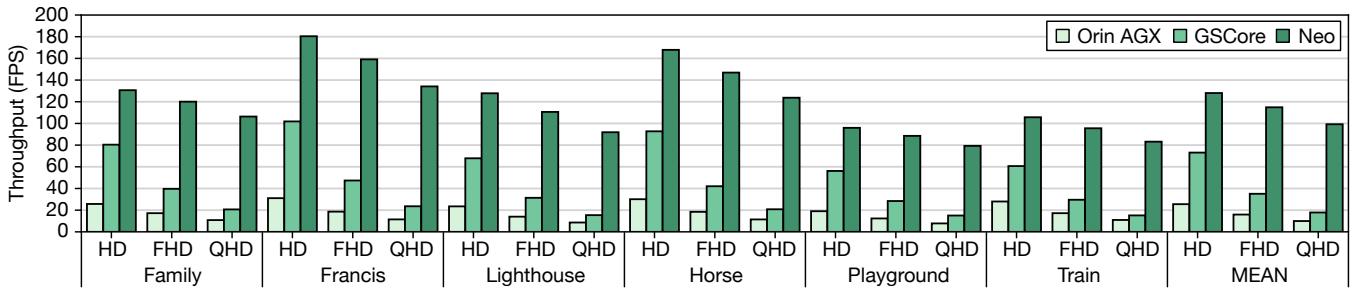


Figure 15. End-to-end system throughput of GSCore and Neo on six 3D scenes.

Table 1. Configuration of Neo system.

Hardware Component		Configuration
Neo	Tile Size	64×64 px
Preprocessing Engine	Projection Unit	4 units
	Color Unit	4 units
	Duplication Unit	4 units
Sorting Engine	Bitonic Sort Unit	16 units
	Merge Sort Unit+	16 units
	I/O Buffer Size	64 KB
Rasterization Engine	Subtile Compute Unit	16 units
	Intersection Test Unit	16 units
	Buffer Size	200 KB
	Subtile Size	8×8 px

## 6 Evaluation

### 6.1 Methodology

**Benchmarks.** We select six scenes from the Tanks and Temples dataset [42], namely Family, Francis, Horse, Lighthouse, Playground, and Train, as representative benchmarks for evaluating 3DGS rendering quality. We capture each frame at 30 FPS in UHD resolution (3840×2160). Following the standard training procedure, we use 400 images per scene and train for 200K iterations to ensure model convergence. For inference, we configure each scene to one of three target resolutions: HD (1280×720), FHD (1920×1080), or QHD (2560×1440), and evaluate how many unique frames the system renders per second, with each frame using a distinct camera pose from the original sequence of the dataset.

**Hardware development and synthesis.** Table 1 shows the configurations of our hardware. We prototype Neo architecture at RTL level using Verilog, and measure power, area, and timing parameters using Synopsys Design Compiler with ASAP7 [98] 7 nm library. We measure the power and area of on-chip buffers using CACTI [72] under 22 nm technology and scale them to 7 nm using DeepScaleTool [87].

**Baseline.** We evaluate Neo against two baseline systems: NVIDIA Orin AGX 64GB (Orin AGX), GSCore. Orin AGX [37] is a high-performance on-device platform designed for autonomous systems. It supports up to 60W of power and provides 204.8 GB/s of memory bandwidth. This baseline enables evaluation of rendering performance on real on-device

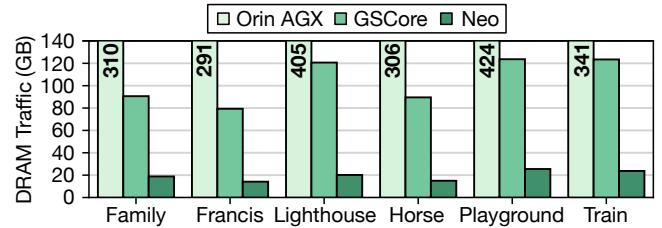


Figure 16. Comparison of DRAM traffic (GB) between Neo and GSCore for rendering 60 frames.

hardware. GSCore [50] originally features four sorting and rasterization cores. To support high-resolution workloads and enable a fair comparison with Neo, which includes 16 hardware units, we scale GSCore to 16 cores.

**Cycle accurate simulator.** We measure the latency of GSCore, and Neo using a cycle-accurate simulator based on the timing parameters obtained from RTL synthesis, with off-chip memory modeled as LPDDR4 based on Ramulator [41].

### 6.2 Performance Results

**End-to-end throughput.** Figure 15 presents the end-to-end rendering throughput for six scenes rendered at three target resolutions (HD, FHD, and QHD) on Orin AGX, GSCore, and Neo. Across all scenes and resolutions, Neo consistently outperforms both Orin AGX and GSCore, achieving average 5.0×, 7.2×, and 10.0× speedup over Orin AGX and 1.8×, 3.3×, and 5.6× over GSCore for HD, FHD, and QHD, respectively. The performance gains are particularly significant at higher resolutions, where sorting bottlenecks intensify, demonstrating Neo’s effectiveness in addressing bandwidth bottlenecks through temporal similarity. Unlike Orin AGX and GSCore, which sort from scratch in every frame, Neo reduces bandwidth usage with a reuse-and-update sorting approach. It applies *Dynamic Partial Sorting* to tables from the previous frame while performing conventional sorting only on small incoming Gaussian tables. Notably, Neo achieves an average throughput of 99.3 FPS at QHD resolution, meeting the real-time rendering requirement.

**End-to-end memory traffic.** Figure 16 shows the required DRAM traffic to render 60 frames in QHD resolution on Orin AGX, GSCore, and Neo. For Orin AGX, rendering 60

**Table 2.** Quality comparison of original 3DGS and Neo.

Scene	Original 3DGS		Neo	
	PSNR↑	LPIPS↓	PSNR↑	LPIPS↓
Family	28.2	0.096	28.1 (▼0.1)	0.097 (▲0.001)
Francis	28.9	0.203	28.9 (●)	0.203 (●)
Horse	28.0	0.110	27.9 (▼0.1)	0.110 (●)
Lighthouse	26.0	0.096	26.0 (●)	0.096 (●)
Playground	25.1	0.208	25.0 (▼0.1)	0.208 (●)
Train	25.0	0.113	24.9 (▼0.1)	0.113 (●)

**Table 3.** Evaluated GSCore and Neo accelerators.

Device	Technology	Frequency	Area (mm <sup>2</sup> )	Power (mW)
GSCore	7 nm	1 GHz	0.417	719.9
Neo			0.387	797.8

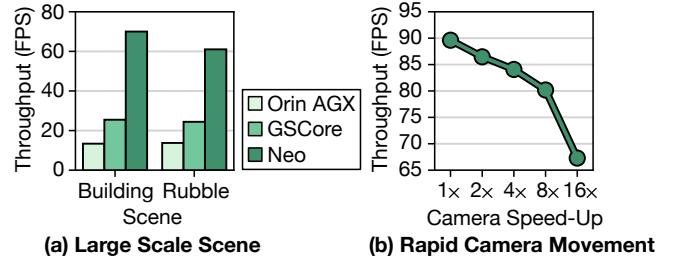
**Table 4.** Area and power breakdown of hardware components in Neo accelerator.

Component	Area (mm <sup>2</sup> )	Power (mW)
<b>Preprocessing Engine</b>	<b>0.026</b>	<b>194.9</b>
Merge Sort Unit+	0.005	12.4
Bitonic Sort Unit	0.008	75.0
Buffers + others	0.040	71.6
<b>Sorting Engine</b>	<b>0.053</b>	<b>159.0</b>
Subtile Compute Unit	0.228	375.0
Intersection Test Unit	0.030	58.7
Buffers + others	0.050	10.2
<b>Rasterization Engine</b>	<b>0.308</b>	<b>443.9</b>
<b>Total</b>	<b>0.387</b>	<b>797.8</b>

frames requires an average of 346.5 GB across six scenes, compared to 104.6 GB for GSCore and 19.6 GB for Neo, representing a 94.4% and 81.3% reduction over OrinAGX and GSCore, respectively. This reduction is largely due to significant traffic savings achieved through reuse-and-update sorting. As a result, even in scenarios with limited bandwidth (e.g., 51.2 GB/s), the system can perform computations without being bottlenecked by the bandwidth constraints.

**Rendering quality.** Table 2 compares the rendering quality of GSCore and Neo. We evaluate rendering quality using standard graphics metrics: PSNR, where higher values indicate better image fidelity, and LPIPS, where lower values indicate better perceptual quality. Across all scenes, the maximum observed difference is less than 0.1 dB in PSNR and 0.001 in LPIPS, an imperceptible level of quality degradation [19, 20]. These results highlight the effectiveness of Neo’s reuse-and-update sorting mechanism in maintaining high rendering quality while significantly reducing sorting overhead by exploiting temporal similarity.

**Area and power.** Table 3 compares the evaluated area and power of Neo and GSCore. For a fair comparison, we scale GSCore’s area and frequency estimates down to 7 nm using DeepScaleTool [87], as it was originally synthesized in a

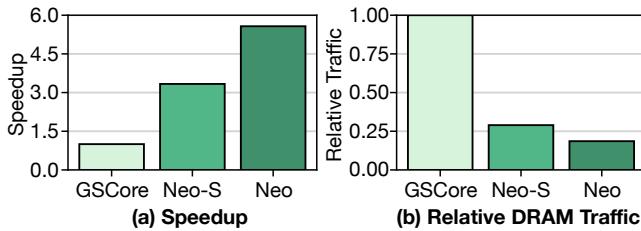
**Figure 17.** Throughput of 3DGS rendering systems in extreme AR/VR scenarios: (a) Large-Scale Scene, and (b) Rapid Camera Movement.

28 nm process. The results show that Neo achieves a slightly smaller total area than GSCore with a marginal increase in power consumption. To further understand the area and power overhead, Table 4 provides a detailed breakdown of our Neo accelerator, showing that its additional hardware components (Merge Sort Unit+ and Intersection Test Unit) together account for 9.04% and 8.91% of the total area and power consumption, respectively. With minimal overhead, our additional hardware block delivers high throughput under high-resolution settings.

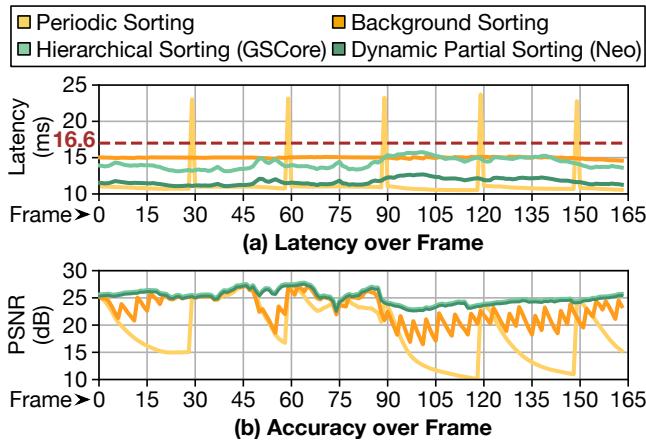
**Performance results of extreme AR/VR scenarios.** Figure 17 shows the throughput of Neo under the more stringent constraints of AR/VR scenarios, including large scale scene rendering and rapid camera movement. Figure 17(a) shows the results of Building and Rubble scenes from Mill 19 [96] which features high-resolution aerial imagery commonly used to represent complex, large-scale scene. Neo delivers an average throughput of 65.2 FPS whereas both Orin AGX and GSCore struggle to meet the high frame rate requirements, dropping below 13.6 FPS and 24.9 FPS, respectively. Figure 17(b) presents Neo’s performance under different levels of rapid camera movement (2x, 4x, 8x and 16x). In these scenarios, although Gaussian reusability decreases under rapid camera motion, Neo maintains a frame rate above 60 FPS, satisfying the conservative SLO requirement for rendering. These results demonstrate the effectiveness of Neo’s reuse-and-update sorting mechanism, exhibiting superior rendering performance across extreme AR/VR scenarios.

### 6.3 Ablation Studies

**Performance breakdown of Neo hardware.** The hardware of Neo consists of two main components: the Sorting Engine and the Rasterization Engine. The Sorting Engine implements the first three steps of Neo’s reuse-and-update sorting algorithm: reordering, insertion, and deletion, while the Rasterization Engine performs subtile-based rasterization and depth update. Figure 18 shows the incremental benefits of integrating these components into GSCore. Although GSCore alone does not support Neo’s algorithm, adding the Sorting Engine (Neo-S) enables reuse-and-update



**Figure 18.** Speedup and DRAM traffic normalized to GSCore. Neo-S replaces GSCore Sorting Engine with Neo’s Sorting Engine.



**Figure 19.** Latency and rendering quality across frames for four sorting reuse methods.

sorting, reducing memory traffic by 71.1% and improving performance by 3.3×. However, without hardware support for depth update, the system requires separate post-processing to update Gaussian table metadata (e.g., depth, valid bit), which incurs additional delay. Integrating the Rasterization Engine removes this overhead, achieving a further 35.8% traffic reduction and an additional 1.7× speedup. While the Sorting Engine provides substantial benefits, full algorithm support requires a co-designed sorting and rasterization engine. Accordingly, Neo adopts a holistic hardware design that integrates both components to maximize performance.

**Comparison with existing sorting methods.** In Section 4.1, we explore the design space of sorting reuse methods, including periodic sorting, background sorting, and incremental update sorting. Based on this analysis, we adopt incremental update sorting in our design. To evaluate its effectiveness in terms of latency and rendering quality, we compare it against two alternative strategies on the Neo hardware: (1) periodic sorting and (2) background sorting. We also consider (3) hierarchical sorting, originally proposed in GSCore, which accelerates sorting by combining coarse-grained and fine-grained sorting. We evaluate hierarchical sorting in conjunction with incremental update sorting to quantify the benefits of the *Dynamic Partial Sorting*.

Figure 19 compares the three sorting methods. (1) Periodic sorting achieves lower average latency than Neo by avoiding continuous updates. However, it introduces periodic latency spikes that violate the 16.6 ms SLO for 60 FPS and suffers from severe quality degradation due to error accumulation between updates. (2) Background sorting maintains relatively stable latency by continuously sorting in the background. Despite this, it incurs higher average latency than Neo and degrades rendering quality due to temporal viewpoint discrepancies between sorting and rendering. (3) Hierarchical sorting accurately sorts reused Gaussians and delivers rendering quality comparable to Neo. However, it requires multiple passes over off-chip memory, which increases latency. These results demonstrate the effectiveness of Neo’s sorting scheme and support our design choice.

## 7 Related Work

**View synthesis acceleration.** Neural rendering has driven significant advances, prompting the architecture community to explore hardware acceleration [20, 22, 47, 48, 53, 55, 56, 61, 70, 80, 89, 90]. With the emergence of 3D Gaussian Splatting (3DGS), research focus has shifted accordingly. GSCore [50] introduces hierarchical sorting and an optimized rasterization pipeline. GBU [104] improves efficiency by reusing rasterization results. VR-Pipe [49] repurposes the GPU rasterization engine with microarchitectural optimizations. MetaSapiens [59] applies load balancing techniques to tile-based rasterization. For training, ARC [13] and GSArch [29] mitigate atomic overheads using warp-level reductions and gradient filtering. GauSPU [103] targets SLAM-integrated 3DGS with a sparsity-adaptive rasterizer and a relaxed-memory backpropagation engine. Our work builds on prior 3DGS accelerators that address rasterization bottlenecks and shifts the focus to a more practical constraint in high resolution rendering, revealing sorting as the next critical performance limiter. Neo targets this bottleneck with a lightweight, reuse-aware sorting engine that complements prior efforts.

**Memory-efficient 3DGS.** Another branch of research reduces the memory footprint of 3DGS through pruning and quantization. Pruning eliminates low-impact Gaussians based on importance metrics such as opacity [16, 73] or  $\alpha$ -blending weights [17, 59]. Quantization techniques, including vector quantization [16] and learned compression [17, 25, 73, 78], reduce both memory and storage overhead. However, these approaches require retraining or fine-tuning. In contrast, Neo introduces an orthogonal sorting scheme that requires no retraining. Moreover, it complements existing methods, enabling further gains in bandwidth efficiency.

**Leveraging temporal similarity.** Numerous studies on real-time streaming systems [10, 14, 21, 35, 36, 40, 58, 64, 79, 91, 92, 94, 105, 107, 108] have been proposed to reduce computation while maintaining accuracy. Across diverse domains, one of the most effective strategies is to exploit temporal

redundancy. In graphics, prior work [11, 20, 26, 57, 63, 88] applies this principle through pixel-wise reuse, known as warping. Neural rendering also benefits from temporal redundancy. For example, Potamoi [19] leverages it to bypass MLP overheads in NeRF through pixel reuse. However, 3DGS performs Gaussian-wise feature extraction and tile-wise sorting and rasterization, which limit the applicability of pixel-wise reuse and fail to address the memory traffic induced by sorting. In contrast, Lumina [18] leverages temporal similarity at the sorting stage but performs background sorting, which continuously consumes memory bandwidth, incurs contention, and increases average latency, as discussed in Section 4.1 and Section 6.3. Neo instead exploits temporal similarity at the sorting stage through an incremental update strategy, effectively reducing the associated memory traffic.

## 8 Conclusion

Real-time on-device 3D Gaussian Splatting (3DGS) rendering demands both low latency and high frame generation rate, yet existing solutions struggle to meet these conflicting requirements under stringent resource constraints. This work identifies Gaussian sorting as a key bottleneck in the 3DGS inference pipeline, and presents Neo, an on-device acceleration solution that introduces a reuse-and-update sorting algorithm and a hardware-accelerated sorting pipeline to reduce redundant computations and alleviate memory bandwidth pressure. By tackling this challenge, Neo takes a step toward enabling real-time, on-device generative virtual worlds, bringing us closer to immersive AR/VR experiences.

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