Report-1

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Task: Implement adaptive cache replacement in Gem5

Components:

1. Gem5
2. Python3
3. Crosstool
4. arm_gcc
5. Benchmarks

Process:

1. For implement I used two cache replacement policy. One is Optimal cache replacement and another is FIFO.

2. Used slave port of memory.

3. Used Gem5 mode : Syscall emulation mode

4. I write the implementation code in c language.
Here the code:

```
#include<stdio.h>
#include<stdlib.h>
#include<string.h>
int nframes=3;
int optimal(int x[],int y)
{
int frames[10], pages[30], temp[10], f1, f2, f3, i, j, k, pos, max,
faults = 0;
printf("Cache replacement policy is optimal");
for(i = 0; i < y; ++i){
pages[i]=x[i];
}
for(i = 0; i < nframes; ++i)
{
  frames[i] = -1;
}
for(i = 0; i < y; ++i){
f1 = f2 = 0;
for(j = 0; j < nframes; ++j){
if(frames[j] == pages[i]){
f1 = f2 = 1;
break;
```

```
}   }
if(f1 == 0){
for(j = 0; j < nframes; ++j){
if(frames[j] == -1){
faults++;
frames[j] = pages[i];
f2 = 1;
break;
}   }  }
if(f2 == 0){
f3 =0;
for(j = 0; j < nframes; ++j){
temp[j] = -1;
for(k = i + 1; k < y; ++k){
if(frames[j] == pages[k]){
temp[j] = k;
break;
} }  }
for(j = 0; j < nframes; ++j){
if(temp[j] == -1){
pos = j;
f3 = 1;
break;
}  }
if(f3 ==0){ max = temp[0];
pos = 0;
for(j = 1; j < nframes; ++j){
if(temp[j] > max){
max = temp[j];
pos = j;
}  }  }
frames[pos] = pages[i];
faults++;
}
printf("\n");
for(j = 0; j < nframes; ++j){
printf("%d\t", frames[j]);
}  }
printf("\n\nTotal Page Faults = %d\n", faults);
return(y-faults);
}
int fifo(int x[],int y)
{
  int frame[30],page[100];
 int i,j,k,flag=0,pfault=0,pos=0;
 printf("Cache replacement policy is fifo");
 for(i=0;i<nframes;i++)
 frame[i]=-1;
   for(i=0;i<y;i++){
        page[i]=x[i];
   }
    for(i=0;i<y;i++){
         flag=0;
        for(j=0;j<nframes;j++){

             if(frame[j]==page[i]){
               printf("\n  Hit:    ");
               flag=1;
               break;
             }
        }
        if(flag==0){
          frame[pos]=page[i];
```

```
          pos++;
          printf("\n  Fault:  ");
          pfault++;
          if(pos>=nframes)
          pos=0;

        }
        for(k=0;k<nframes;k++)
        printf("%d\t",frame[k]);
    }
    printf("\nNumber of page fault is: %d \n",pfault);
    return(y-pfault);
}
int main()
{
  int c,k=0,m=0,i,a[150],b[20],l,hits,total_accesses;
  float hit_ratio=0.0,prev_hit_ratio;
  char cache_repl_policy[10]="optimal";
  srand(time(0));
  for(c=0;c<100;c++)
  {
     a[c]=rand()%10;
  }
  while(c>0)
  {
     l=0;
    for(i=k;i<k+10;i++)
    {
       b[l++]=a[i];
    }
    total_accesses=l;
    if(strcmp(cache_repl_policy,"optimal")==0)
    {
       hits=optimal(b,10);
    }
    else if(strcmp(cache_repl_policy,"fifo")==0)
    {
       hits=fifo(b,10);
    }
    prev_hit_ratio=hit_ratio;
    hit_ratio=(float)hits/total_accesses;
    printf("previous hit ratio is %.1f and current hit ratio is %.1f\n",prev_hit_ratio,hit_ratio);
    if(c==100)
     {
        m++;
        k=m*10;
        c=c-10;
        continue;
     }
     if(total_accesses%10 == 0)
     {
        if(hit_ratio<prev_hit_ratio&&(strcmp(cache_repl_policy,"optimal")==0))
           strcpy(cache_repl_policy,"fifo");
        else if(hit_ratio<prev_hit_ratio&&(strcmp(cache_repl_policy,"fifo")==0))
           strcpy(cache_repl_policy,"optimal");
      }
     m++;
     k=m*10;
     c=c-10;
  }
  return 0;
}
```

3. Here I used random input.

4. Now I run this code in gem5 but for run the code first we need to install crosstool for run c code.

Wget http://www.m5sim.org/dist/current/alpha_crosstool.tar.bz2
tar xjf alpha -crosstool.tar.bz2

5. Then I make the .c file to binary file.

gcc adc.c -o acd

6. Now the file is ready for run use Gem5

7. In this implement process I use CPU model X86 and the configuration file se.py

build/X86/gem5.opt configs/example/se.py -c acd

Output:

```
shantonu@shantonu:~/gem5$ build/X86/gem5.opt configs/example/se.py -c acd
gem5 Simulator System.  http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 21.0.0.0
gem5 compiled Jun 14 2021 16:00:49
gem5 started Jun 18 2021 13:38:32
gem5 executing on shantonu, pid 3042
command line: build/X86/gem5.opt configs/example/se.py -c acd

warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.master is deprecated. `master` is now called `mem_side_ports`
warn: membus.master is deprecated. `master` is now called `mem_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
**** REAL SIMULATION ****
info: Entering event queue @ 0.  Starting simulation...
warn: ignoring syscall access(...)
warn: ignoring syscall access(...)
warn: ignoring syscall access(...)
warn: ignoring syscall mprotect(...)
warn: ignoring syscall mprotect(...)
warn: ignoring syscall mprotect(...)
warn: ignoring syscall mprotect(...)
info: Increasing stack size by one page.
Cache replacement policy is optimal
3       -1      -1
3       -1      -1
3       7       -1
3       7       -1
3       7       0
8       7       0
```

2 7 0
2 7 0
9 7 0
1 7 0

Total Page Faults = 7
previous hit ratio is 0.0 and current hit ratio is 0.3
Cache replacement policy is optimal
6 -1 -1
6 8 -1
6 8 9
0 8 9
0 8 9
0 8 9
0 5 9
0 3 9
0 3 9
0 3 9

Total Page Faults = 6
previous hit ratio is 0.3 and current hit ratio is 0.4
Cache replacement policy is optimal
8 -1 -1
8 7 -1
8 7 5
8 2 5
8 6 5
8 6 5
8 6 5
8 6 5
3 6 5
7 6 5

Total Page Faults = 7
previous hit ratio is 0.4 and current hit ratio is 0.3
Cache replacement policy is fifo
Fault: 5 -1 -1
Fault: 5 8 -1
Fault: 5 8 2
Fault: 4 8 2
Fault: 4 6 2
Fault: 4 6 3
Fault: 2 6 3
Fault: 2 0 3
Fault: 2 0 5
Hit: 2 0 5
Number of page fault is: 9
previous hit ratio is 0.3 and current hit ratio is 0.1
Cache replacement policy is optimal
1 -1 -1
1 3 -1
1 3 2
1 3 2
4 3 2
4 3 2
4 3 2
4 9 2
4 9 2
4 9 2

Total Page Faults = 5
previous hit ratio is 0.1 and current hit ratio is 0.5
Cache replacement policy is optimal

4 -1 -1
4 8 -1
4 8 1
9 8 1
2 8 1
7 8 1
7 5 1
7 5 1
7 5 1
0 5 1

Total Page Faults = 8
previous hit ratio is 0.5 and current hit ratio is 0.2
Cache replacement policy is fifo
Fault: 0 -1 -1
Fault: 0 2 -1
Fault: 0 2 1
Hit: 0 2 1
Fault: 6 2 1
Fault: 6 7 1
Hit: 6 7 1
Hit: 6 7 1
Hit: 6 7 1
Fault: 6 7 4
Number of page fault is: 6
previous hit ratio is 0.2 and current hit ratio is 0.4
Cache replacement policy is fifo
Fault: 5 -1 -1
Fault: 5 0 -1
Fault: 5 0 8
Fault: 7 0 8
Fault: 7 2 8
Fault: 7 2 4
Hit: 7 2 4
Fault: 8 2 4
Fault: 8 3 4
Hit: 8 3 4
Number of page fault is: 8
previous hit ratio is 0.4 and current hit ratio is 0.2
Cache replacement policy is optimal
2 -1 -1
2 9 -1
2 9 1
2 9 5
2 9 5
2 6 5
2 6 5
2 6 5
2 7 5
2 7 5

Total Page Faults = 6
previous hit ratio is 0.2 and current hit ratio is 0.4
Cache replacement policy is optimal
6 -1 -1
6 7 -1
6 7 -1
6 7 9
6 1 9
6 1 3
6 1 3
6 1 3
6 1 3

5 1 3

Total Page Faults = 6
previous hit ratio is 0.4 and current hit ratio is 0.4
Exiting @ tick 531097000 because exiting with last active thread context

It’s working fine.

8. I find the simulation out in m5out/stats.txt file

```
---------- Begin Simulation Statistics ----------
simSeconds                                   0.000531                       # Number of seconds simulated (Second)
simTicks                                    531097000                       # Number of ticks simulated (Tick)
finalTick                                   531097000                       # Number of ticks from beginning of simulation (restored from checkpoints and never reset)
(Tick)
simFreq                                  1000000000000                       # The number of ticks per simulated second ((Tick/Second))
hostSeconds                                  0.58                        # Real time elapsed on the host (Second)
hostTickRate                                922925553                       # The number of ticks simulated per host second (ticks/s) ((Tick/Second))
hostMemory                                   686440                       # Number of bytes of host memory used (Byte)
simInsts                                     463082                       # Number of instructions simulated (Count)
simOps                                       900315                       # Number of ops (including micro ops) simulated (Count)
hostInstRate                                 804592                       # Simulator instruction rate (inst/s) ((Count/Second))
hostOpRate                                   1564251                       # Simulator op (including micro ops) rate (op/s) ((Count/Second))
system.clk_domain.clock                         1000                       # Clock period in ticks (Tick)
system.cpu.numCycles                         1062195                       # Number of cpu cycles simulated (Cycle)
system.cpu.numWorkItemsStarted                     0                       # Number of work items this cpu started (Count)
system.cpu.numWorkItemsCompleted                   0                       # Number of work items this cpu completed (Count)
system.cpu.exec_context.thread_0.numInsts       463082                       # Number of instructions committed (Count)
system.cpu.exec_context.thread_0.numOps       900315                       # Number of ops (including micro ops) committed (Count)
system.cpu.exec_context.thread_0.numIntAluAccesses       878070                       # Number of integer alu accesses (Count)
system.cpu.exec_context.thread_0.numFpAluAccesses        28201                       # Number of float alu accesses (Count)
system.cpu.exec_context.thread_0.numVecAluAccesses            0                       # Number of vector alu accesses (Count)
system.cpu.exec_context.thread_0.numCallsReturns        11720                       # Number of times a function call or return occured (Count)
system.cpu.exec_context.thread_0.numCondCtrlInsts        82340                       # Number of instructions that are conditional controls (Count)
system.cpu.exec_context.thread_0.numIntInsts       878070                       # Number of integer instructions (Count)
system.cpu.exec_context.thread_0.numFpInsts        28201                       # Number of float instructions (Count)
system.cpu.exec_context.thread_0.numVecInsts            0                       # Number of vector instructions (Count)
system.cpu.exec_context.thread_0.numIntRegReads      1716941                       # Number of times the integer registers were read (Count)
system.cpu.exec_context.thread_0.numIntRegWrites       715723                       # Number of times the integer registers were written (Count)
system.cpu.exec_context.thread_0.numFpRegReads        47639                       # Number of times the floating registers were read (Count)
system.cpu.exec_context.thread_0.numFpRegWrites        23561                       # Number of times the floating registers were written (Count)
system.cpu.exec_context.thread_0.numVecRegReads            0                       # Number of times the vector registers were read (Count)
system.cpu.exec_context.thread_0.numVecRegWrites            0                       # Number of times the vector registers were written (Count)
system.cpu.exec_context.thread_0.numVecPredRegReads            0                       # Number of times the predicate registers were read (Count)
system.cpu.exec_context.thread_0.numVecPredRegWrites            0                       # Number of times the predicate registers were written (Count)
system.cpu.exec_context.thread_0.numCCRegReads       550151                       # Number of times the CC registers were read (Count)
system.cpu.exec_context.thread_0.numCCRegWrites       300746                       # Number of times the CC registers were written (Count)
system.cpu.exec_context.thread_0.numMemRefs       180196                       # Number of memory refs (Count)
system.cpu.exec_context.thread_0.numLoadInsts       121036                       # Number of load instructions (Count)
system.cpu.exec_context.thread_0.numStoreInsts        59160                       # Number of store instructions (Count)
system.cpu.exec_context.thread_0.numIdleCycles     0.002000                       # Number of idle cycles (Cycle)
system.cpu.exec_context.thread_0.numBusyCycles 1062194.998000                       # Number of busy cycles (Cycle)
system.cpu.exec_context.thread_0.notIdleFraction     1.000000                       # Percentage of non-idle cycles (Ratio)
system.cpu.exec_context.thread_0.idleFraction     0.000000                       # Percentage of idle cycles (Ratio)
system.cpu.exec_context.thread_0.numBranches       104115                       # Number of branches fetched (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::No_OpClass         3660      0.41%      0.41% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::IntAlu       695341     77.21%     77.62% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::IntMult          641      0.07%     77.69% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::IntDiv         1774      0.20%     77.89% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatAdd          940      0.10%     77.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatCmp            0      0.00%     77.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatCvt           32      0.00%     78.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMult            0      0.00%     78.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMultAcc            0      0.00%     78.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatDiv            0      0.00%     78.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMisc            0      0.00%     78.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatSqrt            0      0.00%     78.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAdd          980      0.11%     78.11% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAddAcc            0      0.00%     78.11% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAlu         4246      0.47%     78.58% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdCmp            0      0.00%     78.58% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdCvt         4636      0.51%     79.09% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdMisc         7502      0.83%     79.92% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdMult            0      0.00%     79.92% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdMultAcc            0      0.00%     79.92% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShift          481      0.05%     79.98% # Class of executed instruction. (Count)
```

```
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShiftAcc 0 0.00% 79.98% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdDiv 0 0.00% 79.98% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSqrt 0 0.00% 79.98% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatAdd 0 0.00% 79.98% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatAlu 0 0.00% 79.98% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatCmp 0 0.00% 79.98% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatCvt 96 0.01% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatDiv 10 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatMisc 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatMult 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatMultAcc 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatSqrt 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdReduceAdd 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdReduceAlu 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdReduceCmp 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatReduceAdd 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatReduceCmp 0 0.00% 79.99% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAes 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAesMix 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha1Hash 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha1Hash2 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha256Hash 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha256Hash2 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShaSigma2 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShaSigma3 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdPredAlu 0 0.00% 79.99% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::MemRead 116720 12.96% 92.95% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::MemWrite 57053 6.34% 99.29% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMemRead 4316 0.48% 99.77% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMemWrite 2107 0.23% 100.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::IprAccess 0 0.00% 100.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::InstPrefetch 0 0.00% 100.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::total 900535 # Class of executed instruction. (Count)
system.cpu.interrupts.clk_domain.clock 8000 # Clock period in ticks (Tick)
system.cpu.mmu.dtb.rdAccesses 121067 # TLB accesses on read requests (Count)
system.cpu.mmu.dtb.wrAccesses 59176 # TLB accesses on write requests (Count)
system.cpu.mmu.dtb.rdMisses 157 # TLB misses on read requests (Count)
system.cpu.mmu.dtb.wrMisses 29 # TLB misses on write requests (Count)
system.cpu.mmu.dtb.walker.power_state.pwrStateResidencyTicks::UNDEFINED 531097000 # Cumulative time (in ticks) in various
power states (Tick)
system.cpu.mmu.itb.rdAccesses 0 # TLB accesses on read requests (Count)
system.cpu.mmu.itb.wrAccesses 624962 # TLB accesses on write requests (Count)
system.cpu.mmu.itb.rdMisses 0 # TLB misses on read requests (Count)
system.cpu.mmu.itb.wrMisses 179 # TLB misses on write requests (Count)
system.cpu.mmu.itb.walker.power_state.pwrStateResidencyTicks::UNDEFINED 531097000 # Cumulative time (in ticks) in various
power states (Tick)
system.cpu.power_state.pwrStateResidencyTicks::ON 531097000 # Cumulative time (in ticks) in various power states (Tick)
system.cpu.thread_0.numInsts 0 # Number of Instructions committed (Count)
system.cpu.thread_0.numOps 0 # Number of Ops committed (Count)
system.cpu.thread_0.numMemRefs 0 # Number of Memory References (Count)
system.cpu.workload.numSyscalls 159 # Number of system calls (Count)
system.cpu_clk_domain.clock 500 # Clock period in ticks (Tick)
system.cpu_voltage_domain.voltage 1 # Voltage in Volts (Volt)
system.mem_ctrls.priorityMinLatency 0.000000000000 # per QoS priority minimum request to response latency (Second)
system.mem_ctrls.priorityMaxLatency 0.000000000000 # per QoS priority maximum request to response latency (Second)
system.mem_ctrls.numReadWriteTurnArounds 0 # Number of turnarounds from READ to WRITE (Count)
system.mem_ctrls.numWriteReadTurnArounds 0 # Number of turnarounds from WRITE to READ (Count)
system.mem_ctrls.numStayReadState 0 # Number of times bus staying in READ state (Count)
system.mem_ctrls.numStayWriteState 0 # Number of times bus staying in WRITE state (Count)
system.mem_ctrls.readReqs 0 # Number of read requests accepted (Count)
system.mem_ctrls.writeReqs 0 # Number of write requests accepted (Count)
system.mem_ctrls.readBursts 0 # Number of controller read bursts, including those serviced by the write queue (Count)
system.mem_ctrls.writeBursts 0 # Number of controller write bursts, including those merged in the write queue (Count)
system.mem_ctrls.servicedByWrQ 0 # Number of controller read bursts serviced by the write queue (Count)
system.mem_ctrls.mergedWrBursts 0 # Number of controller write bursts merged with an existing one (Count)
system.mem_ctrls.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write (Count)
system.mem_ctrls.avgRdQLen 0.00 # Average read queue length when enqueuing ((Count/Tick))
system.mem_ctrls.avgWrQLen 0.00 # Average write queue length when enqueuing ((Count/Tick))
system.mem_ctrls.numRdRetry 0 # Number of times read queue was full causing retry (Count)
system.mem_ctrls.numWrRetry 0 # Number of times write queue was full causing retry (Count)
system.mem_ctrls.readPktSize::0 0 # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::1 0 # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::2 0 # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::3 0 # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::4 0 # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::5 0 # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::6 0 # Read request sizes (log2) (Count)
system.mem_ctrls.writePktSize::0 0 # Write request sizes (log2) (Count)
```

```
system.mem_ctrls.writePktSize::1                0                # Write request sizes (log2) (Count)
system.mem_ctrls.writePktSize::2                0                # Write request sizes (log2) (Count)
system.mem_ctrls.writePktSize::3                0                # Write request sizes (log2) (Count)
system.mem_ctrls.writePktSize::4                0                # Write request sizes (log2) (Count)
system.mem_ctrls.writePktSize::5                0                # Write request sizes (log2) (Count)
system.mem_ctrls.writePktSize::6                0                # Write request sizes (log2) (Count)
system.mem_ctrls.rdQLenPdf::0                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::1                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::2                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::3                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::4                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::5                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::6                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::7                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::8                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::9                   0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::10                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::11                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::12                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::13                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::14                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::15                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::16                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::17                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::18                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::19                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::20                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::21                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::22                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::23                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::24                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::25                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::26                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::27                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::28                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::29                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::30                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::31                  0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::0                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::1                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::2                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::3                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::4                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::5                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::6                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::7                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::8                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::9                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::10                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::11                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::12                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::13                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::14                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::15                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::16                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::17                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::18                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::19                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::20                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::21                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::22                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::23                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::24                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::25                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::26                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::27                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::28                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::29                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::30                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::31                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::32                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::33                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::34                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::35                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::36                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::37                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::38                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::39                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::40                  0                # What write queue length does an incoming req see (Count)
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system.mem_ctrls.wrQLenPdf::41                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::42                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::43                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::44                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::45                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::46                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::47                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::48                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::49                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::50                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::51                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::52                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::53                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::54                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::55                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::56                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::57                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::58                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::59                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::60                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::61                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::62                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::63                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.bytesReadWrQ                   0                # Total number of bytes read from write queue (Byte)
system.mem_ctrls.bytesReadSys                   0                # Total read bytes from the system interface side (Byte)
system.mem_ctrls.bytesWrittenSys                0                # Total written bytes from the system interface side (Byte)
system.mem_ctrls.avgRdBWSys                     0.00000000       # Average system read bandwidth in Byte/s ((Byte/Second))
system.mem_ctrls.avgWrBWSys                     0.00000000       # Average system write bandwidth in Byte/s ((Byte/Second))
system.mem_ctrls.totGap                         0                # Total gap between requests (Tick)
system.mem_ctrls.avgGap                         nan              # Average gap between requests ((Tick/Count))
system.mem_ctrls.dram.bytesRead::cpu.inst        4999280         # Number of bytes read from this memory (Byte)
system.mem_ctrls.dram.bytesRead::cpu.data         726552         # Number of bytes read from this memory (Byte)
system.mem_ctrls.dram.bytesRead::total           5725832         # Number of bytes read from this memory (Byte)
system.mem_ctrls.dram.bytesInstRead::cpu.inst    4999280         # Number of instructions bytes read from this memory (Byte)
system.mem_ctrls.dram.bytesInstRead::total       4999280         # Number of instructions bytes read from this memory (Byte)
system.mem_ctrls.dram.bytesWritten::cpu.data      399928         # Number of bytes written to this memory (Byte)
system.mem_ctrls.dram.bytesWritten::total         399928         # Number of bytes written to this memory (Byte)
system.mem_ctrls.dram.numReads::cpu.inst          624910         # Number of read requests responded to by this memory (Count)
system.mem_ctrls.dram.numReads::cpu.data          121017         # Number of read requests responded to by this memory (Count)
system.mem_ctrls.dram.numReads::total             745927         # Number of read requests responded to by this memory (Count)
system.mem_ctrls.dram.numWrites::cpu.data          59165         # Number of write requests responded to by this memory (Count)
system.mem_ctrls.dram.numWrites::total             59165         # Number of write requests responded to by this memory (Count)
system.mem_ctrls.dram.bwRead::cpu.inst       9413120390         # Total read bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwRead::cpu.data       1368021284         # Total read bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwRead::total         10781141675         # Total read bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwInstRead::cpu.inst   9413120390         # Instruction read bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwInstRead::total      9413120390         # Instruction read bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwWrite::cpu.data       753022518         # Write bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwWrite::total          753022518         # Write bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwTotal::cpu.inst      9413120390         # Total bandwidth to/from this memory ((Byte/Second))
system.mem_ctrls.dram.bwTotal::cpu.data      2121043802         # Total bandwidth to/from this memory ((Byte/Second))
system.mem_ctrls.dram.bwTotal::total        11534164192         # Total bandwidth to/from this memory ((Byte/Second))
system.mem_ctrls.dram.readBursts                0                # Number of DRAM read bursts (Count)
system.mem_ctrls.dram.writeBursts               0                # Number of DRAM write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::0        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::1        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::2        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::3        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::4        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::5        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::6        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::7        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::8        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::9        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::10       0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::11       0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::12       0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::13       0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::14       0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::15       0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::0        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::1        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::2        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::3        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::4        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::5        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::6        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::7        0                # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::8        0                # Per bank write bursts (Count)
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system.mem_ctrls.dram.perBankWrBursts::9 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::10 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::11 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::12 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::13 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::14 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::15 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.totQLat 0 # Total ticks spent queuing (Tick)
system.mem_ctrls.dram.totBusLat 0 # Total ticks spent in databus transfers (Tick)
system.mem_ctrls.dram.totMemAccLat 0 # Total ticks spent from burst creation until serviced by the DRAM (Tick)
system.mem_ctrls.dram.avgQLat nan # Average queueing delay per DRAM burst ((Tick/Count))
system.mem_ctrls.dram.avgBusLat nan # Average bus latency per DRAM burst ((Tick/Count))
system.mem_ctrls.dram.avgMemAccLat nan # Average memory access latency per DRAM burst ((Tick/Count))
system.mem_ctrls.dram.readRowHits 0 # Number of row buffer hits during reads (Count)
system.mem_ctrls.dram.writeRowHits 0 # Number of row buffer hits during writes (Count)
system.mem_ctrls.dram.readRowHitRate nan # Row buffer hit rate for reads (Ratio)
system.mem_ctrls.dram.writeRowHitRate nan # Row buffer hit rate for writes (Ratio)
system.mem_ctrls.dram.bytesRead 0 # Total number of bytes read from DRAM (Byte)
system.mem_ctrls.dram.bytesWritten 0 # Total number of bytes written to DRAM (Byte)
system.mem_ctrls.dram.avgRdBW 0 # Average DRAM read bandwidth in MiBytes/s ((Byte/Second))
system.mem_ctrls.dram.avgWrBW 0 # Average DRAM write bandwidth in MiBytes/s ((Byte/Second))
system.mem_ctrls.dram.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s ((Byte/Second))
system.mem_ctrls.dram.busUtil 0.00 # Data bus utilization in percentage (Ratio)
system.mem_ctrls.dram.busUtilRead 0.00 # Data bus utilization in percentage for reads (Ratio)
system.mem_ctrls.dram.busUtilWrite 0.00 # Data bus utilization in percentage for writes (Ratio)
system.mem_ctrls.dram.pageHitRate nan # Row buffer hit rate, read and write combined (Ratio)
system.mem_ctrls.dram.power_state.pwrStateResidencyTicks::UNDEFINED 531097000 # Cumulative time (in ticks) in various power states (Tick)
system.mem_ctrls.dram.rank0.actEnergy 0 # Energy for activate commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.preEnergy 0 # Energy for precharge commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.readEnergy 0 # Energy for read commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.writeEnergy 0 # Energy for write commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.refreshEnergy 0 # Energy for refresh commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.actBackEnergy 0 # Energy for active background per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.preBackEnergy 203941440 # Energy for precharge background per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.totalEnergy 203941440 # Total energy per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.averagePower 384.000362 # Core power per rank (mW) (Watt)
system.mem_ctrls.dram.rank0.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::IDLE 531097000 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::REF 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::SREF 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::PRE_PDN 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::ACT 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::ACT_PDN 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.actEnergy 0 # Energy for activate commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.preEnergy 0 # Energy for precharge commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.readEnergy 0 # Energy for read commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.writeEnergy 0 # Energy for write commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.refreshEnergy 0 # Energy for refresh commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.actBackEnergy 0 # Energy for active background per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.preBackEnergy 203941440 # Energy for precharge background per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.totalEnergy 203941440 # Total energy per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.averagePower 384.000362 # Core power per rank (mW) (Watt)
system.mem_ctrls.dram.rank1.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::IDLE 531097000 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::REF 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::SREF 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::PRE_PDN 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::ACT 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::ACT_PDN 0 # Time in different power states (Tick)
system.mem_ctrls.power_state.pwrStateResidencyTicks::UNDEFINED 531097000 # Cumulative time (in ticks) in various power states (Tick)
system.membus.transDist::ReadReq 745927 # Transaction distribution (Count)
system.membus.transDist::ReadResp 745927 # Transaction distribution (Count)
system.membus.transDist::WriteReq 59165 # Transaction distribution (Count)
system.membus.transDist::WriteResp 59165 # Transaction distribution (Count)
system.membus.pktCount_system.cpu.icache_port::system.mem_ctrls.port 1249820 # Packet count per connected requestor and responder (Count)
system.membus.pktCount_system.cpu.icache_port::total 1249820 # Packet count per connected requestor and responder (Count)
system.membus.pktCount_system.cpu.dcache_port::system.mem_ctrls.port 360364 # Packet count per connected requestor and responder (Count)
system.membus.pktCount_system.cpu.dcache_port::total 360364 # Packet count per connected requestor and responder (Count)
system.membus.pktCount::total 1610184 # Packet count per connected requestor and responder (Count)

system.membus.pktSize_system.cpu.icache_port::system.mem_ctrls.port 4999280 # Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize_system.cpu.icache_port::total 4999280 # Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize_system.cpu.dcache_port::system.mem_ctrls.port 1126480 # Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize_system.cpu.dcache_port::total 1126480 # Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize::total 6125760 # Cumulative packet size per connected requestor and responder (Byte)
system.membus.snoops 0 # Total snoops (Count)
system.membus.snoopTraffic 0 # Total snoop traffic (Byte)
system.membus.snoopFanout::samples 805092 # Request fanout histogram
system.membus.snoopFanout::mean 0 # Request fanout histogram
system.membus.snoopFanout::stdev 0 # Request fanout histogram
system.membus.snoopFanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.membus.snoopFanout::0 805092 100.00% 100.00% # Request fanout histogram
system.membus.snoopFanout::1 0 0.00% 100.00% # Request fanout histogram
system.membus.snoopFanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.membus.snoopFanout::min_value 0 # Request fanout histogram
system.membus.snoopFanout::max_value 0 # Request fanout histogram
system.membus.snoopFanout::total 805092 # Request fanout histogram
system.membus.power_state.pwrStateResidencyTicks::UNDEFINED 531097000 # Cumulative time (in ticks) in various power states (Tick)
system.membus.snoop_filter.totRequests 0 # Total number of requests made to the snoop filter. (Count)
system.membus.snoop_filter.hitSingleRequests 0 # Number of requests hitting in the snoop filter with a single holder of the requested data. (Count)
system.membus.snoop_filter.hitMultiRequests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)
system.membus.snoop_filter.totSnoops 0 # Total number of snoops made to the snoop filter. (Count)
system.membus.snoop_filter.hitSingleSnoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data. (Count)
system.membus.snoop_filter.hitMultiSnoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)
system.voltage_domain.voltage 1 # Voltage in Volts (Volt)
system.workload.inst.arm 0 # number of arm instructions executed (Count)
system.workload.inst.quiesce 0 # number of quiesce instructions executed (Count)

---------- End Simulation Statistics ----------

9. Now I run the with cache :

build/X86/gem5.opt configs/example/se.py --caches --l2cache -c acd

it’s working fine

10. Now implement that program with the input.

11. We need to download Benchmarks:

https://drive.google.com/drive/folders/1mNrcayXQVRjiSttXwZyW_Hcm3PxroaaH?usp=sharing

12. Now run the benchmarks for check:

build/X86/gem5.opt -d pro configs/example/se.py --cpu-type=TimingSimpleCPU --caches –l1d_size=1kB --l1d_assoc=1 --cacheline_size=16 --l2cache --num-l2caches=1 --l2_size=16kB --l2_assoc=16 --l1i_size=2kB --l1i_assoc=1 -c dijkstra_small -o input.dat

it’s working fine. So the benchmarks is ok.

13. Now we set the run funtion to use the caches input in our expected program.

14. Create new file

vi run.sh

15. Write that code:

```
#!/bin/bash

build/X86/gem5.opt -d pro configs/example/se.py --cpu-type=AtomicSimpleCPU --caches --l1d_size=1kB --
l1d_assoc=1 --cacheline_size=16 --l2cache --num-l2caches=1 --l2_size=16kB --l2_assoc=16 --l1i_size=2kB --
l1i_assoc=1 -c acd -o input.dat
```

Here we are add our replacement code acd

16. Check the code right or wrong:

```
chmod +x run.sh
```

it’s working fine.

17. Run the code:

```
./run.sh
```

Result:

```
gem5 Simulator System.  http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 21.0.0.0
gem5 compiled Jun 14 2021 16:00:49
gem5 started Jun 19 2021 15:21:30
gem5 executing on shantonu, pid 3091
command line: build/X86/gem5.opt -d pro configs/example/se.py --cpu-type=AtomicSimpleCPU --caches --l1d_size=1kB --
l1d_assoc=1 --cacheline_size=16 --l2cache --num-l2caches=1 --l2_size=16kB --l2_assoc=16 --l1i_size=2kB --l1i_assoc=1 -c acd -o
input.dat

warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: tol2bus.master is deprecated. `master` is now called `mem_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: tol2bus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: tol2bus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: tol2bus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: tol2bus.slave is deprecated. `slave` is now called `cpu_side_ports`
warn: membus.master is deprecated. `master` is now called `mem_side_ports`
warn: membus.master is deprecated. `master` is now called `mem_side_ports`
warn: membus.slave is deprecated. `slave` is now called `cpu_side_ports`
Global frequency set at 1000000000000 ticks per second
warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7000
**** REAL SIMULATION ****
info: Entering event queue @ 0.  Starting simulation...
warn: ignoring syscall access(...)
warn: ignoring syscall access(...)
warn: ignoring syscall access(...)
warn: ignoring syscall mprotect(...)
warn: ignoring syscall mprotect(...)
warn: ignoring syscall mprotect(...)
warn: ignoring syscall mprotect(...)
info: Increasing stack size by one page.
Cache replacement policy is optimal
3       -1      -1
3       -1      -1
3       7       -1
3       7       -1
3       7       0
8       7       0
2       7       0
2       7       0
9       7       0
1       7       0
```

Total Page Faults = 7
previous hit ratio is 0.0 and current hit ratio is 0.3
Cache replacement policy is optimal
6 -1 -1
6 8 -1
6 8 9
0 8 9
0 8 9
0 8 9
0 5 9
0 3 9
0 3 9
0 3 9

Total Page Faults = 6
previous hit ratio is 0.3 and current hit ratio is 0.4
Cache replacement policy is optimal
8 -1 -1
8 7 -1
8 7 5
8 2 5
8 6 5
8 6 5
8 6 5
8 6 5
3 6 5
7 6 5

Total Page Faults = 7
previous hit ratio is 0.4 and current hit ratio is 0.3
Cache replacement policy is fifo
Fault: 5 -1 -1
Fault: 5 8 -1
Fault: 5 8 2
Fault: 4 8 2
Fault: 4 6 2
Fault: 4 6 3
Fault: 2 6 3
Fault: 2 0 3
Fault: 2 0 5
Hit: 2 0 5
Number of page fault is: 9
previous hit ratio is 0.3 and current hit ratio is 0.1
Cache replacement policy is optimal
1 -1 -1
1 3 -1
1 3 2
1 3 2
4 3 2
4 3 2
4 3 2
4 9 2
4 9 2
4 9 2

Total Page Faults = 5
previous hit ratio is 0.1 and current hit ratio is 0.5
Cache replacement policy is optimal
4 -1 -1
4 8 -1
4 8 1
9 8 1
2 8 1
7 8 1
7 5 1
7 5 1
7 5 1
0 5 1

Total Page Faults = 8
previous hit ratio is 0.5 and current hit ratio is 0.2
Cache replacement policy is fifo
Fault: 0 -1 -1
Fault: 0 2 -1
Fault: 0 2 1
Hit: 0 2 1
Fault: 6 2 1
Fault: 6 7 1
Hit: 6 7 1
Hit: 6 7 1
Hit: 6 7 1
Fault: 6 7 4
Number of page fault is: 6
previous hit ratio is 0.2 and current hit ratio is 0.4
Cache replacement policy is fifo
Fault: 5 -1 -1
Fault: 5 0 -1
Fault: 5 0 8
Fault: 7 0 8
Fault: 7 2 8
Fault: 7 2 4
Hit: 7 2 4
Fault: 8 2 4
Fault: 8 3 4
Hit: 8 3 4
Number of page fault is: 8
previous hit ratio is 0.4 and current hit ratio is 0.2
Cache replacement policy is optimal
2 -1 -1
2 9 -1
2 9 1
2 9 5
2 9 5
2 6 5
2 6 5
2 6 5
2 7 5
2 7 5

Total Page Faults = 6
previous hit ratio is 0.2 and current hit ratio is 0.4
Cache replacement policy is optimal
6 -1 -1
6 7 -1
6 7 -1
6 7 9
6 1 9
6 1 3
6 1 3
6 1 3
6 1 3
5 1 3

Total Page Faults = 6
previous hit ratio is 0.4 and current hit ratio is 0.4
Exiting @ tick 532315000 because exiting with last active thread context.

18. The main result save in the following path: grm5/pro/stats.txt Result is:

---------- Begin Simulation Statistics ----------
simSeconds 0.000532 # Number of seconds simulated (Second)
simTicks 532315000 # Number of ticks simulated (Tick)
finalTick 532315000 # Number of ticks from beginning of simulation (restored from checkpoints and never reset) (Tick)
simFreq 1000000000000 # The number of ticks per simulated second ((Tick/Second))
hostSeconds 0.96 # Real time elapsed on the host (Second)

```
hostTickRate                                552582824                       # The number of ticks simulated per host second (ticks/s) ((Tick/Second))
hostMemory                                  692880                          # Number of bytes of host memory used (Byte)
simInsts                                    464073                          # Number of instructions simulated (Count)
simOps                                      902436                          # Number of ops (including micro ops) simulated (Count)
hostInstRate                                481657                          # Simulator instruction rate (inst/s) ((Count/Second))
hostOpRate                                  936617                          # Simulator op (including micro ops) rate (op/s) ((Count/Second))
system.clk_domain.clock                     1000                            # Clock period in ticks (Tick)
system.cpu.numCycles                        1064631                         # Number of cpu cycles simulated (Cycle)
system.cpu.numWorkItemsStarted              0                               # Number of work items this cpu started (Count)
system.cpu.numWorkItemsCompleted            0                               # Number of work items this cpu completed (Count)
system.cpu.dcache.demandHits::cpu.data      142407                          # number of demand (read+write) hits (Count)
system.cpu.dcache.demandHits::total         142407                          # number of demand (read+write) hits (Count)
system.cpu.dcache.overallHits::cpu.data     142407                          # number of overall hits (Count)
system.cpu.dcache.overallHits::total        142407                          # number of overall hits (Count)
system.cpu.dcache.demandMisses::cpu.data    38735                           # number of demand (read+write) misses (Count)
system.cpu.dcache.demandMisses::total       38735                           # number of demand (read+write) misses (Count)
system.cpu.dcache.overallMisses::cpu.data   38735                           # number of overall misses (Count)
system.cpu.dcache.overallMisses::total      38735                           # number of overall misses (Count)
system.cpu.dcache.demandAccesses::cpu.data  181142                          # number of demand (read+write) accesses (Count)
system.cpu.dcache.demandAccesses::total     181142                          # number of demand (read+write) accesses (Count)
system.cpu.dcache.overallAccesses::cpu.data 181142                          # number of overall (read+write) accesses (Count)
system.cpu.dcache.overallAccesses::total    181142                          # number of overall (read+write) accesses (Count)
system.cpu.dcache.demandMissRate::cpu.data  0.213838                        # miss rate for demand accesses (Ratio)
system.cpu.dcache.demandMissRate::total     0.213838                        # miss rate for demand accesses (Ratio)
system.cpu.dcache.overallMissRate::cpu.data 0.213838                        # miss rate for overall accesses (Ratio)
system.cpu.dcache.overallMissRate::total    0.213838                        # miss rate for overall accesses (Ratio)
system.cpu.dcache.blockedCycles::no_mshrs   0                               # number of cycles access was blocked (Cycle)
system.cpu.dcache.blockedCycles::no_targets 0                               # number of cycles access was blocked (Cycle)
system.cpu.dcache.blockedCauses::no_mshrs   0                               # number of times access was blocked (Count)
system.cpu.dcache.blockedCauses::no_targets 0                               # number of times access was blocked (Count)
system.cpu.dcache.avgBlocked::no_mshrs      nan                             # average number of cycles each access was blocked
((Cycle/Count))
system.cpu.dcache.avgBlocked::no_targets    nan                             # average number of cycles each access was blocked
((Cycle/Count))
system.cpu.dcache.writebacks::writebacks    17924                           # number of writebacks (Count)
system.cpu.dcache.writebacks::total         17924                           # number of writebacks (Count)
system.cpu.dcache.replacements              38671                           # number of replacements (Count)
system.cpu.dcache.ReadReq.hits::cpu.data    94313                           # number of ReadReq hits (Count)
system.cpu.dcache.ReadReq.hits::total       94313                           # number of ReadReq hits (Count)
system.cpu.dcache.ReadReq.misses::cpu.data  27630                           # number of ReadReq misses (Count)
system.cpu.dcache.ReadReq.misses::total     27630                           # number of ReadReq misses (Count)
system.cpu.dcache.ReadReq.accesses::cpu.data 121943                         # number of ReadReq accesses(hits+misses) (Count)
system.cpu.dcache.ReadReq.accesses::total   121943                          # number of ReadReq accesses(hits+misses) (Count)
system.cpu.dcache.ReadReq.missRate::cpu.data 0.226581                       # miss rate for ReadReq accesses (Ratio)
system.cpu.dcache.ReadReq.missRate::total   0.226581                        # miss rate for ReadReq accesses (Ratio)
system.cpu.dcache.WriteReq.hits::cpu.data   48094                           # number of WriteReq hits (Count)
system.cpu.dcache.WriteReq.hits::total      48094                           # number of WriteReq hits (Count)
system.cpu.dcache.WriteReq.misses::cpu.data 11105                           # number of WriteReq misses (Count)
system.cpu.dcache.WriteReq.misses::total    11105                           # number of WriteReq misses (Count)
system.cpu.dcache.WriteReq.accesses::cpu.data 59199                         # number of WriteReq accesses(hits+misses) (Count)
system.cpu.dcache.WriteReq.accesses::total  59199                           # number of WriteReq accesses(hits+misses) (Count)
system.cpu.dcache.WriteReq.missRate::cpu.data 0.187588                      # miss rate for WriteReq accesses (Ratio)
system.cpu.dcache.WriteReq.missRate::total  0.187588                        # miss rate for WriteReq accesses (Ratio)
system.cpu.dcache.power_state.pwrStateResidencyTicks::UNDEFINED 532315000   # Cumulative time (in ticks) in
various power states (Tick)
system.cpu.dcache.tags.tagsInUse            63.957663                       # Average ticks per tags in use ((Tick/Count))
system.cpu.dcache.tags.totalRefs            181142                          # Total number of references to valid blocks. (Count)
system.cpu.dcache.tags.sampledRefs          38735                           # Sample count of references to valid blocks. (Count)
system.cpu.dcache.tags.avgRefs              4.676442                        # Average number of references to valid blocks. ((Count/Count))
system.cpu.dcache.tags.warmupTick           1500                            # The tick when the warmup percentage was hit. (Tick)
system.cpu.dcache.tags.occupancies::cpu.data 63.957663                      # Average occupied blocks per tick, per requestor
((Count/Tick))
system.cpu.dcache.tags.avgOccs::cpu.data    0.999338                        # Average percentage of cache occupancy ((Ratio/Tick))
system.cpu.dcache.tags.avgOccs::total       0.999338                        # Average percentage of cache occupancy ((Ratio/Tick))
system.cpu.dcache.tags.occupanciesTaskId::1024 64                           # Occupied blocks per task id (Count)
system.cpu.dcache.tags.ageTaskId_1024::0    63                              # Occupied blocks per task id, per block age (Count)
system.cpu.dcache.tags.ageTaskId_1024::1    1                               # Occupied blocks per task id, per block age (Count)
system.cpu.dcache.tags.ratioOccsTaskId::1024 1                              # Ratio of occupied blocks and all blocks, per task id (Ratio)
system.cpu.dcache.tags.tagAccesses          219877                          # Number of tag accesses (Count)
system.cpu.dcache.tags.dataAccesses         219877                          # Number of data accesses (Count)
```

system.cpu.dcache.tags.power_state.pwrStateResidencyTicks::UNDEFINED 532315000 # Cumulative time (in ticks) in various power states (Tick)
system.cpu.dtb_walker_cache.blockedCycles::no_mshrs 0 # number of cycles access was blocked (Cycle)
system.cpu.dtb_walker_cache.blockedCycles::no_targets 0 # number of cycles access was blocked (Cycle)
system.cpu.dtb_walker_cache.blockedCauses::no_mshrs 0 # number of times access was blocked (Count)
system.cpu.dtb_walker_cache.blockedCauses::no_targets 0 # number of times access was blocked (Count)
system.cpu.dtb_walker_cache.avgBlocked::no_mshrs nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.dtb_walker_cache.avgBlocked::no_targets nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.dtb_walker_cache.replacements 0 # number of replacements (Count)
system.cpu.dtb_walker_cache.power_state.pwrStateResidencyTicks::UNDEFINED 532315000 # Cumulative time (in ticks) in various power states (Tick)
system.cpu.dtb_walker_cache.tags.tagsInUse 0 # Average ticks per tags in use ((Tick/Count))
system.cpu.dtb_walker_cache.tags.totalRefs 0 # Total number of references to valid blocks. (Count)
system.cpu.dtb_walker_cache.tags.sampledRefs 0 # Sample count of references to valid blocks. (Count)
system.cpu.dtb_walker_cache.tags.avgRefs nan # Average number of references to valid blocks. ((Count/Count))
system.cpu.dtb_walker_cache.tags.warmupTick 0 # The tick when the warmup percentage was hit. (Tick)
system.cpu.dtb_walker_cache.tags.tagAccesses 0 # Number of tag accesses (Count)
system.cpu.dtb_walker_cache.tags.dataAccesses 0 # Number of data accesses (Count)
system.cpu.dtb_walker_cache.tags.power_state.pwrStateResidencyTicks::UNDEFINED 532315000 # Cumulative time (in ticks) in various power states (Tick)
system.cpu.exec_context.thread_0.numInsts 464073 # Number of instructions committed (Count)
system.cpu.exec_context.thread_0.numOps 902436 # Number of ops (including micro ops) committed (Count)
system.cpu.exec_context.thread_0.numIntAluAccesses 879719 # Number of integer alu accesses (Count)
system.cpu.exec_context.thread_0.numFpAluAccesses 28641 # Number of float alu accesses (Count)
system.cpu.exec_context.thread_0.numVecAluAccesses 0 # Number of vector alu accesses (Count)
system.cpu.exec_context.thread_0.numCallsReturns 11726 # Number of times a function call or return occured (Count)
system.cpu.exec_context.thread_0.numCondCtrlInsts 82553 # Number of instructions that are conditional controls (Count)
system.cpu.exec_context.thread_0.numIntInsts 879719 # Number of integer instructions (Count)
system.cpu.exec_context.thread_0.numFpInsts 28641 # Number of float instructions (Count)
system.cpu.exec_context.thread_0.numVecInsts 0 # Number of vector instructions (Count)
system.cpu.exec_context.thread_0.numIntRegReads 1719771 # Number of times the integer registers were read (Count)
system.cpu.exec_context.thread_0.numIntRegWrites 717098 # Number of times the integer registers were written (Count)
system.cpu.exec_context.thread_0.numFpRegReads 48379 # Number of times the floating registers were read (Count)
system.cpu.exec_context.thread_0.numFpRegWrites 23973 # Number of times the floating registers were written (Count)
system.cpu.exec_context.thread_0.numVecRegReads 0 # Number of times the vector registers were read (Count)
system.cpu.exec_context.thread_0.numVecRegWrites 0 # Number of times the vector registers were written (Count)
system.cpu.exec_context.thread_0.numVecPredRegReads 0 # Number of times the predicate registers were read (Count)
system.cpu.exec_context.thread_0.numVecPredRegWrites 0 # Number of times the predicate registers were written (Count)
system.cpu.exec_context.thread_0.numCCRegReads 551405 # Number of times the CC registers were read (Count)
system.cpu.exec_context.thread_0.numCCRegWrites 301502 # Number of times the CC registers were written (Count)
system.cpu.exec_context.thread_0.numMemRefs 180340 # Number of memory refs (Count)
system.cpu.exec_context.thread_0.numLoadInsts 121177 # Number of load instructions (Count)
system.cpu.exec_context.thread_0.numStoreInsts 59163 # Number of store instructions (Count)
system.cpu.exec_context.thread_0.numIdleCycles 0.002000 # Number of idle cycles (Cycle)
system.cpu.exec_context.thread_0.numBusyCycles 1064630.998000 # Number of busy cycles (Cycle)
system.cpu.exec_context.thread_0.notIdleFraction 1.000000 # Percentage of non-idle cycles (Ratio)
system.cpu.exec_context.thread_0.idleFraction 0.000000 # Percentage of idle cycles (Ratio)
system.cpu.exec_context.thread_0.numBranches 104367 # Number of branches fetched (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::No_OpClass 3800 0.42% 0.42% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::IntAlu 696855 77.20% 77.62% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::IntMult 641 0.07% 77.69% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::IntDiv 1770 0.20% 77.89% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatAdd 954 0.11% 77.99% # Class of executed instruction.

(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatCmp 0 0.00% 77.99% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatCvt 32 0.00% 78.00% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMult 0 0.00% 78.00% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMultAcc 0 0.00% 78.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatDiv 0 0.00% 78.00% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMisc 0 0.00% 78.00% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatSqrt 0 0.00% 78.00% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAdd 1008 0.11% 78.11% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAddAcc 0 0.00% 78.11% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAlu 4335 0.48% 78.59% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdCmp 0 0.00% 78.59% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdCvt 4692 0.52% 79.11% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdMisc 7530 0.83% 79.94% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdMult 0 0.00% 79.94% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdMultAcc 0 0.00% 79.94% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShift 594 0.07% 80.01% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShiftAcc 0 0.00% 80.01% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdDiv 0 0.00% 80.01% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSqrt 0 0.00% 80.01% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatAdd 0 0.00% 80.01% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatAlu 0 0.00% 80.01% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatCmp 0 0.00% 80.01% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatCvt 96 0.01% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatDiv 10 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatMisc 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatMult 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatMultAcc 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatSqrt 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdReduceAdd 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdReduceAlu 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdReduceCmp 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatReduceAdd 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatReduceCmp 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAes 0 0.00% 80.02% # Class of executed instruction.
(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAesMix 0 0.00% 80.02% # Class of executed instruction.

(Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha1Hash 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha1Hash2 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha256Hash 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha256Hash2 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShaSigma2 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShaSigma3 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::SimdPredAlu 0 0.00% 80.02% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::MemRead 116777 12.94% 92.96% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::MemWrite 57056 6.32% 99.28% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMemRead 4400 0.49% 99.77% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMemWrite 2107 0.23% 100.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::IprAccess 0 0.00% 100.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::InstPrefetch 0 0.00% 100.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread_0.statExecutedInstType::total 902657 # Class of executed instruction. (Count)
system.cpu.icache.demandHits::cpu.inst 552178 # number of demand (read+write) hits (Count)
system.cpu.icache.demandHits::total 552178 # number of demand (read+write) hits (Count)
system.cpu.icache.overallHits::cpu.inst 552178 # number of overall hits (Count)
system.cpu.icache.overallHits::total 552178 # number of overall hits (Count)
system.cpu.icache.demandMisses::cpu.inst 74038 # number of demand (read+write) misses (Count)
system.cpu.icache.demandMisses::total 74038 # number of demand (read+write) misses (Count)
system.cpu.icache.overallMisses::cpu.inst 74038 # number of overall misses (Count)
system.cpu.icache.overallMisses::total 74038 # number of overall misses (Count)
system.cpu.icache.demandAccesses::cpu.inst 626216 # number of demand (read+write) accesses (Count)
system.cpu.icache.demandAccesses::total 626216 # number of demand (read+write) accesses (Count)
system.cpu.icache.overallAccesses::cpu.inst 626216 # number of overall (read+write) accesses (Count)
system.cpu.icache.overallAccesses::total 626216 # number of overall (read+write) accesses (Count)
system.cpu.icache.demandMissRate::cpu.inst 0.118231 # miss rate for demand accesses (Ratio)
system.cpu.icache.demandMissRate::total 0.118231 # miss rate for demand accesses (Ratio)
system.cpu.icache.overallMissRate::cpu.inst 0.118231 # miss rate for overall accesses (Ratio)
system.cpu.icache.overallMissRate::total 0.118231 # miss rate for overall accesses (Ratio)
system.cpu.icache.blockedCycles::no_mshrs 0 # number of cycles access was blocked (Cycle)
system.cpu.icache.blockedCycles::no_targets 0 # number of cycles access was blocked (Cycle)
system.cpu.icache.blockedCauses::no_mshrs 0 # number of times access was blocked (Count)
system.cpu.icache.blockedCauses::no_targets 0 # number of times access was blocked (Count)
system.cpu.icache.avgBlocked::no_mshrs nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.icache.avgBlocked::no_targets nan # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.icache.writebacks::writebacks 73910 # number of writebacks (Count)
system.cpu.icache.writebacks::total 73910 # number of writebacks (Count)
system.cpu.icache.replacements 73910 # number of replacements (Count)
system.cpu.icache.ReadReq.hits::cpu.inst 552178 # number of ReadReq hits (Count)
system.cpu.icache.ReadReq.hits::total 552178 # number of ReadReq hits (Count)
system.cpu.icache.ReadReq.misses::cpu.inst 74038 # number of ReadReq misses (Count)
system.cpu.icache.ReadReq.misses::total 74038 # number of ReadReq misses (Count)
system.cpu.icache.ReadReq.accesses::cpu.inst 626216 # number of ReadReq accesses(hits+misses) (Count)
system.cpu.icache.ReadReq.accesses::total 626216 # number of ReadReq accesses(hits+misses) (Count)
system.cpu.icache.ReadReq.missRate::cpu.inst 0.118231 # miss rate for ReadReq accesses (Ratio)
system.cpu.icache.ReadReq.missRate::total 0.118231 # miss rate for ReadReq accesses (Ratio)
system.cpu.icache.power_state.pwrStateResidencyTicks::UNDEFINED 532315000 # Cumulative time (in ticks) in various power states (Tick)
system.cpu.icache.tags.tagsInUse 127.783574 # Average ticks per tags in use ((Tick/Count))
system.cpu.icache.tags.totalRefs 626216 # Total number of references to valid blocks. (Count)
system.cpu.icache.tags.sampledRefs 74038 # Sample count of references to valid blocks. (Count)
system.cpu.icache.tags.avgRefs 8.458035 # Average number of references to valid blocks. ((Count/Count))
system.cpu.icache.tags.warmupTick 0 # The tick when the warmup percentage was hit. (Tick)

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system.cpu.icache.tags.occupancies::cpu.inst   127.783574                # Average occupied blocks per tick, per requestor ((Count/Tick))
system.cpu.icache.tags.avgOccs::cpu.inst     0.998309                # Average percentage of cache occupancy ((Ratio/Tick))
system.cpu.icache.tags.avgOccs::total        0.998309                # Average percentage of cache occupancy ((Ratio/Tick))
system.cpu.icache.tags.occupanciesTaskId::1024          128                # Occupied blocks per task id (Count)
system.cpu.icache.tags.ageTaskId_1024::0         128                # Occupied blocks per task id, per block age (Count)
system.cpu.icache.tags.ratioOccsTaskId::1024           1                # Ratio of occupied blocks and all blocks, per task id (Ratio)
system.cpu.icache.tags.tagAccesses            700254                # Number of tag accesses (Count)
system.cpu.icache.tags.dataAccesses           700254                # Number of data accesses (Count)
system.cpu.icache.tags.power_state.pwrStateResidencyTicks::UNDEFINED    532315000                # Cumulative time (in ticks) in various power states (Tick)
system.cpu.interrupts.clk_domain.clock          8000                # Clock period in ticks (Tick)
system.cpu.itb_walker_cache.blockedCycles::no_mshrs           0                # number of cycles access was blocked (Cycle)
system.cpu.itb_walker_cache.blockedCycles::no_targets           0                # number of cycles access was blocked (Cycle)
system.cpu.itb_walker_cache.blockedCauses::no_mshrs           0                # number of times access was blocked (Count)
system.cpu.itb_walker_cache.blockedCauses::no_targets           0                # number of times access was blocked (Count)
system.cpu.itb_walker_cache.avgBlocked::no_mshrs         nan                # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.itb_walker_cache.avgBlocked::no_targets         nan                # average number of cycles each access was blocked ((Cycle/Count))
system.cpu.itb_walker_cache.replacements           0                # number of replacements (Count)
system.cpu.itb_walker_cache.power_state.pwrStateResidencyTicks::UNDEFINED    532315000                # Cumulative time (in ticks) in various power states (Tick)
system.cpu.itb_walker_cache.tags.tagsInUse           0                # Average ticks per tags in use ((Tick/Count))
system.cpu.itb_walker_cache.tags.totalRefs           0                # Total number of references to valid blocks. (Count)
system.cpu.itb_walker_cache.tags.sampledRefs           0                # Sample count of references to valid blocks. (Count)
system.cpu.itb_walker_cache.tags.avgRefs         nan                # Average number of references to valid blocks. ((Count/Count))
system.cpu.itb_walker_cache.tags.warmupTick           0                # The tick when the warmup percentage was hit. (Tick)
system.cpu.itb_walker_cache.tags.tagAccesses           0                # Number of tag accesses (Count)
system.cpu.itb_walker_cache.tags.dataAccesses           0                # Number of data accesses (Count)
system.cpu.itb_walker_cache.tags.power_state.pwrStateResidencyTicks::UNDEFINED    532315000                # Cumulative time (in ticks) in various power states (Tick)
system.cpu.mmu.dtb.rdAccesses          121994                # TLB accesses on read requests (Count)
system.cpu.mmu.dtb.wrAccesses           59210                # TLB accesses on write requests (Count)
system.cpu.mmu.dtb.rdMisses              159                # TLB misses on read requests (Count)
system.cpu.mmu.dtb.wrMisses               29                # TLB misses on write requests (Count)
system.cpu.mmu.dtb.walker.power_state.pwrStateResidencyTicks::UNDEFINED    532315000                # Cumulative time (in ticks) in various power states (Tick)
system.cpu.mmu.itb.rdAccesses               0                # TLB accesses on read requests (Count)
system.cpu.mmu.itb.wrAccesses          626268                # TLB accesses on write requests (Count)
system.cpu.mmu.itb.rdMisses                 0                # TLB misses on read requests (Count)
system.cpu.mmu.itb.wrMisses               179                # TLB misses on write requests (Count)
system.cpu.mmu.itb.walker.power_state.pwrStateResidencyTicks::UNDEFINED    532315000                # Cumulative time (in ticks) in various power states (Tick)
system.cpu.power_state.pwrStateResidencyTicks::ON    532315000                # Cumulative time (in ticks) in various power states (Tick)
system.cpu.thread_0.numInsts                0                # Number of Instructions committed (Count)
system.cpu.thread_0.numOps                  0                # Number of Ops committed (Count)
system.cpu.thread_0.numMemRefs              0                # Number of Memory References (Count)
system.cpu.workload.numSyscalls           159                # Number of system calls (Count)
system.cpu_clk_domain.clock               500                # Clock period in ticks (Tick)
system.cpu_voltage_domain.voltage           1                # Voltage in Volts (Volt)
system.l2.demandHits::cpu.inst          69729                # number of demand (read+write) hits (Count)
system.l2.demandHits::cpu.data          28178                # number of demand (read+write) hits (Count)
system.l2.demandHits::total             97907                # number of demand (read+write) hits (Count)
system.l2.overallHits::cpu.inst         69729                # number of overall hits (Count)
system.l2.overallHits::cpu.data         28178                # number of overall hits (Count)
system.l2.overallHits::total            97907                # number of overall hits (Count)
system.l2.demandMisses::cpu.inst         4309                # number of demand (read+write) misses (Count)
system.l2.demandMisses::cpu.data        10557                # number of demand (read+write) misses (Count)
system.l2.demandMisses::total           14866                # number of demand (read+write) misses (Count)
system.l2.overallMisses::cpu.inst        4309                # number of overall misses (Count)
system.l2.overallMisses::cpu.data       10557                # number of overall misses (Count)
system.l2.overallMisses::total          14866                # number of overall misses (Count)
system.l2.demandAccesses::cpu.inst       74038                # number of demand (read+write) accesses (Count)
system.l2.demandAccesses::cpu.data       38735                # number of demand (read+write) accesses (Count)
system.l2.demandAccesses::total         112773                # number of demand (read+write) accesses (Count)
system.l2.overallAccesses::cpu.inst      74038                # number of overall (read+write) accesses (Count)
system.l2.overallAccesses::cpu.data      38735                # number of overall (read+write) accesses (Count)
system.l2.overallAccesses::total        112773                # number of overall (read+write) accesses (Count)
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system.l2.demandMissRate::cpu.inst          0.058200                # miss rate for demand accesses (Ratio)
system.l2.demandMissRate::cpu.data          0.272544                # miss rate for demand accesses (Ratio)
system.l2.demandMissRate::total             0.131822                # miss rate for demand accesses (Ratio)
system.l2.overallMissRate::cpu.inst         0.058200                # miss rate for overall accesses (Ratio)
system.l2.overallMissRate::cpu.data         0.272544                # miss rate for overall accesses (Ratio)
system.l2.overallMissRate::total            0.131822                # miss rate for overall accesses (Ratio)
system.l2.blockedCycles::no_mshrs                 0                 # number of cycles access was blocked (Cycle)
system.l2.blockedCycles::no_targets               0                 # number of cycles access was blocked (Cycle)
system.l2.blockedCauses::no_mshrs                 0                 # number of times access was blocked (Count)
system.l2.blockedCauses::no_targets               0                 # number of times access was blocked (Count)
system.l2.avgBlocked::no_mshrs                  nan                 # average number of cycles each access was blocked ((Cycle/Count))
system.l2.avgBlocked::no_targets                nan                 # average number of cycles each access was blocked ((Cycle/Count))
system.l2.writebacks::writebacks                2179                # number of writebacks (Count)
system.l2.writebacks::total                     2179                # number of writebacks (Count)
system.l2.replacements                          14159               # number of replacements (Count)
system.l2.ReadCleanReq.hits::cpu.inst           69729               # number of ReadCleanReq hits (Count)
system.l2.ReadCleanReq.hits::total              69729               # number of ReadCleanReq hits (Count)
system.l2.ReadCleanReq.misses::cpu.inst          4309               # number of ReadCleanReq misses (Count)
system.l2.ReadCleanReq.misses::total             4309               # number of ReadCleanReq misses (Count)
system.l2.ReadCleanReq.accesses::cpu.inst        74038              # number of ReadCleanReq accesses(hits+misses) (Count)
system.l2.ReadCleanReq.accesses::total           74038              # number of ReadCleanReq accesses(hits+misses) (Count)
system.l2.ReadCleanReq.missRate::cpu.inst     0.058200              # miss rate for ReadCleanReq accesses (Ratio)
system.l2.ReadCleanReq.missRate::total        0.058200              # miss rate for ReadCleanReq accesses (Ratio)
system.l2.ReadExReq.hits::cpu.data               8971               # number of ReadExReq hits (Count)
system.l2.ReadExReq.hits::total                  8971               # number of ReadExReq hits (Count)
system.l2.ReadExReq.misses::cpu.data             2134               # number of ReadExReq misses (Count)
system.l2.ReadExReq.misses::total                2134               # number of ReadExReq misses (Count)
system.l2.ReadExReq.accesses::cpu.data           11105              # number of ReadExReq accesses(hits+misses) (Count)
system.l2.ReadExReq.accesses::total              11105              # number of ReadExReq accesses(hits+misses) (Count)
system.l2.ReadExReq.missRate::cpu.data        0.192166              # miss rate for ReadExReq accesses (Ratio)
system.l2.ReadExReq.missRate::total           0.192166              # miss rate for ReadExReq accesses (Ratio)
system.l2.ReadSharedReq.hits::cpu.data           19207              # number of ReadSharedReq hits (Count)
system.l2.ReadSharedReq.hits::total              19207              # number of ReadSharedReq hits (Count)
system.l2.ReadSharedReq.misses::cpu.data          8423              # number of ReadSharedReq misses (Count)
system.l2.ReadSharedReq.misses::total             8423              # number of ReadSharedReq misses (Count)
system.l2.ReadSharedReq.accesses::cpu.data       27630              # number of ReadSharedReq accesses(hits+misses) (Count)
system.l2.ReadSharedReq.accesses::total          27630              # number of ReadSharedReq accesses(hits+misses) (Count)
system.l2.ReadSharedReq.missRate::cpu.data    0.304850              # miss rate for ReadSharedReq accesses (Ratio)
system.l2.ReadSharedReq.missRate::total       0.304850              # miss rate for ReadSharedReq accesses (Ratio)
system.l2.WritebackClean.hits::writebacks        73910              # number of WritebackClean hits (Count)
system.l2.WritebackClean.hits::total             73910              # number of WritebackClean hits (Count)
system.l2.WritebackClean.accesses::writebacks    73910              # number of WritebackClean accesses(hits+misses) (Count)
system.l2.WritebackClean.accesses::total         73910              # number of WritebackClean accesses(hits+misses) (Count)
system.l2.WritebackDirty.hits::writebacks        17924              # number of WritebackDirty hits (Count)
system.l2.WritebackDirty.hits::total             17924              # number of WritebackDirty hits (Count)
system.l2.WritebackDirty.accesses::writebacks    17924              # number of WritebackDirty accesses(hits+misses) (Count)
system.l2.WritebackDirty.accesses::total         17924              # number of WritebackDirty accesses(hits+misses) (Count)
system.l2.power_state.pwrStateResidencyTicks::UNDEFINED    532315000          # Cumulative time (in ticks) in various
power states (Tick)
system.l2.tags.tagsInUse                  1020.223126               # Average ticks per tags in use ((Tick/Count))
system.l2.tags.totalRefs                     225354                 # Total number of references to valid blocks. (Count)
system.l2.tags.sampledRefs                    15183                 # Sample count of references to valid blocks. (Count)
system.l2.tags.avgRefs                    14.842521                 # Average number of references to valid blocks. ((Count/Count))
system.l2.tags.warmupTick                         0                 # The tick when the warmup percentage was hit. (Tick)
system.l2.tags.occupancies::writebacks    34.920862                 # Average occupied blocks per tick, per requestor ((Count/Tick))
system.l2.tags.occupancies::cpu.inst      558.389364                # Average occupied blocks per tick, per requestor ((Count/Tick))
system.l2.tags.occupancies::cpu.data      426.912901                # Average occupied blocks per tick, per requestor ((Count/Tick))
system.l2.tags.avgOccs::writebacks         0.034102                 # Average percentage of cache occupancy ((Ratio/Tick))
system.l2.tags.avgOccs::cpu.inst           0.545302                 # Average percentage of cache occupancy ((Ratio/Tick))
system.l2.tags.avgOccs::cpu.data           0.416907                 # Average percentage of cache occupancy ((Ratio/Tick))
system.l2.tags.avgOccs::total              0.996312                 # Average percentage of cache occupancy ((Ratio/Tick))
system.l2.tags.occupanciesTaskId::1024         1024                 # Occupied blocks per task id (Count)
system.l2.tags.ageTaskId_1024::0                394                 # Occupied blocks per task id, per block age (Count)
system.l2.tags.ageTaskId_1024::1                 25                 # Occupied blocks per task id, per block age (Count)
system.l2.tags.ageTaskId_1024::2                605                 # Occupied blocks per task id, per block age (Count)
system.l2.tags.ratioOccsTaskId::1024             1                  # Ratio of occupied blocks and all blocks, per task id (Ratio)
system.l2.tags.tagAccesses                3620847                   # Number of tag accesses (Count)
system.l2.tags.dataAccesses               3620847                   # Number of data accesses (Count)
system.l2.tags.power_state.pwrStateResidencyTicks::UNDEFINED    532315000          # Cumulative time (in ticks) in
various power states (Tick)
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system.mem_ctrls.priorityMinLatency       0.000000000000                # per QoS priority minimum request to response latency
(Second)
system.mem_ctrls.priorityMaxLatency       0.000000000000                # per QoS priority maximum request to response latency
(Second)
system.mem_ctrls.numReadWriteTurnArounds          0                # Number of turnarounds from READ to WRITE (Count)
system.mem_ctrls.numWriteReadTurnArounds          0                # Number of turnarounds from WRITE to READ (Count)
system.mem_ctrls.numStayReadState                 0                # Number of times bus staying in READ state (Count)
system.mem_ctrls.numStayWriteState                0                # Number of times bus staying in WRITE state (Count)
system.mem_ctrls.readReqs                         0                # Number of read requests accepted (Count)
system.mem_ctrls.writeReqs                        0                # Number of write requests accepted (Count)
system.mem_ctrls.readBursts                       0                # Number of controller read bursts, including those serviced by the write
queue (Count)
system.mem_ctrls.writeBursts                      0                # Number of controller write bursts, including those merged in the write
queue (Count)
system.mem_ctrls.servicedByWrQ                    0                # Number of controller read bursts serviced by the write queue
(Count)
system.mem_ctrls.mergedWrBursts                   0                # Number of controller write bursts merged with an existing one
(Count)
system.mem_ctrls.neitherReadNorWriteReqs          0                # Number of requests that are neither read nor write (Count)
system.mem_ctrls.avgRdQLen                     0.00                # Average read queue length when enqueuing ((Count/Tick))
system.mem_ctrls.avgWrQLen                     0.00                # Average write queue length when enqueuing ((Count/Tick))
system.mem_ctrls.numRdRetry                       0                # Number of times read queue was full causing retry (Count)
system.mem_ctrls.numWrRetry                       0                # Number of times write queue was full causing retry (Count)
system.mem_ctrls.readPktSize::0                   0                # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::1                   0                # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::2                   0                # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::3                   0                # Read request sizes (log2) (Count)
system.mem_ctrls.readPktSize::4                   0                # Read request sizes (log2) (Count)
system.mem_ctrls.writePktSize::0                  0                # Write request sizes (log2) (Count)
system.mem_ctrls.writePktSize::1                  0                # Write request sizes (log2) (Count)
system.mem_ctrls.writePktSize::2                  0                # Write request sizes (log2) (Count)
system.mem_ctrls.writePktSize::3                  0                # Write request sizes (log2) (Count)
system.mem_ctrls.writePktSize::4                  0                # Write request sizes (log2) (Count)
system.mem_ctrls.rdQLenPdf::0                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::1                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::2                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::3                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::4                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::5                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::6                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::7                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::8                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::9                     0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::10                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::11                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::12                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::13                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::14                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::15                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::16                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::17                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::18                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::19                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::20                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::21                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::22                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::23                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::24                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::25                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::26                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::27                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::28                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::29                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::30                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.rdQLenPdf::31                    0                # What read queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::0                     0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::1                     0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::2                     0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::3                     0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::4                     0                # What write queue length does an incoming req see (Count)
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system.mem_ctrls.wrQLenPdf::5                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::6                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::7                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::8                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::9                   0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::10                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::11                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::12                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::13                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::14                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::15                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::16                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::17                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::18                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::19                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::20                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::21                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::22                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::23                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::24                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::25                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::26                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::27                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::28                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::29                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::30                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::31                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::32                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::33                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::34                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::35                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::36                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::37                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::38                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::39                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::40                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::41                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::42                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::43                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::44                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::45                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::46                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::47                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::48                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::49                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::50                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::51                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::52                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::53                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::54                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::55                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::56                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::57                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::58                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::59                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::60                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::61                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::62                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.wrQLenPdf::63                  0                # What write queue length does an incoming req see (Count)
system.mem_ctrls.bytesReadWrQ                   0                # Total number of bytes read from write queue (Byte)
system.mem_ctrls.bytesReadSys                   0                # Total read bytes from the system interface side (Byte)
system.mem_ctrls.bytesWrittenSys                0                # Total written bytes from the system interface side (Byte)
system.mem_ctrls.avgRdBWSys                     0.00000000       # Average system read bandwidth in Byte/s ((Byte/Second))
system.mem_ctrls.avgWrBWSys                     0.00000000       # Average system write bandwidth in Byte/s ((Byte/Second))
system.mem_ctrls.totGap                         0                # Total gap between requests (Tick)
system.mem_ctrls.avgGap                         nan              # Average gap between requests ((Tick/Count))
system.mem_ctrls.dram.bytesRead::cpu.inst       68944            # Number of bytes read from this memory (Byte)
system.mem_ctrls.dram.bytesRead::cpu.data       168912           # Number of bytes read from this memory (Byte)
system.mem_ctrls.dram.bytesRead::total          237856           # Number of bytes read from this memory (Byte)
system.mem_ctrls.dram.bytesInstRead::cpu.inst   68944            # Number of instructions bytes read from this memory
```

(Byte)
system.mem_ctrls.dram.bytesInstRead::total 68944 # Number of instructions bytes read from this memory (Byte)
system.mem_ctrls.dram.bytesWritten::writebacks 34864 # Number of bytes written to this memory (Byte)
system.mem_ctrls.dram.bytesWritten::total 34864 # Number of bytes written to this memory (Byte)
system.mem_ctrls.dram.numReads::cpu.inst 4309 # Number of read requests responded to by this memory
(Count)
system.mem_ctrls.dram.numReads::cpu.data 10557 # Number of read requests responded to by this memory
(Count)
system.mem_ctrls.dram.numReads::total 14866 # Number of read requests responded to by this memory (Count)
system.mem_ctrls.dram.numWrites::writebacks 2179 # Number of write requests responded to by this memory
(Count)
system.mem_ctrls.dram.numWrites::total 2179 # Number of write requests responded to by this memory (Count)
system.mem_ctrls.dram.bwRead::cpu.inst 129517297 # Total read bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwRead::cpu.data 317315875 # Total read bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwRead::total 446833172 # Total read bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwInstRead::cpu.inst 129517297 # Instruction read bandwidth from this memory
((Byte/Second))
system.mem_ctrls.dram.bwInstRead::total 129517297 # Instruction read bandwidth from this memory
((Byte/Second))
system.mem_ctrls.dram.bwWrite::writebacks 65495055 # Write bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwWrite::total 65495055 # Write bandwidth from this memory ((Byte/Second))
system.mem_ctrls.dram.bwTotal::writebacks 65495055 # Total bandwidth to/from this memory ((Byte/Second))
system.mem_ctrls.dram.bwTotal::cpu.inst 129517297 # Total bandwidth to/from this memory ((Byte/Second))
system.mem_ctrls.dram.bwTotal::cpu.data 317315875 # Total bandwidth to/from this memory ((Byte/Second))
system.mem_ctrls.dram.bwTotal::total 512328227 # Total bandwidth to/from this memory ((Byte/Second))
system.mem_ctrls.dram.readBursts 0 # Number of DRAM read bursts (Count)
system.mem_ctrls.dram.writeBursts 0 # Number of DRAM write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::0 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::1 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::2 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::3 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::4 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::5 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::6 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::7 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::8 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::9 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::10 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::11 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::12 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::13 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::14 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankRdBursts::15 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::0 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::1 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::2 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::3 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::4 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::5 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::6 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::7 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::8 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::9 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::10 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::11 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::12 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::13 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::14 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.perBankWrBursts::15 0 # Per bank write bursts (Count)
system.mem_ctrls.dram.totQLat 0 # Total ticks spent queuing (Tick)
system.mem_ctrls.dram.totBusLat 0 # Total ticks spent in databus transfers (Tick)
system.mem_ctrls.dram.totMemAccLat 0 # Total ticks spent from burst creation until serviced by the
DRAM (Tick)
system.mem_ctrls.dram.avgQLat nan # Average queueing delay per DRAM burst ((Tick/Count))
system.mem_ctrls.dram.avgBusLat nan # Average bus latency per DRAM burst ((Tick/Count))
system.mem_ctrls.dram.avgMemAccLat nan # Average memory access latency per DRAM burst
((Tick/Count))
system.mem_ctrls.dram.readRowHits 0 # Number of row buffer hits during reads (Count)
system.mem_ctrls.dram.writeRowHits 0 # Number of row buffer hits during writes (Count)
system.mem_ctrls.dram.readRowHitRate nan # Row buffer hit rate for reads (Ratio)

system.mem_ctrls.dram.writeRowHitRate nan # Row buffer hit rate for writes (Ratio)
system.mem_ctrls.dram.bytesRead 0 # Total number of bytes read from DRAM (Byte)
system.mem_ctrls.dram.bytesWritten 0 # Total number of bytes written to DRAM (Byte)
system.mem_ctrls.dram.avgRdBW 0 # Average DRAM read bandwidth in MiBytes/s ((Byte/Second))
system.mem_ctrls.dram.avgWrBW 0 # Average DRAM write bandwidth in MiBytes/s ((Byte/Second))
system.mem_ctrls.dram.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s ((Byte/Second))
system.mem_ctrls.dram.busUtil 0.00 # Data bus utilization in percentage (Ratio)
system.mem_ctrls.dram.busUtilRead 0.00 # Data bus utilization in percentage for reads (Ratio)
system.mem_ctrls.dram.busUtilWrite 0.00 # Data bus utilization in percentage for writes (Ratio)
system.mem_ctrls.dram.pageHitRate nan # Row buffer hit rate, read and write combined (Ratio)
system.mem_ctrls.dram.power_state.pwrStateResidencyTicks::UNDEFINED 532315000 # Cumulative time (in ticks) in various power states (Tick)
system.mem_ctrls.dram.rank0.actEnergy 0 # Energy for activate commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.preEnergy 0 # Energy for precharge commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.readEnergy 0 # Energy for read commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.writeEnergy 0 # Energy for write commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.refreshEnergy 0 # Energy for refresh commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.actBackEnergy 0 # Energy for active background per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.preBackEnergy 204408960 # Energy for precharge background per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.totalEnergy 204408960 # Total energy per rank (pJ) (Joule)
system.mem_ctrls.dram.rank0.averagePower 384 # Core power per rank (mW) (Watt)
system.mem_ctrls.dram.rank0.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::IDLE 532315000 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::REF 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::SREF 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::PRE_PDN 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::ACT 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank0.pwrStateTime::ACT_PDN 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.actEnergy 0 # Energy for activate commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.preEnergy 0 # Energy for precharge commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.readEnergy 0 # Energy for read commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.writeEnergy 0 # Energy for write commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.refreshEnergy 0 # Energy for refresh commands per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.actBackEnergy 0 # Energy for active background per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.preBackEnergy 204408960 # Energy for precharge background per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.actPowerDownEnergy 0 # Energy for active power-down per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.prePowerDownEnergy 0 # Energy for precharge power-down per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.totalEnergy 204408960 # Total energy per rank (pJ) (Joule)
system.mem_ctrls.dram.rank1.averagePower 384 # Core power per rank (mW) (Watt)
system.mem_ctrls.dram.rank1.totalIdleTime 0 # Total Idle time Per DRAM Rank (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::IDLE 532315000 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::REF 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::SREF 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::PRE_PDN 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::ACT 0 # Time in different power states (Tick)
system.mem_ctrls.dram.rank1.pwrStateTime::ACT_PDN 0 # Time in different power states (Tick)
system.mem_ctrls.power_state.pwrStateResidencyTicks::UNDEFINED 532315000 # Cumulative time (in ticks) in various power states (Tick)
system.membus.transDist::ReadResp 12732 # Transaction distribution (Count)
system.membus.transDist::WritebackDirty 2179 # Transaction distribution (Count)
system.membus.transDist::CleanEvict 11663 # Transaction distribution (Count)
system.membus.transDist::ReadExReq 2134 # Transaction distribution (Count)
system.membus.transDist::ReadExResp 2134 # Transaction distribution (Count)
system.membus.transDist::ReadSharedReq 12732 # Transaction distribution (Count)
system.membus.pktCount_system.l2.mem_side_port::system.mem_ctrls.port 43574 # Packet count per connected requestor and responder (Count)
system.membus.pktCount_system.l2.mem_side_port::total 43574 # Packet count per connected requestor and responder (Count)
system.membus.pktCount::total 43574 # Packet count per connected requestor and responder (Count)
system.membus.pktSize_system.l2.mem_side_port::system.mem_ctrls.port 272720 # Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize_system.l2.mem_side_port::total 272720 # Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize::total 272720 # Cumulative packet size per connected requestor and responder

(Byte)
system.membus.snoops 0 # Total snoops (Count)
system.membus.snoopTraffic 0 # Total snoop traffic (Byte)
system.membus.snoopFanout::samples 14866 # Request fanout histogram
system.membus.snoopFanout::mean 0 # Request fanout histogram
system.membus.snoopFanout::stdev 0 # Request fanout histogram
system.membus.snoopFanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.membus.snoopFanout::0 14866 100.00% 100.00% # Request fanout histogram
system.membus.snoopFanout::1 0 0.00% 100.00% # Request fanout histogram
system.membus.snoopFanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.membus.snoopFanout::min_value 0 # Request fanout histogram
system.membus.snoopFanout::max_value 0 # Request fanout histogram
system.membus.snoopFanout::total 14866 # Request fanout histogram
system.membus.power_state.pwrStateResidencyTicks::UNDEFINED 532315000 # Cumulative time (in ticks) in various power states (Tick)
system.membus.snoop_filter.totRequests 28708 # Total number of requests made to the snoop filter. (Count)
system.membus.snoop_filter.hitSingleRequests 13842 # Number of requests hitting in the snoop filter with a single holder of the requested data. (Count)
system.membus.snoop_filter.hitMultiRequests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)
system.membus.snoop_filter.totSnoops 0 # Total number of snoops made to the snoop filter. (Count)
system.membus.snoop_filter.hitSingleSnoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data. (Count)
system.membus.snoop_filter.hitMultiSnoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)
system.tol2bus.transDist::ReadResp 101668 # Transaction distribution (Count)
system.tol2bus.transDist::WritebackDirty 17924 # Transaction distribution (Count)
system.tol2bus.transDist::WritebackClean 73910 # Transaction distribution (Count)
system.tol2bus.transDist::CleanEvict 20747 # Transaction distribution (Count)
system.tol2bus.transDist::ReadExReq 11105 # Transaction distribution (Count)
system.tol2bus.transDist::ReadExResp 11105 # Transaction distribution (Count)
system.tol2bus.transDist::ReadCleanReq 74038 # Transaction distribution (Count)
system.tol2bus.transDist::ReadSharedReq 27630 # Transaction distribution (Count)
system.tol2bus.pktCount_system.cpu.icache.mem_side_port::system.l2.cpu_side_port 221986 # Packet count per connected requestor and responder (Count)
system.tol2bus.pktCount_system.cpu.dcache.mem_side_port::system.l2.cpu_side_port 116141 # Packet count per connected requestor and responder (Count)
system.tol2bus.pktCount::total 338127 # Packet count per connected requestor and responder (Count)
system.tol2bus.pktSize_system.cpu.icache.mem_side_port::system.l2.cpu_side_port 2367168 # Cumulative packet size per connected requestor and responder (Byte)
system.tol2bus.pktSize_system.cpu.dcache.mem_side_port::system.l2.cpu_side_port 906544 # Cumulative packet size per connected requestor and responder (Byte)
system.tol2bus.pktSize::total 3273712 # Cumulative packet size per connected requestor and responder (Byte)
system.tol2bus.snoops 14159 # Total snoops (Count)
system.tol2bus.snoopTraffic 34864 # Total snoop traffic (Byte)
system.tol2bus.snoopFanout::samples 126932 # Request fanout histogram
system.tol2bus.snoopFanout::mean 0.002497 # Request fanout histogram
system.tol2bus.snoopFanout::stdev 0.049912 # Request fanout histogram
system.tol2bus.snoopFanout::underflows 0 0.00% 0.00% # Request fanout histogram
system.tol2bus.snoopFanout::0 126615 99.75% 99.75% # Request fanout histogram
system.tol2bus.snoopFanout::1 317 0.25% 100.00% # Request fanout histogram
system.tol2bus.snoopFanout::2 0 0.00% 100.00% # Request fanout histogram
system.tol2bus.snoopFanout::3 0 0.00% 100.00% # Request fanout histogram
system.tol2bus.snoopFanout::4 0 0.00% 100.00% # Request fanout histogram
system.tol2bus.snoopFanout::overflows 0 0.00% 100.00% # Request fanout histogram
system.tol2bus.snoopFanout::min_value 0 # Request fanout histogram
system.tol2bus.snoopFanout::max_value 1 # Request fanout histogram
system.tol2bus.snoopFanout::total 126932 # Request fanout histogram
system.tol2bus.power_state.pwrStateResidencyTicks::UNDEFINED 532315000 # Cumulative time (in ticks) in various power states (Tick)
system.tol2bus.snoop_filter.totRequests 225354 # Total number of requests made to the snoop filter. (Count)
system.tol2bus.snoop_filter.hitSingleRequests 112581 # Number of requests hitting in the snoop filter with a single holder of the requested data. (Count)
system.tol2bus.snoop_filter.hitMultiRequests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)
system.tol2bus.snoop_filter.totSnoops 317 # Total number of snoops made to the snoop filter. (Count)
system.tol2bus.snoop_filter.hitSingleSnoops 317 # Number of snoops hitting in the snoop filter with a single holder of the requested data. (Count)
system.tol2bus.snoop_filter.hitMultiSnoops 0 # Number of snoops hitting in the snoop filter with multiple (>1)

holders of the requested data. (Count)
system.voltage_domain.voltage 1 # Voltage in Volts (Volt)
system.workload.inst.arm 0 # number of arm instructions executed (Count)
system.workload.inst.quiesce 0 # number of quiesce instructions executed (Count)

---------- End Simulation Statistics ----------

This is the final result.

THE END