

Report-3

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Cache file Simulate use Gem5

Now, we are implement cache.py configure for find the Hit ratio:

Command:

```
build/X86/gem5.opt -d pro configs/learning_gem5/part2/simple_cache.py --cpu-  
type=TimingSimpleCPU --caches --l1d_size=1kB --l1d_assoc=1 --cacheline_size=16 --l2cache --num-  
l2caches=1 --l2_size=16kB --l2_assoc=16 --l1i_size=2kB --l1i_assoc=1 --bench= qsort/qqc -o qsort/qqc.dat
```

Answer:

```
----- Begin Simulation Statistics -----  
simSeconds                0.005738                # Number of seconds  
simulated (Second)  
simTicks                  5737602000              # Number of ticks  
simulated (Tick)  
finalTick                 5737602000              # Number of ticks from  
beginning of simulation (restored from checkpoints and never reset) (Tick)  
simFreq                   1000000000000            # The number of ticks per  
simulated second ((Tick/Second))  
hostSeconds               0.82                   # Real time elapsed on the  
host (Second)  
hostTickRate              7001784643              # The number of ticks  
simulated per host second (ticks/s) ((Tick/Second))  
hostMemory                684724                 # Number of bytes of host  
memory used (Byte)  
simInsts                  462907                 # Number of instructions  
simulated (Count)  
simOps                    900065                 # Number of ops (including  
micro ops) simulated (Count)  
hostInstRate              564839                 # Simulator instruction rate  
(inst/s) ((Count/Second))  
hostOpRate                1098251                 # Simulator op (including  
micro ops) rate (op/s) ((Count/Second))  
system.cache.hits         708689                 # Number of hits (Count)  
system.cache.misses      95970                   # Number of misses  
(Count)  
system.cache.missLatency::samples 95970          # Ticks for misses  
to the cache
```

system.cache.missLatency::mean	51400.885693			# Ticks for
misses to the cache				
system.cache.missLatency::gmean	43617.238631			# Ticks for
misses to the cache				
system.cache.missLatency::stdev	35449.425571			# Ticks for
misses to the cache				
system.cache.missLatency::0-32767	30683	31.97%	31.97%	# Ticks for
misses to the cache				
system.cache.missLatency::32768-65535	47212	49.19%	81.17%	# Ticks
for misses to the cache				
system.cache.missLatency::65536-98303	13041	13.59%	94.75%	# Ticks
for misses to the cache				
system.cache.missLatency::98304-131071	1355	1.41%	96.17%	# Ticks
for misses to the cache				
system.cache.missLatency::131072-163839	2283	2.38%	98.55%	# Ticks
for misses to the cache				
system.cache.missLatency::163840-196607	663	0.69%	99.24%	# Ticks
for misses to the cache				
system.cache.missLatency::196608-229375	39	0.04%	99.28%	# Ticks
for misses to the cache				
system.cache.missLatency::229376-262143	54	0.06%	99.33%	# Ticks
for misses to the cache				
system.cache.missLatency::262144-294911	190	0.20%	99.53%	# Ticks
for misses to the cache				
system.cache.missLatency::294912-327679	348	0.36%	99.89%	# Ticks
for misses to the cache				
system.cache.missLatency::327680-360447	68	0.07%	99.96%	# Ticks
for misses to the cache				
system.cache.missLatency::360448-393215	6	0.01%	99.97%	# Ticks for
misses to the cache				
system.cache.missLatency::393216-425983	8	0.01%	99.98%	# Ticks for
misses to the cache				
system.cache.missLatency::425984-458751	13	0.01%	99.99%	# Ticks
for misses to the cache				
system.cache.missLatency::458752-491519	5	0.01%	100.00%	# Ticks
for misses to the cache				
system.cache.missLatency::491520-524287	2	0.00%	100.00%	# Ticks
for misses to the cache				
system.cache.missLatency::total	95970			# Ticks for misses to
the cache				
system.cache.hitRatio	0.880732			# The ratio of hits to the
total accesses to the cache (Ratio)				
system.cache.power_state.pwrStateResidencyTicks::UNDEFINED	5737602000			
# Cumulative time (in ticks) in various power states (Tick)				

system.clk_domain.clock (Tick)	1000	# Clock period in ticks
system.clk_domain.voltage_domain.voltage (Volt)	1	# Voltage in Volts
system.cpu.numCycles cycles simulated (Cycle)	5737602	# Number of cpu
system.cpu.numWorkItemsStarted items this cpu started (Count)	0	# Number of work
system.cpu.numWorkItemsCompleted items this cpu completed (Count)	0	# Number of work
system.cpu.exec_context.thread_0.numInsts instructions committed (Count)	462907	# Number of
system.cpu.exec_context.thread_0.numOps ops (including micro ops) committed (Count)	900065	# Number of
system.cpu.exec_context.thread_0.numIntAluAccesses Number of integer alu accesses (Count)	877853	#
system.cpu.exec_context.thread_0.numFpAluAccesses Number of float alu accesses (Count)	28147	#
system.cpu.exec_context.thread_0.numVecAluAccesses Number of vector alu accesses (Count)	0	#
system.cpu.exec_context.thread_0.numCallsReturns Number of times a function call or return occurred (Count)	11726	#
system.cpu.exec_context.thread_0.numCondCtrlInsts Number of instructions that are conditional controls (Count)	82335	#
system.cpu.exec_context.thread_0.numIntInsts integer instructions (Count)	877853	# Number of
system.cpu.exec_context.thread_0.numFpInsts float instructions (Count)	28147	# Number of
system.cpu.exec_context.thread_0.numVecInsts vector instructions (Count)	0	# Number of
system.cpu.exec_context.thread_0.numIntRegReads Number of times the integer registers were read (Count)	1716304	#
system.cpu.exec_context.thread_0.numIntRegWrites Number of times the integer registers were written (Count)	715525	#
system.cpu.exec_context.thread_0.numFpRegReads Number of times the floating registers were read (Count)	47559	#
system.cpu.exec_context.thread_0.numFpRegWrites Number of times the floating registers were written (Count)	23520	#
system.cpu.exec_context.thread_0.numVecRegReads Number of times the vector registers were read (Count)	0	#
system.cpu.exec_context.thread_0.numVecRegWrites Number of times the vector registers were written (Count)	0	#
system.cpu.exec_context.thread_0.numVecPredRegReads Number of times the predicate registers were read (Count)	0	#

system.cpu.exec_context.thread_0.numVecPredRegWrites	0	#
Number of times the predicate registers were written (Count)		
system.cpu.exec_context.thread_0.numCCRegReads	550042	#
Number of times the CC registers were read (Count)		
system.cpu.exec_context.thread_0.numCCRegWrites	300671	#
Number of times the CC registers were written (Count)		
system.cpu.exec_context.thread_0.numMemRefs	180060	# Number
of memory refs (Count)		
system.cpu.exec_context.thread_0.numLoadInsts	120942	# Number
of load instructions (Count)		
system.cpu.exec_context.thread_0.numStoreInsts	59118	# Number
of store instructions (Count)		
system.cpu.exec_context.thread_0.numIdleCycles	0.001000	#
Number of idle cycles (Cycle)		
system.cpu.exec_context.thread_0.numBusyCycles	5737601.999000	#
Number of busy cycles (Cycle)		
system.cpu.exec_context.thread_0.notIdleFraction	1.000000	#
Percentage of non-idle cycles (Ratio)		
system.cpu.exec_context.thread_0.idleFraction	0.000000	#
Percentage of idle cycles (Ratio)		
system.cpu.exec_context.thread_0.numBranches	104119	# Number
of branches fetched (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::No_OpClass	3655	
0.41% 0.41%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::IntAlu	695284	
77.23% 77.64%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::IntMult	641	0.07%
77.71%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::IntDiv	1759	0.20%
77.90%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::FloatAdd	939	
0.10% 78.01%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::FloatCmp	0	
0.00% 78.01%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::FloatCvt	32	
0.00% 78.01%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMult	0	
0.00% 78.01%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMultAcc	0	
0.00% 78.01%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::FloatDiv	0	0.00%
78.01%	# Class of executed instruction. (Count)	
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMisc	0	
0.00% 78.01%	# Class of executed instruction. (Count)	

system.cpu.exec_context.thread_0.statExecutedInstType::FloatSqrt	0	
0.00% 78.01% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAdd	976	
0.11% 78.12% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAddAcc	0	
0.00% 78.12% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAlu	4240	
0.47% 78.59% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdCmp	0	
0.00% 78.59% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdCvt	4622	
0.51% 79.10% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdMisc	7492	
0.83% 79.93% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdMult	0	
0.00% 79.93% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdMultAcc	0	
0.00% 79.93% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShift	481	
0.05% 79.99% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShiftAcc	0	
0.00% 79.99% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdDiv	0	0.00%
79.99% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSqrt	0	
0.00% 79.99% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatAdd	0	
0.00% 79.99% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatAlu	0	
0.00% 79.99% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatCmp	0	
0.00% 79.99% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatCvt	96	
0.01% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatDiv	10	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatMisc	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatMult	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatMultAcc	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatSqrt	0	
0.00% 80.00% # Class of executed instruction. (Count)		

system.cpu.exec_context.thread_0.statExecutedInstType::SimdReduceAdd	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdReduceAlu	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdReduceCmp	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatReduceAdd	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdFloatReduceCmp	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAes	0	0.00%
80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdAesMix	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha1Hash	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha1Hash2	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha256Hash	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdSha256Hash2	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShaSigma2	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdShaSigma3	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::SimdPredAlu	0	
0.00% 80.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::MemRead	116641	
12.96% 92.96% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::MemWrite	57015	
6.33% 99.29% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMemRead	4301	
0.48% 99.77% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::FloatMemWrite	2103	
0.23% 100.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::IprAccess	0	
0.00% 100.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::InstPrefetch	0	
0.00% 100.00% # Class of executed instruction. (Count)		
system.cpu.exec_context.thread_0.statExecutedInstType::total	900287	
# Class of executed instruction. (Count)		
system.cpu.interrupts.clk_domain.clock	16000	# Clock period in ticks (Tick)

system.cpu.mmu.dtb.rdAccesses read requests (Count)	120974	# TLB accesses on
system.cpu.mmu.dtb.wrAccesses write requests (Count)	59134	# TLB accesses on
system.cpu.mmu.dtb.rdMisses requests (Count)	162	# TLB misses on read
system.cpu.mmu.dtb.wrMisses requests (Count)	29	# TLB misses on write
system.cpu.mmu.dtb.walker.power_state.pwrStateResidencyTicks::UNDEFINED 5737602000		# Cumulative time (in ticks) in various power states (Tick)
system.cpu.mmu.itb.rdAccesses requests (Count)	0	# TLB accesses on read
system.cpu.mmu.itb.wrAccesses write requests (Count)	624670	# TLB accesses on
system.cpu.mmu.itb.rdMisses requests (Count)	0	# TLB misses on read
system.cpu.mmu.itb.wrMisses requests (Count)	188	# TLB misses on write
system.cpu.mmu.itb.walker.power_state.pwrStateResidencyTicks::UNDEFINED 5737602000		# Cumulative time (in ticks) in various power states (Tick)
system.cpu.power_state.pwrStateResidencyTicks::ON 5737602000		# Cumulative time (in ticks) in various power states (Tick)
system.cpu.thread_0.numInsts Instructions committed (Count)	0	# Number of
system.cpu.thread_0.numOps committed (Count)	0	# Number of Ops
system.cpu.thread_0.numMemRefs Memory References (Count)	0	# Number of
system.cpu.workload.numSyscalls calls (Count)	159	# Number of system
system.mem_ctrl.avgPriority_writebacks::samples 75810.00		# Average QoS priority value for accepted requests (Count)
system.mem_ctrl.avgPriority_cpu.inst::samples 36862.00		# Average QoS priority value for accepted requests (Count)
system.mem_ctrl.avgPriority_cpu.data::samples 28425.00		# Average QoS priority value for accepted requests (Count)
system.mem_ctrl.priorityMinLatency 0.000000018750		# per QoS priority minimum request to response latency (Second)
system.mem_ctrl.priorityMaxLatency 0.000087099750		# per QoS priority maximum request to response latency (Second)
system.mem_ctrl.numReadWriteTurnArounds 4662		# Number of turnarounds from READ to WRITE (Count)
system.mem_ctrl.numWriteReadTurnArounds 4662		# Number of turnarounds from WRITE to READ (Count)

system.mem_ctrl.numStayReadState times bus staying in READ state (Count)	221803	# Number of
system.mem_ctrl.numStayWriteState bus staying in WRITE state (Count)	71173	# Number of times
system.mem_ctrl.readReqs requests accepted (Count)	95970	# Number of read
system.mem_ctrl.writeReqs requests accepted (Count)	95954	# Number of write
system.mem_ctrl.readBursts read bursts, including those serviced by the write queue (Count)	95970	# Number of controller
system.mem_ctrl.writeBursts controller write bursts, including those merged in the write queue (Count)	95954	# Number of
system.mem_ctrl.servicedByWrQ controller read bursts serviced by the write queue (Count)	30683	# Number of
system.mem_ctrl.mergedWrBursts controller write bursts merged with an existing one (Count)	20144	# Number of
system.mem_ctrl.neitherReadNorWriteReqs requests that are neither read nor write (Count)	0	# Number of
system.mem_ctrl.avgRdQLen length when enqueueing ((Count/Tick))	1.00	# Average read queue
system.mem_ctrl.avgWrQLen queue length when enqueueing ((Count/Tick))	25.87	# Average write
system.mem_ctrl.numRdRetry read queue was full causing retry (Count)	0	# Number of times
system.mem_ctrl.numWrRetry write queue was full causing retry (Count)	0	# Number of times
system.mem_ctrl.readPktSize::0 (log2) (Count)	0	# Read request sizes
system.mem_ctrl.readPktSize::1 (log2) (Count)	0	# Read request sizes
system.mem_ctrl.readPktSize::2 (log2) (Count)	0	# Read request sizes
system.mem_ctrl.readPktSize::3 (log2) (Count)	0	# Read request sizes
system.mem_ctrl.readPktSize::4 (log2) (Count)	0	# Read request sizes
system.mem_ctrl.readPktSize::5 (log2) (Count)	0	# Read request sizes
system.mem_ctrl.readPktSize::6 (log2) (Count)	95970	# Read request sizes
system.mem_ctrl.writePktSize::0 (log2) (Count)	0	# Write request sizes
system.mem_ctrl.writePktSize::1 (log2) (Count)	0	# Write request sizes

system.mem_ctrl.writePktSize::2 (log2) (Count)	0	# Write request sizes
system.mem_ctrl.writePktSize::3 (log2) (Count)	0	# Write request sizes
system.mem_ctrl.writePktSize::4 (log2) (Count)	0	# Write request sizes
system.mem_ctrl.writePktSize::5 (log2) (Count)	0	# Write request sizes
system.mem_ctrl.writePktSize::6 (log2) (Count)	95954	# Write request sizes
system.mem_ctrl.rdQLenPdf::0 length does an incoming req see (Count)	65287	# What read queue
system.mem_ctrl.rdQLenPdf::1 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::2 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::3 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::4 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::5 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::6 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::7 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::8 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::9 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::10 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::11 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::12 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::13 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::14 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::15 length does an incoming req see (Count)	0	# What read queue
system.mem_ctrl.rdQLenPdf::16 length does an incoming req see (Count)	0	# What read queue

system.mem_ctrl.rdQLenPdf::17	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::18	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::19	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::20	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::21	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::22	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::23	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::24	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::25	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::26	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::27	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::28	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::29	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::30	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.rdQLenPdf::31	0	# What read queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::0	1	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::1	1	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::2	1	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::3	1	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::4	1	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::5	1	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::6	1	# What write queue
length does an incoming req see (Count)		

system.mem_ctrl.wrQLenPdf::7 length does an incoming req see (Count)	1	# What write queue
system.mem_ctrl.wrQLenPdf::8 length does an incoming req see (Count)	1	# What write queue
system.mem_ctrl.wrQLenPdf::9 length does an incoming req see (Count)	1	# What write queue
system.mem_ctrl.wrQLenPdf::10 length does an incoming req see (Count)	1	# What write queue
system.mem_ctrl.wrQLenPdf::11 length does an incoming req see (Count)	1	# What write queue
system.mem_ctrl.wrQLenPdf::12 length does an incoming req see (Count)	1	# What write queue
system.mem_ctrl.wrQLenPdf::13 length does an incoming req see (Count)	1	# What write queue
system.mem_ctrl.wrQLenPdf::14 length does an incoming req see (Count)	1	# What write queue
system.mem_ctrl.wrQLenPdf::15 length does an incoming req see (Count)	287	# What write queue
system.mem_ctrl.wrQLenPdf::16 length does an incoming req see (Count)	406	# What write queue
system.mem_ctrl.wrQLenPdf::17 length does an incoming req see (Count)	3971	# What write queue
system.mem_ctrl.wrQLenPdf::18 length does an incoming req see (Count)	4746	# What write queue
system.mem_ctrl.wrQLenPdf::19 length does an incoming req see (Count)	4777	# What write queue
system.mem_ctrl.wrQLenPdf::20 length does an incoming req see (Count)	4720	# What write queue
system.mem_ctrl.wrQLenPdf::21 length does an incoming req see (Count)	4797	# What write queue
system.mem_ctrl.wrQLenPdf::22 length does an incoming req see (Count)	5227	# What write queue
system.mem_ctrl.wrQLenPdf::23 length does an incoming req see (Count)	4873	# What write queue
system.mem_ctrl.wrQLenPdf::24 length does an incoming req see (Count)	4679	# What write queue
system.mem_ctrl.wrQLenPdf::25 length does an incoming req see (Count)	4669	# What write queue
system.mem_ctrl.wrQLenPdf::26 length does an incoming req see (Count)	4663	# What write queue
system.mem_ctrl.wrQLenPdf::27 length does an incoming req see (Count)	4662	# What write queue
system.mem_ctrl.wrQLenPdf::28 length does an incoming req see (Count)	4662	# What write queue

system.mem_ctrl.wrQLenPdf::29	4662	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::30	4662	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::31	4662	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::32	4662	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::33	7	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::34	1	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::35	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::36	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::37	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::38	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::39	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::40	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::41	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::42	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::43	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::44	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::45	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::46	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::47	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::48	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::49	0	# What write queue
length does an incoming req see (Count)		
system.mem_ctrl.wrQLenPdf::50	0	# What write queue
length does an incoming req see (Count)		

system.mem_ctrl.wrQLenPdf::51 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::52 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::53 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::54 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::55 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::56 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::57 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::58 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::59 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::60 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::61 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::62 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.wrQLenPdf::63 length does an incoming req see (Count)	0			# What write queue
system.mem_ctrl.rdPerTurnAround::samples turning the bus around for writes (Count)	4662			# Reads before
system.mem_ctrl.rdPerTurnAround::mean before turning the bus around for writes (Count)	14.003861			# Reads
system.mem_ctrl.rdPerTurnAround::gmean before turning the bus around for writes (Count)	13.794488			# Reads
system.mem_ctrl.rdPerTurnAround::stdev turning the bus around for writes (Count)	2.387118			# Reads before
system.mem_ctrl.rdPerTurnAround::2-3 before turning the bus around for writes (Count)	1	0.02%	0.02%	# Reads
system.mem_ctrl.rdPerTurnAround::4-5 before turning the bus around for writes (Count)	3	0.06%	0.09%	# Reads
system.mem_ctrl.rdPerTurnAround::6-7 before turning the bus around for writes (Count)	30	0.64%	0.73%	# Reads
system.mem_ctrl.rdPerTurnAround::8-9 before turning the bus around for writes (Count)	97	2.08%	2.81%	# Reads
system.mem_ctrl.rdPerTurnAround::10-11 before turning the bus around for writes (Count)	420	9.01%	11.82%	# Reads

system.mem_ctrl.rdPerTurnAround::12-13 before turning the bus around for writes (Count)	1332	28.57%	40.39% # Reads
system.mem_ctrl.rdPerTurnAround::14-15 before turning the bus around for writes (Count)	1690	36.25%	76.64% # Reads
system.mem_ctrl.rdPerTurnAround::16-17 before turning the bus around for writes (Count)	809	17.35%	93.99% # Reads
system.mem_ctrl.rdPerTurnAround::18-19 before turning the bus around for writes (Count)	211	4.53%	98.52% # Reads
system.mem_ctrl.rdPerTurnAround::20-21 before turning the bus around for writes (Count)	51	1.09%	99.61% # Reads
system.mem_ctrl.rdPerTurnAround::22-23 before turning the bus around for writes (Count)	15	0.32%	99.94% # Reads
system.mem_ctrl.rdPerTurnAround::24-25 before turning the bus around for writes (Count)	1	0.02%	99.96% # Reads
system.mem_ctrl.rdPerTurnAround::26-27 before turning the bus around for writes (Count)	1	0.02%	99.98% # Reads
system.mem_ctrl.rdPerTurnAround::46-47 before turning the bus around for writes (Count)	1	0.02%	100.00% # Reads
system.mem_ctrl.rdPerTurnAround::total turning the bus around for writes (Count)	4662		# Reads before
system.mem_ctrl.wrPerTurnAround::samples turning the bus around for reads (Count)	4662		# Writes before
system.mem_ctrl.wrPerTurnAround::mean before turning the bus around for reads (Count)	16.257400		# Writes
system.mem_ctrl.wrPerTurnAround::gmean before turning the bus around for reads (Count)	16.238413		# Writes
system.mem_ctrl.wrPerTurnAround::stdev before turning the bus around for reads (Count)	0.826913		# Writes
system.mem_ctrl.wrPerTurnAround::16 before turning the bus around for reads (Count)	4198	90.05%	90.05% # Writes
system.mem_ctrl.wrPerTurnAround::17 before turning the bus around for reads (Count)	48	1.03%	91.08% # Writes
system.mem_ctrl.wrPerTurnAround::18 before turning the bus around for reads (Count)	184	3.95%	95.02% # Writes
system.mem_ctrl.wrPerTurnAround::19 before turning the bus around for reads (Count)	148	3.17%	98.20% # Writes
system.mem_ctrl.wrPerTurnAround::20 before turning the bus around for reads (Count)	80	1.72%	99.91% # Writes
system.mem_ctrl.wrPerTurnAround::21 before turning the bus around for reads (Count)	4	0.09%	100.00% # Writes
system.mem_ctrl.wrPerTurnAround::total turning the bus around for reads (Count)	4662		# Writes before
system.mem_ctrl.bytesReadWrQ bytes read from write queue (Byte)	1963712		# Total number of

system.mem_ctrl.bytesReadSys	6142080	# Total read bytes
from the system interface side (Byte)		
system.mem_ctrl.bytesWrittenSys	6141056	# Total written
bytes from the system interface side (Byte)		
system.mem_ctrl.avgRdBWSys	1070496001.63970947	#
Average system read bandwidth in Byte/s ((Byte/Second))		
system.mem_ctrl.avgWrBWSys	1070317529.86700726	#
Average system write bandwidth in Byte/s ((Byte/Second))		
system.mem_ctrl.totGap	5737598000	# Total gap between
requests (Tick)		
system.mem_ctrl.avgGap	29895.16	# Average gap
between requests ((Tick/Count))		
system.mem_ctrl.requestorReadBytes::cpu.inst	2359168	# Per-
requestor bytes read from memory (Byte)		
system.mem_ctrl.requestorReadBytes::cpu.data	1819200	# Per-
requestor bytes read from memory (Byte)		
system.mem_ctrl.requestorWriteBytes::writebacks	4850688	# Per-
requestor bytes write to memory (Byte)		
system.mem_ctrl.requestorReadRate::cpu.inst	411176655.334406256676	
# Per-requestor bytes read from memory rate ((Byte/Second))		
system.mem_ctrl.requestorReadRate::cpu.data	317066258.691348791122	
# Per-requestor bytes read from memory rate ((Byte/Second))		
system.mem_ctrl.requestorWriteRate::writebacks	845420787.290578961372	
# Per-requestor bytes write to memory rate ((Byte/Second))		
system.mem_ctrl.requestorReadAccesses::cpu.inst	46855	# Per-
requestor read serviced memory accesses (Count)		
system.mem_ctrl.requestorReadAccesses::cpu.data	49115	# Per-
requestor read serviced memory accesses (Count)		
system.mem_ctrl.requestorWriteAccesses::writebacks	95954	# Per-
requestor write serviced memory accesses (Count)		
system.mem_ctrl.requestorReadTotalLat::cpu.inst	1189973250	# Per-
requestor read total memory access latency (Tick)		
system.mem_ctrl.requestorReadTotalLat::cpu.data	1018136250	# Per-
requestor read total memory access latency (Tick)		
system.mem_ctrl.requestorWriteTotalLat::writebacks	142026632000	#
Per-requestor write total memory access latency (Tick)		
system.mem_ctrl.requestorReadAvgLat::cpu.inst	25396.93	# Per-
requestor read average memory access latency ((Tick/Count))		
system.mem_ctrl.requestorReadAvgLat::cpu.data	20729.64	# Per-
requestor read average memory access latency ((Tick/Count))		
system.mem_ctrl.requestorWriteAvgLat::writebacks	1480153.32	#
Per-requestor write average memory access latency ((Tick/Count))		
system.mem_ctrl.dram.bytesRead::cpu.inst	2998720	# Number of
bytes read from this memory (Byte)		

system.mem_ctrl.dram.bytesRead::cpu.data	3143360	# Number of
bytes read from this memory (Byte)		
system.mem_ctrl.dram.bytesRead::total	6142080	# Number of
bytes read from this memory (Byte)		
system.mem_ctrl.dram.bytesInstRead::cpu.inst	2998720	# Number
of instructions bytes read from this memory (Byte)		
system.mem_ctrl.dram.bytesInstRead::total	2998720	# Number of
instructions bytes read from this memory (Byte)		
system.mem_ctrl.dram.bytesWritten::writebacks	6141056	# Number
of bytes written to this memory (Byte)		
system.mem_ctrl.dram.bytesWritten::total	6141056	# Number of
bytes written to this memory (Byte)		
system.mem_ctrl.dram.numReads::cpu.inst	46855	# Number of
read requests responded to by this memory (Count)		
system.mem_ctrl.dram.numReads::cpu.data	49115	# Number of
read requests responded to by this memory (Count)		
system.mem_ctrl.dram.numReads::total	95970	# Number of read
requests responded to by this memory (Count)		
system.mem_ctrl.dram.numWrites::writebacks	95954	# Number of
write requests responded to by this memory (Count)		
system.mem_ctrl.dram.numWrites::total	95954	# Number of
write requests responded to by this memory (Count)		
system.mem_ctrl.dram.bwRead::cpu.inst	522643432	# Total read
bandwidth from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwRead::cpu.data	547852570	# Total read
bandwidth from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwRead::total	1070496002	# Total read
bandwidth from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwInstRead::cpu.inst	522643432	# Instruction
read bandwidth from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwInstRead::total	522643432	# Instruction
read bandwidth from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwWrite::writebacks	1070317530	# Write
bandwidth from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwWrite::total	1070317530	# Write
bandwidth from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwTotal::writebacks	1070317530	# Total
bandwidth to/from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwTotal::cpu.inst	522643432	# Total
bandwidth to/from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwTotal::cpu.data	547852570	# Total
bandwidth to/from this memory ((Byte/Second))		
system.mem_ctrl.dram.bwTotal::total	2140813532	# Total
bandwidth to/from this memory ((Byte/Second))		

system.mem_ctrl.dram.readBursts DRAM read bursts (Count)	65287	# Number of
system.mem_ctrl.dram.writeBursts DRAM write bursts (Count)	75792	# Number of
system.mem_ctrl.dram.perBankRdBursts::0 bursts (Count)	8665	# Per bank write
system.mem_ctrl.dram.perBankRdBursts::1 bursts (Count)	2955	# Per bank write
system.mem_ctrl.dram.perBankRdBursts::2 bursts (Count)	525	# Per bank write
system.mem_ctrl.dram.perBankRdBursts::3 bursts (Count)	1430	# Per bank write
system.mem_ctrl.dram.perBankRdBursts::4 bursts (Count)	276	# Per bank write
system.mem_ctrl.dram.perBankRdBursts::5 bursts (Count)	1749	# Per bank write
system.mem_ctrl.dram.perBankRdBursts::6 bursts (Count)	674	# Per bank write
system.mem_ctrl.dram.perBankRdBursts::7 bursts (Count)	3972	# Per bank write
system.mem_ctrl.dram.perBankRdBursts::8 write bursts (Count)	13108	# Per bank
system.mem_ctrl.dram.perBankRdBursts::9 bursts (Count)	909	# Per bank write
system.mem_ctrl.dram.perBankRdBursts::10 write bursts (Count)	1256	# Per bank
system.mem_ctrl.dram.perBankRdBursts::11 write bursts (Count)	1339	# Per bank
system.mem_ctrl.dram.perBankRdBursts::12 write bursts (Count)	4441	# Per bank
system.mem_ctrl.dram.perBankRdBursts::13 write bursts (Count)	2849	# Per bank
system.mem_ctrl.dram.perBankRdBursts::14 write bursts (Count)	13659	# Per bank
system.mem_ctrl.dram.perBankRdBursts::15 write bursts (Count)	7480	# Per bank
system.mem_ctrl.dram.perBankWrBursts::0 write bursts (Count)	10057	# Per bank
system.mem_ctrl.dram.perBankWrBursts::1 write bursts (Count)	3163	# Per bank
system.mem_ctrl.dram.perBankWrBursts::2 bursts (Count)	549	# Per bank write
system.mem_ctrl.dram.perBankWrBursts::3 write bursts (Count)	1580	# Per bank

system.mem_ctrl.dram.perBankWrBursts::4 bursts (Count)	384	# Per bank write
system.mem_ctrl.dram.perBankWrBursts::5 write bursts (Count)	2021	# Per bank
system.mem_ctrl.dram.perBankWrBursts::6 bursts (Count)	758	# Per bank write
system.mem_ctrl.dram.perBankWrBursts::7 write bursts (Count)	4361	# Per bank
system.mem_ctrl.dram.perBankWrBursts::8 write bursts (Count)	17963	# Per bank
system.mem_ctrl.dram.perBankWrBursts::9 write bursts (Count)	1003	# Per bank
system.mem_ctrl.dram.perBankWrBursts::10 write bursts (Count)	1383	# Per bank
system.mem_ctrl.dram.perBankWrBursts::11 write bursts (Count)	1362	# Per bank
system.mem_ctrl.dram.perBankWrBursts::12 write bursts (Count)	4662	# Per bank
system.mem_ctrl.dram.perBankWrBursts::13 write bursts (Count)	3207	# Per bank
system.mem_ctrl.dram.perBankWrBursts::14 write bursts (Count)	15499	# Per bank
system.mem_ctrl.dram.perBankWrBursts::15 write bursts (Count)	7840	# Per bank
system.mem_ctrl.dram.totQLat queuing (Tick)	983978250	# Total ticks spent
system.mem_ctrl.dram.totBusLat in databus transfers (Tick)	326435000	# Total ticks spent
system.mem_ctrl.dram.totMemAccLat spent from burst creation until serviced by the DRAM (Tick)	2208109500	# Total ticks
system.mem_ctrl.dram.avgQLat queueing delay per DRAM burst ((Tick/Count))	15071.58	# Average
system.mem_ctrl.dram.avgBusLat latency per DRAM burst ((Tick/Count))	5000.00	# Average bus
system.mem_ctrl.dram.avgMemAccLat memory access latency per DRAM burst ((Tick/Count))	33821.58	# Average
system.mem_ctrl.dram.readRowHits buffer hits during reads (Count)	42474	# Number of row
system.mem_ctrl.dram.writeRowHits buffer hits during writes (Count)	68351	# Number of row
system.mem_ctrl.dram.readRowHitRate rate for reads (Ratio)	65.06	# Row buffer hit
system.mem_ctrl.dram.writeRowHitRate rate for writes (Ratio)	90.18	# Row buffer hit

system.mem_ctrl.dram.bytesPerActivate::samples	30243			# Bytes
accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::mean	298.467745			# Bytes
accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::gmean	203.358310			# Bytes
accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::stdev	270.854203			# Bytes
accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::0-127	7394	24.45%	24.45%	#
Bytes accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::128-255	8957	29.62%	54.07%	#
Bytes accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::256-383	4803	15.88%	69.95%	#
Bytes accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::384-511	3329	11.01%	80.95%	#
Bytes accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::512-639	1761	5.82%	86.78%	#
Bytes accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::640-767	1097	3.63%	90.40%	#
Bytes accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::768-895	635	2.10%	92.50%	#
Bytes accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::896-1023	390	1.29%	93.79%	#
Bytes accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::1024-1151	1877	6.21%	100.00%	
# Bytes accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesPerActivate::total	30243			# Bytes
accessed per row activation (Byte)				
system.mem_ctrl.dram.bytesRead	4178368			# Total number of
bytes read from DRAM (Byte)				
system.mem_ctrl.dram.bytesWritten	4850688			# Total number of
bytes written to DRAM (Byte)				
system.mem_ctrl.dram.avgRdBW	728.242914			# Average
DRAM read bandwidth in MiBytes/s ((Byte/Second))				
system.mem_ctrl.dram.avgWrBW	845.420787			# Average
DRAM write bandwidth in MiBytes/s ((Byte/Second))				
system.mem_ctrl.dram.peakBW	12800.00			# Theoretical peak
bandwidth in MiByte/s ((Byte/Second))				
system.mem_ctrl.dram.busUtil	12.29			# Data bus utilization
in percentage (Ratio)				
system.mem_ctrl.dram.busUtilRead	5.69			# Data bus
utilization in percentage for reads (Ratio)				
system.mem_ctrl.dram.busUtilWrite	6.60			# Data bus
utilization in percentage for writes (Ratio)				

system.mem_ctrl.dram.pageHitRate	78.56	# Row buffer hit
rate, read and write combined (Ratio)		
system.mem_ctrl.dram.power_state.pwrStateResidencyTicks::UNDEFINED		
5737602000		# Cumulative time (in ticks) in various power states (Tick)
system.mem_ctrl.dram.rank0.actEnergy	77019180	# Energy for
activate commands per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.preEnergy	40917690	# Energy for
precharge commands per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.readEnergy	144556440	# Energy for
read commands per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.writeEnergy	119397060	# Energy for
write commands per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.refreshEnergy	452375040.000000	#
Energy for refresh commands per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.actBackEnergy	2446938180	# Energy
for active background per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.preBackEnergy	142659840	# Energy
for precharge background per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.actPowerDownEnergy	0	# Energy
for active power-down per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.prePowerDownEnergy	0	# Energy
for precharge power-down per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.selfRefreshEnergy	0	# Energy for
self refresh per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.totalEnergy	3423863430	# Total energy
per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank0.averagePower	596.741187	# Core
power per rank (mW) (Watt)		
system.mem_ctrl.dram.rank0.totalIdleTime	0	# Total Idle time
Per DRAM Rank (Tick)		
system.mem_ctrl.dram.rank0.pwrStateTime::IDLE	348160500	#
Time in different power states (Tick)		
system.mem_ctrl.dram.rank0.pwrStateTime::REF	191360000	# Time
in different power states (Tick)		
system.mem_ctrl.dram.rank0.pwrStateTime::SREF	0	# Time in
different power states (Tick)		
system.mem_ctrl.dram.rank0.pwrStateTime::PRE_PDN	0	#
Time in different power states (Tick)		
system.mem_ctrl.dram.rank0.pwrStateTime::ACT	5198081500	# Time
in different power states (Tick)		
system.mem_ctrl.dram.rank0.pwrStateTime::ACT_PDN	0	#
Time in different power states (Tick)		
system.mem_ctrl.dram.rank1.actEnergy	138994380	# Energy for
activate commands per rank (pJ) (Joule)		

system.mem_ctrl.dram.rank1.preEnergy	73854495	# Energy for
precharge commands per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.readEnergy	321592740	# Energy for
read commands per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.writeEnergy	276237180	# Energy for
write commands per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.refreshEnergy	452375040.000000	#
Energy for refresh commands per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.actBackEnergy	2571144030	# Energy
for active background per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.preBackEnergy	38065440	# Energy for
precharge background per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.actPowerDownEnergy	0	# Energy
for active power-down per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.prePowerDownEnergy	0	# Energy
for precharge power-down per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.selfRefreshEnergy	0	# Energy for
self refresh per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.totalEnergy	3872263305	# Total energy
per rank (pJ) (Joule)		
system.mem_ctrl.dram.rank1.averagePower	674.892282	# Core
power per rank (mW) (Watt)		
system.mem_ctrl.dram.rank1.totalIdleTime	0	# Total Idle time
Per DRAM Rank (Tick)		
system.mem_ctrl.dram.rank1.pwrStateTime::IDLE	77377250	# Time
in different power states (Tick)		
system.mem_ctrl.dram.rank1.pwrStateTime::REF	191360000	# Time
in different power states (Tick)		
system.mem_ctrl.dram.rank1.pwrStateTime::SREF	0	# Time in
different power states (Tick)		
system.mem_ctrl.dram.rank1.pwrStateTime::PRE_PDN	0	#
Time in different power states (Tick)		
system.mem_ctrl.dram.rank1.pwrStateTime::ACT	5468864750	# Time
in different power states (Tick)		
system.mem_ctrl.dram.rank1.pwrStateTime::ACT_PDN	0	#
Time in different power states (Tick)		
system.mem_ctrl.power_state.pwrStateResidencyTicks::UNDEFINED	5737602000	
# Cumulative time (in ticks) in various power states (Tick)		
system.membus.transDist::ReadReq	95970	# Transaction
distribution (Count)		
system.membus.transDist::ReadResp	95970	# Transaction
distribution (Count)		
system.membus.transDist::WritebackDirty	95954	# Transaction
distribution (Count)		

system.membus.pktCount_system.cache.mem_side::system.mem_ctrl.port	287894	# Packet count per connected requestor and responder (Count)
system.membus.pktCount_system.cache.mem_side::total	287894	# Packet count per connected requestor and responder (Count)
system.membus.pktCount::total	287894	# Packet count per connected requestor and responder (Count)
system.membus.pktSize_system.cache.mem_side::system.mem_ctrl.port	12283136	# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize_system.cache.mem_side::total	12283136	# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize::total	12283136	# Cumulative packet size per connected requestor and responder (Byte)
system.membus.snoops	0	# Total snoops (Count)
system.membus.snoopTraffic (Byte)	0	# Total snoop traffic
system.membus.snoopFanout::samples histogram	95970	# Request fanout
system.membus.snoopFanout::mean histogram	0	# Request fanout
system.membus.snoopFanout::stdev histogram	0	# Request fanout
system.membus.snoopFanout::underflows fanout histogram	0	0.00% 0.00% # Request fanout histogram
system.membus.snoopFanout::0 fanout histogram	95970	100.00% 100.00% # Request fanout histogram
system.membus.snoopFanout::overflows fanout histogram	0	0.00% 100.00% # Request fanout histogram
system.membus.snoopFanout::min_value histogram	0	# Request fanout
system.membus.snoopFanout::max_value histogram	0	# Request fanout
system.membus.snoopFanout::total histogram	95970	# Request fanout
system.membus.power_state.pwrStateResidencyTicks::UNDEFINED	5737602000	# Cumulative time (in ticks) in various power states (Tick)
system.membus.reqLayer2.occupancy occupancy (ticks) (Tick)	575740000	# Layer
system.membus.reqLayer2.utilization (Ratio)	0.1	# Layer utilization
system.membus.respLayer0.occupancy occupancy (ticks) (Tick)	503654500	# Layer
system.membus.respLayer0.utilization (Ratio)	0.1	# Layer utilization
system.membus.snoop_filter.totRequests requests made to the snoop filter. (Count)	0	# Total number of

system.membus.snoop_filter.hitSingleRequests	0	# Number of requests hitting in the snoop filter with a single holder of the requested data. (Count)
system.membus.snoop_filter.hitMultiRequests	0	# Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)
system.membus.snoop_filter.totSnoops	0	# Total number of snoops made to the snoop filter. (Count)
system.membus.snoop_filter.hitSingleSnoops	0	# Number of snoops hitting in the snoop filter with a single holder of the requested data. (Count)
system.membus.snoop_filter.hitMultiSnoops	0	# Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data. (Count)
system.workload.inst.arm	0	# number of arm instructions executed (Count)
system.workload.inst.quiesce	0	# number of quiesce instructions executed (Count)

----- End Simulation Statistics -----