SRAM read operation

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Netlist for read:

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*source
vdd vdd 0 dc 1

*initial conditions stored for read operation
.ic v(Q)=0
.ic v(QR)=1

*data control
.ic v(bl)=1
.ic v(blb)=0

*access control
vwl wl 0 pwl(0 0 1ns 0 1.2ns 1 5ns 1)

*transistors used for latching
m1 QR Q 0 0 NMOS l=0.18u w=0.36u
m2 QR Q vdd vdd PMOS l=0.18u w=0.72u
m3 Q QR 0 0 NMOS l=0.18u w=0.36u
m4 Q QR vdd vdd PMOS l=0.18u w=0.72u

*transistors used for data access
m5 bl 1 Q 0 NMOS l=0.18u w=0.36u
m6 blb 1 QR 0 NMOS l=0.18u w=0.36u

.tran 1n 5n

.MODEL NMOS NMOS
+ LEVEL = 3
+ VTO = 0.41
+ TOX = 2.2E-09
+ NSUB = 2.0E+18
+ NFS = 6.0E+12
+ XJ = 6E-8
+ LD = 9e-9
+ UO = 390
+ VMAX = 2.2E+05
+ THETA = 0.80
+ ETA = 2.8E-03
+ KAPPA = 0.2
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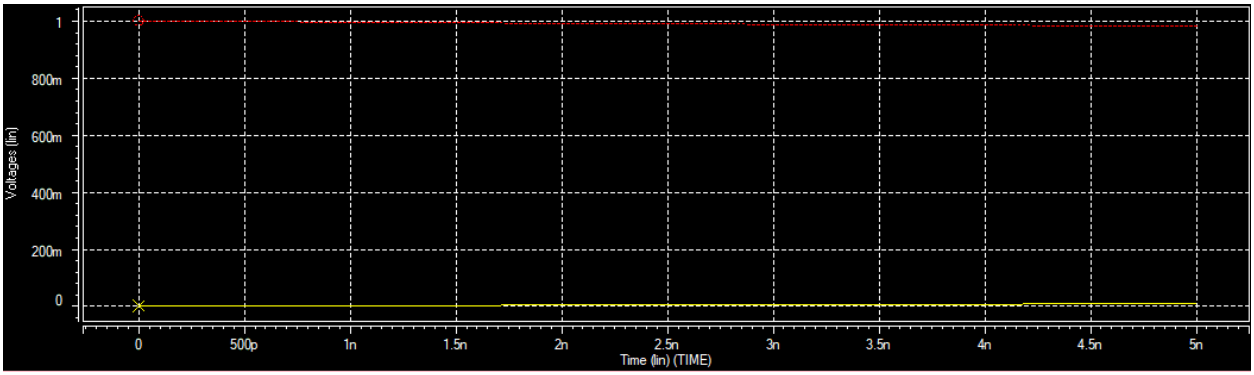
```
+ GAMMA = 0.40
+ RSH = 500
+ CGSO = 3.33449e-10
+ CGDO = 3.33449e-10
+ CGBO = 0.0
+ CJ = 4.96491e-3
+ CJSW = 2.45744e-10
.MODEL PMOS PMOS
+ LEVEL = 3
+ VTO = -0.41
+ TOX = 2.2E-09
+ NSUB = 2.0E+18
+ NFS = 6.0E+12
+ XJ = 6E-8
+ LD = 9e-9
+ UO = 175
+ VMAX = 1.1E+05
+ THETA = 0.80
+ ETA = 2.8E-03
+ KAPPA = 0.2
+ GAMMA = 0.40
+ RSH = 500
+ CGSO = 3.33449e-10
+ CGDO = 3.33449e-10
+ CGBO = 0.0
+ CJ = 4.96491e-3
+ CJSW = 2.45744e-10

*.model NMOS NMOS [kp=20u vto=0 lambda=0]
*.model PMOS PMOS [kp=20u vto=0 lambda=0]

.options POST=2
.options AUTOSTOP
.options INGOLD=2 DCON=1
.options GSHUNT=1e-12 RMIN=1e-15
.options ABSTOL=1e-5 ABSVDC=1e-4
.options RELTOL=1e-2 RELVDC=1e-2
.options NUMDGT=4 PIVOT=13
.options runlvl=6

.end
```

Result:

When bit low read 0
And when bit bar low read 1



Write 1 Red: Bit Yellow: Bit bar

Reference:

1. https://www.youtube.com/watch?v=vlHHFIrTTnA&list=PLfP-D1tg0DI2Sn1DVzGdIeGyuIUjhJ9zp&index=8