3D NoC with Inductive-Coupling Links for Building-Block SiPs

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Abstract—A wireless 3D NoC architecture is described for building-block SiPs, in which the number of hardware components (or chips) in a package can be changed after chips have been fabricated. The architecture uses inductive-coupling links that can connect more than two examined dies without wire connections. Each chip has data transceivers for the uplink and downlink in order to communicate with its neighboring chips in the package. These chips form a vertical unidirectional ring network so as to fully exploit the flexibility of the wireless approach that enables us to add, remove, and swap the chips in the ring. To avoid protocol and structural deadlocks in the ring, we use bubble flow control, which does not rely on the conventional VC-based deadlock avoidance mechanism. In addition, we propose a bidirectional communication scheme to form a bidirectional ring network by using the inductive-coupling transceivers that can dynamically change the communication modes, such as TX, RX, and Idle modes. This paper illustrates the inductive-coupling transceiver circuits, which can carry high data transfer rates of up to 8 Gbps per channel, for the wireless 3D NoC. It also illustrates an implementation of a wireless 3D NoC that has on-chip routers and transceivers implemented with a 65 nm process in order to show the feasibility of our proposal. The vertical bubble flow control and conventional VC-based approach on the uni- and bidirectional ring networks are compared with the vertical broadcast bus in terms of throughput, hardware amount, and application performance using a full system multiprocessor simulator. The results show that the proposed bidirectional communication scheme efficiently improves application performance without adding any inductive-coupling transceivers. In addition, the proposed vertical bubble flow network outperforms the conventional VC-based approach by 7.9-12.5 percent with a 33.5 percent smaller router area for building-block SiPs connecting up to eight chips.

Index Terms—Interconnection networks, network-on-chips (NoCs), 3D ICs, 3D NoCs, inductive coupling

1 Introduction

The 3D Network-on-Chip (3D NoC) [1] is an emerging research topic. Three-dimensional ICs stack several smaller wafers or dies in order to reduce the wire length and wire delay, and the 3D NoC architecture has been extensively studied in terms of its network topology [2], [3], [4], router architecture [5], [6], [7], and routing strategy [8].

Various interconnection techniques have been developed to connect multiple chips in a 3D IC package: wire-bonding, microbump [9], [10], wireless (e.g., capacitive and inductive coupling) [11], [12], [13], [14] between stacked dies, and through-silicon via (TSV) [11], [15] between stacked wafers (see Fig. 1 for details). These 3D IC technologies are compared in [11]. Many recent studies on 3D IC architectures focus on micro-bump and TSV techniques that offer the highest level of interconnect density. On the other hand, as another 3D integration technique, the inductive coupling can connect more than two examined dies without wire connections. Although power supplies are provided by bonding wires at this moment, wireless power transmission techniques using inductive coupling have been improved recently [16], [17], [18]. The inductive-coupling power transmission can be used for card-style components (or chips) inserted to a cartridge [19]. In this case, adding, removing, and swapping chips in a package after the chips have been inserted to a cartridge are possible, which will bring us a great flexibility of "field stackable systems" using the card-style components in the future.

In this paper, we propose a wireless 3D NoC architecture for building-block SiPs, in which the number of hardware components (or chips) in a package can be changed after the chips have been fabricated by virtue of inductive coupling. Since a wireless building-block SiP is a collection of various chips possibly made by different vendors (e.g., processor, memory, accelerator, and sensor), a simple and flexible network architecture would be one that enables us to customize the hardware components in a package by minimum modifications to the chips. To fully exploit the flexibility of the wireless approach, we introduce a simple vertical unidirectional ring network, in which each chip has data transceivers (or inductors) for the uplink and downlink for communicating only with its neighboring chips in the package. Furthermore, to avoid protocol and structural deadlocks in the ring network, we use bubble flow control [20], [21] that does not rely on any virtual channels (VCs);

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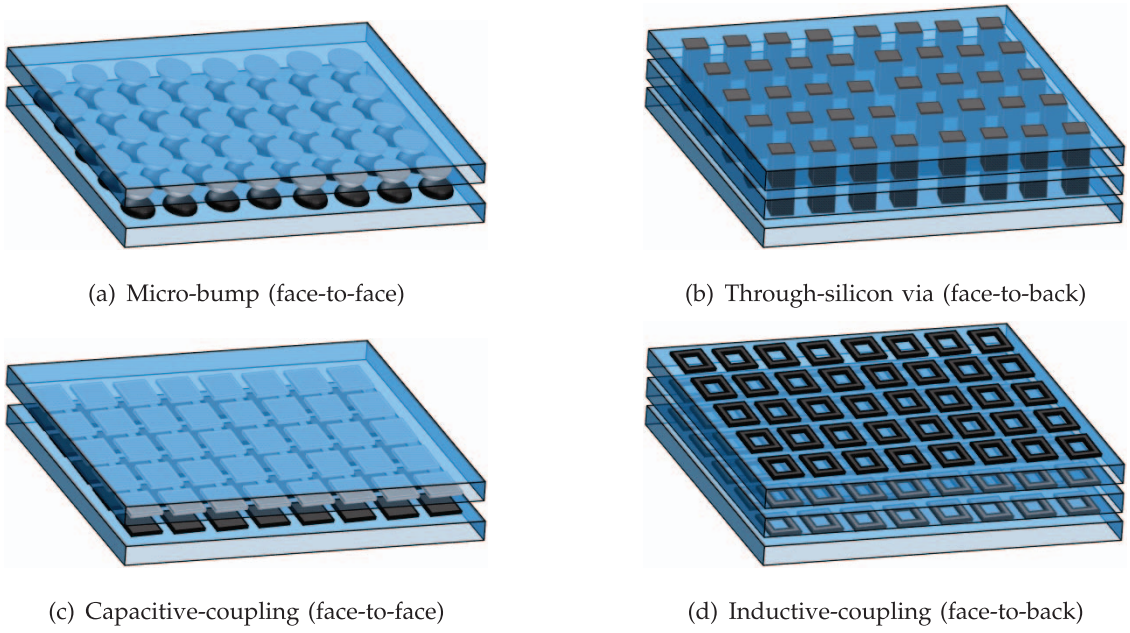


(a) Micro-bump (face-to-face)

(b) Through-silicon via (face-to-back)

(c) Capacitive-coupling (face-to-face)

(d) Inductive-coupling (face-to-back)

Fig. 1. 3D IC technologies. The wired approaches include microbump and through-silicon via. The wireless approaches include capacitive coupling and inductive coupling.

note that the conventional VC-based deadlock avoidance limits the flexibility of the building-block 3D ICs, depending on the number of VCs available on the system. In addition, we propose a bidirectional communication scheme to form a bidirectional ring network by using the inductive-coupling transceivers that can dynamically change their communication modes (i.e., TX, RX, and Idle modes) in a single cycle.

We implemented a prototype 3D IC that has on-chip routers and inductive-coupling data transceivers using a 65-nm CMOS technology. In this paper, we illustrate the transceiver circuits, which support high data transfer rates of up to 8-Gbps per channel. Furthermore, we compare the vertical bubble flow control and the conventional VC-based approach on the uni- and bidirectional ring networks with the vertical broadcast bus in terms of the throughput, hardware amount, and application performance by analyzing the results of an experiment using a full system multiprocessor simulator.

We previously proposed a unidirectional ring-based wireless 3D NoC architecture with a vertical bubble flow control [22] from the viewpoint of system-level architecture. The current paper is an extended version of our previous work, which complements the key technologies of the inductive-coupling-based 3D NoCs, i.e., the circuit-level inductor design and chip stacking issues. This paper also proposes a bidirectional communication scheme that significantly improves the application performance relative to that of the original unidirectional ring [22] without adding any inductors by dynamically changing the communication direction.

The rest of this paper is organized as follows. Section 2 overviews existing 3D IC technologies and shows advantages of the inductive coupling. Section 3 describes the uni- and bidirectional ring-based wireless 3D NoC architecture and Section 4 illustrates its test chip implementation. Section 5 shows the evaluation results and Section 6 concludes this paper.

2 Overview of 3D IC Technologies

Three-dimensional integration technologies are classified into wired and wireless approaches. This section surveys these approaches and discusses possibility of the inductive-coupling technology.

2.1 Wired 3D Interconnection

- **Wire-bonding** is a die-level interconnection that uses bonding wires. It is currently utilized for SiPs since no special process technology is required. However, the number of wires and their density are limited because only the edges of a chip can be used for the bonding. In addition, wired links in conventional board implementations take up as large area because they require long bonding wires and highly capacitive electrostatic-discharge (ESD) protection devices. As a result, it causes considerable wire delays in communications and limits the data bandwidth.
- **Microbump** [9], [10] is a die-level interconnection that uses solder balls formed on the surface of each chip (Fig. 1a). This approach is typically used for making face-to-face connections of only two dies.
- **Through-silicon via** [11], [15] is a wafer-level interconnection that uses via-holes formed through multiple wafers (Fig. 1b). More than two wafers can be connected by using a face-to-back connection. Compared with wireless coupling, the footprint of each TSV is relatively small, so a high-density implementation is possible. The wafers can be selected and stacked in a package to meet application requirements. However, the number and order

of the wafers in a package cannot be changed once the wafers have been connected in the wired approaches.

These wired approaches have been utilized in actual products. They are mature technologies and they have been extensively researched. On the other hand, wireless approaches have the potential to enable components or chips in a package to be customized to application requirements after the chip fabrication with a low cost.

2.2 Wireless 3D Interconnection

- **Capacitive-coupling** [12] is a die-level wireless interconnection between two metal plates, each of which is formed on the topmost metal layer of a chip (Fig. 1c). It can connect two dies without wire connections. However, only the face-to-face connection is allowed since its communication distance is typically shorter than the chip thickness. Thus, the number of connected chips in a package is limited to only two.
- **Inductive coupling** [11], [13], [14], [23] is a die-level wireless interconnection that uses square or hexagon coils as data transmitters (Fig. 1d). The coils can be implemented with common metal layers of the chip (Fig. 8a); thus, no special process technology is required for them. By stacking chips in a package, the communication distance between them can be reduced to the order of tens of micrometers. In addition, by increasing the number of coil turns by using metal layers, the transmission gain can be increased and the communication distance can be longer than the chip thickness. Thus, more than two examined dies can be connected by using a face-to-back connection.

Inductive coupling has potential as an interconnection technology for custom building-block SiPs, since it can stack a number of examined dies wirelessly. That is, addition, removal, and swapping of hardware components (e.g., processor and memory chips) become possible after the chips have been fabricated and stacked in a package with a low cost. Inductive-coupling techniques have improved to the extent that a contact-less interface without an ESD protection device has been shown to be able to handle bit rate of more than 1 GHz with a low-energy dissipation (0.14 pJ per bit) and a low bit-error rate ($\mathrm{BER} < 10^{-12}$) [13].

In the inductive-coupling approach, data modulated by a driver are transferred between two coils that are exactly superimposed on each other. The driver and inductor pair for sending data is called the TX channel, while the receiver and inductor pair is called the RX channel. Data multicast can be used if a TX channel is placed at the same location of multiple RX channels in different chips. On the other hand, stacked multiple TX channels at the same location cannot send the data simultaneously in order to avoid interference.

The footprint of an inductor ranges from $30\ \mathrm{um} \times 30\ \mathrm{um}$ [13], [14] to $150\ \mathrm{um} \times 150\ \mathrm{um}$ [11], depending on the communication distance (i.e., chip thickness). In addition, a number of TX and RX channels can be used in parallel in order to handle the required vertical bandwidth. A 1-Tbps inductive-coupling clock and data links have been developed by using 1,024 transceivers arranged with a pitch of 30 um [14]. Inductive coupling has already been used in various purposes, such as multicore processors [24] and dynamically reconfigurable processors [23]. Sections 3.4 and 4.2 describe the design and implementation of the inductors.

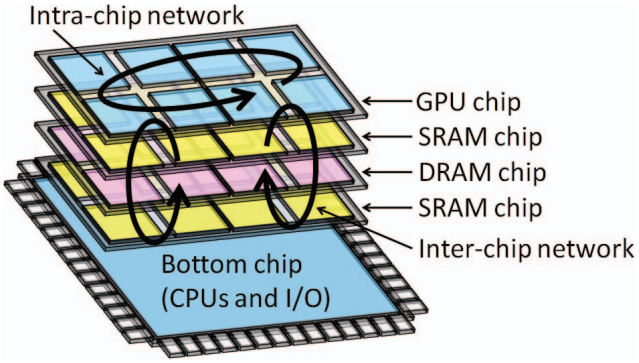


Fig. 2. Concept of building-block 3D SiP. Bottom chip has I/O and fundamental functional modules whereas additional chips are stacked on bottom chip.

3 Wireless 3D NoC for Building-Block SiPs

We apply inductive coupling to wireless building-block SiPs, in which the number and types of hardware components can be customized to the performance and cost requirements.

3.1 Building-Block SiPs

Fig. 2 illustrates the concept of the building-block SiP architecture. A powerful System-on-a-Chip (SoC) including multiple processors, accelerators, memory modules, and I/O modules is required for recent personal mobile devices. Since the required functions and performance are highly dependent on the applications of such devices, it is difficult to supply all of them with a single configuration. On the other hand, developing various chips for each product would be expensive because of the high development costs of recent process technology.

The building-block SiP enables one to customize configurations by selecting chips as required and stacking them with inductive-coupling links. As shown in Fig. 2, the bottom chip has I/O and fundamental functional modules, such as processors. Additional processors, accelerators, and memory modules are implemented on separate chips, that are connected with the bottom chip after fabrication. The balance between cost and performance can be adapted to individual products by adding, removing, and swapping chips.

A power transmission technique using inductive coupling has been researched [16], a simultaneous 6-Gbps data and 10-mW power transmission has been developed [17], and more recently a 6 W/25 mm^2 inductive power transfer has been reported [18]. However, the wireless power transmission is still a developing technology. For the inductive-coupling-based wireless 3D NoCs, we are considering the following two options, depending on the power delivery.

- In a conservative approach, power supplies are provided by bonding wires. The chips are stacked by a SiP assembly maker and cannot be changed once they have been connected. Although this approach cannot fully exploit the benefit of wireless, it can stack multiple examined chips in a lower cost than that of TSV approach that requires extra process steps for forming the TSVs.
- In an aggressive approach, inductive-coupling power transmission is assumed to be used for card-style components (or chips) inserted to a cartridge [19]. In this case, adding, removing, and swapping chips in a package after the chips have been inserted to a cartridge are possible. This is a unique property of the wireless approach.

In both the cases, flexible interconnection architecture is highly required; thus, the wireless 3D NoC architecture proposed in this paper is a key enabler for the wireless building-block SiPs. Note that each chip can have cores supplied by different vendors. Planar NoCs with various topologies and communication protocols can be used as an intrachip network. To connect such chips, interchip networks with inductive-coupling links must be flexible yet deadlock-free.

3.2 Network Design

We shall consider the intraplane[1] and interplane networks separately. Their requirements are as follows:

- **An intraplane network** connects various IP cores (e.g., processors, memory, accelerators, and sensors) on a single chip by using on-chip wires. Various types of chips can be stacked depending on the application requirements; thus, the network topology can be changed as long as each chip has data transceivers for the uplink and downlink at prespecified locations. That is, except for the data transceivers for vertical communication, some chips may have a 2D mesh-based intraplane network, while the others may not have any intraplane network. Needless to say, each intraplane network itself must be deadlock-free if it exists, because adding "deadlocked chips" will kill the whole system.
- **An interplane network** wirelessly connects the data transceivers of all intraplane networks in a package by using inductive coupling and forms a single vertical network. It should be simple enough to make it easy to add, remove, swap chips in a package. Of course, it must be deadlock-free.

A unidirectional ring network can meet the requirements for the interplane network. Moreover, it can be extended to a bidirectional ring by exploiting the bidirectional communication scheme described later.

3.2.1 Unidirectional Ring Network

The unidirectional ring network (Fig. 3) is the simplest way to add, remove, and swap nodes without having to update the routing tables of the routers. This is because

1. In the inductive coupling, "plane" and "chip" are interchangeable.

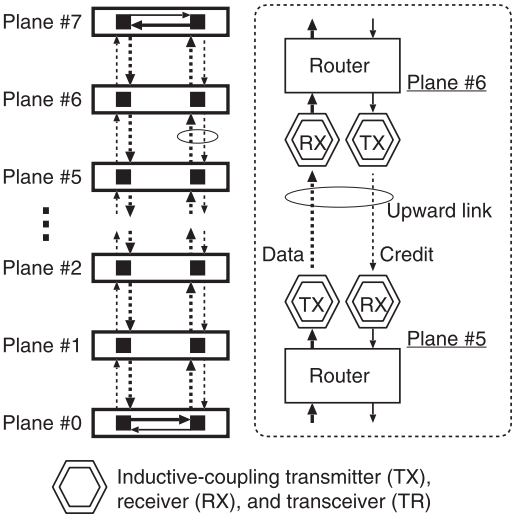


Fig. 3. Unidirectional ring network.

the routing computation of a unidirectional ring does not use any routing tables; it just forwards incoming packets to the next router or local cores if the current router is the final destination.

To form a unidirectional ring network with building-block SiPs, each chip must comply with the following simple design rules.

- **Network design rule 1.** Each chip has upward and downward inductive-coupling links, each of which consists of two opposite lines: data line and flow control (credit) line. For each link, an end-point has a data transmitter and a credit receiver while another end-point has a data receiver and a credit transmitter. These transmitters and receivers are placed at prespecified locations on each chip for enabling vertical communications between neighboring chips.
- **Network design rule 2.** All cores are connected to one of vertical links (upward or downward) on the same chip via an intraplane deadlock-free network.
- **Network design rule 3.** Only the intraplane networks for the top and bottom chips must connect their upward and downward links on the same plane; thus they must have a horizontal link.

Network design rule 3 is required in order to form a single unidirectional ring (see Planes 0 and 7 in Fig. 3). Otherwise, no such connection is needed. Note that a ring network inherently contains a cyclic dependence, which causes structural deadlocks. The router and flow control design to assure that no deadlock occurs will be discussed in Section 3.3.

3.2.2 Bidirectional Ring Network

Typically, downside of a unidirectional ring is poor scalability on throughput and communication latency. As for the throughput, the inductive-coupling link can offer ample throughput by increasing the transceivers' local clock frequency or duplicating multiple transceivers. For example, it has been reported that a 1-Tbps throughput can be achieved by using 1,024 transceivers [14]. The communication latency can be also mitigated by duplicating another

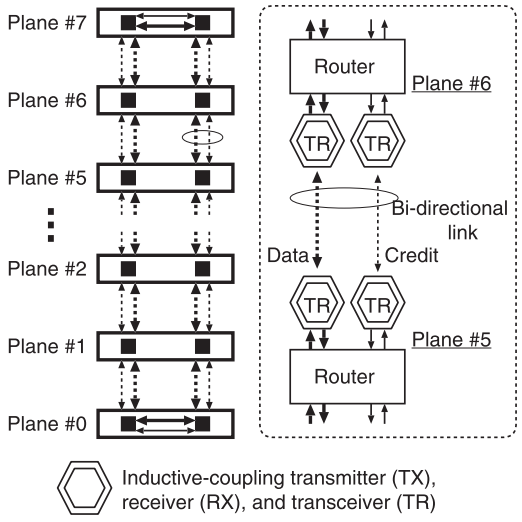


Fig. 4. Bidirectional communication scheme.

unidirectional ring to form a single bi-directional ring. However, the footprint of one inductor is not small; it can range from $30\ \text{um} \times 30\ \text{um}$ to $150\ \text{um} \times 150\ \text{um}$.

To shorten the communication latency without adding any inductors, we propose a bidirectional communication scheme that exploits the dynamic mode change capability of the inductive-coupling transceivers, as shown in Fig. 4. That is, by changing the communication direction (i.e., upward or downward) of each inductive-coupling link at runtime, the communication latency can be reduced to that of a bidirectional ring, without adding more inductors.

To support the bidirectional communication scheme, the following modifications are required for routers and inductors.

- **Routers** must have a pair of input and output ports for upward, downward, and horizontal connections, respectively. This assumption is reasonable since most on-chip routers have a pair of input and output ports for every direction. Both the input and output ports from and to the same chip (upper or lower) are connected to the same inductive-coupling transceiver (TR), as shown in Fig. 4. Either input port or output port is dynamically selected to be connected to the transceiver by a data selector.
- **Inductors** are implemented as transceivers (Fig. 4). Both end-points of an inductive-coupling link inherently use a coil to transmit data or receive data. This coil is made from metal layers fabricated with common CMOS technology, and it occupies most of the inductor area. The proposed inductor is implemented as a transceiver that shares the same coil for TX and RX. The transceiver's modes (TX, RX, and Idle modes) can be configured with a 3-bit mode signal in a single cycle.

Inductive-coupling links support bidirectional communication. Here, two end-points of a bidirectional link are called end-points A and B. If end-points A and B are configured as TX and RX, respectively, end-point A can transmit data and end-point B can receive them. Direction (or mode) of the end-points can be changed dynamically by using the credit back line which is originally used for the credit-based flow control. A mode change is accepted only when the current TX end-point does not have data but the current RX end-point has data to transmit.

Assume a router connected to end-point A has data to transmit. If end-point A is configured as TX (i.e., end-point B is configured as RX), the router can transmit the data. Otherwise, end-point A requests end-point B to be reconfigured as RX via the credit back line. After receiving the acknowledgement from end-point B via the data line, it reconfigures itself as TX. Thus, the reconfiguration takes three steps: the first step for sending a reconfiguration request to another end-point, the second step for receiving the acknowledgement, and the last step for reconfiguring the inductors. Although the reconfiguration overhead degrades network throughput, the zero-load communication latency is significantly shortened. RTL simulations of the wireless 3D NoC confirm the bidirectional communication scheme and evaluate the throughput and latency in Section 5.

3.3 Router and Flow Control Design

This section discusses the router and flow control design for a deadlock-free interplane ring network. Various deadlock-free strategies have been used for ring networks, and they are summarized as follows:

- **The VC-based approach** is a conventional deadlock avoidance technique for rings. At least two VCs (e.g., VC-0 and VC-1) are required for each message class. VC-0 is used except in the case that packets go over a wrap-around channel or dateline in the ring. VC-1 is used in that case. Thus, the cyclic dependence of a ring is cut at the dateline.
- **The bubble flow approach** [20], [21] is also a deadlock avoidance technique for rings with virtual cut-through (VCT) switching. It does not require any VCs but requires a single buffer with a capacity of at least two packets for each input port. By limiting the packet injection so as not to consume all the buffer resources in a ring, packets on the ring continuously move without any deadlocks.
- **The detection and recovery approach** [25] detects deadlocks when they occur. It recovers from the deadlock by discarding related packets or moving them to another network resources, such as escape VCs.

The detection and recovery approach requires a deadlock detection mechanism for routers. It also imposes a performance overhead for recovery. Since a simple deadlock-free mechanism is preferable for on-chip purposes, we shall focus on deadlock avoidance in this paper.

3.3.1 VC-Based Approach

Practical systems often employ sophisticated communication protocols that define multiple message classes, e.g., cache coherence protocols [26] on shared-memory CMPs, and VCs are typically assigned for a group of message classes in order to separate them into different virtual networks, balance communication workloads, and/or avoid protocol deadlocks. For the building-block SiPs, the bubble

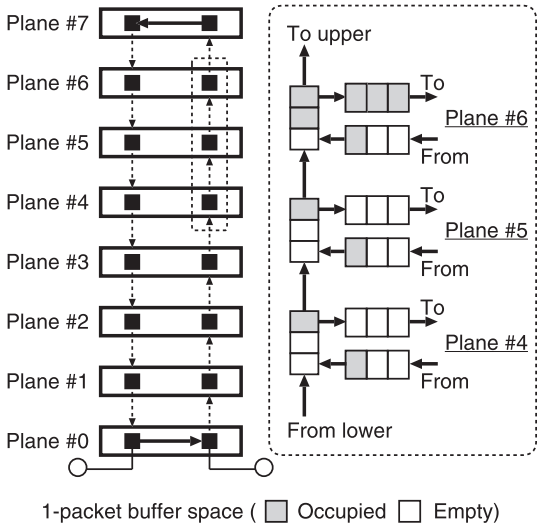


Fig. 5. Vertical bubble flow network. Each input port of routers has a buffer with capacity of three packets in this example.

flow approach is more suitable than the conventional VC-based approach.

The problem of the VC-based approach is that the communication protocol to be used would be limited, depending on the number of VCs available on chips. This is because at the design time we cannot know the numbers of VCs available on the other chips or communication protocol that will be used. For example, if one chip has only two VCs while the others have four, the system never update to a new communication protocol that requires four VCs. Such a limitation will hamper the flexibility of the building-block SiPs that can be customized after their chips have been fabricated. On the other hand, the bubble flow approach does not rely on any VCs to avoid protocol or structural deadlocks.

Another problem of the VC-based approach is the hardware complexity of additional VCs, because a group of message classes require separated VCs. In addition, to avoid structural deadlocks inside a ring, two VCs are required for each message class group. For example, a communication protocol that uses three VCs for protocol deadlock-avoidance will require six VCs in the case of ring networks. As the number of VCs increases, the router hardware complexity also increases. The VC-based approach is useful to improve the throughput if the communication workload is well balanced over all VCs.

3.3.2 *Vertical Bubble Flow*

The bubble flow control [20], [21] is applied to the interplane vertical ring network of the building-block SiPs.

Fig. 5 illustrates its behavior. In this figure, each input port of the routers has a buffer with a capacity of three packets. Each white box indicates an empty buffer with the capacity of a single packet while the gray box is an occupied one. The routers must follow the flow control rules listed below.

- **Flow control rule 1.** A packet on a ring can move to the next router along the ring when the input buffer of the next router has an empty space of at least one packet.
- **Flow control rule 2.** An intraplane network can inject a packet into a ring when the vertical input buffer of the ingress router has an empty space of at least two packets. For example, Planes 4 and 5 can inject a packet to the ring, while Plane 6 cannot.
- **Flow control rule 3.** A packet can exit from a ring only when the horizontal output buffer of the egress router has an empty space of at least one packet. Otherwise, the packet must go around the ring again (i.e., miss-routing). For example, packets destined to Planes 4 and 5 can exit from the ring, while packets destined to Plane 6 cannot exit and must go around the ring until an empty space appears in the horizontal output buffer of Plane 6.

Based on these rules, the packet injection is limited so as not to consume all the buffer resources in a ring. This guarantees that the packets can continuously move along the ring. As long as the packets are continuously moving on the ring, no deadlocks can occur even though multiple message classes coexist in the same virtual network. The reader is referred to [20] and [21] for details about the bubble flow control.

Adding these rules to the conventional VCT router is simple. To confirm this, we implemented test chips and built a vertical bubble flow network using the inductive-coupling links (see Section 4).

Note that the miss-routing, in which packets go around the ring again, significantly degrades the network performance; to reduce the amount of miss-routing, we can use routers with deep input buffers that can hold three packets. We compare the VC-based approach and vertical bubble flow control in terms of application performance on CMPs in Section 5.

3.4 Inductive-Coupling Link Design

High-speed serial data transfer is done between two coils placed at the same location of the stacked chips. Since the data transfer rate is more than 8-Gbps, the TX channel needs a dedicated clock (TX clock) for recovering data correctly. A pair of inductors, one for the data and the other for the TX clock are used, and the data transfer is synchronized with TX clock on the neighboring inductors.

Typically, the system clock used in the cores is much slower than TX clock of 4 GHz. In this case, a flit is written to a shift register in the TX channel in a single clock cycle, and the data is transferred on the inductive-coupling link synchronized with the TX clock. After the data corresponding to a flit is transferred, the shift register in the RX channel can be read out by the receiver router. That is, two clock cycles are required to transfer a flit from the transmitter router to the receiver router. The maximum size of the flit is determined by the ratio of the system clock to the TX clock.

Serialized data and the TX clock are transferred through the two inductors by using a dedicated transmitter and receiver. Circuit-level techniques around the transmitter and receiver for inductive coupling have been established in previous work [13], [14], and those for NoC design are shown in Section 4.2.

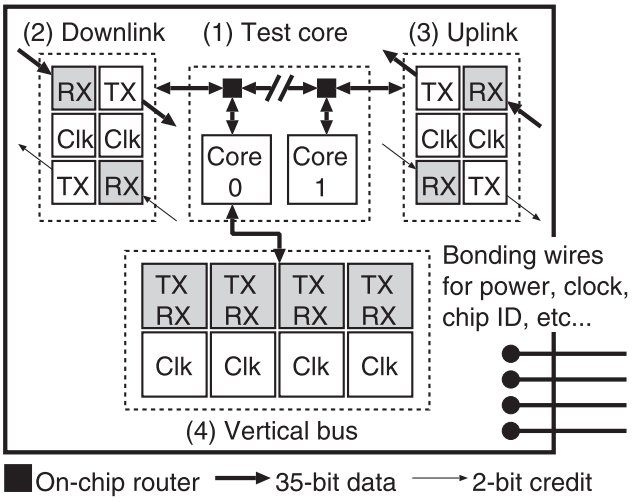


Fig. 6. Test chip architecture (top view). It consists of four parts: 1) test core, 2) downlink, 3) uplink, and 4) vertical bus parts. The Test core, downlink, and uplink are used for point-to-point stack, whereas the Test core and vertical bus are for bus-based stack.

4 Inductive-Coupling 3D NoC Implementation

To show the feasibility of our proposal, we used a 65-nm CMOS technology to make an inductive-coupling 3D NoC in which each chip had two on-chip routers and two inductive-coupling data transceivers.

The following subsections describe the system-level implementation, and the details of circuit-level implementation of the inductors.

4.1 System-Level Implementation

4.1.1 Communication Schemes

To explore possible network architectures suitable for the building-block 3D ICs, our test inductive-coupling 3D IC supports the point-to-point stack and bus-based stack. A uni-directional ring network is used for the point-to-point stack. Fig. 6 is the top view of the test chip architecture (each component is described later). Fig. 7 illustrates side views of stacks of four test chips.

For the point-to-point stack shown in Fig. 7a, each chip has a pair of data transceivers for the uplink and downlink to form a unidirectional ring network. The data transceiver for the uplink receives data from a neighboring lower chip, and transfers them to the neighboring upper chip. The downlink is used for transferring to the opposite direction of the uplink. To avoid deadlocks in the ring, we can use either the VC-based approach or the bubble flow approach.

For the bus-based stack shown in Fig. 7b, each chip uses a single data transceiver that can switch its communication modes (i.e., TX and RX modes) in a system clock cycle. All chips share the same clock counter, and an 8-cycle time-slot is assigned to each chip periodically. A chip transmits data (if any) in TX mode in its assigned time-slot. Otherwise, it listens to other chips in the RX mode.

In summary, our test inductive-coupling 3D NoC supported three communication schemes.

- Point-to-point unidirectional ring network with the bubble flow approach.
- Point-to-point unidirectional ring network with the VC-based approach.
- Vertical broadcast bus.

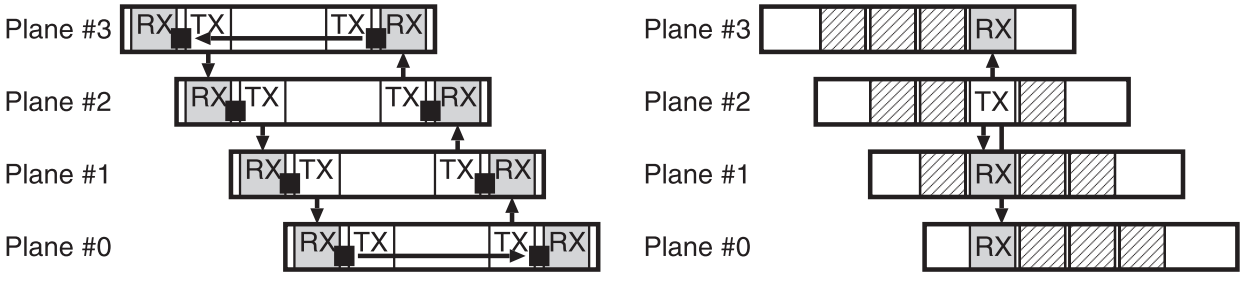
4.1.2 Test Chip Architecture

The test chip consists of four parts:

1. Test core,
2. Downlink,
3. Uplink, and
4. Vertical bus (Fig. 6).

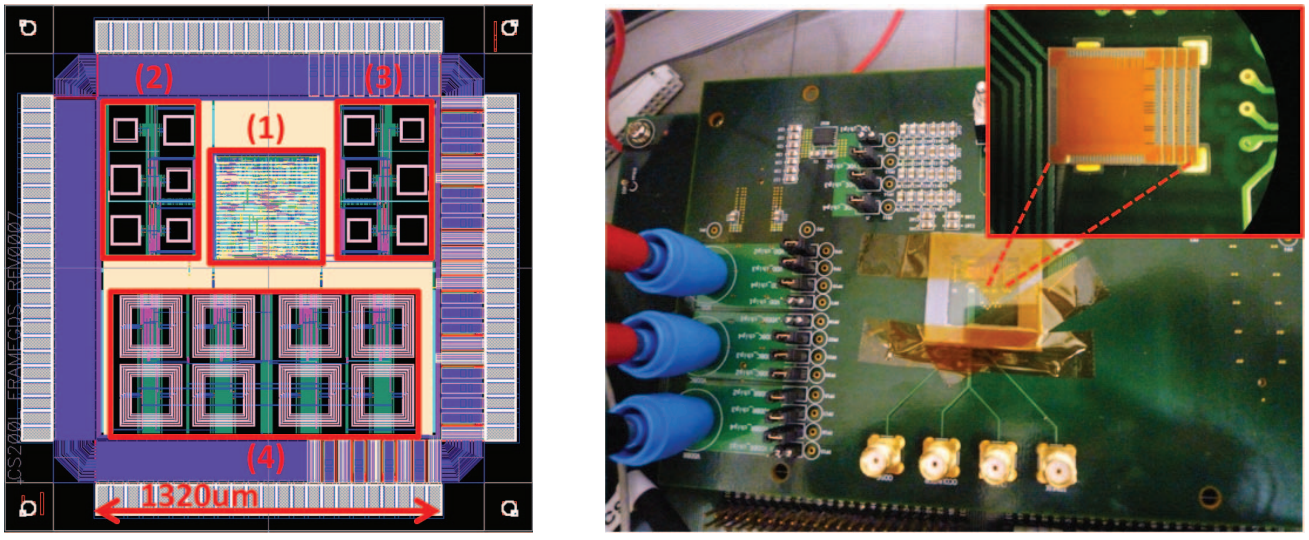
The Test core, Downlink, and Uplink are used for the point-to-point ring network, whereas the Test core and Vertical bus are for the vertical bus. Fig. 8a shows the layout of the test chip. Note the numbers in the figure correspond to those in Fig. 6. The components on the chip are summarized as follows:

1. **The Test core** consists of two cores and two routers. The core has a packet generator and a packet receiver with a 45-bit packet counter. One router is connected to Downlink data transceiver and another for the Uplink. Although every chip has an on-chip wired link that connects two routers on the chip, only the top and bottom chips actually use one unidirectional link to form an interplane vertical ring.
2. **The Downlink and Uplink** consist of two pairs of TX and RX channels, respectively. One TX and RX pair is used for 35-bit flit transfer, while the other pair is for 2-bit credit back used for the flow control. The wireless data are serially transferred at the double communication rate of the 4 GHz local clock



(a) Point-to-point stack (uni-directional ring) (b) Bus-based stack

Fig. 7. Test chip architecture (side view). The chips communicate with their adjacent (upper and lower) chips for point-to-point stack, while vertical broadcasting is used for bus-based stack. The communication mode (TX or RX) of the inductors is fixed for point-to-point unidirectional ring, while it periodically changes for vertical bus.



(a) Chip layout (b) Package and board (four chips)

Fig. 8. Prototype implementation of inductive-coupling 3D NoC.

shared by two neighboring chips. Thus, each TX channel is capable of transmitting a 35-bit flit during each 200 MHz system clock. The implementation of the inductors is shown in Section 4.2.

3. **The Vertical bus** consists of four TX/RX channels and four clock channels. The TX/RX channel works in TX mode when a time-slot is assigned to the chip, and in RX mode otherwise. As mentioned, an 8-cycle time-slot is periodically assigned to each chip for vertical broadcasting.

In the case of the vertical bus, only one TX/RX channel among four is used, and it is chosen depending on the chip ID (Fig. 7b). In Plane 0, for example, only the leftmost channel is used, while the others are not used. Obviously, this is inefficient since the other three channels are never used. In this test chip, we chose this architecture in order to implement and verify the point-to-point ring network and the vertical bus by using a single mask pattern.

4.1.3 Implementation and Stacking

The test chip was fabricated with Fujitsu 65-nm CMOS technology. Tables 1 and 2 list design parameters of the chip, such as process technology, stacking, router, and inductor. Although the inductor size can be reduced to 30 um × 30 um [13], we chose conservative design parameters instead. Note that we can duplicate the inductors for parallel transfer if a higher vertical bandwidth is required.

Fig. 8a shows the layout of the test chip. The digital part (Test core) was designed with Verilog HDL. It was synthesized with Synopsys Design Compiler and placed and routed with Synopsys IC Compiler. The inductor parts (Downlink, Uplink, and Vertical bus) were laid out manually with Cadence Virtuoso. The final GDS was verified with Mentor Graphics Calibre. Fig. 8b shows the test package that stacks four chips. The surface of the fabricated chips was polished in order to trim the chip thickness down to 40 um since the chip thickness directly affects the communication distance. Four polished chips were stacked in a package in order to verify communications on the point-to-point ring and vertical bus. As shown in Figs. 7 and 8b, each chip was shifted to the left and then stacked in order to form a point-to-point vertical link between two inductors on upper and lower chips. The shift distance depended on the location of the inductors: 210 um

TABLE 1
Chip Parameters (Process Technology)

Process technology	Fujitsu CS202SZ 65-nm
Supply voltage	Core: 1.2V, I/O: 3.3V
Chip size	2.1 mm×2.1 mm
System clock	200 MHz
Inductor clock	4 GHz (both edges)
Number of chips in SiP	4/8
Chip thickness	40 um (+ glue 10 um)
Shift distance for p2p	210 um
Shift distance for bus	290 um

TABLE 2
Chip Parameters (Router and Inductor)

Flit size	32-bit data + 3-bit control
Packet size	1-flit / 5-flit
Packet switching	Virtual cut-through
# of router ports	3
# of VCs	2 (VC-based approach)
Input VC buffer	16-flit FIFO
Inductor for p2p	150 um×150 um
Inductor for bus	250 um×250 um
Inductor data rate	35 [bit/cycle/channel]

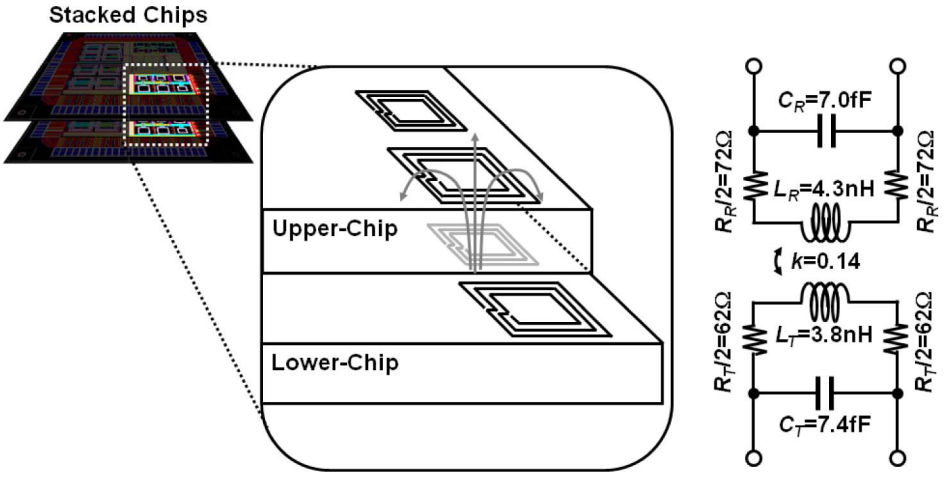


Fig. 9. Image of stacked chips and equivalent circuit of inductive-coupling channel.

for point-to-point and 290 um for bus. This "shift and stack" method makes a free contact space on the right edge of each chip, which can be used for bonding wires for the clock, power supply, chip configuration signals, probe, and debug signals.

The clock and power supplies were provided by using a few bonding wires for simplicity. Although the wireless power transmission has recently been improved [16], [17], [18], it is not still good enough for some processors. Thus, only a few cheap bonding wires (not TSVs) are used for the common power and ground lines.

4.2 Inductive-Coupling Link Implementation

4.2.1 Channel Modeling

Fig. 9 shows a simple equivalent circuit of an inductive-coupling link between stacked test chips. The inductive coupling is modeled as a transformer whose coupling strength is denoted as a coupling-coefficient, $k = M/\sqrt{L_T L_R}$ which strongly depends on the communication distance between the inductors. Parasitic elements like series resistances, R_T and R_R, and parallel capacitances, C_T and C_R, are extracted by a 3D field solver. On the basis of the equivalent circuit, the transimpedance of the inductive coupling is given by

$$\frac{V_R}{I_T} = \frac{1}{(1-\omega^2 L_R C_R) + j\omega R_R C_R} \cdot j\omega k\sqrt{L_T L_R} \cdot \frac{1}{(1-\omega^2 L_T C_T) + j\omega R_T C_T}.$$

Transmitter and receiver inductors are modeled as second-order low-pass filters which have a peak at self-resonant frequencies of $1/2\pi\sqrt{L_T C_T}$ and $1/2\pi\sqrt{L_R C_R}$, respectively. The resonant frequency of the inductive coupling, fr, is almost equal to the self-resonant frequency of the transmitter and receiver inductors. fr should be higher than $2fp$ (signal frequency) in order to suppress intersymbol interference (ISI). An frequency close to self-resonant frequency produces a ringing effect which causes ISI. The transceiver inductor is thus designed for maximizing self-inductance and keeping fr (=26 GHz) higher than $2fp$ (=16 GHz).

4.2.2 Interference Issue

ISI can also cause interference between coils. It can be avoided by placing inductors with a pitch of several tens of micrometers. The pitch of coils in the test chip is 50 um, but it could be able to reduced to 30 um. Generally, the pitch is determined by coupling-coefficient k between neighboring coils and transmitter energy. This pitch should be carefully designed, because if the coil misalignment occurs, the actual pitch is shifted from the designed value. In addition, the coupling-coefficient between TX coil and RX coil becomes weak. As a result, a signal to noise ratio (SNR) decreases as the misalignment distance increases.

Fig. 10 shows the relationship between coil misalignment distance Δx and coupling-coefficient k. The coupling-coefficient k changes linearly when the coil misalignment distance Δx increases. A magnetic coupling is characterized as a differential operator whose gain is $k\sqrt{L_T L_R}$. In an actual inductive-coupling channel, the coupling-coefficient, k would be higher than 0.1 in order to guarantee an enough gain. Fig. 10 indicates that the coupling-coefficient is 0.1 when the misalignment is 30 um. In this situation, the distance between neighboring coils is 150 um, and the coupling-coefficient is $k < 0.01$. Because the interference noise is low, a high SNR is guaranteed. The chip has a misalignment

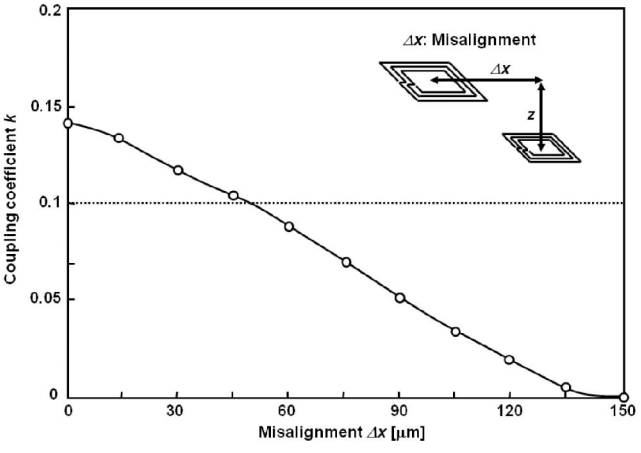


Fig. 10. Coupling-coefficient of TX and RX coils.

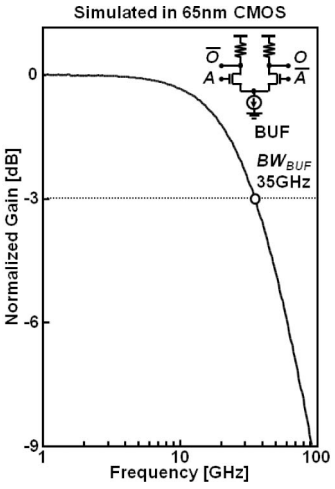


Fig. 11. Bandwidth of the CML buffer.

tolerance of ± 30 um. Details about the misalignment tolerance have been analyzed in [27].

Another problem is the interference between inductors and other digital signals. Although a 4 GHz clock is sometimes used for high-performance CPUs, the electric field from a wire segment is much weaker than the field of the inductors. Thus, the interference from digital signals is negligible even if the digital wires cross over inductors. Electrical noise coming from the power grid shared with the digital domain of the chip is the only possible interference. In the prototype chip, we used a fine grained power grid in the layout of the analog domain to avoid the noise problem. The previous paper [24] reported a practical system, in which GPUs and DRAMs are connected with inductive coupling, and the feasibility of this system has been confirmed with real 3D ICs implementation in a 65-nm CMOS technology.

4.2.3 Burst Transmission Scheme

Fig. 12 illustrates the block diagram of proposed inductive-coupling transceiver. It is based on the burst transmission scheme [28]. A transmit clock $Txclk$ is needed for the burst transmission. It is generated by a local ring oscillator whose tail current source is controlled by a tune bias voltage V_T. The free-running frequency of the local ring oscillator does not completely match the intended value, but this mismatch can be compensated by V_T. 200-Mbps 35-bit parallel data ($Mtxdata$) are multiplexed into 8-Gbps burst data ($Txdata$) and transmitted to a receiver by inductive-coupling link. The $Txclk$ provides the timing for the MUX. A clock counter generates the same number of clock waves as the number of data bits after the 200 MHz system clock ($Sysclk$) rises. This clock signal is needed for demultiplexing signals on the receiver side. In the test chip, $Txclk$ is transferred using the inductive-coupling link, but it can be eliminated by using clock and data recovery (CDR) [24]. On the receiver side, the hysteresis comparator recovers the receiver clock $Rxclk$ synchronized with the 8-Gbps received burst data ($Rxdata$). Finally, $Rxdata$ is demultiplexed by $Rxclk$ into 200-Mbps 35-bit signal ($Mrxdata$).

Since a pair of coils can provide several Gb/s data channel, many bit signals are serialized in a transmitter, communicated by a pair of coils, and deserialized in a receiver. The timing clock for a parallel-serial converter is generated by a simple ring oscillator with a counter. The timing clock and the data are both transmitted side by side, and the received timing clock is used for a serial-parallel converter in the receiver. Therefore, delay variations caused by process fluctuations and VDD changes will add in both the timing signal and the data in the same way, and they will be canceled out in the receiver. In this way, the source synchronous scheme makes simple and yet secure communications possible without an expensive PLL.

Again, Table 2 shows the performance of the inductive-coupling link. The number of bits can be increased, since the aggregated data rate can be increased. The maximum data rate of the inductive-coupling link is determined by circuit bandwidth. Fig. 11 shows a simulated bandwidth in 65-nm CMOS technology. It is higher than 30 GHz. In addition, the self-resonant frequency of the coil can be designed to be higher than 100 GHz in 65-nm CMOS. Therefore, the data rate of the inductive-coupling link can be designed to be higher than 30-Gbps per channel.

5 Evaluations

The vertical bubble flow control and the conventional VC-based approach on uni- and bidirectional ring networks were compared with the vertical broadcast bus in terms of their communication latency, throughput, application performance, and hardware amount.

5.1 Zero-Load Latency

The zero-load latency for the ring network, $T_{0,ring}$, is calculated as

$$T_{0,ring} = (H+1)T_{router} + HT_{link} + L/BW, \quad (1)$$

where H is the average hop count and L is the packet length. T_{router} and T_{link} are the latencies for transferring a header flit on a router and a link, respectively.

The zero-load latency for the vertical bus, $T_{0,bus}$, is calculated as

$$T_{0,bus} = T_{link} + L/BW + T_{slot}/N \sum_{i=0}^{N-1} i, \quad (2)$$

where N is number of stacked chips and T_{slot} is the length of each time slot. The rightmost term indicates the average waiting time to be assigned a time slot.

Here, we assume the following three traffic patterns:

- **Uniform traffic.** The source node sends packets to randomly selected destinations. Assuming each chip has two nodes, $H = N$ for a unidirectional ring while $H = N/2$ for a bidirectional ring.
- **Neighbor traffic.** The source node sends packets to the nearest destination. Thus, $H = 1$ for both cases.
- **Adversary traffic.** The source node sends packets to the farthest destination. Thus, $H = 2N - 1$ for unidirectional ring while $H = N$ for a bidirectional ring.

Table 3 shows the zero-load latencies for these traffic patterns, assuming $L = 5$, $T_{router} = 2$, $T_{link} = 1$, and $T_{slot} = 8$. The zero-load latency for the vertical bus is constant

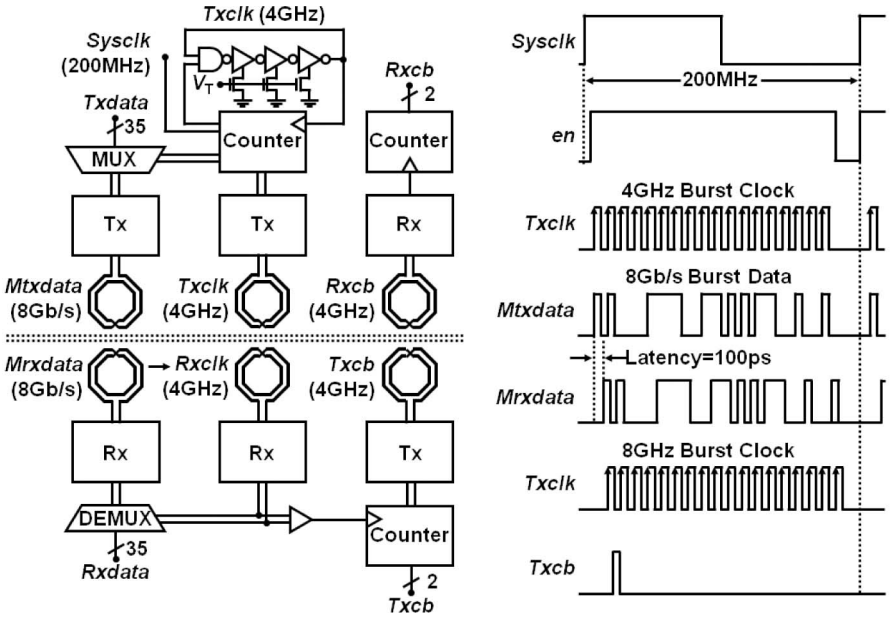


Fig. 12. Block diagram of burst transmission inductive coupling channel.

regardless of the traffic patterns. In uniform traffic, the zero-load latencies for the vertical ring and vertical bus are comparable. The results also show that the bidirectional communication scheme has a great potential to reduce the communication latency compared to the unidirectional one. This will be confirmed on latency-sensitive shared-memory CMPs in Section 5.3.

5.2 Network Throughput

We performed RTL simulations of the vertical bubble flow, the conventional VC-based approach, and the vertical bus to measure their network throughputs for uniform, neighbor, and adversary traffics on a uni- and bidirectional ring networks.

In the vertical bubble flow control, we implemented a 15-flit FIFO buffer for each input port. In the VC-based approach, two VCs are required for deadlock-freedom with a single message class. Here, 2-VC (n-flit) means each input port has two VCs, each of which has an $(n/2)$-flit FIFO buffer. The exception is 2-VC (15-flit). Because VCT switching is used for this router, 2-VC (15-flit) indicates the average throughput of the following two sub-configurations: 1) a 5-flit buffer for VC-0 and a 10-flit buffer for VC-1, and 2) a 10-flit buffer for VC-0 and a 5-flit buffer for VC-1. Notice that the buffer requirements of Bubble (15-flit) and 2-VC (15-flit) are the same.

TABLE 3
Zero-Load Latency ($N = 4, 6, 8$) [Cycle]

Topology	Traffic	$N = 4$	$N = 6$	$N = 8$
Uni-directional ring	Uniform	19	25	31
Uni-directional ring	Neighbor	10	10	10
Uni-directional ring	Adversary	28	40	52
Bi-directional ring	Uniform	13	16	19
Bi-directional ring	Neighbor	10	10	10
Bi-directional ring	Adversary	19	25	31
Vertical bus	Any	18	26	34

Figs. 13a and 13b show the network throughputs for 4-chip and 8-chip unidirectional ring networks, respectively. Bubble (15-flit) outperforms 2-VC (15-flit) and is roughly comparable to 2-VC (30-flit). Notice that the throughput of Vertical bus is quite low compared with the ring-based networks and is constant regardless of the traffic patterns.

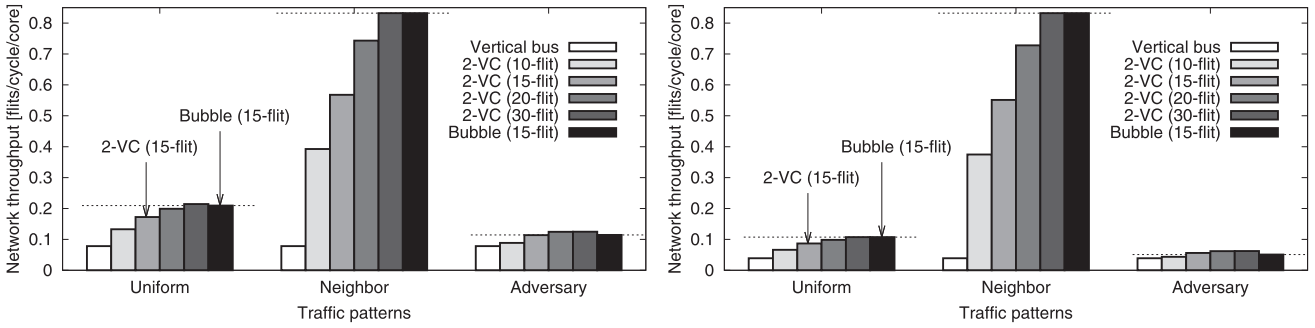
We shift to the network throughput with the bidirectional communication scheme. As proposed in Section 3.2, the bidirectional communication scheme dynamically switches communication direction of the inductive-coupling links; thus, it can shorten the communication latency without additional inductors, although it does not improve the throughput since the vertical bandwidth is equal to or less than that of unidirectional ring due to the switching overhead.

Figs. 13a and 13b show the network throughputs of 4-chip and 8-chip networks when the bidirectional communication scheme is applied. As shown, the network throughput of the bidirectional scheme is lower than that of the original unidirectional ring because of the switching overhead of the communication direction. For uniform traffic on 4-chip network, for example, throughput of Bubble (15-flit) with the bidirectional scheme is reduced by 19.1 percent compared to the unidirectional one, although it can significantly reduce the zero-load communication latency.

5.3 Application Performance

5.3.1 A Practical Building-Block SiP Example

As a practical case study of building-block SiPs, we applied inductive-coupling 3D NoC architecture to latency-sensitive shared-memory CMPs in which multiple processors (or CPUs) and shared L2 cache banks are interconnected by on-chip routers. These L2 cache banks were shared by all processors. A cache coherence protocol ran on it.



(a) $N = 4$ (uni-directional) (b) $N = 8$ (uni-directional)

Fig. 13. Network throughput with unidirectional ring ($N = 4, 8$).

Fig. 15 illustrates the target 3D CMP architecture. It consists of eight planes, each of which has on-chip routers, processors, and/or shared L2 cache banks. These planes are stacked vertically and connected by the inductive-coupling links. Memory controllers and external I/O pins are connected to the bottom chip. Three types of planes are illustrated in this figure: Type A (CPU and cache), Type B (CPU and CPU), and Type C (cache and cache). Depending on the set of target applications, the building-block SiP using the inductive-coupling links enables us to customize the number and types of planes stacked in a package after the chips have been fabricated.

5.3.2 Simulation Environment

Full system simulations of 3D CMPs stacking four and eight Type A chips were performed to measure the application performance. The vertical bubble flow, the conventional VC-based approach, and the vertical bus were compared. Tables 4 and 5 list the processor, memory, and network parameters. Each Type A chip had one processor, four shared L2 cache banks, and two on-chip routers. Two memory controllers were connected to the bottom chip, as shown in Fig. 15. The cache architecture was SNUCA [29].

To simulate the building-block 3D CMPs, we used a full-system multi-processor simulator: GEMS [30] and Wind River Simics [31]. We modified a detailed network model of GEMS, called Garnet [32], in order to accurately simulate the communication schemes on the uni- and bidirectional ring networks.

A directory-based MOESI coherence protocol that defines three message classes was used. Thus, the VC-based approach required six VCs for each input port, because each message class required two VCs for avoiding structural deadlocks. We used the default VC assignments of GEMS for this protocol.

Here, 6-VC (n-flit) means each input port has six VCs, each of which has an $(n/6)$-flit FIFO buffer. We compared 6-VC (18-flit), 6-VC (30-flit), and Bubble (15-flit). Because the packet length was up to 5-flit, 6-VC (30-flit), and Bubble (15-flit) used VCT switching, while 6-VC (18-flit) used wormhole, the buffer requirement of Bubble (15-flit) was less than that of 6-VC (18-flit).

To evaluate the application performance of these communication schemes on the building-block 3D CMPs, we used 10 parallel programs from the OpenMP implementation of the NAS Parallel Benchmarks [33]. Sun Solaris 9 operating system ran on the 4-chip and 8-chip CMPs. These benchmark programs were compiled by Sun Studio 12 and executed on Solaris 9. The number of threads was set to four or eight, depending on the number of stacked Type A chips.

5.3.3 Simulation Results

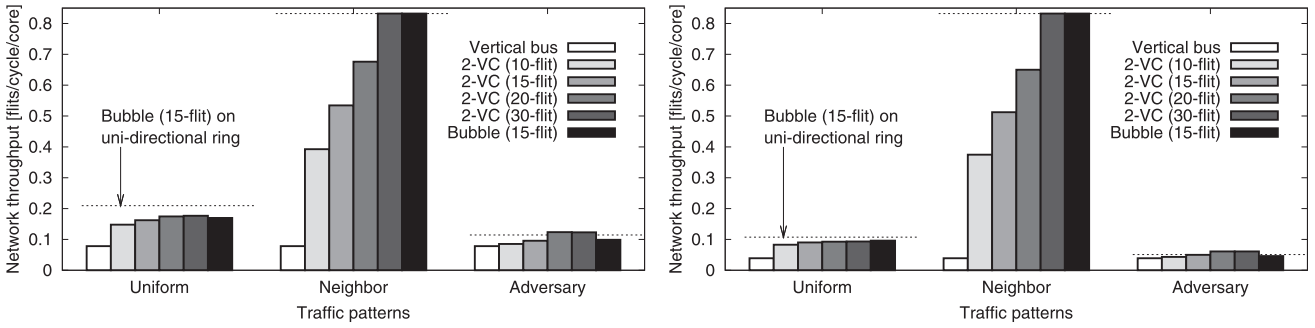
First, let us compare 6-VC (18-flit), 6-VC (30-flit), and Bubble (15-flit) on a unidirectional ring network with that

TABLE 4
Simulation Parameters (CPU and Memory)

Processor	UltraSPARC-III
L1 I/D cache size	64 KB (line:64B)
# of processors	4/8
L1 cache latency	1 cycle
L2 cache bank size	256 KB (assoc:4)
# of L2 cache banks	16/32
L2 cache latency	6 cycle
Memory size	4 GB
Memory latency	160 (± 2) cycle
# of memory controllers	2

TABLE 5
Simulation Parameters (Network)

Topology	Uni-/bi-directional rings
# of routers	8/16
Router pipeline	[RC/VSA][ST][LT]
Packet switching	Wormhole/VCT
Flit size	128 bit
	(4 inductors per channel)
Protocol	MOESI directory
# of message classes	3
Control packet size	1 flit
Data packet size	5 flit



(a) $N = 4$ (bi-directional) (b) $N = 8$ (bi-directional)

Fig. 14. Network throughput with bidirectional ring ($N = 4, 8$).

of a vertical bus in terms of application performance. The bidirectional communication scheme will be evaluated after that.

Figs. 16a and 16b show the application execution cycles of ten benchmark programs (BT, CG, DC, EP, FT, IS, LU, MG, SP, and UA) for unidirectional ring networks consisting of four and eight chips, respectively. The application execution time (Y-axis) is normalized so that the execution time using the vertical bus indicates 100 percent. As shown, Bubble (15-flit) outperforms 6-VC (18-flit) by 7.9-12.5 percent, because it uses a deep 15-flit FIFO buffer while 6-VC (18-flit) and 6-VC (30-flit) use shallow 3-flit and 5-flit FIFO buffers, respectively. Vertical bus outperforms 6-VC (18-flit) only for the 4-chip network. However, its performance falls as the number of chips stacked increases, such as the 8-chip network.

Figs. 17a and 17b show the application execution cycles on the 4- and 8-chip networks when the proposed bidirectional communication scheme is used. Again, the Y-axis is normalized so that the execution time using the vertical bus indicates 100 percent. As well as the unidirectional ring results, Bubble (15-flit) outperforms 6-VC (18-flit) by 8.6-11.6 percent. The bidirectional communication scheme does not add any inductors and does not improve the bisection bandwidth, but it significantly improves the communication latency if the bandwidth requirement is not severe, as indicated in Section 5.1. The simulation results also show that the bidirectional communication scheme significantly improves the application performance compared to the unidirectional one, especially for larger network sizes. For example, it improves the application performances of 6-VC (18-flit) and Bubble (15-flit) on the 8-chip network by 20.0 and 20.7 percent, respectively.

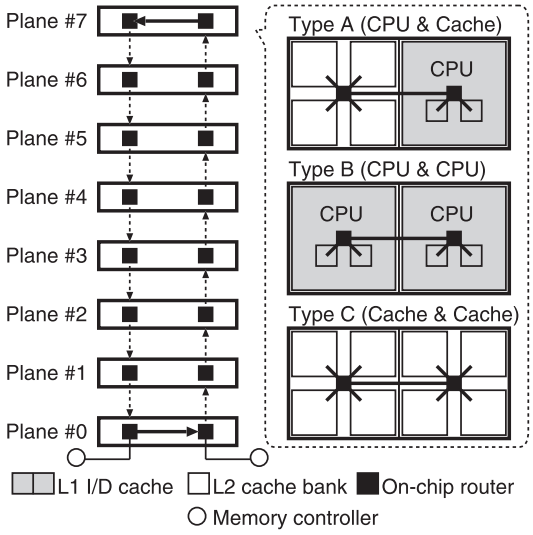


Fig. 15. Example of building-block SiP (shared-memory CMPs). Type B chips can be added for computation-bound applications while Type C is for memory-bound ones.

5.4 Router Hardware Amount

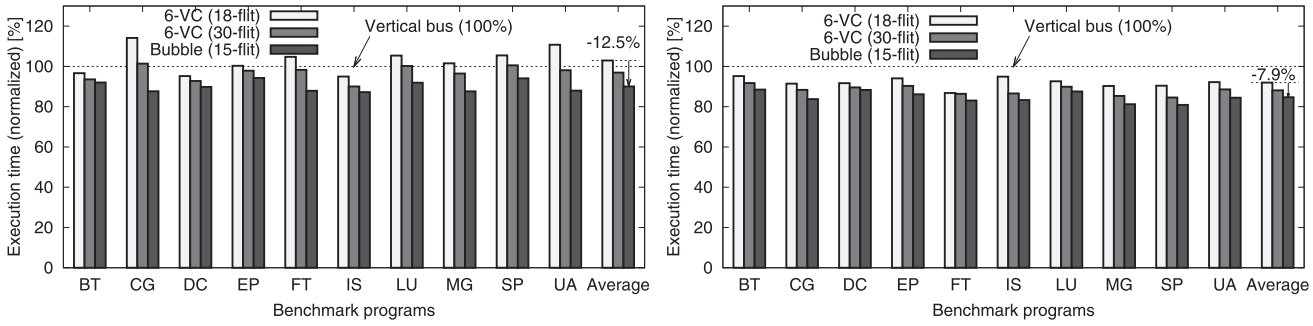
The 6-VC (18-flit), 6-VC (30-flit), and Bubble (15-flit) were compared in terms of the router hardware amount using the RTL model of the test chip.

For the unidirectional communication scheme, each router has three bidirectional ports: two bidirectional ports for a local core and another router on the same chip, and two unidirectional ports for routers on upper and lower chips, respectively, as shown in Fig. 6. For the bidirectional scheme, the router uses four bidirectional ports for the local core, horizontal link, upward link, and downward link. The flit size was set to 128 bits, although the test chip conservatively employed a 32-bit data width (Table 2). These routers were synthesized with Synopsys Design Compiler, and placed and routed with Synopsys IC Compiler. We used the same 65-nm CMOS technology for these designs.

Fig. 18 shows the gate counts of the three port routers: 6-VC (18-flit), 6-VC (30-flit), and Bubble (15-flit). As shown, the input ports consume most of the router area while the crossbar area is quite small, because the number of crossbar ports is only three in these routers. The input port area is divided into FIFO buffers and the other control circuits. Bubble (15-flit) and 6-VC (18-flit) have almost the same buffer areas. However, 6-VC (18-flit) requires more control circuits for supporting six VCs, such as the VC state controllers and VC multiplexers. As a result, Bubble (15-flit) requires a 33.5 percent less router area compared with 6-VC (18-flit). The same tendency can be observed on the four port routers used for the bidirectional communication scheme.

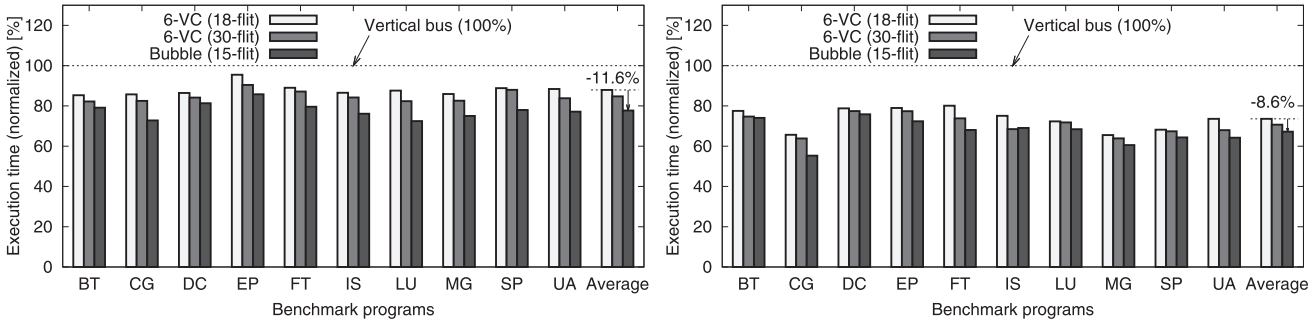
6 Conclusions

We described wireless 3D NoC architecture for the building-block SiPs, in which the number and types of



(a) $N = 4$ (uni-directional) (b) $N = 8$ (uni-directional)

Fig. 16. Application performance with unidirectional ring ($N = 4, 8$).



(a) $N = 4$ (bi-directional) (b) $N = 8$ (bi-directional)

Fig. 17. Application performance with bidirectional ring ($N = 4, 8$).

chips stacked in a package can be changed after the chips have been fabricated, by virtue of the inductive coupling. These chips can be formed into a single unidirectional ring network so as to fully exploit the flexibility of the wireless connections that enables us to add, remove, and swap chips in a package without updating any routing information. The unidirectional ring can be extended to a bidirectional ring network by using the inductive-coupling transceivers that can dynamically change their communication direction in a single cycle. We compared the vertical bubble flow control, conventional VC-based approach, and vertical bus, in terms of their latency, throughput, hardware amount, and application performance.

The results of the evaluation can be summarized as follows:

- **The vertical bus** is simple and low-latency (Table 3). However, its network throughput is quite low (Figs. 13 and 14) and its application performance is lower than the other approaches in the 8-chip network (Figs. 16b and 17b).
- **The VC-based approach** is a conventional deadlock avoidance technique for rings. However, the required number of VCs increases with the number of message classes on the network. Moreover, the network protocols are limited by the number of available VCs. This will harm the flexibility of the wireless building-block SiPs that can customize their structure for given purposes.
- **The vertical bubble flow** does not rely on any VCs; thus, the communication protocols to be used are not limited by the number of available VCs. It outperforms the VC-based approach by 7.9-12.5 percent (Figs. 16 and 17) with a 33.5 percent smaller router area (Fig. 18). However, the performance improvement decreases slightly as the number of chips increases, since the impacts of miss-routing grows with the ring size.
- **The bidirectional communication scheme** does not add any inductors and does not improve the bisection bandwidth, but it significantly improves the communication latency if the bandwidth requirement is not severe. It improves the application performances by up to 20.7 percent compared with the unidirectional ring network (Figs. 16b and 17b). Its benefit increases as the network size increases, and its communication latency is shorter than that of vertical bus for the 8-chip network.

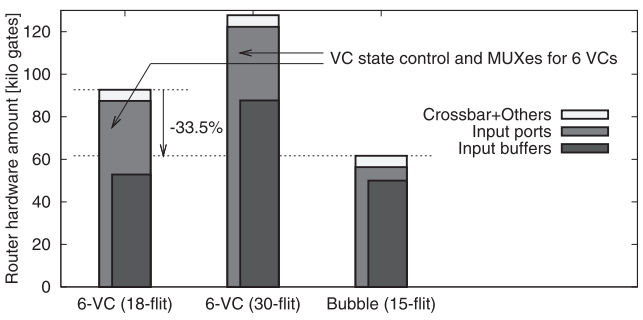


Fig. 18. Router hardware amount (3 ports).

Although current power supplies require bonding wires, inductive coupling will be available for them in the near future [16], [17], [18]. Field-stackable SiPs will be also

available so that users can extend functions and scale the performance by themselves. The above-mentioned techniques proposed in this paper will be fundamentals for such building-block SiPs.

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REFERENCES

[1] A. Sheibanyrad, F. Petrot, and A. Janstch, *3D Integration for NoC-Based SoC Architectures.* Springer, 2010.

[2] H. Matsutani, M. Koibuchi, Y. Yamada, D.F. Hsu, and H. Amano, "Fat H-Tree: A Cost-Efficient Tree-Based On-Chip Network," *IEEE Trans. Parallel and Distributed Systems,* vol. 20, no. 8, pp. 1126-1141, Aug. 2009.

[3] B. Feero and P.P. Pande, "Networks-on-Chip in a Three-Dimensional Environment: A Performance Evaluation," *IEEE Trans. Computers,* vol. 58, no. 1, pp. 32-45, Jan. 2009.

[4] V.F. Pavlidis and E.G. Friedman, "3-D Topologies for Networks-on-Chip," *IEEE Trans. Very Large Scale Integration Systems,* vol. 15, no. 10, pp. 1081-1090, Oct. 2007.

[5] J. Kim, C. Nicopoulos, D. Park, R. Das, Y. Xie, N. Vijaykrishnan, M. Yousif, and C. Das, "A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures," *Proc. Int'l Symp. Computer Architecture (ISCA '07),* pp. 138-149, 2007.

[6] F. Li, C. Nicopoulos, T. Richardson, Y. Xie, V. Narayanan, and M. Kandemir, "Design and Management of 3D Chip Multiprocessors Using Network-in-Memory," *Proc. Int'l Symp. Computer Architecture (ISCA '06),* pp. 130-141, June 2006.

[7] D. Park, S. Eachempati, R. Das, A.K. Mishra, V. Narayanan, Y. Xie, and C.R. Das, "MIRA: A Multi-Layered On-Chip Interconnect Router Architecture," *Proc. Int'l Symp. Computer Architecture (ISCA '08),* pp. 251-261, 2008.

[8] R.S. Ramanujam and B. Lin, "Randomized Partially-Minimal Routing on Three-Dimensional Mesh Networks," *IEEE Computer Architecture Letters,* vol. 7, no. 2, pp. 37-40, July-Dec. 2008.

[9] B. Black, M. Annavaram, N. Brekelbaum, J. DeVale, L. Jiang, G.H. Loh, D. McCaule, P. Morrow, D.W. Nelson, D. Pantuso, P. Reed, J. Rupley, S. Shankar, J.P. Shen, and C. Webb, "Die Stacking (3D) Microarchitecture," *Proc. Int'l Symp. Microarchitecture (MICRO '06),* pp. 469-479, Dec. 2006.

[10] K. Kumagai, C. Yang, S. Goto, T. Ikenaga, Y. Mabuchi, and K. Yoshida, "System-in-Silicon Architecture and Its Application to an H.264/AVC Motion Estimation Fort 1080HDTV," *Proc. Int'l Solid-State Circuits Conf. (ISSCC '06),* pp. 430-431, Feb. 2006.

[11] W.R. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A.M. Sule, M. Steer, and P.D. Franzon, "Demystifying 3D ICs: The Pros and Cons of Going Vertical," *IEEE Design and Test of Computers,* vol. 22, no. 6, pp. 498-510, Nov./Dec. 2005.

[12] K. Kanda, D.D. Antono, K. Ishida, H. Kawaguchi, T. Kuroda, and T. Sakurai, "1.27-Gbps/pin, 3mW/pin Wireless Superconnect (WSC) Interface Scheme," *Proc. Int'l Solid-State Circuits Conf. (ISSCC '03),* pp. 186-187, Feb. 2003.

[13] N. Miura, H. Ishikuro, T. Sakurai, and T. Kuroda, "A 0.14pJ/b Inductive-Coupling interChip Data Transceiver with Digitally-Controlled Precise Pulse Shaping," *Proc. Int'l Solid-State Circuits Conf. (ISSCC '07),* pp. 358-359, Feb. 2007.

[14] N. Miura, D. Mizoguchi, M. Inoue, K. Niitsu, Y. Nakagawa, M. Tago, M. Fukaishi, T. Sakurai, and T. Kuroda, "A 1Tb/s 3W Inductive-Coupling Transceiver for interChip Clock and Data Link," *Proc. Int'l Solid-State Circuits Conf. (ISSCC '06),* pp. 424-425, Feb. 2006.

[15] J. Burns, L. McIlrath, C. Keast, C. Lewis, A. Loomis, K. Warner, and P. Wyatt, "Three-Dimensional Integrated Circuits for Low-Power High-Bandwidth Systems on a Chip," *Proc. Int'l Solid-State Circuits Conf. (ISSCC '01),* pp. 268-269, Feb. 2001.

[16] Y. Yuan, Y. Yoshida, N. Yamagishi, and T. Kuroda, "Chip-to-Chip Power Delivery by Inductive Coupling with Ripple Canceling Scheme," *Proc. Int'l Conf. Solid State Devices and Materials (SSDM '07),* pp. 502-503, Sept. 2007.

[17] Y. Yuan, A. Radecki, N. Miura, I. Aikawa, Y. Take, H. Ishikuro, and T. Kuroda, "Simultaneous 6Gb/s Data and 10mW Power Transmission Using Nested Clover Coils for Non-Contact Memory Card," *Proc. Symp. VLSI Circuits (VLSIC '10),* pp. 199-200, June 2010.

[18] A. Radecki, H. Chung, Y. Yoshida, N. Miura, T. Shidei, H. Ishikuro, and T. Kuroda, "6W/25mm2 Inductive Power Transfer for Non-Contact Wafer-Level Testing," *Proc. Int'l Solid-State Circuits Conf. (ISSCC '12),* pp. 230-232, Feb. 2012.

[19] H. Chung, A. Radecki, N. Miura, H. Ishikuro, and T. Kuroda, "A 0.025-0.45 W 60 Percent-Efficiency Inductive-Coupling Power Transceiver with 5-Bit Dual-Frequency Feedforward Control for Non-Contact Memory Cards," *IEEE J. Solid-State Circuits,* vol. 47, no. 10, pp. 2496-2504, Oct. 2012.

[20] P. Abad, V. Puente, P. Prieto, and J.A. Gregorio, "Rotary Router: An Efficient Architecture for CMP Interconnection Networks," *Proc. Int'l Symp. Computer Architecture (ISCA '07),* pp. 116-125, May 2007.

[21] V. Puente, R. Beivide, J.A. Gregorio, J.M. Prellezo, J. Duato, and C. Izu, "Adaptive Bubble Router: A Design to Improve Performance in Torus Networks," *Proc. Int'l Conf. Parallel Processing (ICPP '99),* pp. 58-67, Sept. 1999.

[22] H. Matsutani, Y. Take, D. Sasaki, M. Kimura, Y. Ono, Y. Nishiyama, M. Koibuchi, T. Kuroda, and H. Amano, "A Vertical Bubble Flow Network Using Inductive-Coupling for 3-D CMPs," *Proc. Int'l Symp. Networks-on-Chip (NOCS '11),* pp. 49-56, May 2011.

[23] S. Saito, Y. Kohama, Y. Sugimori, Y. Hasegawa, H. Matsutani, T. Sano, K. Kasuga, Y. Yoshida, K. Niitsu, N. Miura, T. Kuroda, and H. Amano, "MuCCRA-Cube: A 3D Dynamically Reconfigurable Processor with Inductive-Coupling Link," *Proc. Field-Programmable Logic and Applications (FPL '09),* pp. 6-11, Sept. 2009.

[24] N. Miura, K. Kasuga, M. Saito, and T. Kuroda, "An 8Tb/s 1pJ/b 0.8mm2/Tb/s QDR Inductive-Coupling Interface between 65nm CMOS and 0.1um DRAM," *Proc. Int'l Solid-State Circuits Conf. (ISSCC '10),* pp. 436-437, Feb. 2010.

[25] W.J. Dally and B. Towles, *Principles and Practices of Interconnection Networks.* Morgan Kaufmann, 2004.

[26] Y. Solihin, *Fundamentals of Parallel Computer Architecture.* Solihin Publishing & Consulting LLC, 2009.

[27] K. Niitsu, Y. Kohama, Y. Sugimori, K. Kasuga, K. Osada, N. Irie, H. Ishikuro, and T. Kuroda, "Modeling and Experimental Verification of Misalignment Tolerance in Inductive-Coupling interChip Link for Low-Power 3D System Integration," *IEEE Trans. Very Large Scale Integration Systems,* vol. 18, no. 8, pp. 1238-1243, Aug. 2010.

[28] N. Miura, Y. Kohama, Y. Sugimori, H. Ishikuro, T. Sakurai, and T. Kuoda, "A High-Speed Inductive-Coupling Link with Burst Transmission," *IEEE J. Solid-State Circuits,* vol. 44, no. 3, pp. 947-955, Mar. 2009.

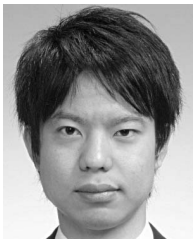
[29] C. Kim, D. Burger, and S.W. Keckler, "An Adaptive, Non-Uniform Cache Structure for Wire-Delay Dominated On-Chip Caches," *Proc. Int'l Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS '02),* pp. 211-222, Oct. 2002.

[30] M.M.K. Martin, D.J. Sorin, B.M. Beckmann, M.R. Marty, M. Xu, A.R. Alameldeen, K.E. Moore, M.D. Hill, and D.A. Wood, "Multifacet General Execution-Driven Multiprocessor Simulator (GEMS) Toolset," *ACM SIGARCH Computer Architecture News,* vol. 33, no. 4, pp. 92-99, Nov. 2005.

[31] P.S. Magnusson, M. Christensson, J. Eskilson, D. Forsgren, G. Hallberg, J. Hogberg, F. Larsson, A. Moestedt, and B. Werner, "Simics: A Full System Simulation Platform," *Computer,* vol. 35, no. 2, pp. 50-58, Feb. 2002.

[32] N. Agarwal, L.-S. Peh, and N. Jha, "Garnet: A Detailed Interconnection Network Model inside a Full-System Simulation Framework," Technical Report CE-P08-001, Princeton Univ., 2008.

[33] H. Jin, M. Frumkin, and J. Yan, "The OpenMP Implementation of NAS Parallel Benchmarks and Its Performance," Technical Report NAS-99-011, NAS, Oct. 1999.



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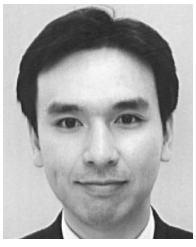

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