Intel 80286/80386/80486

	80286	80386	80486
Date	1982	1985	1989
CPU speed	6 - 25 MHz	12- 40 MHz	16 - 100 MHz
Cores	1	1	1
Registers (Programmer)	8, 15 total	16, ?	16, ?
RAM	16 MB	4 GB	4 GB
Functional Units	4	6	9
Pipeline stages	3	3	5
Cache off chip	0	Yes (support)	Yes (support)
Cache on chip	0	0	8 KB
Transistors	134,000	275,000	> 1,000,000

Specifications

i286 Features

- 16-bit registers & data bus, 24-bit address
- Addresses 1 GB of virtual memory
- MMU
- Task Management
- Protection Mechanism
- Built-in memory protection
- Operates in Real and Protected mode

i386 Features

- 32-bit registers, address, & data bus
- Backwards Compatibility with 80x86 CPUs
- Improved Protected Mode
- Paged Virtual Memory
- Virtual-86 Mode

i486 Features

- On-chip 8 KB Level 1 Cache
- Integrated FPU
- Improved MMU performance
  - Memory segmentation and paging are supported
  - Address management and memory-space protection mechanisms
- Tightly coupled pipelining
  - Fetching, decoding, address translation overlapped
  - => Single Cycle Execution

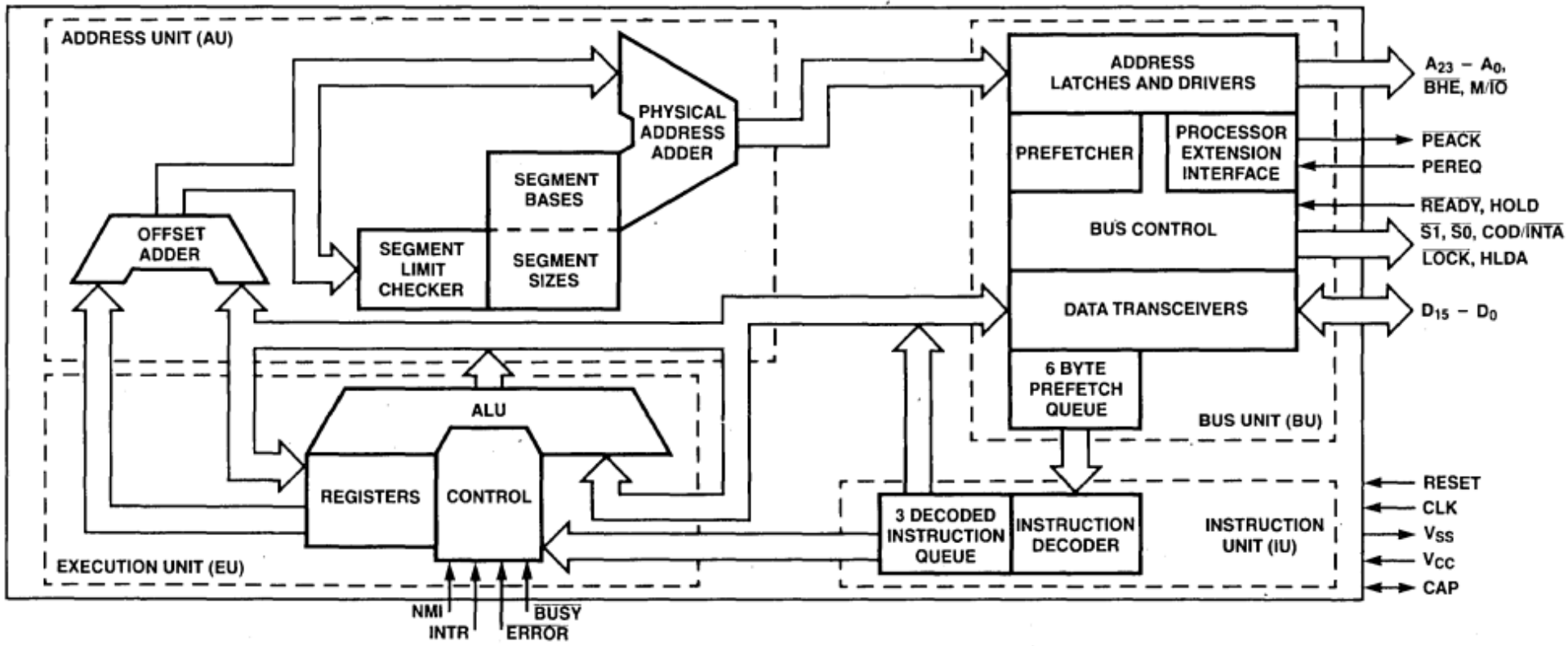
Pipeline Stages

286 and 386 Pipeline stages

- Fetch
- Decode
- Execute

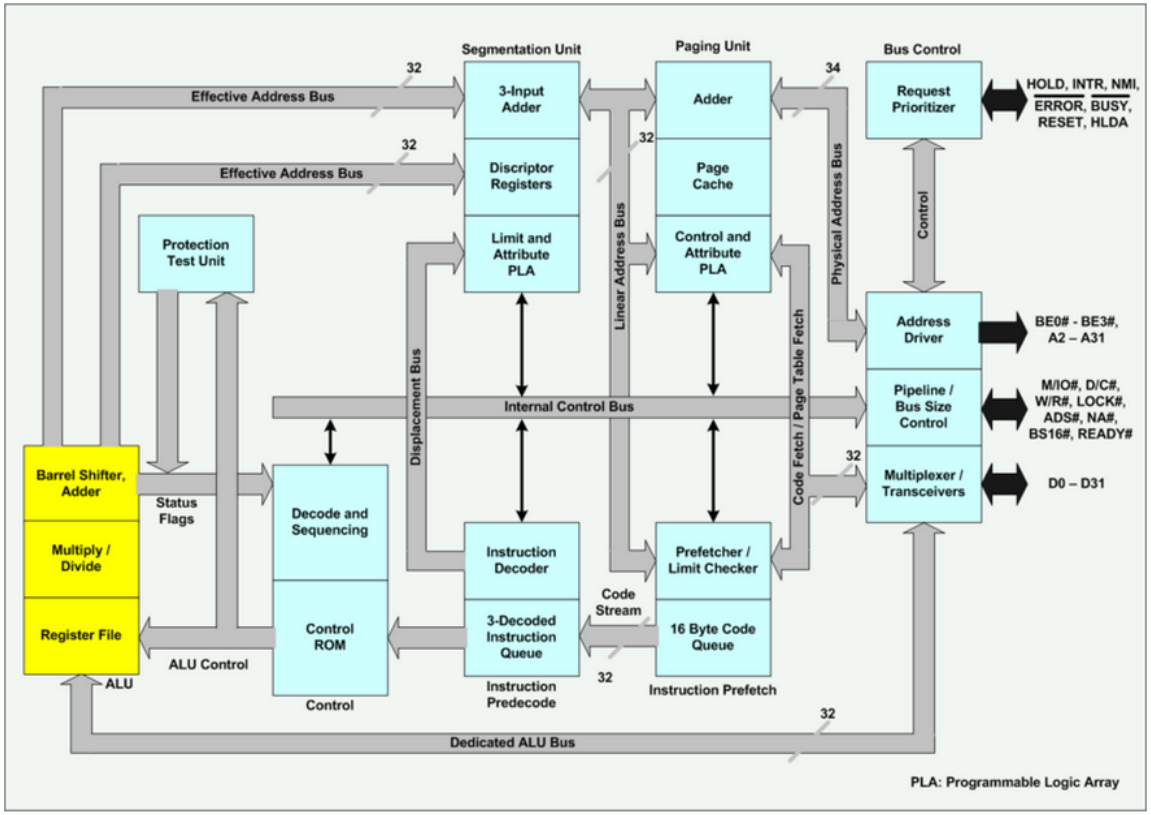
486 Pipeline stages

- Fetch:
  - Load 16 bytes of instructions into prefetch buffer
- Decode1:
  - Determine instruction length
  - Determine instruction type
- Decode2:
  - compute memory address
  - generate immediate operands
- Execute
  - Read register operands
  - Compute ALU function
  - Read/write memory
- Write-Back
  - Update register file



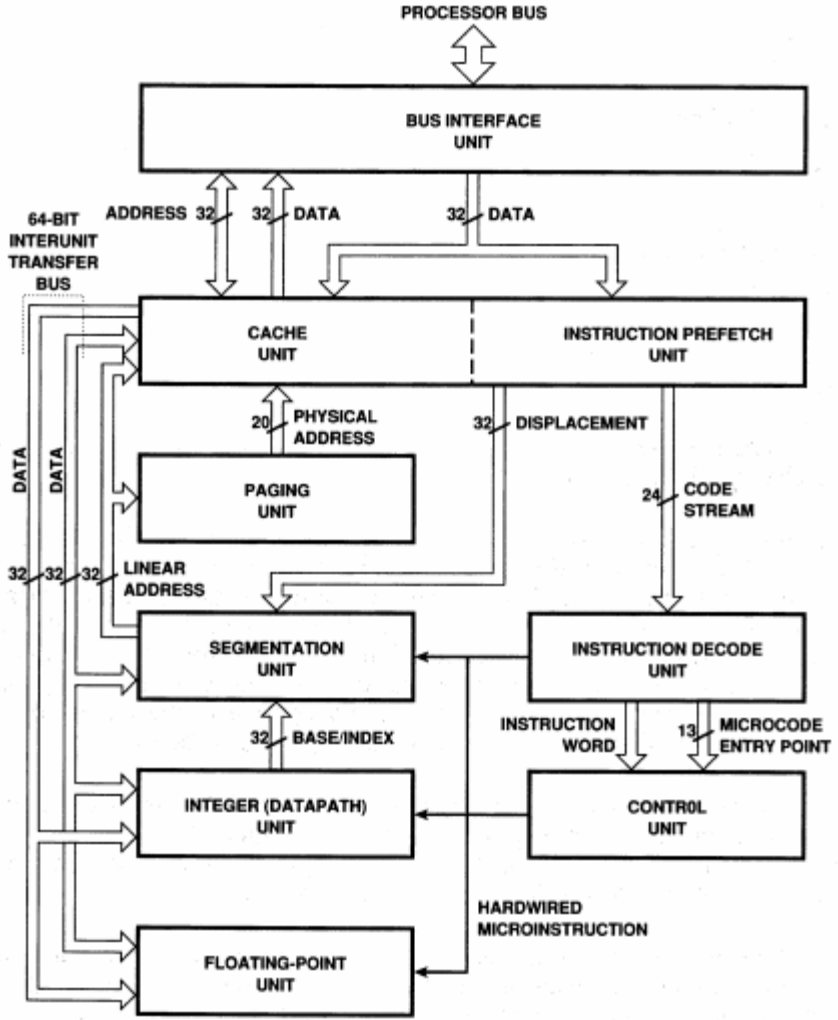
i286 - Internal Block Diagram

- Code Prefetch Unit *Half IU
  - Program look ahead func.
  - 16-byte Code Queue
- Instruction Decode Unit *Half IU
  - Takes from Prefetch Queue
  - Translates instructions into microcode
  - Stores in 3-deep instruction queue for EU
- Segmentation Unit *AU
  - Translates logical address into linear addresses
  - Checks for bus-cycle segmentation violations
  - Linear addr. -> Paging unit
- Paging Unit * NEW
  - Translates linear addr. to physical addr.

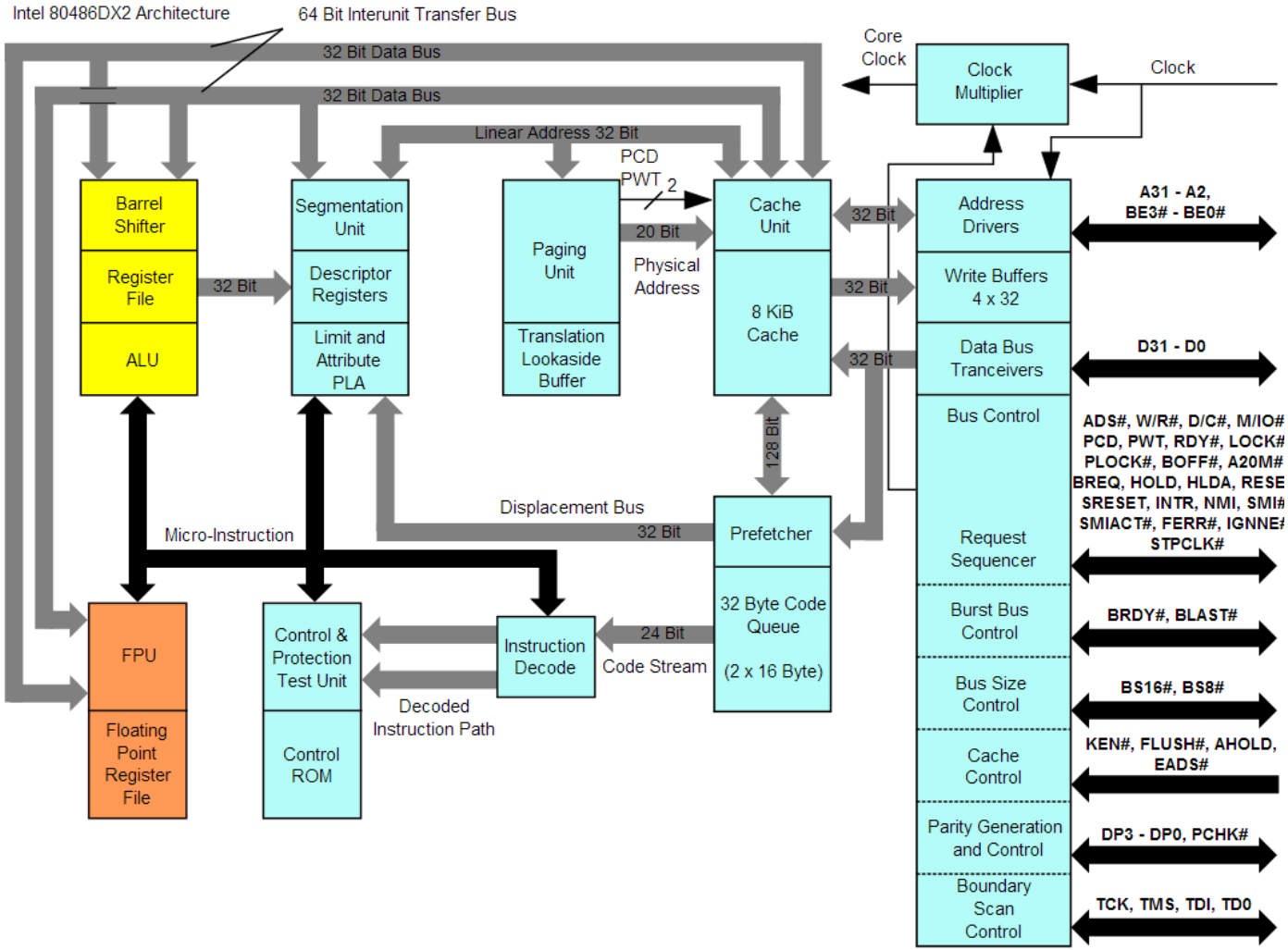


i386 - Block Diagram

- Cache Unit *NEW
  - 4-way set associative
  - Closely coupled with IPU
- Control Unit *Half EU
  - Interprets instructions from IDU
  - Controls IU, FPU, SU
- Integer (datapath) Unit *Half EU
  - Identifies where data is
  - Performs arithmetic & logic operations, in 386 instruction set
- Floating-point Unit *NEW



i486 - Internal Architecture


Intel 80486DX2 Architecture
64 Bit Interunit Transfer Bus
32 Bit Data Bus
32 Bit Data Bus
Core Clock
Clock Multiplier
Clock
Linear Address 32 Bit
PCD
PWT
2
Barrel Shifter
Register File
ALU
32 Bit
Segmentation Unit
Descriptor Registers
Limit and Attribute PLA
Paging Unit
Translation Lookaside Buffer
20 Bit
Physical Address
Cache Unit
8 KiB Cache
32 Bit
32 Bit
32 Bit
Address Drivers
Write Buffers 4 x 32
Data Bus Tranceivers
A31 - A2,
BE3# - BE0#
D31 - D0
Bus Control
ADS#, W/R#, D/C#, M/IO#
PCD, PWT, RDY#, LOCK#
PLOCK#, BOFF#, A20M#
BREQ, HOLD, HLDA, RESE
SRESET, INTR, NMI, SMI#
SMIACT#, FERR#, IGNNE#
STPCLK#
Request Sequencer
Burst Bus Control
BRDY#, BLAST#
Bus Size Control
BS16#, BS8#
Cache Control
KEN#, FLUSH#, AHOLD,
EADS#
Parity Generation and Control
DP3 - DP0, PCHK#
Boundary Scan Control
TCK, TMS, TDI, TD0
128 Bit
Displacement Bus
32 Bit
Prefetcher
Micro-Instruction
32 Byte Code Queue
(2 x 16 Byte)
24 Bit
Code Stream
Instruction Decode
Control & Protection Test Unit
Decoded Instruction Path
Control ROM
FPU
Floating Point Register File

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Questions?