A. INTRODUCTION

A.1. **Problem to be addressed:** Since the initial development of Positron Emission Tomography (PET) in the 1970's, a centralized coincidence processor (CCP) with single-thread data processing has been applied for PET online coincidence events selection and data acquisition [1]. Many current commercial and research PET scanners still use CCP. CCP has the technical advantages of a highly integrated circuit, a compact signal connection between the detector front-end and system electronics, and a centralized event selection and decision making. On the other hand, because of its single processor, CCP has several technical drawbacks that include *signal processing delay*, *loss of coincidence events at high count-rates of singles and coincidence events*, and *an algorithm that is too complicated for many research groups to implement* without extensive expertise and resource. These drawbacks are exacerbated when implementing an online CCP on a field-programmable-gate-array (FPGA), a critical component of system electronics in almost all modern PET scanners, because a complex single-thread processing leads to routing congestions of wires and interconnections and increases signal processing delay [2-6]. Therefore, these drawbacks of CCPs could severely limit the overall imaging performance and future technology development of PET. For example:

- There is a strong interest in and trend toward developing and applying a large axial field-of-view (FOV) human PET (i.e. total-body human PET) to explore new innovations in biomedical imaging, as well as therapy and drug development, given the unique advantages of a large FOV and ultrahigh sensitivity [7]. One serious problem is that, at the individual detector level, the count-rate of singles events is normal, but at the system level, it is challenging for CCP to process at a high enough rate for all incoming singles events from a large number of detectors. This could lead to severe data loss of coincidence events during the online PET data acquisition [8].
- For fast dynamic or real-time imaging applications that requires several image frames per second, such as tracking a moving tumor for motion-compensated precision radiotherapy, even a moderate number (~100s) of coincidence detector pairs could make it difficult for CCP to meet the fast imaging requirement of less than a 0.2 to 0.4 sec coincidence data acquisition and processing time per frame [9].
- Except for commercial companies, it is rather challenging for small to large research groups in the PET instrumentation research field to implement an online CCP for a human brain or animal imaging PET, let alone a larger scanner.

Therefore, **there is a strong need to develop a new CP technology** beyond the current CCP to provide ***adequate online coincidence data acquisition*** to improve the above advanced PET imaging capability and performance and to enable ***an easy CP implementation*** to accelerate the development of new PET systems.

A.2. **Current research efforts to address the problem**:

1) Non-centralized CP: Commercial companies used multiple coincidence processors to circumvent the problem. For example, a circular topology of electronics and data processing was implemented that uses a coincidence processor at each detector event processing level to compare the timing difference between the singles events from two detectors [10, 11]. Singles events are stored and transferred among detectors in a loop pattern for coincidence processing. This "daisy-chain" based ring data processing and transmission topology provides a flexible and high-speed coincidence data processing. However, the technology remains proprietary and is also complicated and difficult for most academic groups to implement. For example, it uses a multiple-gigabit transmission interface on each detector for massive data routing.

2) Mixed FPGA and on-board CPU coincidence processing: FPGA is particularly suited for well-defined parallel data processes and computations but inefficient for flexible multi-functional operations and processing controls, while CPU is the opposite: it is well suited for flexible multi-functional operations and processing controls but not designed for many parallel processes. One approach to overcome the challenge of implementing CCP on an FPGA is to combine FPGA with an on-board CPU to compensate for the drawbacks and enhance the strengths of both [12, 13]. This approach provides better CP performance with more flexibility in multi-functional operations and process controls; however, it also substantially increases the firmware/software programming complexity and data transfer between the FPGA and CPU. So far, this type of CCP has only been explored by few groups with sophisticated experience and they had only limited success.

3) Offline software-based coincidence sorting and selection: Instead of acquiring coincidence events, this approach acquires singles events online, then sorts out the stored singles events and selects coincidence events offline. Many research groups have to rely on this offline approach to remedy the problem either because the high count-rate of coincidence data acquisition is beyond what CCP can handle or because the technical challenge of implementing CCP is beyond their capability [14-19]. However, this offline method is very inefficient, as the ratio of singles-to-coincidence events can range from 10:1 to 70:1. This method also requires very large data storage and substantial extra data processes, and prevents online (i.e. during the image session) image display, interpretation and intervention that could be extremely valuable for interventional applications [20]. For

total-body PET, its unique total-body FOV and ultrahigh sensitivity would make it possible for these invaluable studies, such as image-based brain-body dynamic responses to multiple external physical or pharmaceutical stimulations, if such online coincidence data acquisition could be achieved.

Conclusion: There is **a strong need** and **an unmet technical challenge** to develop a new CP that can substantially improve the count-rate of coincidence data acquisition and ease the implementation on FPGA. Addressing both challenges will require an *unconventional approach* with a new concept of CP.

A.3. **Solution:** This problem can be solved by breaking a *single system-level centralized complex* coincidence process into *many detector-pair-level simple* coincidence processes. Specifically, we *propose* to use a network of distributed coincidence processors (DCP), with each individual processor *exclusively* connecting to one designated detector pair and selecting coincidence events from this detector pair only (**Fig. 1**). DCP extends the non-centralized CP to *completely parallel* coincidence processes to avoid inter-detector data transfer, which *simplifies* the system-level coincidence process to a collection of individual detector-pair-level coincidence processes. DCP can provide the following additional **advantages**: ***1)*** The workload for *each CP* will not increase substantially even as the number of detector pairs increases substantially, which will provide a very high count-rate online coincidence data acquisition even for a PET with a large number of detectors. ***2)*** The coincidence processing algorithm at *each detector pair level* is simple and identical, so it can be easily developed, tested with one detector pair and replicated (or populated) to the rest.

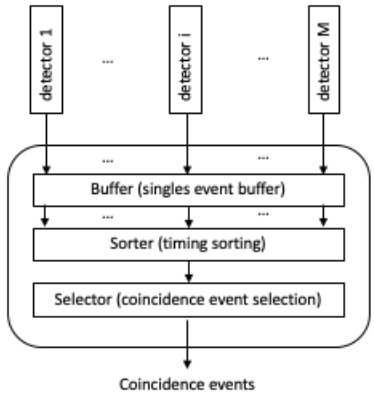

Fig. 1 (a) Schematics of centralized coincidence processor

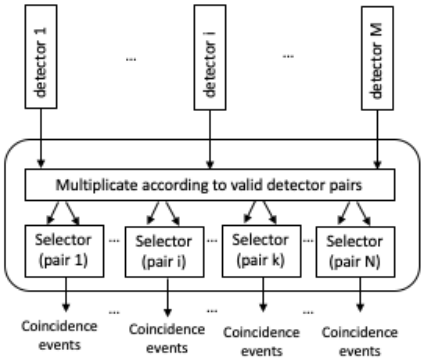

Fig. 1 (b) Schematics of distributed coincidence processors.

Briefly, DCP consists of a three-stage data process (**Fig. 2**): **1)** Scatter-stage receives singles events from all detectors, multiplicates each singles event from a detector and distributes them to the next stage according to a predefined map of valid coincidence detector pairs for imaging. For a PET with M detectors and N valid detector pairs, M inputs to the Scatter-stage will be multiplicated to N pairs and be distributed to N inputs of the next stage. **2)** Select-stage consists of N independent selectors that work in parallel. Each selector selects the two input singles events as a coincidence event if their timing difference is within the coincidence window width. **3)** Gather-stage collects and transfers the coincidence events to the data acquisition computer.

If successfully developed, DCP should provide a novel and different technology platform for coincidence processing to solve the problems with CCP. DCP can yield a very high count-rate PET *online* coincidence data acquisition far beyond the limit of what CCP can provide and can be implemented on FPGA with much less technical challenging than implementing CCP (**Fig. 3**). By addressing the problems with CCP and providing the solutions to the research community (see C.2), this project would have a transformative impact on improving the capability and performance of PET imaging and accelerating the development of new PET systems and technologies.

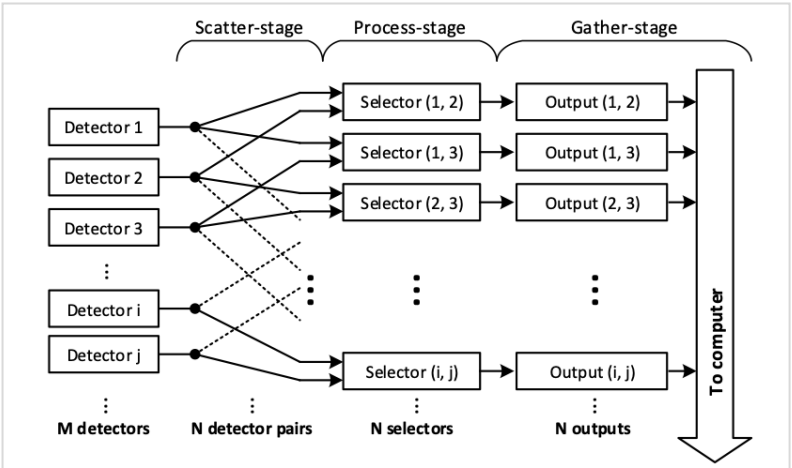

Fig. 2. Schematics of a three-staged DCP event processing structure with M detectors and N valid detector pairs for imaging.

B. INNOVATION

Compared to CCP, ***DCP would shift the technology platform of coincidence processing,*** with the tradeoffs of FPGA resources for speeding up coincidence processing with many independent and parallel data processes. In principle, this would fundamentally address the problems with CCP to significantly improve coincidence processing performance and simplify the algorithm. As an analogy, the differences between CCP and DCP are similar to those between a single central processing unit (CPU) and a graphics processing unit (GPU). As intuitive

as this is, however, ***the proposed DCP approach***, and FPGA-based DCP in particular, ***is new and innovative*** for PET coincidence data acquisition. In brief, the innovations of DCP include the following:

- Introduces distributed coincide processors to minimize the detector-pair-level workload of each coincidence processor to improve the system-level count-rate of coincidence processing.
- Applies the unique strength of FPGA, the architecture of which is well-suited to parallel data and logic processing of many processors, which provides the technical basis for realizing DCP.
- Simplifies the algorithm of a complex centralized coincidence process into a collection of simple and identical coincidence processes.

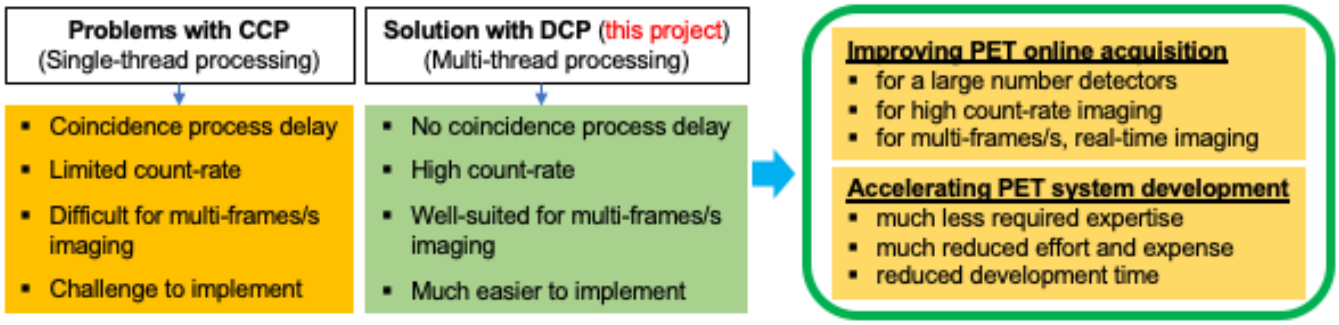

Fig. 3: Innovation, significance and impact of this project: to fundamentally and significantly improve PET online coincidence data acquisition for improving PET imaging capability, performance and accelerating PET system development.

C. PLAN and TASK

C.1. **Overview (Fig. 4):** We used the ***interplay*** between designing DCP technology (**Aim 1**) and implementing, evaluating DCP and enhancing its capability and performance (**Aim 2**) through most of the tasks to increasingly improve the design and development of various FPGA functions, guide the experimental setup and measurement, and scale up the DCP's capability and enhance its performance.

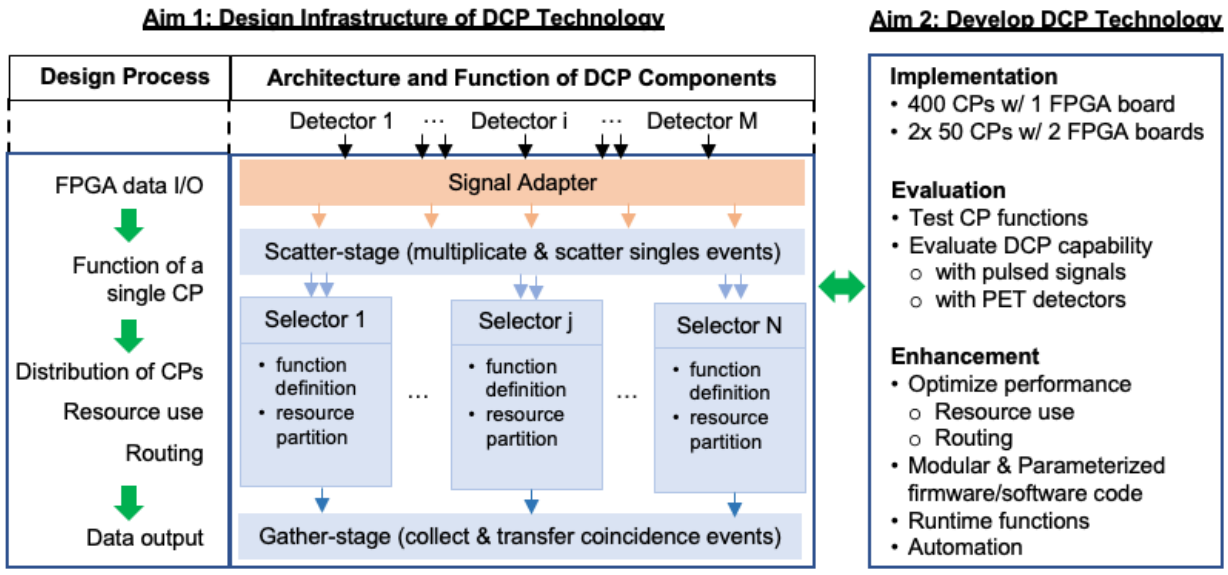

Fig. 4: Overview of research tasks to design, implement, evaluate DCP technology and enhance its capability and performance.

C.2. **Targeted project outcomes**:

1) A developed and evaluated DCP on a mid-range FPGA with at least 400 coincidence processors. As a practical solution for other research groups, this DCP can be directly applied for a *human brain* or a small animal PET.

2) A developed and evaluated DCP with a total of 100 coincidence processors on two cascaded FPGA boards. This will provide an *expandable solution* to implement DCP over multiple FPGA boards to increase the DCP capacity for a PET with a large number of detector pairs.

For both DCPs implemented in the above **1)** and **2)**, their ***measured*** count-rate of coincidence data acquisition at the detector pair level can achieve ≥250 k/s. The ***measured*** maximum count-rate of coincidence data acquisition at the system level will be proportional to the total number of valid detector pairs.

C.3. **Preliminary feasibility study:** We implemented a ***primitive*** version of DCP on an existing FPGA board to test whether the basic concept of DCP would be implementable and workable. Details can be found in a recent publication [21]. Briefly:

1) ***Hardware and firmware: (a)*** We implemented DCP with an existing low-end Stratix IV GX EP4SGX230 FPGA (Intel Corporation) development board that was previously used as the system electronics board for a prototype small PET with 12 detectors and 42 detector pairs (**Fig. 5**). The board was connected to 12 detector front-end readouts with 12 miniDP cables through a customized adapter board and to a PC computer through a PCI-e cable for data transfer. ***(b)*** The DCP had 42 coincidence processors to match the 42 detector pairs. FPGA resources were utilized, and the percentages used from the total available for registers, memories and adaptive lookup tables were 51K (28%), 72 Kbit (0.4%), and 10K (11%), respectively. The resources utilized were evenly distributed over the available FPGA resources, which indicates minimal routing congestion.

2) ***Performance***: ***(a)*** We tested with 250 k/s paired pulse signals inputting simultaneously to all 42 detector pairs and found no coincidence event loss. The measured coincidence time resolution (FWHM) was 89.1 ps. ***(b)*** We tested with a ^{22}Na point source at the center of FOV; coincidence events from all 42 detector pairs were acquired with DCP. The measured coincidence time resolution was ~3.6 ns with a single pair and ~4.1 ns with all 42 pairs (**Fig. 6**). ***(c)*** more details are shown in Appendix (an accepted manuscript of this preliminary study).

3) ***Conclusion***: Even the primitive DCP was only simply implemented without device upgrades or programming optimization, the preliminary study still demonstrated the feasibility of DCP for PET coincidence data acquisition.

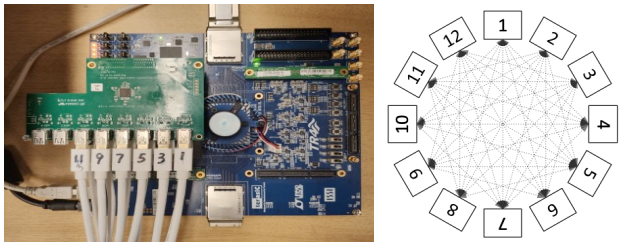

Fig. 5: Left: the FPGA board, adapter board and miniDP cables. Right: PET configuration with 42 detector pairs.

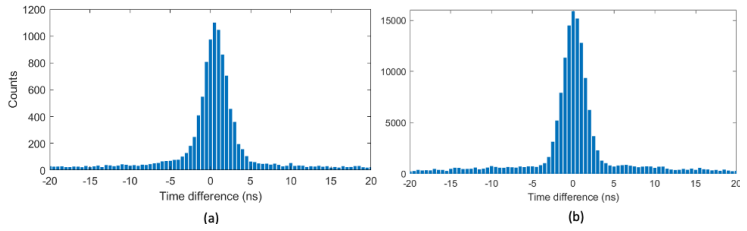

Fig. 6: Left to right: coincidence time spectrum measured with a single detector pair and with 42 detector pairs.

The following are the major research aims and tasks:

C.4. **Aim 1: Design DCP technology**. As shown in **Fig. 4**, the design processes will include the following:

C.4.1. The hardware *(at FPGA device level)* ***infrastructure of DCP components and functions*****.**

1) Signal adapter that streamlines input singles data into the FPGA I/O will be developed.

2) The components of a single CP and its functions will be defined for general coincidence data acquisition and implementation by users.

3) The replication and distribution of N CPs, where N is the number of valid coincidence detector pairs to be defined by the specific implementation.

4) The output of selected coincidence events will collect and transfer selected coincidence events data.

C.4.2. The firmware program that will realize the DCP components and functions on FPGA according to the hardware design (C.4.1). Major design considerations include:

1) *Accommodate different singles data format.*

2) *Minimize resource use.*

3) *Achieve desired DCP performance*.

4) *Implement DCP over cascaded multiple FPGA boards.*

C.5. **Aim 2: Implement and evaluate DCP and enhance its capability and performance**.

C.5.1. Implement DCP: To implement two different DCP prototypes.

1) DCP with 400 CPs on a single FPGA:

2) DCP with 100 CPs over two FPGAs.

C.5.2. Evaluate DCP capability and performance**:** To evaluate the DCP on several levels: We will use paired pulsed signals to evaluate the count-rate of a single CP, the performance uniformity over different CPs, the possible coincidence data loss under different rates of singles data, and the system-level count-rate with different CPs. Like in C.3.2, to use a prototype PET with multiple detectors to evaluate the DCP performance for PET coincidence data acquisition through a ^{22}Na point source.

C.5.3. Enhance DCP capability and performance: To use the valuable information obtained from evaluating DCP performance to improve the DCP design and performance, enhance runtime performance, implement an automatic replication script to automate the DCP parameter setting processes based on the parameters of the PET scanner, such as the number of detectors and detector pairs. Once a user defines the detector pair list, the script will generate CPs for every pair in the list.

C.6. Aim3: Disseminate DCP technology *through publications and providing an open source of DCP codes.*

D. NOTE

D.1. This project was conducted at Division of Medial Physics and Engineering, Department of Radiation Oncology, University of Texas Southwest Medical Center, from 12/2021 to 11/2023.

D.2. The project was supported with a US NIH small grant funded by National Institute of Biomedical Imaging and Bioengineering, R03EB032476.

D.3. Principal investigator: Dr. Yiping Shao. Research staff: Dr. Dongxu Yang.

D.4. More DCP technical details can be found in the DCP Development and Technical Notes and some latest publications on the technology and its applications [21-23].

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