NC State University

Department of Electrical and Computer Engineering

ECE 745 ASIC VERIFICATION

Fall 2015

# LC3 MICROCONTROLLER VERIFICATION
# BUG REPORT

Group 23

## Brief Introduction

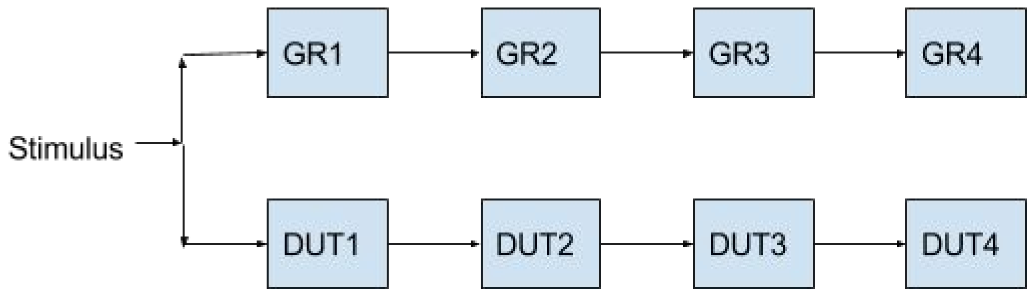
Verification is to verify whether the design meets the specifications.

In this project there are 7 unknown bugs for LC3 Microcontroller, and the testbench is able to detect all of them.

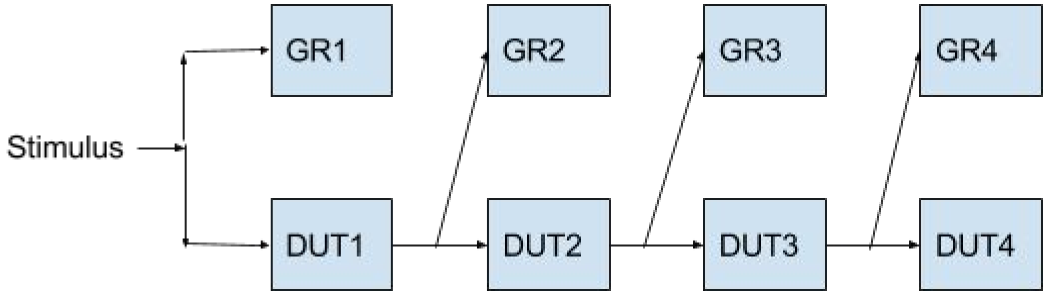
## Methodology

It is natural to think of two ways to write the testbenches:

Strategy 1:



Strategy 2:



## Strategy 1:

**Description**: Golden reference follow the same data/control flow as DUT does, in other words, each golden reference is fed by the logically previous golden reference's output.

**Analysis**: Bugs of the first few blocks will be carried to the successors.

## Strategy 2:

**Description**: Golden reference follow the same data/control flow differently than DUT does, in other words, each golden reference is fed by the logically previous DUT's output.

**Analysis**: Bugs of the first few blocks will not be carried to the successors.

In conclusion, Strategy 2 is used to detect the potential bugs in each individual block.

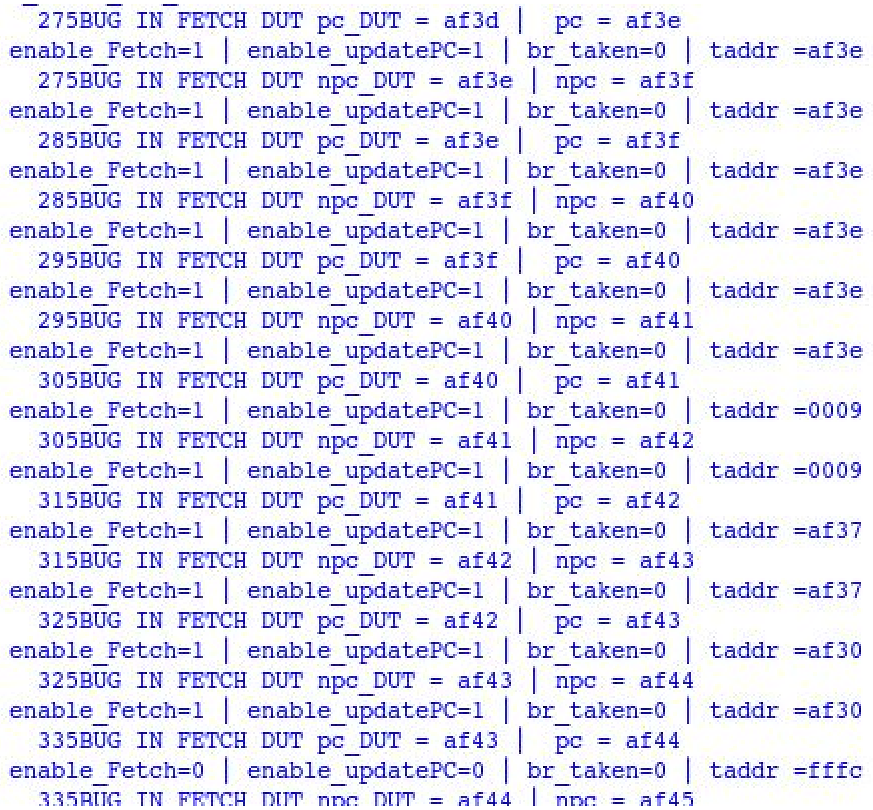
## Results

### Bug 1:

The bug 1 is in **Fetch Stage**.

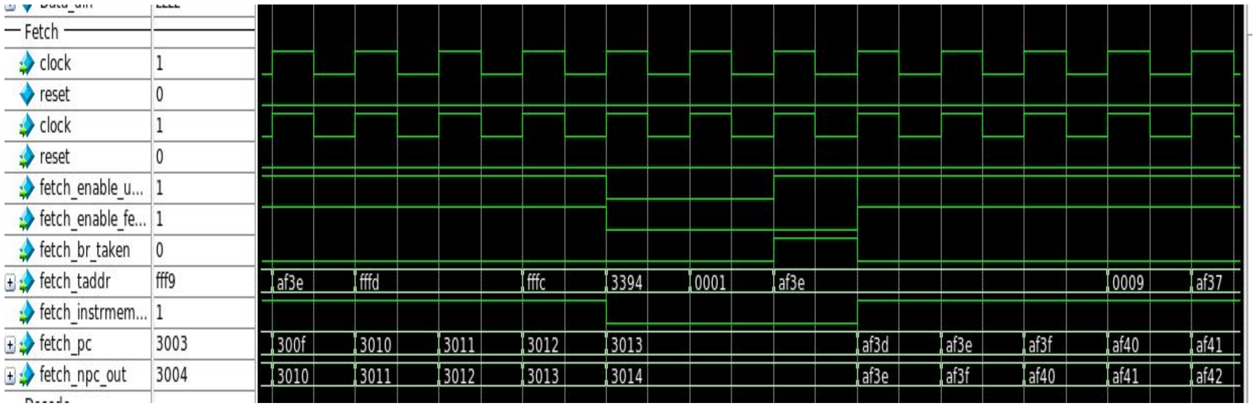
The output of the DUT pc and npc are both incorrect in the way of correct_value-1. For example, if correct output (golden reference) are (0036, 0037), the actual output is (0035, 0036).

Report Segment Example of Bug 1:



```
  275BUG IN FETCH DUT pc_DUT = af3d |  pc = af3e
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af3e
  275BUG IN FETCH DUT npc_DUT = af3e | npc = af3f
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af3e
  285BUG IN FETCH DUT pc_DUT = af3e |  pc = af3f
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af3e
  285BUG IN FETCH DUT npc_DUT = af3f | npc = af40
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af3e
  295BUG IN FETCH DUT pc_DUT = af3f |  pc = af40
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af3e
  295BUG IN FETCH DUT npc_DUT = af40 | npc = af41
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af3e
  305BUG IN FETCH DUT pc_DUT = af40 |  pc = af41
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =0009
  305BUG IN FETCH DUT npc_DUT = af41 | npc = af42
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =0009
  315BUG IN FETCH DUT pc_DUT = af41 |  pc = af42
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af37
  315BUG IN FETCH DUT npc_DUT = af42 | npc = af43
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af37
  325BUG IN FETCH DUT pc_DUT = af42 |  pc = af43
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af30
  325BUG IN FETCH DUT npc_DUT = af43 | npc = af44
enable_Fetch=1 | enable_updatePC=1 | br_taken=0 | taddr =af30
  335BUG IN FETCH DUT pc_DUT = af43 |  pc = af44
enable_Fetch=0 | enable_updatePC=0 | br_taken=0 | taddr =fffc
  335BUG IN FETCH DUT npc_DUT = af44 | npc = af45
```

Waveform Example of Bug 1:

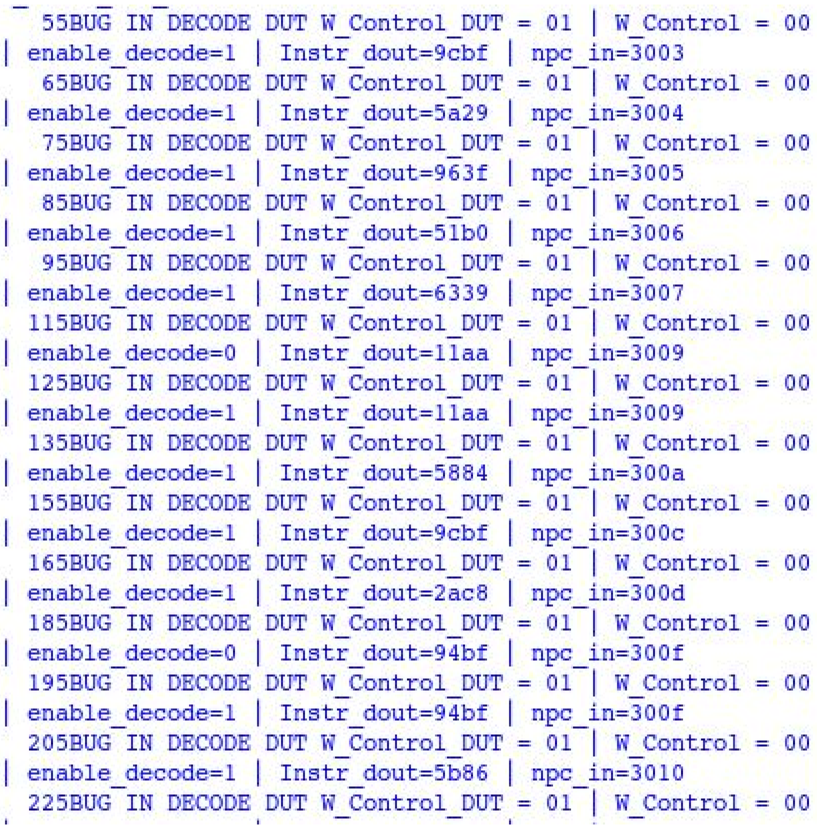


**Bug 2:**

The bug 2 is in **Decode stage.**

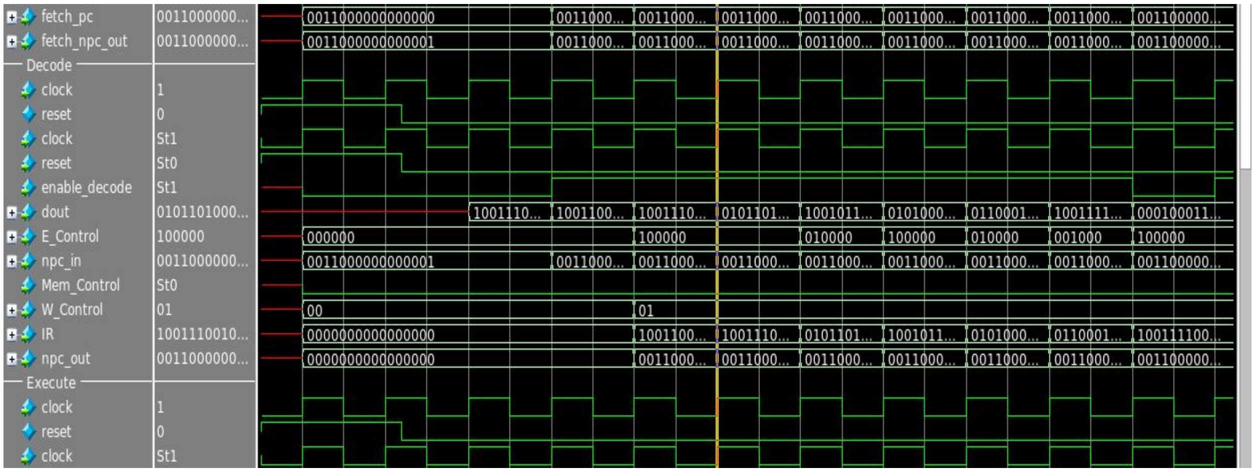
The output signal W_Control of the DUT is always 1 while it should be 0 (as golden reference shows).

Report Segment Example of Bug 2:



```
  55BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=9cbf | npc_in=3003
  65BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=5a29 | npc_in=3004
  75BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=963f | npc_in=3005
  85BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=51b0 | npc_in=3006
  95BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=6339 | npc_in=3007
 115BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=0 | Instr_dout=11aa | npc_in=3009
 125BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=11aa | npc_in=3009
 135BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=5884 | npc_in=300a
 155BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=9cbf | npc_in=300c
 165BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=2ac8 | npc_in=300d
 185BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=0 | Instr_dout=94bf | npc_in=300f
 195BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=94bf | npc_in=300f
 205BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
| enable_decode=1 | Instr_dout=5b86 | npc_in=3010
 225BUG IN DECODE DUT W_Control_DUT = 01 | W_Control = 00
```

Waveform Example of Bug 2:

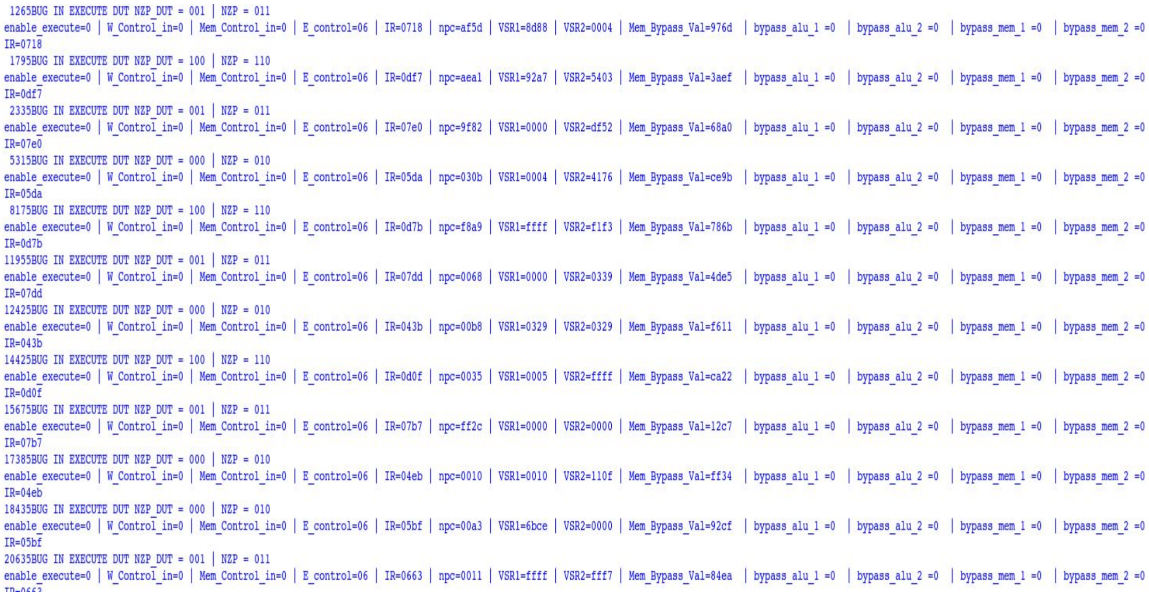


**Bug 3:**

The bug 3 is in **Execute stage.**

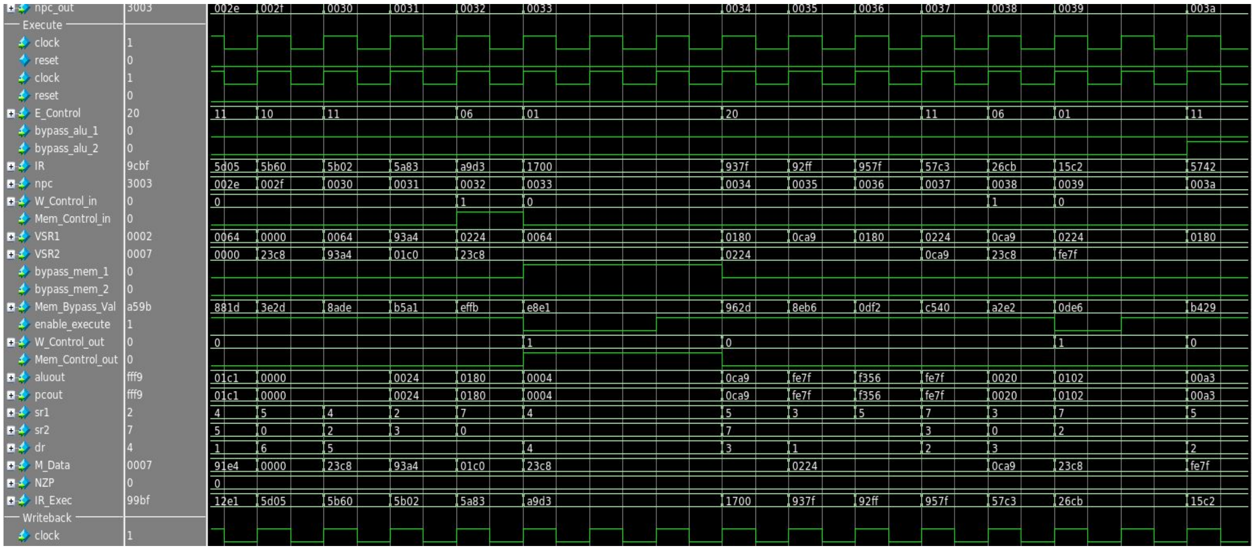
The correct output of NZP should have x1x format, but the acutal output signal NZP of the DUT is x0x. For example, the output NZP signal of the DUT is 000 rather than 010.

Report Segment Example of Bug 3:



```
 1265BUG IN EXECUTE DUT NZP_DUT = 001 | NZP = 011
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=0718 | npc=af5d | VSR1=8d88 | VSR2=0004 | Mem_Bypass_Val=976d  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=0718
 1795BUG IN EXECUTE DUT NZP_DUT = 100 | NZP = 110
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=0df7 | npc=aea1 | VSR1=92a7 | VSR2=5403 | Mem_Bypass_Val=3aef  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=0df7
 2335BUG IN EXECUTE DUT NZP_DUT = 001 | NZP = 011
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=07e0 | npc=9f82 | VSR1=0000 | VSR2=df52 | Mem_Bypass_Val=68a0  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=07e0
 5315BUG IN EXECUTE DUT NZP_DUT = 000 | NZP = 010
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=05da | npc=030b | VSR1=0004 | VSR2=4176 | Mem_Bypass_Val=ce9b  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=05da
 8175BUG IN EXECUTE DUT NZP_DUT = 100 | NZP = 110
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=0d7b | npc=f8a9 | VSR1=ffff | VSR2=f1f3 | Mem_Bypass_Val=786b  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=0d7b
11955BUG IN EXECUTE DUT NZP_DUT = 001 | NZP = 011
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=07dd | npc=0068 | VSR1=0000 | VSR2=0339 | Mem_Bypass_Val=4de5  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=07dd
12425BUG IN EXECUTE DUT NZP_DUT = 000 | NZP = 010
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=043b | npc=00b8 | VSR1=0329 | VSR2=0329 | Mem_Bypass_Val=f611  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=043b
14425BUG IN EXECUTE DUT NZP_DUT = 100 | NZP = 110
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=0d0f | npc=0035 | VSR1=0005 | VSR2=ffff | Mem_Bypass_Val=ca22  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=0d0f
15675BUG IN EXECUTE DUT NZP_DUT = 001 | NZP = 011
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=07b7 | npc=ff2c | VSR1=0000 | VSR2=0000 | Mem_Bypass_Val=12c7  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=07b7
17385BUG IN EXECUTE DUT NZP_DUT = 000 | NZP = 010
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=04eb | npc=0010 | VSR1=0010 | VSR2=110f | Mem_Bypass_Val=ff34  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=04eb
18435BUG IN EXECUTE DUT NZP_DUT = 000 | NZP = 010
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=05bf | npc=00a3 | VSR1=6bce | VSR2=0000 | Mem_Bypass_Val=92cf  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=05bf
20635BUG IN EXECUTE DUT NZP_DUT = 001 | NZP = 011
enable_execute=0 | W_Control_in=0 | Mem_Control_in=0 | E_control=06 | IR=0663 | npc=0011 | VSR1=ffff | VSR2=fff7 | Mem_Bypass_Val=84ea  | bypass_alu_1 =0  | bypass_alu_2 =0  | bypass_mem_1 =0  | bypass_mem_2 =0
IR=0663
```

Waveform Example of Bug 3:

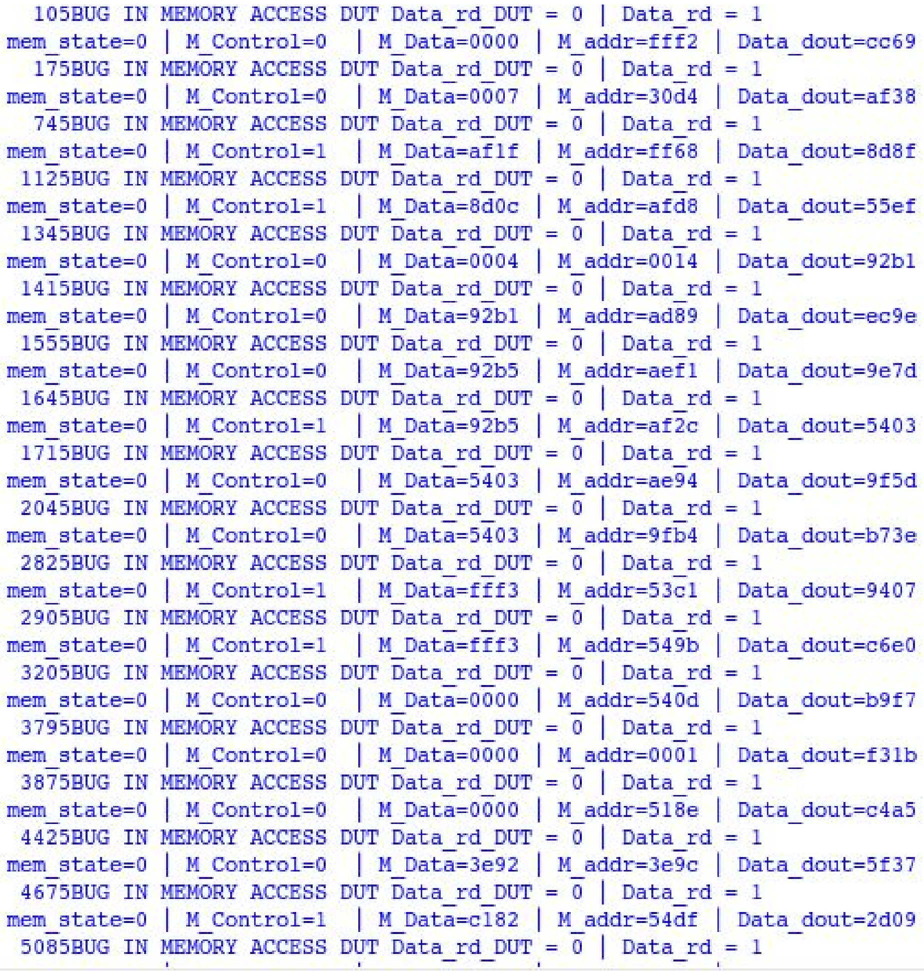

npc_out 3003 002e 002f 0030 0031 0032 0033 0034 0035 0036 0037 0038 0039 003a
Execute
clock 1
reset 0
clock 1
reset 0
E_Control 20 11 10 11 06 01 20 11 06 01 11
bypass_alu_1 0
bypass_alu_2 0
IR 9cbf 5d05 5b60 5b02 5a83 a9d3 1700 937f 92ff 957f 57c3 26cb 15c2 5742
npc 3003 002e 002f 0030 0031 0032 0033 0034 0035 0036 0037 0038 0039 003a
W_Control_in 0 0 1 0 1 0
Mem_Control_in 0
VSR1 0002 0064 0000 0064 93a4 0224 0064 0180 0ca9 0180 0224 0ca9 0224 0180
VSR2 0007 0000 23c8 93a4 01c0 23c8 0224 0ca9 23c8 fe7f
bypass_mem_1 0
bypass_mem_2 0
Mem_Bypass_Val a59b 881d 3e2d 8ade b5a1 effb e8e1 962d 8eb6 0df2 c540 a2e2 0de6 b429
enable_execute 1
W_Control_out 0 0 1 0 1 0
Mem_Control_out 0
aluout fff9 01c1 0000 0024 0180 0004 0ca9 fe7f f356 fe7f 0020 0102 00a3
pcout fff9 01c1 0000 0024 0180 0004 0ca9 fe7f f356 fe7f 0020 0102 00a3
sr1 2 4 5 4 2 7 4 5 3 5 7 3 7 5
sr2 7 5 0 2 3 0 7 3 0 2
dr 4 1 6 5 4 3 1 2 3 2
M_Data 0007 91e4 0000 23c8 93a4 01c0 23c8 0224 0ca9 23c8 fe7f
NZP 0 0
IR_Exec 99bf 12e1 5d05 5b60 5b02 5a83 a9d3 1700 937f 92ff 957f 57c3 26cb 15c2
Writeback
clock 1

**Bug 4:**

The bug 4 is in **Memory Access stage.**

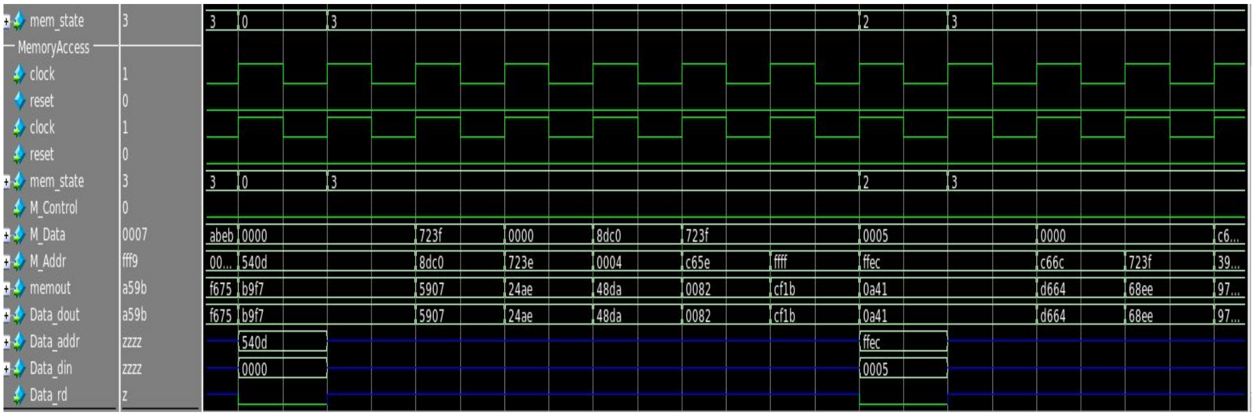
The output signal Data_rd of the DUT is always 0 while it should be 1, as the golden reference shows.

Report Segment Example of Bug 4:



```
  105BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=0000 | M_addr=fff2 | Data_dout=cc69
  175BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=0007 | M_addr=30d4 | Data_dout=af38
  745BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=1  | M_Data=af1f | M_addr=ff68 | Data_dout=8d8f
 1125BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=1  | M_Data=8d0c | M_addr=afd8 | Data_dout=55ef
 1345BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=0004 | M_addr=0014 | Data_dout=92b1
 1415BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=92b1 | M_addr=ad89 | Data_dout=ec9e
 1555BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=92b5 | M_addr=aef1 | Data_dout=9e7d
 1645BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=1  | M_Data=92b5 | M_addr=af2c | Data_dout=5403
 1715BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=5403 | M_addr=ae94 | Data_dout=9f5d
 2045BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=5403 | M_addr=9fb4 | Data_dout=b73e
 2825BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=1  | M_Data=fff3 | M_addr=53c1 | Data_dout=9407
 2905BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=1  | M_Data=fff3 | M_addr=549b | Data_dout=c6e0
 3205BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=0000 | M_addr=540d | Data_dout=b9f7
 3795BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=0000 | M_addr=0001 | Data_dout=f31b
 3875BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=0000 | M_addr=518e | Data_dout=c4a5
 4425BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=0  | M_Data=3e92 | M_addr=3e9c | Data_dout=5f37
 4675BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
mem_state=0 | M_Control=1  | M_Data=c182 | M_addr=54df | Data_dout=2d09
 5085BUG IN MEMORY ACCESS DUT Data_rd_DUT = 0 | Data_rd = 1
```

Waveform Example of Bug 4:

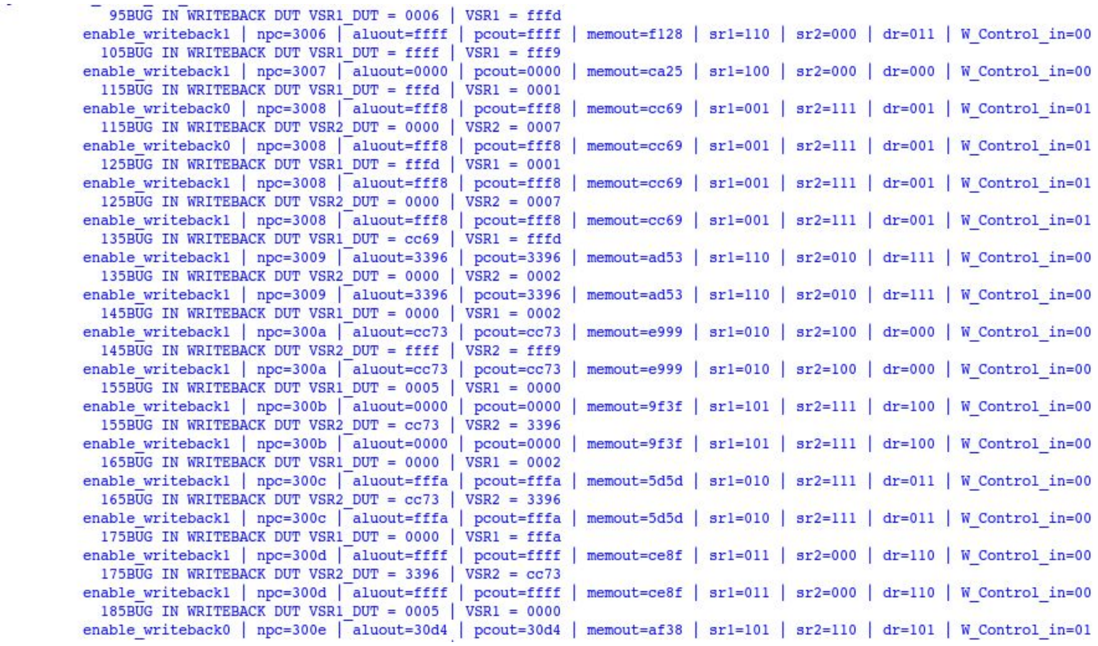

mem_state 3
MemoryAccess
clock 1
reset 0
clock 1
reset 0
mem_state 3
M_Control 0
M_Data 0007
M_Addr fff9
memout a59b
Data_dout a59b
Data_addr zzzz
Data_din zzzz
Data_rd z
3 0 3 2 3
3 0 3 2 3
abeb 0000 723f 0000 8dc0 723f 0005 0000 c6...
00... 540d 8dc0 723e 0004 c65e ffff ffec c66c 723f 39...
f675 b9f7 5907 24ae 48da 0082 cf1b 0a41 d664 68ee 97...
f675 b9f7 5907 24ae 48da 0082 cf1b 0a41 d664 68ee 97...
540d ffec
0000 0005

**Bug 5:**

The bug 5 is in **WriteBack stage.**

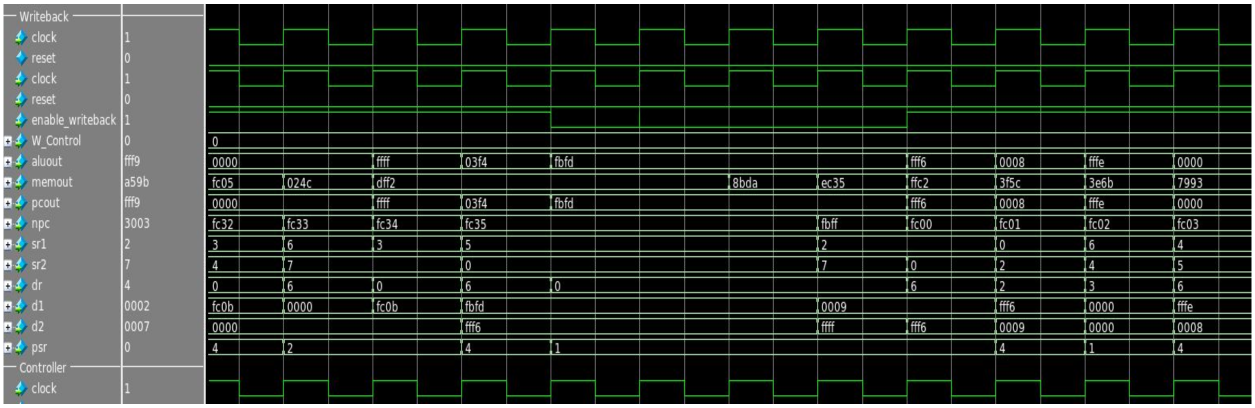
The output signals VSR1 and VSR2 of the DUT are both incorrect, however, this bug is hard to describe, so we put both hex and bin formats to compare the actual output signals VSR1 AND VSR2 of the DUT and the golden reference.

Report Segment Example of Bug 5 in hex:



```
   95BUG IN WRITEBACK DUT VSR1_DUT = 0006 | VSR1 = fffd
enable_writeback1 | npc=3006 | aluout=ffff | pcout=ffff | memout=f128 | sr1=110 | sr2=000 | dr=011 | W_Control_in=00
  105BUG IN WRITEBACK DUT VSR1_DUT = ffff | VSR1 = fff9
enable_writeback1 | npc=3007 | aluout=0000 | pcout=0000 | memout=ca25 | sr1=100 | sr2=000 | dr=000 | W_Control_in=00
  115BUG IN WRITEBACK DUT VSR1_DUT = fffd | VSR1 = 0001
enable_writeback0 | npc=3008 | aluout=fff8 | pcout=fff8 | memout=cc69 | sr1=001 | sr2=111 | dr=001 | W_Control_in=01
  115BUG IN WRITEBACK DUT VSR2_DUT = 0000 | VSR2 = 0007
enable_writeback0 | npc=3008 | aluout=fff8 | pcout=fff8 | memout=cc69 | sr1=001 | sr2=111 | dr=001 | W_Control_in=01
  125BUG IN WRITEBACK DUT VSR1_DUT = fffd | VSR1 = 0001
enable_writeback1 | npc=3008 | aluout=fff8 | pcout=fff8 | memout=cc69 | sr1=001 | sr2=111 | dr=001 | W_Control_in=01
  125BUG IN WRITEBACK DUT VSR2_DUT = 0000 | VSR2 = 0007
enable_writeback1 | npc=3008 | aluout=fff8 | pcout=fff8 | memout=cc69 | sr1=001 | sr2=111 | dr=001 | W_Control_in=01
  135BUG IN WRITEBACK DUT VSR1_DUT = cc69 | VSR1 = fffd
enable_writeback1 | npc=3009 | aluout=3396 | pcout=3396 | memout=ad53 | sr1=110 | sr2=010 | dr=111 | W_Control_in=00
  135BUG IN WRITEBACK DUT VSR2_DUT = 0000 | VSR2 = 0002
enable_writeback1 | npc=3009 | aluout=3396 | pcout=3396 | memout=ad53 | sr1=110 | sr2=010 | dr=111 | W_Control_in=00
  145BUG IN WRITEBACK DUT VSR1_DUT = 0000 | VSR1 = 0002
enable_writeback1 | npc=300a | aluout=cc73 | pcout=cc73 | memout=e999 | sr1=010 | sr2=100 | dr=000 | W_Control_in=00
  145BUG IN WRITEBACK DUT VSR2_DUT = ffff | VSR2 = fff9
enable_writeback1 | npc=300a | aluout=cc73 | pcout=cc73 | memout=e999 | sr1=010 | sr2=100 | dr=000 | W_Control_in=00
  155BUG IN WRITEBACK DUT VSR1_DUT = 0005 | VSR1 = 0000
enable_writeback1 | npc=300b | aluout=0000 | pcout=0000 | memout=9f3f | sr1=101 | sr2=111 | dr=100 | W_Control_in=00
  155BUG IN WRITEBACK DUT VSR2_DUT = cc73 | VSR2 = 3396
enable_writeback1 | npc=300b | aluout=0000 | pcout=0000 | memout=9f3f | sr1=101 | sr2=111 | dr=100 | W_Control_in=00
  165BUG IN WRITEBACK DUT VSR1_DUT = 0000 | VSR1 = 0002
enable_writeback1 | npc=300c | aluout=fffa | pcout=fffa | memout=5d5d | sr1=010 | sr2=111 | dr=011 | W_Control_in=00
  165BUG IN WRITEBACK DUT VSR2_DUT = cc73 | VSR2 = 3396
enable_writeback1 | npc=300c | aluout=fffa | pcout=fffa | memout=5d5d | sr1=010 | sr2=111 | dr=011 | W_Control_in=00
  175BUG IN WRITEBACK DUT VSR1_DUT = 0000 | VSR1 = fffa
enable_writeback1 | npc=300d | aluout=ffff | pcout=ffff | memout=ce8f | sr1=011 | sr2=000 | dr=110 | W_Control_in=00
  175BUG IN WRITEBACK DUT VSR2_DUT = 3396 | VSR2 = cc73
enable_writeback1 | npc=300d | aluout=ffff | pcout=ffff | memout=ce8f | sr1=011 | sr2=000 | dr=110 | W_Control_in=00
  185BUG IN WRITEBACK DUT VSR1_DUT = 0005 | VSR1 = 0000
enable_writeback0 | npc=300e | aluout=30d4 | pcout=30d4 | memout=af38 | sr1=101 | sr2=110 | dr=101 | W_Control_in=01
```

Waveform Example of Bug 5:

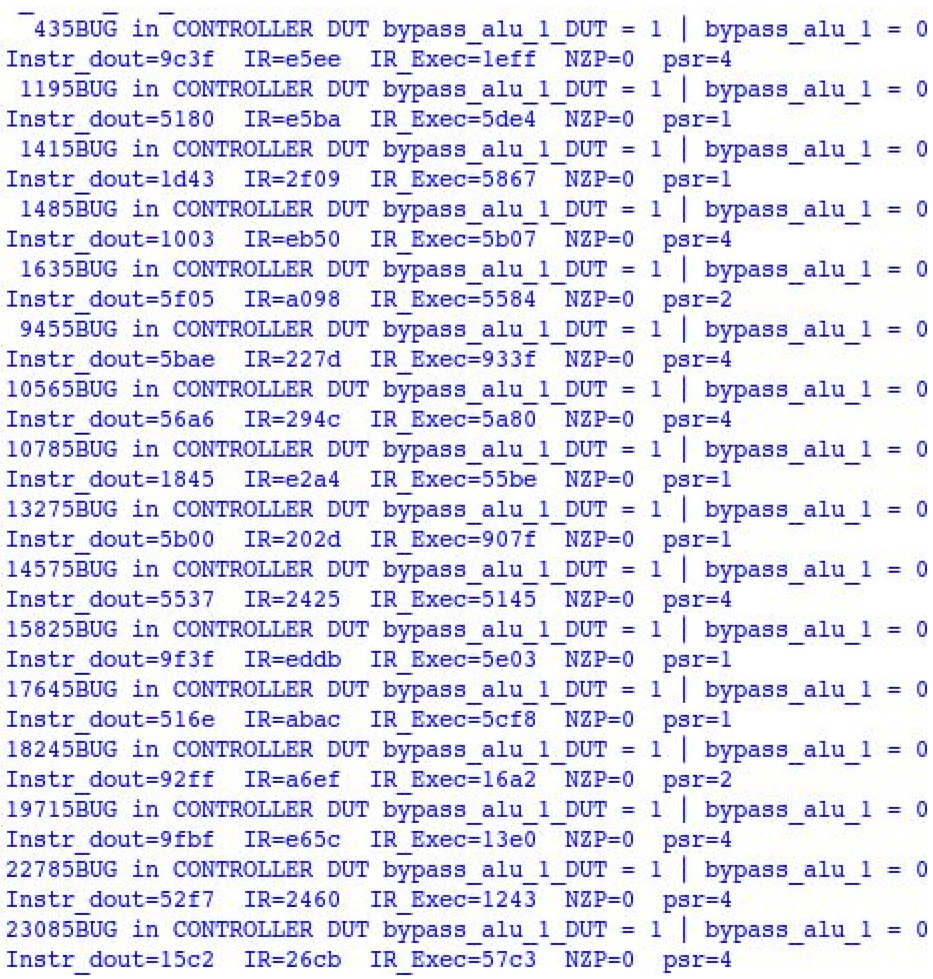

Writeback
clock 1
reset 0
clock 1
reset 0
enable_writeback 1
W_Control 0 0
aluout fff9 0000 ffff 03f4 fbfd fff6 0008 fffe 0000
memout a59b fc05 024c dff2 8bda ec35 ffc2 3f5c 3e6b 7993
pcout fff9 0000 ffff 03f4 fbfd fff6 0008 fffe 0000
npc 3003 fc32 fc33 fc34 fc35 fbff fc00 fc01 fc02 fc03
sr1 2 3 6 3 5 2 0 6 4
sr2 7 4 7 0 7 0 2 4 5
dr 4 0 6 0 6 0 6 2 3 6
d1 0002 fc0b 0000 fc0b fbfd 0009 fff6 0000 fffe
d2 0007 0000 fff6 ffff fff6 0009 0000 0008
psr 0 4 2 4 1 4 1 4
Controller
clock 1

**Bug 6:**

The bug 6 is in **Control stage.**

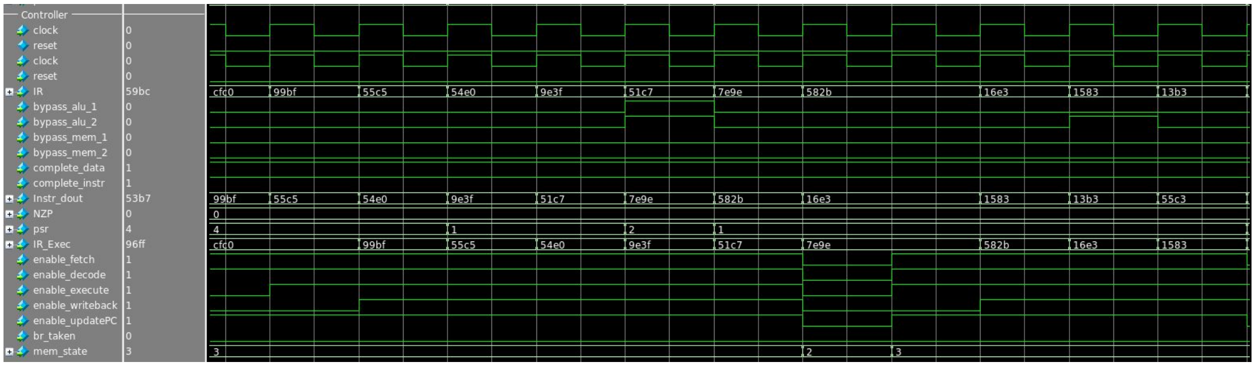
The output signal bypass_alu_1 is always 1 while it should be 0, as the golden reference shows.

Report Segment Example of Bug 6:



```
  435BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=9c3f  IR=e5ee  IR_Exec=1eff  NZP=0  psr=4
 1195BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=5180  IR=e5ba  IR_Exec=5de4  NZP=0  psr=1
 1415BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=1d43  IR=2f09  IR_Exec=5867  NZP=0  psr=1
 1485BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=1003  IR=eb50  IR_Exec=5b07  NZP=0  psr=4
 1635BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=5f05  IR=a098  IR_Exec=5584  NZP=0  psr=2
 9455BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=5bae  IR=227d  IR_Exec=933f  NZP=0  psr=4
10565BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=56a6  IR=294c  IR_Exec=5a80  NZP=0  psr=4
10785BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=1845  IR=e2a4  IR_Exec=55be  NZP=0  psr=1
13275BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=5b00  IR=202d  IR_Exec=907f  NZP=0  psr=1
14575BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=5537  IR=2425  IR_Exec=5145  NZP=0  psr=4
15825BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=9f3f  IR=eddb  IR_Exec=5e03  NZP=0  psr=1
17645BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=516e  IR=abac  IR_Exec=5cf8  NZP=0  psr=1
18245BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=92ff  IR=a6ef  IR_Exec=16a2  NZP=0  psr=2
19715BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=9fbf  IR=e65c  IR_Exec=13e0  NZP=0  psr=4
22785BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=52f7  IR=2460  IR_Exec=1243  NZP=0  psr=4
23085BUG in CONTROLLER DUT bypass_alu_1_DUT = 1 | bypass_alu_1 = 0
Instr_dout=15c2  IR=26cb  IR_Exec=57c3  NZP=0  psr=4
```

Waveform Example of Bug 6:

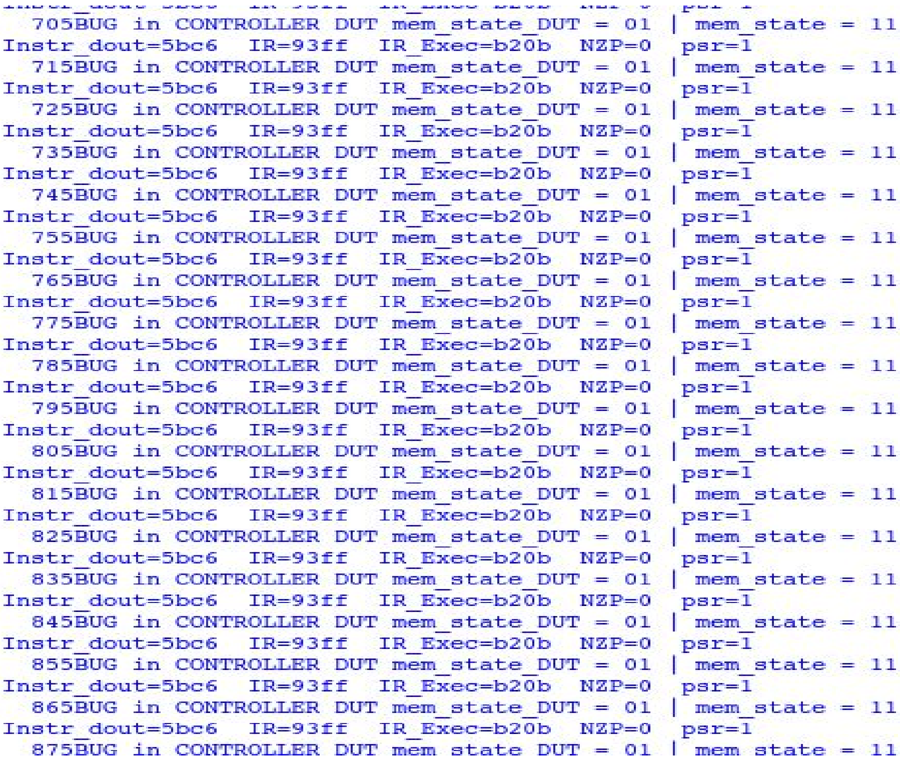


**Bug 7:**

The bug 7 is still in **Control stage.**

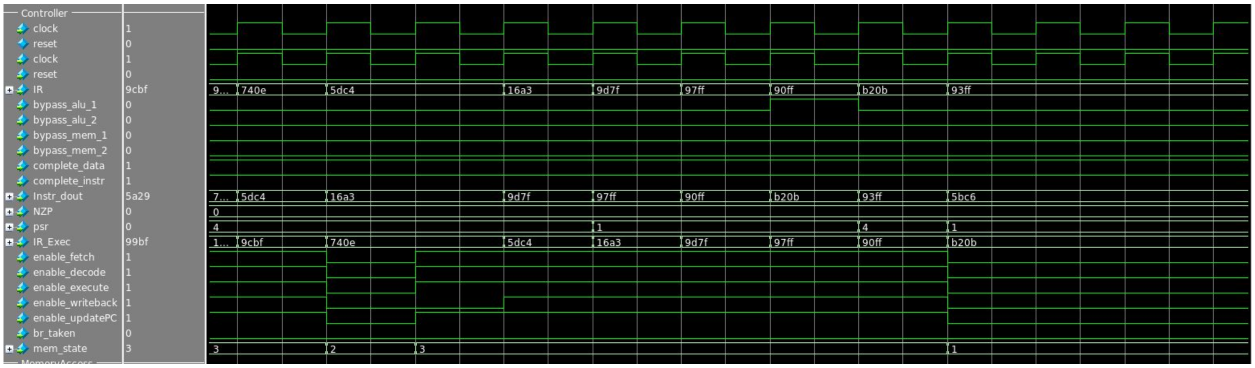
The output signal mem_state is always 1 while it should be 3, and enable_wb 0 while it should be 1, as the golden reference shows. This problem is very explicit when we pass the STI instruction to the controller.

Report Segment Example of Bug 7:



```
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  705BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  715BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  725BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  735BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  745BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  755BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  765BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  775BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  785BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  795BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  805BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  815BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  825BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  835BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  845BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  855BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  865BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
Instr_dout=5bc6  IR=93ff  IR_Exec=b20b  NZP=0  psr=1
  875BUG in CONTROLLER DUT mem_state_DUT = 01 | mem_state = 11
```

Waveform Example of Bug 7:



We made use of Assertions in our code. Due to the bug in the code. The following assertion properties are some of them which weren't satisfied.

```
1.property CTRL_mem_state_1_2;
@(posedge clock)
 (mem_state == 2'b01) && (IR_Exec[15:12] == 4'b1011) |=>  mem_state == 2'b10;
   endproperty
   assert property (CTRL_mem_state_1_2);
   cover property  (CTRL_mem_state_1_2);

2. property CTRL_mem_state_3_2;
   @(posedge clock)
    (mem_state == 2'b11) && (IR[15:12] == 4'b1011) |=>  mem_state == 2'b01 ##1 mem_state == 2'b10;
   endproperty
    assert property (CTRL_mem_state_3_2);
    cover property  (CTRL_mem_state_3_2);

3. property CTRL_enable_mem_state_STI;
    @(posedge clock)
    (IR[15:12] == 4'b1011) |=>  mem_state == 2'b01 ##1 mem_state == 2'b10 ##1 mem_state == 2'b11;
   endproperty
    assert property (CTRL_enable_mem_state_STI);
    cover property  (CTRL_enable_mem_state_STI);

4.property CTRL_enable_mem_state_STI_LDI;
    @(posedge clock)
    (IR[15:12] == 4'b1010 || IR[15:12] == 4'b1011 ) |=>  mem_state == 2'b01 ##2 mem_state == 2'b11;
              endproperty
              assert property (CTRL_enable_mem_state_STI_LDI);
              cover property  (CTRL_enable_mem_state_STI_LDI);
```

These assertions were related to the STI instructions