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Computer Architecture & Organization

DA-1
CA-2

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Q1. Consider a computer that has a byte-addressable memory organized in 32-bit words according to the Big-endian scheme. A program reads ASCII characters entered at a keyboard and stores them in successive byte locations, starting at location 1000.

Show that the contents of the two memory words at locations 1000 and 1004 after word "COMPUTER" has been entered.

Soln The computer that has a byte addressable memory organized in 32-bit words according to the Big-endian scheme reads the ASCII characters of the word "COMPUTER" entered at the keyboard and stores them starting at location 1000 are as follows:-

Hexadecimal equivalent of ASCII value :-

C is 0100 - 0011 (BCD) or 43 (Hexadecimal)

O is 0100 - 1111 (BCD) or 4F (Hexadecimal)

M is 0100 - 1101 (BCD) or 4D (Hexadecimal)

P is 0101 - 0000 (BCD) or 50 (Hexadecimal)

U is 0101 - 0101 (BCD) or 55 (Hexadecimal)

T is 0101 - 0100 (BCD) or 54 (Hexadecimal)

E is 0100 - 0101 (BCD) or 45 (Hexadecimal)

R is 0101 - 0010 (BCD) or 52 (Hexadecimal)

The two words at 1000 and 1004 are →

COMP stored at location 1000 to 1003, and

UTER stored at location 1004 to 1007.

So, they are 434F4D50 and 55544552.

< p.t.o. >

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Q2. A peripheral device wants to read by words from memory locations with address 1800. The transfer is by means of DMA.

(a) Give the initial values that the CPU must transfer to the DMA controller.

(b) Give step-by-step account of the actions taken during the process of the first two roads.

Sol^n →

(a) Whenever a peripheral device requests the DMA for a read or write operation the DMA sends BR (Bus request) signal to the CPU. Now the CPU don't immediately send the Bus grant signal to the DMA; prior to that the CPU stores 3 important values in registers associated to the DMA.

These are :-

(1) Base addresses from where read/write operation has to be started in the address register of the DMA.

(2) Then the CPU also sends the words to be read/write in the word count register.

(3) The control signal is also sent by the CPU in the control register.

Now, after ~~that~~ all these values are provided by the CPU to the DMA, it then provides the Bus-Grant signal to the CPU as well.

(b) Step-by-step action of two reads :—

(i) When the first word of the memory is created, it sends a DMA request, the DMA controller bus cancels the request so that CPU can free the bus control.

(ii) Before leaving bus control, CPU gives address of the starting memory, and DMA writes it to its registers (1800), and sends DMA receipt to the memory.

(iii) The memory then puts first word on data bus, activates DMA-controller which writes to the peripheral device.

(iv) When second word is ready for the memory, it writes DMA request again.

(v) The DMA then sends the current address (1801) on the bus and accepts it on the memory.

(vi) Then the second word after the memory puts data on the bus and activates the DMA-written control line which writes the word to peripheral device.

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(VII) The DMA deactivates written control line incremental addren registration (1802) and decreasing word count register.

Q3. The processor needs to transfer a file of 32768 Kilobytes from disk to main memory. The memory is byte addressable. The size of the data count register of a DMA controller is 16 bits. What is the minimum number of times the DMA controller needs to get the control of system bus from the processor to transfer the file from the ~~processor to~~ disk, to main memory in the following transfer mode ?

[a] cycle stealing mode

[b] Burst transfer mode

solⁿ contd ....

Solⁿ → (i) Cycle stealing mode :-

Here, one block of data is transferred, and then control is returned to the CPU.

Size of the data count register of the DMA controller = 16 bits.

Data can be transferred in one go = 2^{16} bytes

= 64 kilobytes.

File size to be transferred = 32768 Kilobytes.

So, number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory = ceil (32768 / 64)

= 512

(ii) Burst Transfer Mode:-

Here, number of blocks of data are transferred continuously before returning control to CPU until whole data is transferred.

Data transfer in one go = 32768 kilobytes

So, Number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory

$$= \text{ceil}\left(32768/32768\right)$$

$$= 1$$

Q4. Justify the following statements :-

(a) Performance of the ~~peripher~~ pipelined processor increases with increase in the number of stages.

(b) Forwarding can eliminate all possible stalls arises out of data dependencies.

Soln contd.....

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Sol^n (a)

performance of the pipelined processor increases with increase in number of stages, as performance of pipeline processor $= (K + n - 1) t_p$.

$$\text{performance} \propto K$$

As $K \uparrow$, performance $\uparrow$.

Instructor	1				2			
Fetch	✓				✓			
Decode		✓				✓		
~~Encode~~ Execute			✓				✓	
Write				✓				✓
clock	1	2	3	4	5	6	7	8

Non- pipelined

pipelined :→

Instructor	1	2			
Fetch	✓	✓			
Decode		✓	✓		
Execute			✓	✓.	
Write				✓	✓
Clock	1	2	3	4	5

(b) Data foriwarding eliminates all possible stalls arises out of data dependencies such as RAW, WAR, WAW in data forwarding, we use the interface registers present between stages to hold intermediate output so that dependent can access new value from the interface register directly.

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Q5. Specify some of the great ideas exploited extensively by the computer designers in establishing computer architectures.

Soln → Great ideas exploited by computer designers in establishing computer architecture are :-

(i) Design of Moore's Law :

The one constant for computer designers is rapid change, which is driven largely by Moore's Law. It states that integrated circuit resources double every 18-24 months. Moore's Law resulted from a 1965 prediction of such growth in IC capacity, made by Gordon Moore. As computer designs can take years, the resources available per chip can easily double or quadruple between the start and finish of the project. Like a skeet shooter, computer architects must anticipate where the technology will be when the design finishes rather than design for where it starts.

(ii) Make the common case fast :-

Making the common case fast will tend to enhance performance better than optimising rare case. Common case is often simpler than the rare case and hence is often easier to enhance. This common sense advice implies that you know what the common case is which is only possible with careful experimentation and measurement.

(iii) Hierarchy of Memories :-

Programmers want memory to be fast, large and cheap, as memory speed often shapes performance, capacity limits the size of problems that can be solved and the cost of memory today is often the majority of computer's cost. Architects have found they can address these conflicting demands with a hierarchy of memories, with the fastest, smallest and most expensive memory per bit at the top of the hierarchy and the slowest, largest and cheapest per bit at the bottom. Caches give the programmer the illusion that the main memory is nearly as fast as the top of the hierarchy and nearly as big and cheap as the bottom of the hierarchy.

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(iv) performance via pipelining :-

A particular pattern of parallelism is so prevalent in computer architecture that it merits its own name :- pipelining.

e.g. Before fire engines, a "bucket brigade" would respond to a fire, which many cauby movies show in response to a dastardly act by the villain. The townsfolk form a human chain to carry a water source to fire, as they could much more quietly (and quickly) move buckets up the chain instead of individuals running back and forth.

(v) Performance via prediction :-

In some cases, it can be faster on average to guess & start working rather than wait until you know for sure, assuming that the mechanism to recover a ~~misinterpre~~ misprediction is not too expensive & your prediction is relatively accurate. We use the fortune-teller's crystal ball as our prediction icon.

— END —