Q_1. Verify the characteristic table of D and T flip-flops.

Sol^n

ⓐ D-flip-flop:

$S = 0/1$

S'

Q_n

R'

$\overline{Q_n}$

$R = 1/0$
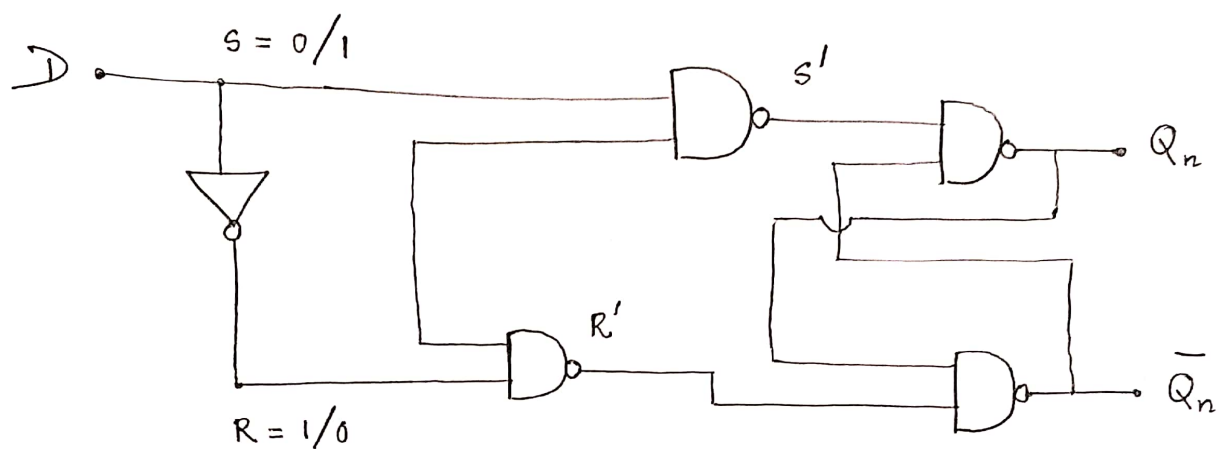
CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

characteristic table : $\boxed{Q_{n+1} = D}$

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Excutation table:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Ⓒ **T- flip flop :**
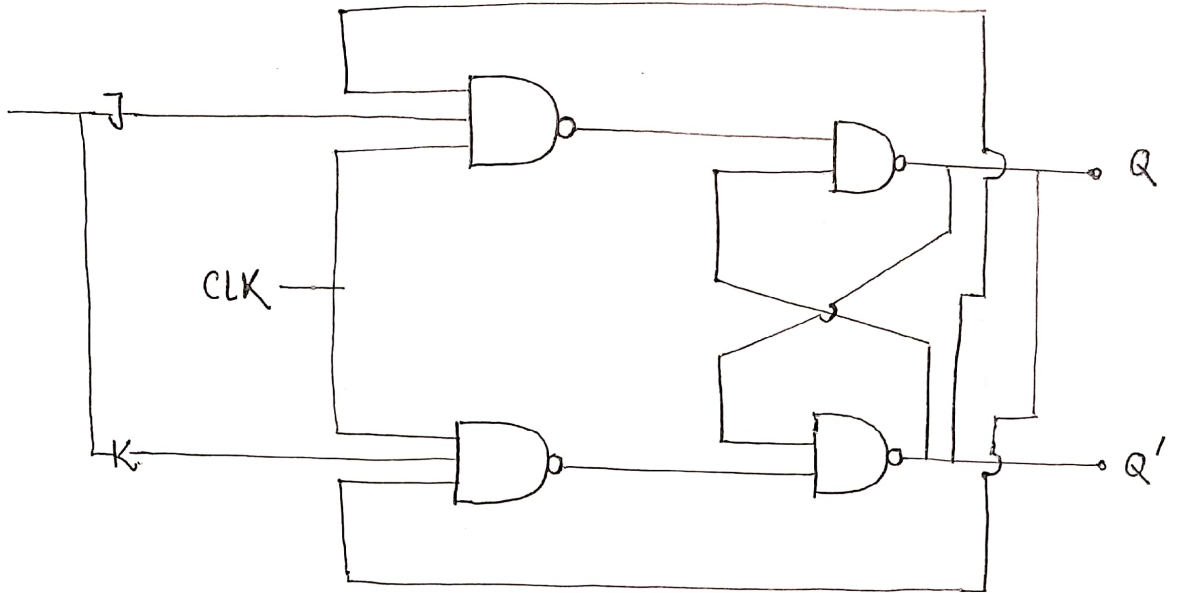
CLK	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	$\overline{Q_n}$

characteristic table :

$$Q_{n+1} = Q_n \oplus T$$

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q2. Design a SISO and PIPO shift register.

Sol:

● 4-Bit SISO register :-

Serial data IN

clock

FFA D Q
CLK

FFB D Q
CLK

FFC D Q
CLK

FFB D Q
CLK
Q ← serial data OUT

● 4-Bit PIPO Register :-

4-bit parallel output

Q_D Q_C Q_B Q_A

CLOCK

P_D P_C P_B P_A

4-Bit parallel data Input
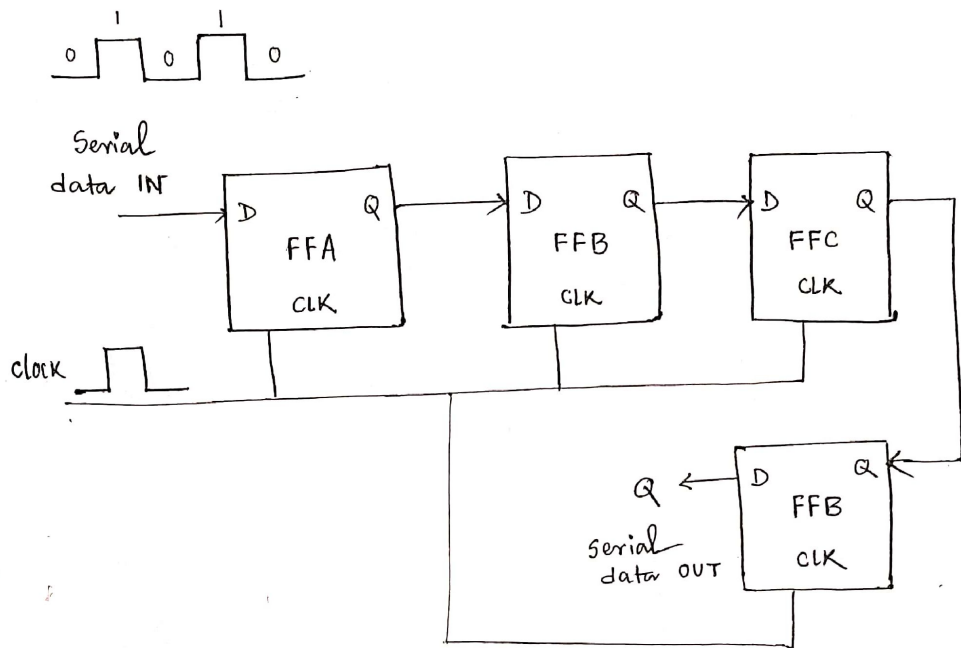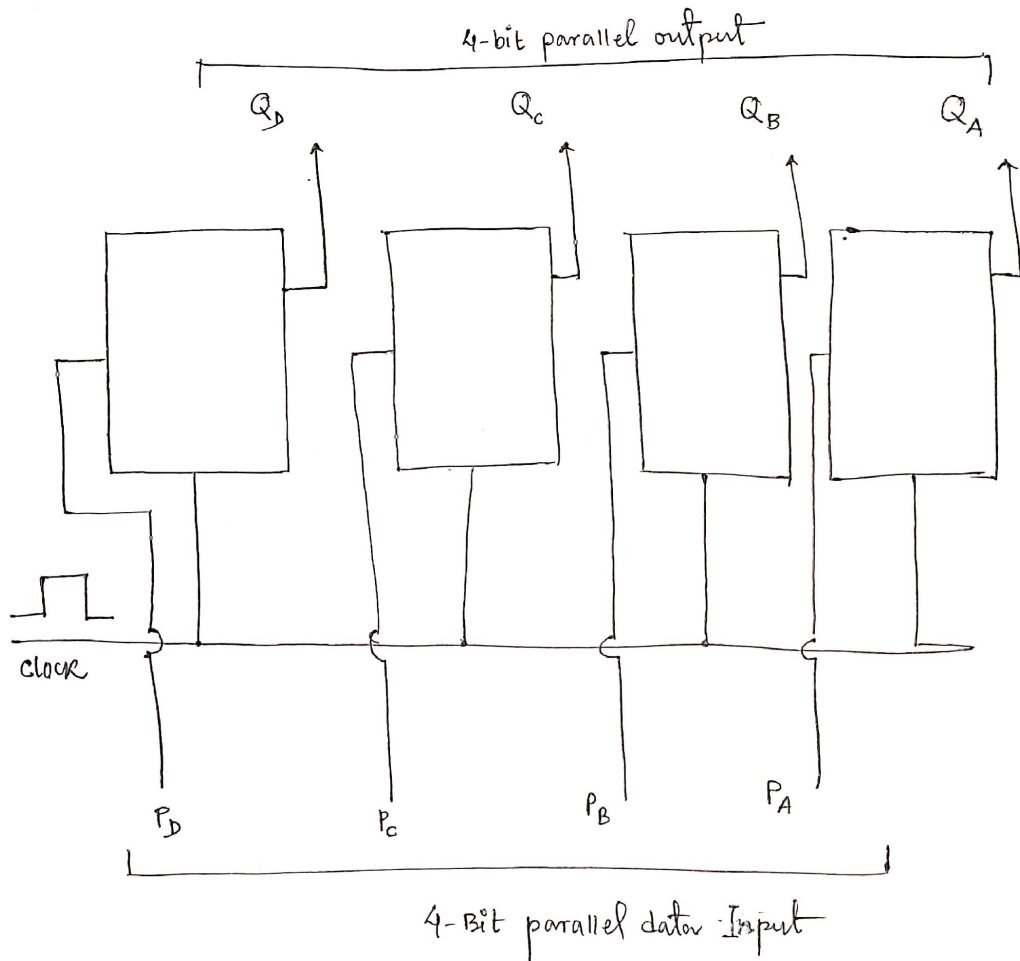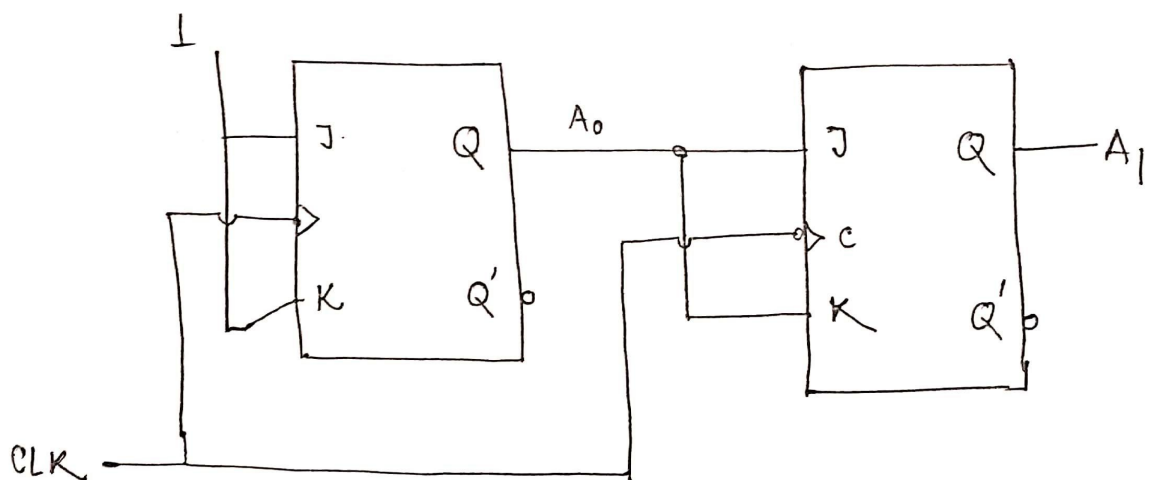
Q3. Design a 2-bit Counter.

Soln

Designing a 2-Bit counter (synchronous) using J & K Flip-flop :-

present state		Next state		Flip-flop Inputs	
A_1	A_0	A_1^+	A_0^+	TA_1	TA_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

$$TA_1 = A_0$$
$$TA_0 = 1$$