Basic Electrical & Electronics Engineering (EEE 1001)

Slot: A1 | Fall Semester 2019 | SJT 322

Digital Assignment – 2

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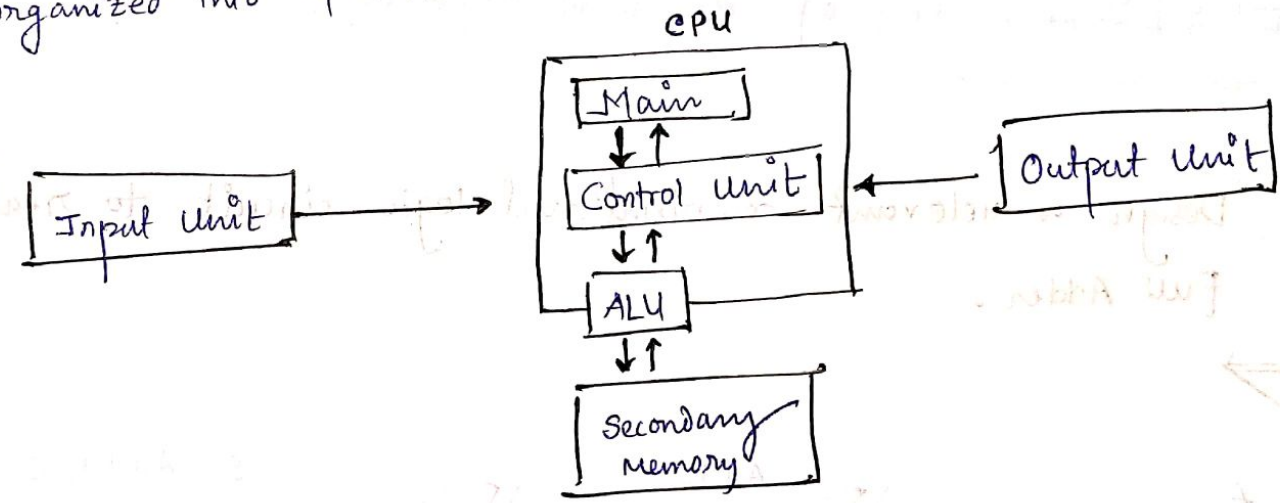
Q1. With a neat block diagram, explain the organization of a digital computer.

⟹ Organization of a computer:

A computer is a fast and accurate device, which can accept data, store data, process them and give, desired results as output. The computer is organized into 4 units as drawn in the following diagram:



• Input Unit:

Any device designed to assist in the entry of data into a computer is known as input device. Input devices convert data from any convenient external format into binary codes that a computer can store and manipulate internally. Some of the most common, most popularly used devices are following :—

(a) Mouse
(b) Light pen
(c) Touch screen
(d) Keyboard
(e) Scanner
(f) OCR and MICR
(g) Bar Code Generator
(h) Joy Stick, etc.

Output Unit :

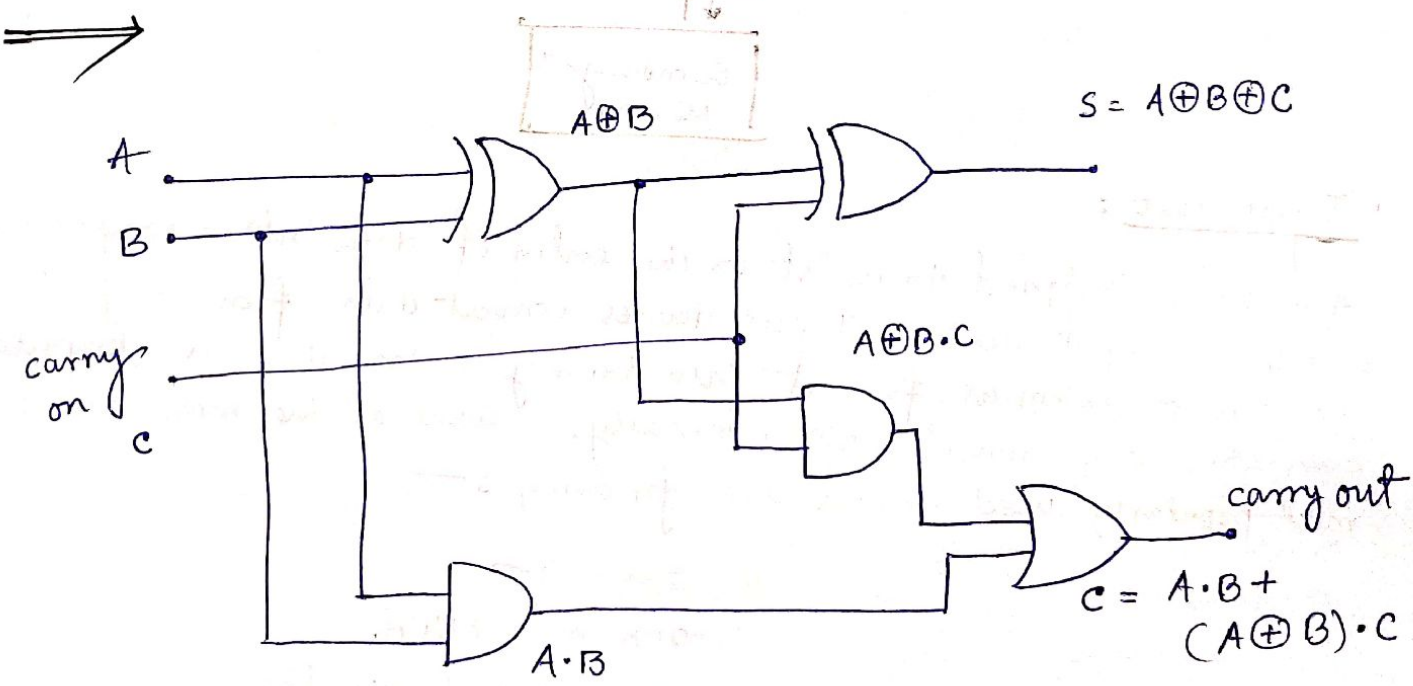
Any peripheral device that converts the stored binary coded data into convenient external forms as text and pictures are known as Output devices.

e.g. a) visual display unit (Monitor)
b) printer
c) plotters, etc.

• Central Procesing Unit :

The CPU is the heart of the computer combined in the system with the procesing system of a computer. The CPU carries out actions with information help of Arithmetic Logic Unit (ALU).

Q2. Design a relevant combinational logic circuit to realize Full Adder.



Truth Table:

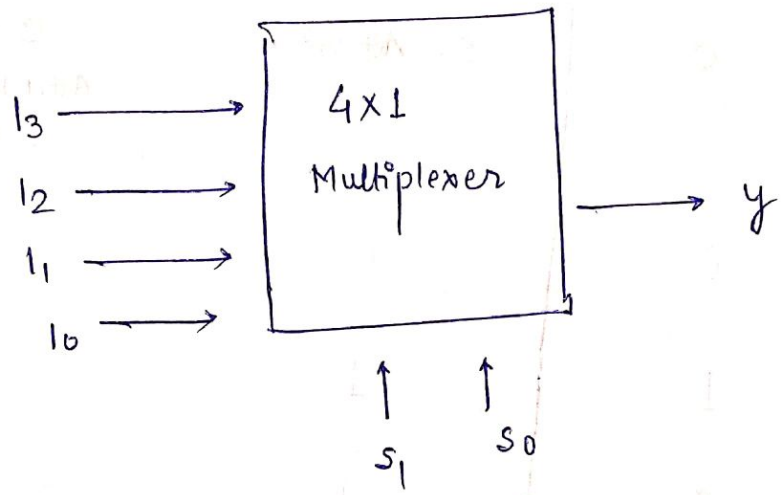
A	B	C	$S = A \oplus B \oplus C$	$C = (A \oplus B) \cdot C + A \cdot B$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Q3. Explain the 4 in 1 MUX & 1 in 4 DEMUX with necessary logic circuits and truth table.

⟹

4×1 Multiplexer

4×1 Multiplexer has four data inputs I_3, I_2, I_1, and I_0, two selection lines S_1 and S_0 and one output y. the block diagram of 4×1 Multiplexer is shown in the following figure :—



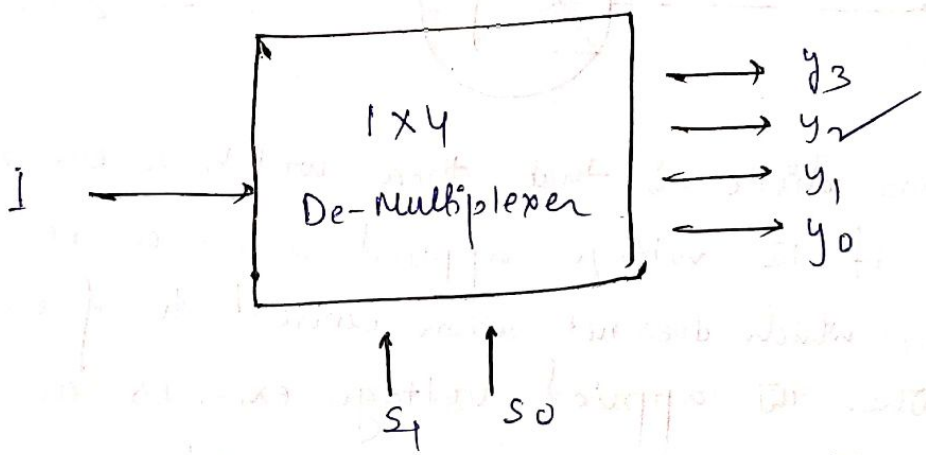
One of these 4 inputs will be connected to the output based on the combination of inputs present at these 2 selection lines. Truth table of 4×1 multiplexer is shown :—

Selection lines		output
S_1	S_0	y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

1×4 De Multiplexer

1×4 De-Multiplexer has one input I and 2 ~~input~~ selection lines S_1 and S_0 and 4 outputs y_3, y_2, y_1 and y_0.

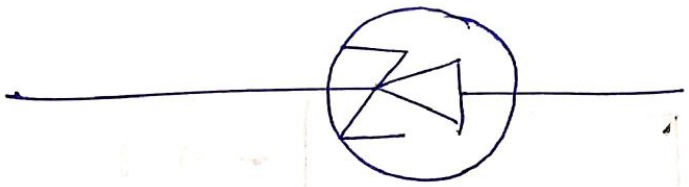
The block diagram of 1×4 De-Multiplexer is shown in the following figure :-



The single input 'I' will be connected to one of the 4 outputs, y_3 to y_0 based on the values of selection lines S_1 and S_0. The truth table of 1×4 De-Multiplexer is shown below :-

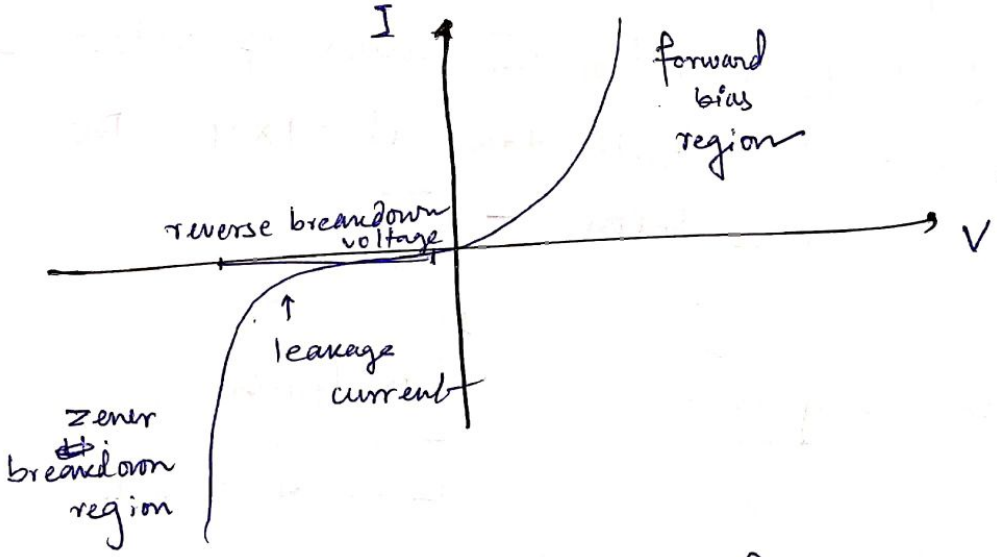
Selection Inputs		Outputs			
S_1	S_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Q4. Draw the VI characteristics of Zener diode & explain its operation with diagram in forward biased and reverse biased region.

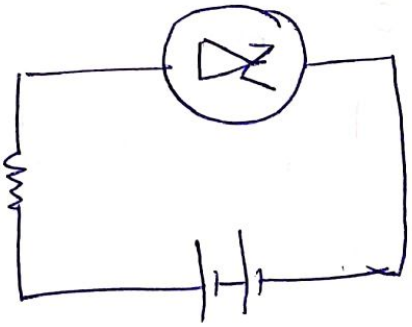


⇒ Zener diode

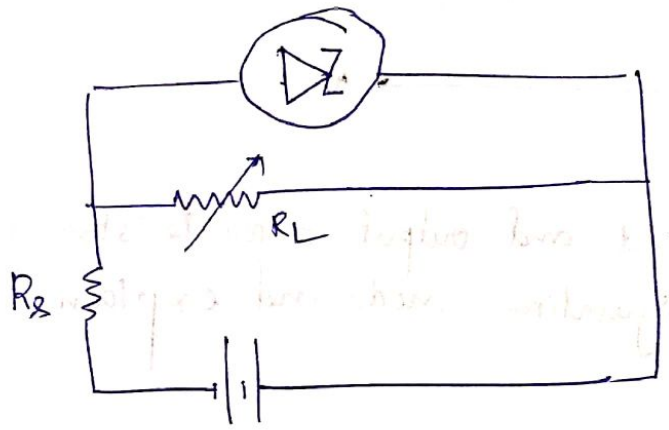
Property of zener diode is that there will be a breakdown in the circuit if the voltage applied across a reversely biased circuit, which does not allow current to flow across it. When the applied voltage exceeds an specifier amount zener breakdown takes place.



Forward bias → when Zener diode is forward biased, it behaves just like a normal signal diode



Reverse bias → when Zener diode is reverse biased, it behaves like a voltage regulator.



Q5. Explain the operation of forward biased PN junction diode.

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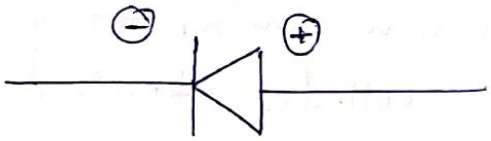
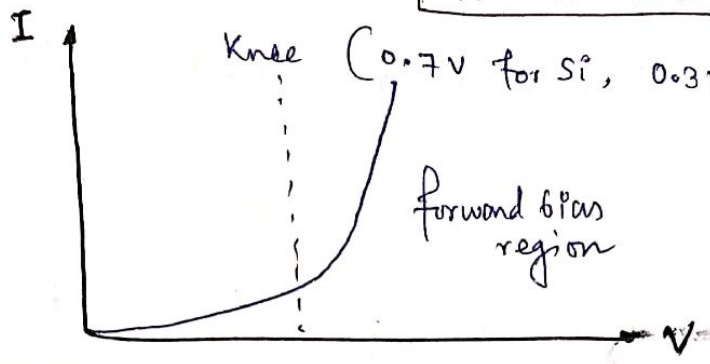


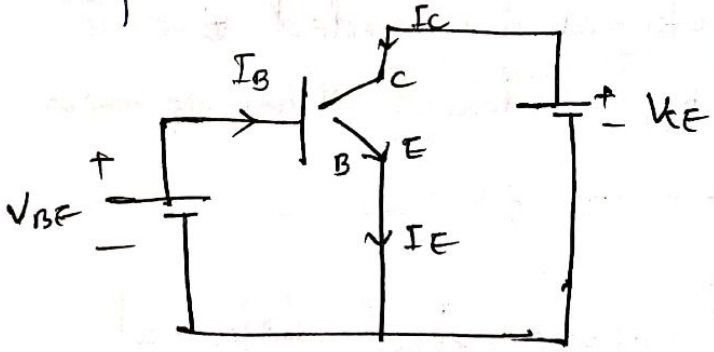
Forward bias → The voltage potential is connected ⊕ve to p-type material & ⊖ve to N-type material which decreases PN junction diodes' width.

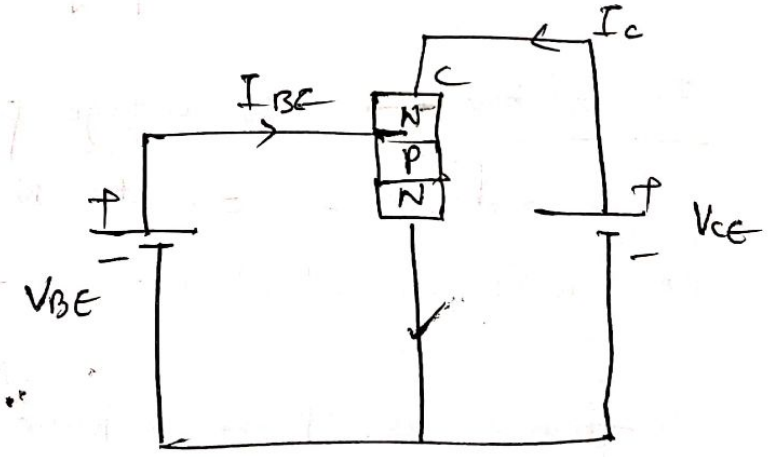
In forward bias, if the external voltage exceeds potential barrier (0.7 V for Si) (0.3 V for Ge) current will start to flow. This is because ⊖ve voltage pushes or repels electrons towards the junction giving them the energy to crossover and combine with the holes being pushed in opposite direction.



Q6. Explain the input and output characteristics of BJT with CE configuration mode and explain different region.

⟹ In common emitter configuration base is the input terminal, collector is the output terminal and emitter is the common terminal for both input and output. That means the base terminal and common emitter terminal are known as input terminals whereas collector terminal are known as output terminals.





CE config.

The CE amplifier are used when large current gain is needed. The input signal is applied between the base and emitter terminals while the output signal is taken between the collector and emitter terminals. Thus, the emitter terminals of a transistor is common for both input and output and hence it is named as CE configuration.

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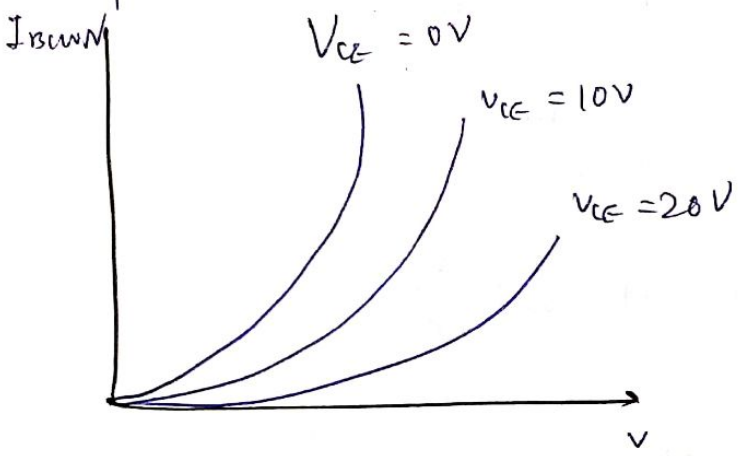
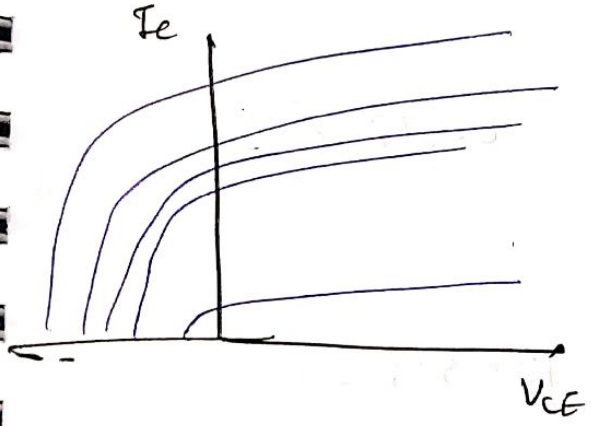
Input characteristics



There describe the changes in input current with the variations in the values of input voltage keeping the output voltage constant due to forward bias.

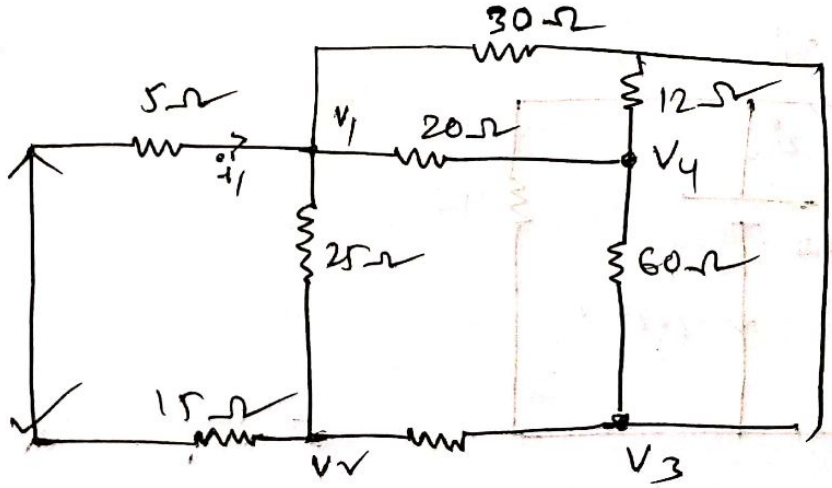
Output characteristics



This is a plot of output current vs output voltage with constant input current.

As we know that the V_{CE} emitter-base function is already forward biased, ∴, when thus the junctions are forward biased.

Q7.



Let V = 10 V

$$\frac{V_1 - 10}{5} + \frac{V_1 - V_2}{25} + \frac{V_1 - V_4}{20} = \frac{V_3 - V_1}{30}$$

$$\frac{V_3 - V_2}{10} + \frac{V_3 - V_1}{30} = \frac{V_4 - V_3}{12} + \frac{V_4 - V_3}{60}$$

$$\frac{V_4 - V_3}{12} + \frac{V_4 - V_3}{60} = \frac{V_1 - V_4}{20}$$

$$\frac{V_2 - 10}{15} = \frac{V_1 - V_2}{25} + \frac{V_3 - V_2}{10}$$

$V_1 = 5.94\ V$

$V_2 = -2.57\ V$

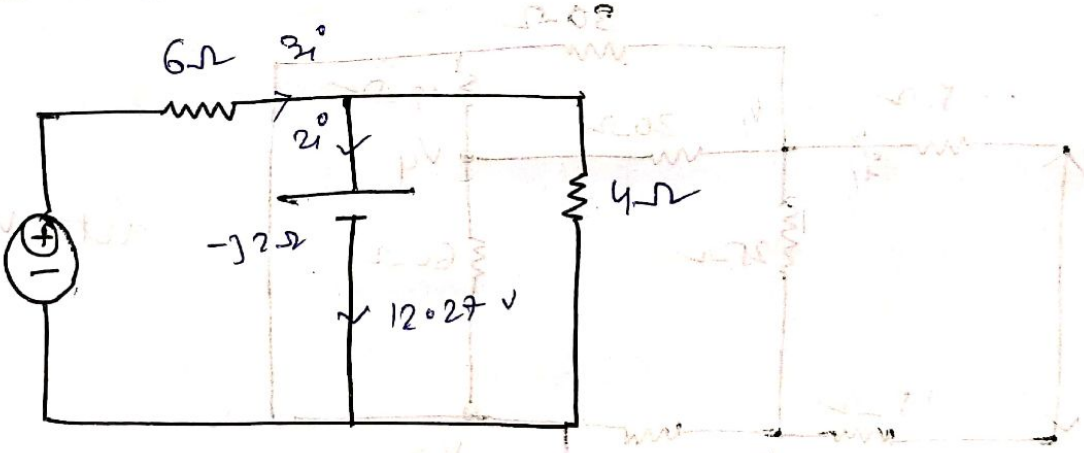
$V_3 = 0.61\ V$

$i_1 = \frac{10 - 5.94}{5}\ A = 0.812\ A$

$V = IR$

$Req = \frac{10}{0.812}\ \Omega = 12.315\ \Omega$

Q 8



$Req = 6 + 4 \parallel 2$

$= 6 + \frac{4 \times 2}{4 + 2}$

$= 6 + \frac{8}{3} = \frac{22}{3} = 7.\overline{33}$

$$i = \frac{30}{7.3} = 4.09$$

$$V_{6\Omega} = 6i = 24.54$$

$$i_{out} = 12.27 \cos(\theta + 90) + 6.135 \cos\theta$$

$$= 6.135 \left(2\cos(\theta+90) + \cos\theta\right)$$

$$= 6.135 \left(\frac{2}{\sqrt{5}} \sin\theta + \frac{1}{\sqrt{5}} \cos\theta\right)$$

$$= 6.135 \left(\sin(\theta + 26.56)\right)$$

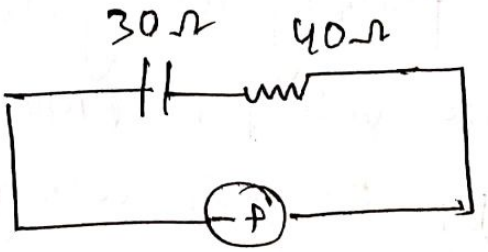
$$= 6.135 \left(\cos(\theta - 63.43)\right)$$

$$\phi = -63.43^\circ$$

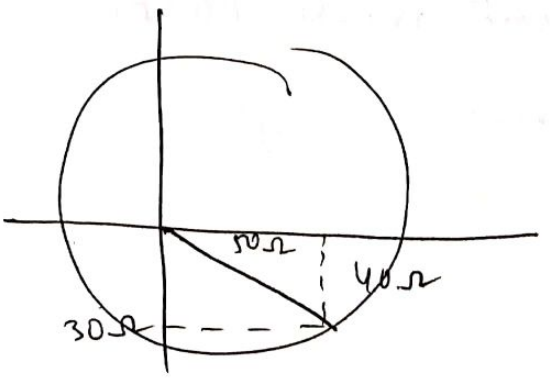
$$P = 30 \times 4.89 \cos\phi$$

$$P = 54.88\ W.$$

Q9.



$f = 60\ Hz.$



$$X_C = \sqrt{2500 - 1600}$$

$$= 30$$

$$Z = \sqrt{40^2 + 30^2}$$

$$= 50\ \Omega$$

$V = 3 \times 50\,V = 150\,V$

$\phi = \tan^{-1}\left(\frac{40}{30}\right) = 53^{\circ}$

$i = 3\,A$

$V_C = \frac{30}{3} = 10\,V$

$V_R = \frac{40}{3} = 13.73\,V$

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10 Ans :

Enhancement-mode MOSFETs (metal-oxide-semiconductor FETs) are the common switching elements in most integrated circuits. These devices are off at zero gate source voltage.

NMOS can be turned on by pulling the gate voltage higher than the source voltage, PMOS can be turned on by pulling the gate voltage lower than the source voltage. In most circuits, this means pulling an enhancement mode MOSFET's gate voltage towards its drain voltage to turns it ON

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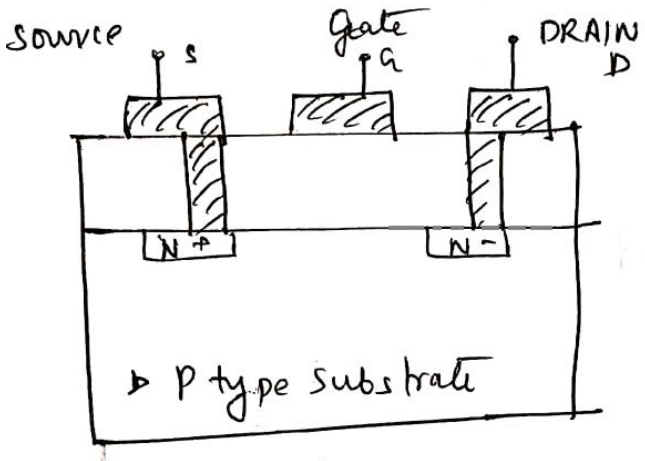
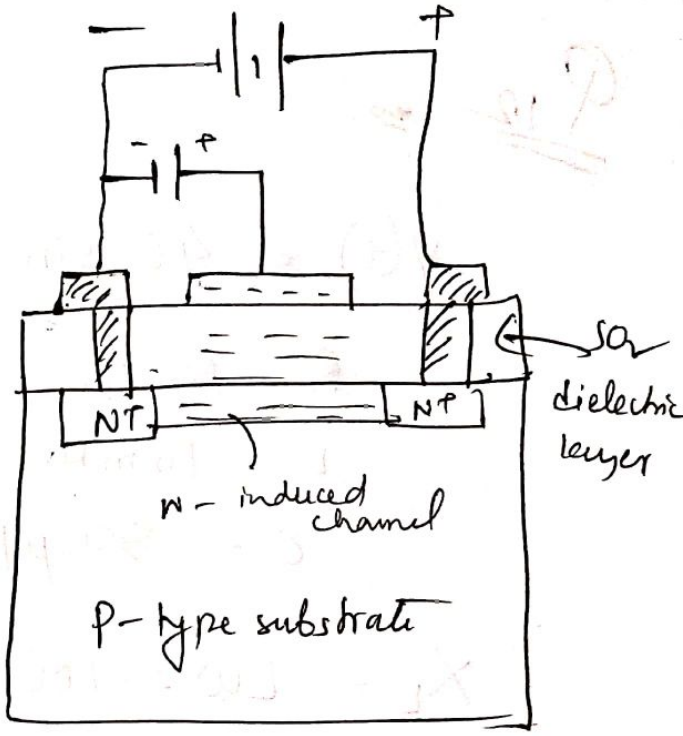


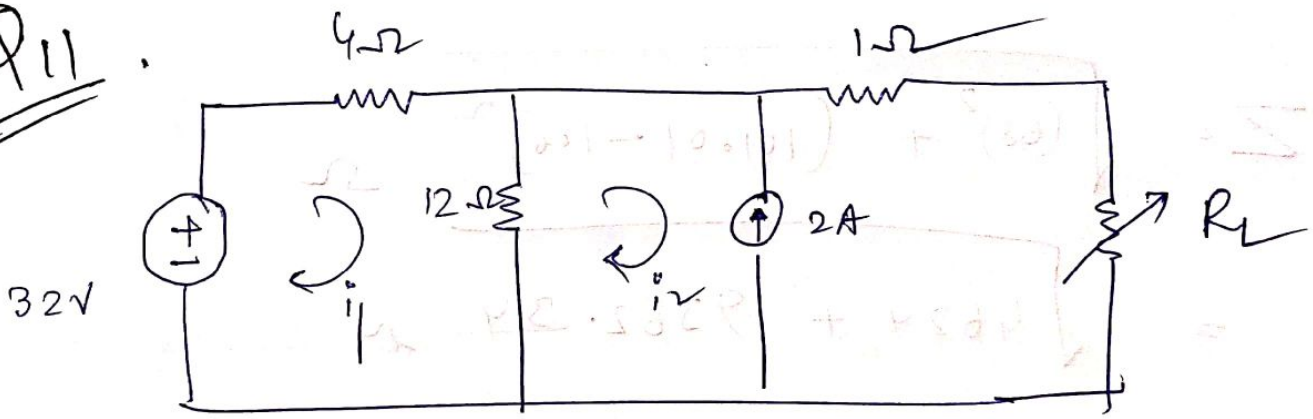
N – channel
E – MOSFET structure

▶ Construction of EMOSFET



▶ Working of an EMOSFET

Q11.



Using Mesh analysis,

$$32 - 4i_1 - 12(i_1 - i_2) = 0$$

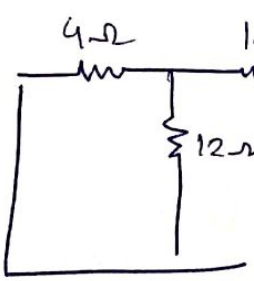
$$i_1 = 0.5\ A$$

$$i_2 = -2\ A$$

$$V_{Th} = 12(i_1 - i_2)$$

$$= 12(0.5 - (-2.0))$$

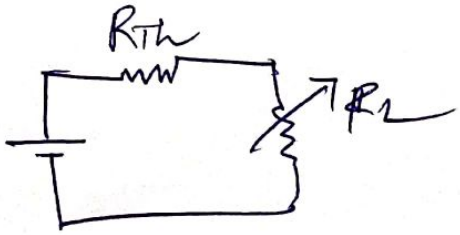
$$= 30\ V$$



$$R_{Th} = 4 \| 12 + 1$$

$$= 4\ \Omega$$

$\Rightarrow$



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Q12 Ans:

$V(t) = 40 \sin 100t$

$R = 68\ \Omega$

$L = 16\ mH$

$C = 99\ \mu F$

$X_L = L\omega = 100 \times 16 \times 10^{-3} = 1.6\ \Omega$

$X_C = \frac{1}{\omega C} = \frac{1}{100 \times 99 \times 10^{-6}} = \frac{10^4}{99}$

$= 101.01\ \Omega$

$Z = \sqrt{(68)^2 + (101.01 - 1.6)^2}\ \Omega$

$= \sqrt{4624 + 9382.34}\ \Omega$

$= \sqrt{14506.34}\ \Omega$

$= 120.45\ \Omega$

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$$I = \frac{40}{120.45} A = 0.33 A$$

$$\phi = \tan^{-1}\left(\left(\frac{R}{(X_L - X_C)}\right)^{-1}\right)$$

$$= \tan^{-1}\left(\frac{X_L - X_C}{R}\right)$$

$$= \tan^{-1}\left(\frac{101.01 - 1.6}{68}\right)$$

$$\phi = 55.6^{\circ}$$