CSE 1003

DLD

Assessment – 2

L27+L28

WINTER SEMESTER 2019–20

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by

SHARADINDU ADHIKARI

19BCE2105

Question 1

Aim: To design a half-subtractor using NAND implementation.

Truth Table:

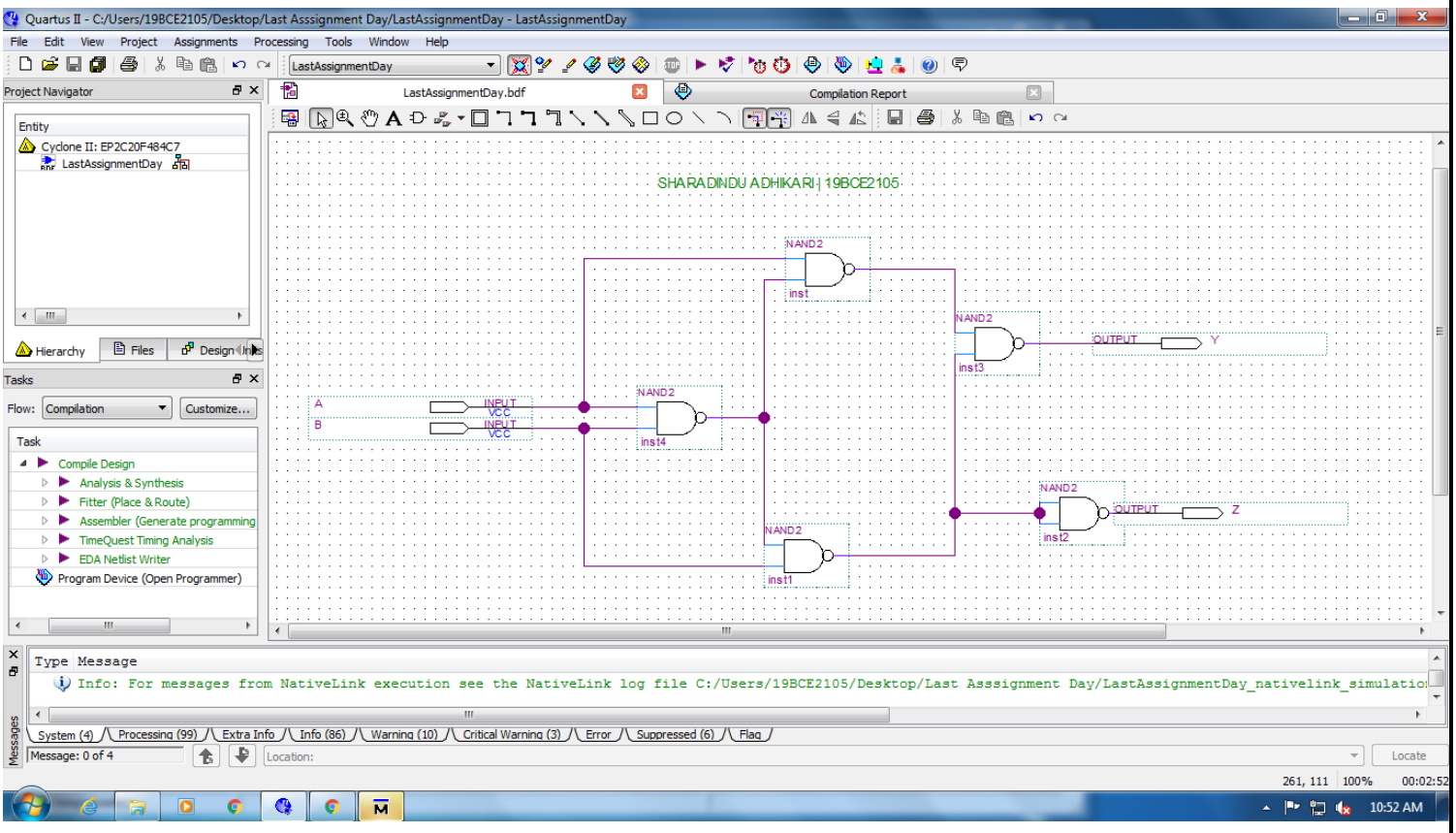
A	B	Difference (Y)	Borrow (Z)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Boolean expression:

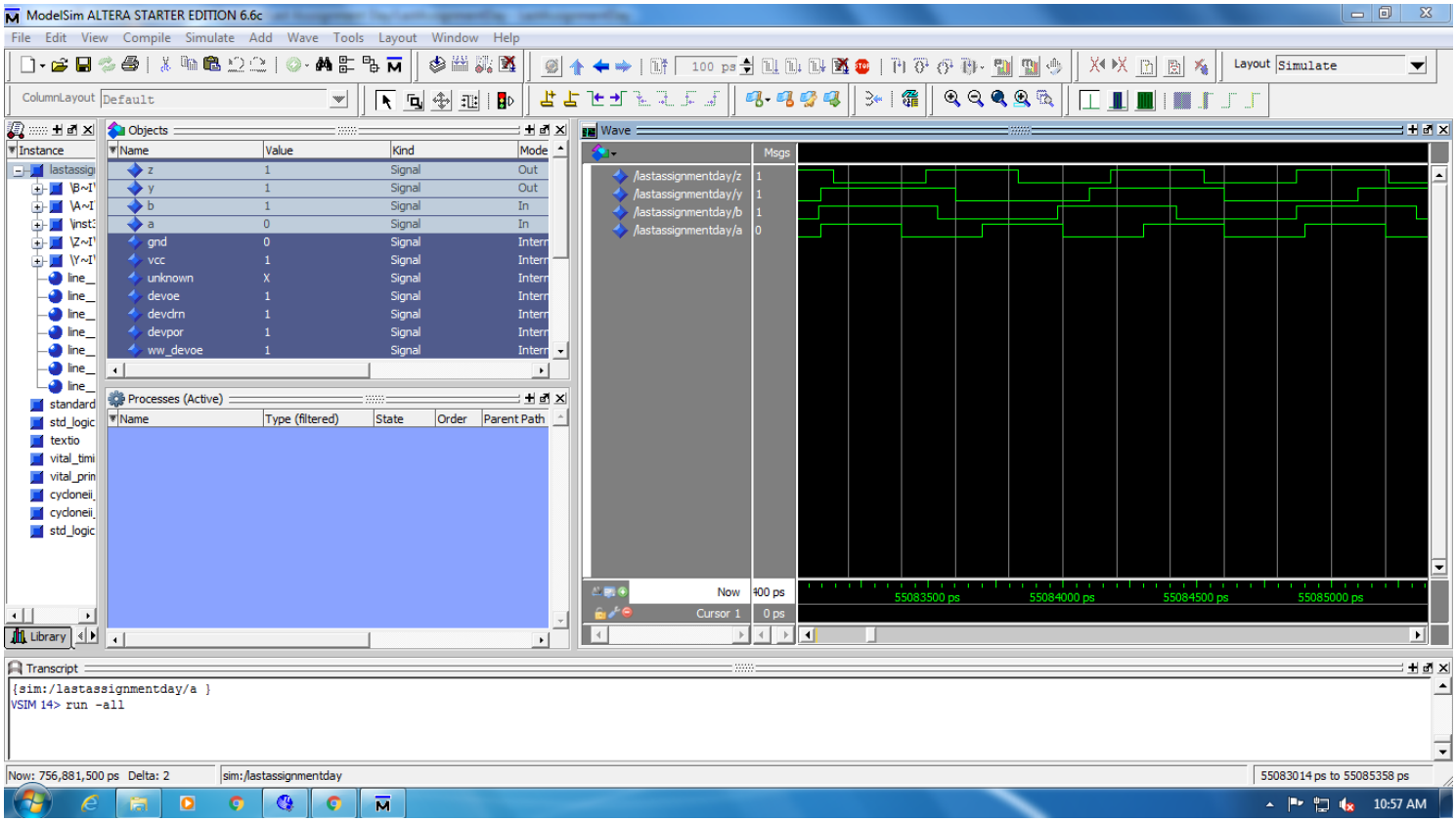
Difference = $A \oplus B$

Borrow = $\overline{A}B$

Logic diagram:



Final output screen:



Test case: Forced the values of **a** & **b** as **0** & **1** respectively.

Result: The half-subtractor using NAND implementation has been verified in Quartus-II ModelSim Altera.

Question 2

Aim: To design a combinational circuit with three inputs: x, y, and z, and three outputs: A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

TruthTable:

X	Y	Z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

Boolean expression:

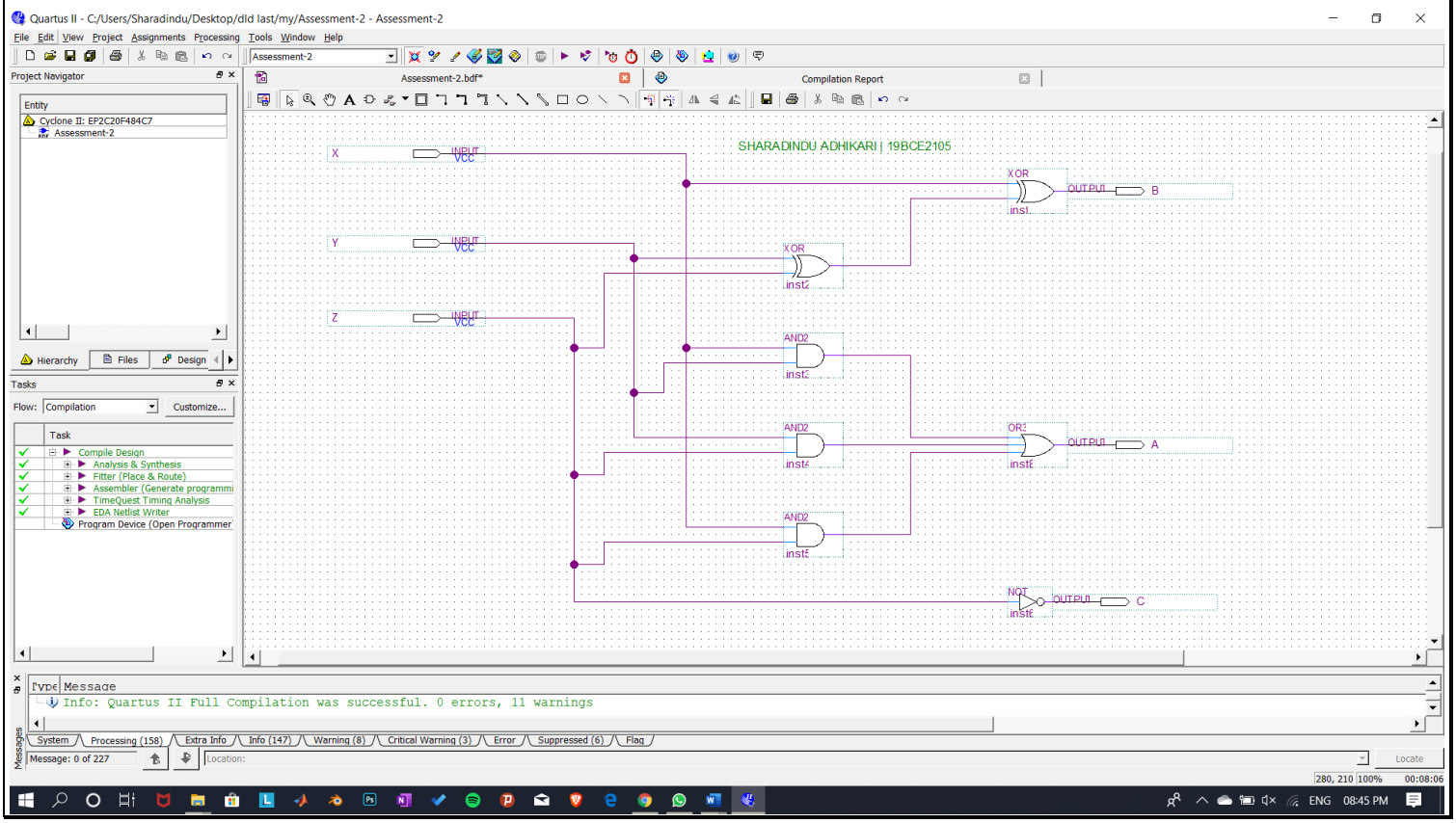
$A = xz + yz + xy$

$B = x \oplus (y \oplus z)$

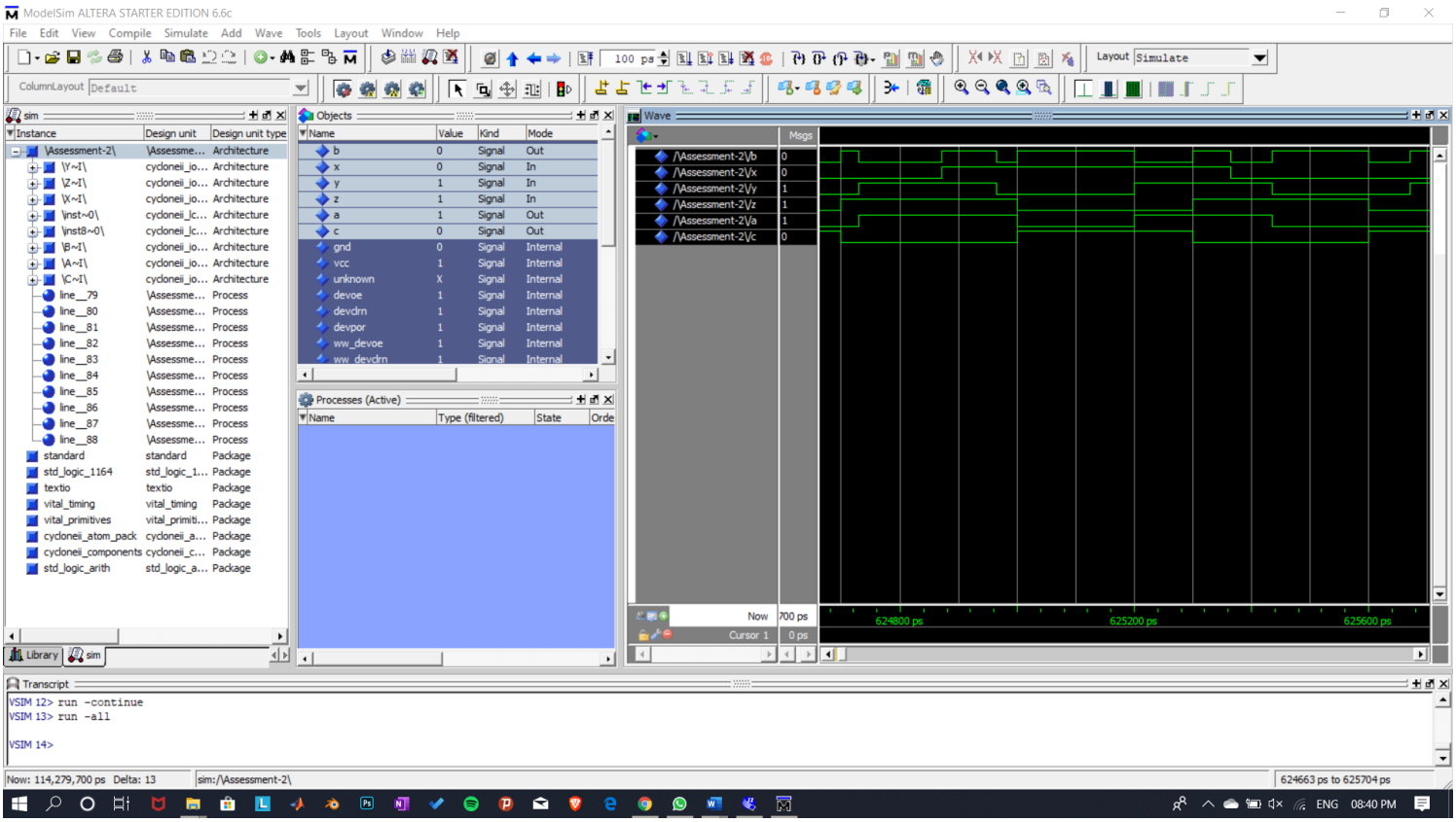
$C = \bar{z}$

[In case of full adder, B = sum, A = carry]

Logic diagram:



Final output screen:



Test case: Forced the values of **`x`**, **`y`**, & **`z`** as **`0`**, **`1`**, & **`1`** respectively.

Result: The combination circuit has been verified in Quartus-II ModelSim Altera.

Question 3

Aim: To design a full adder using two half adders.

Truth Table:

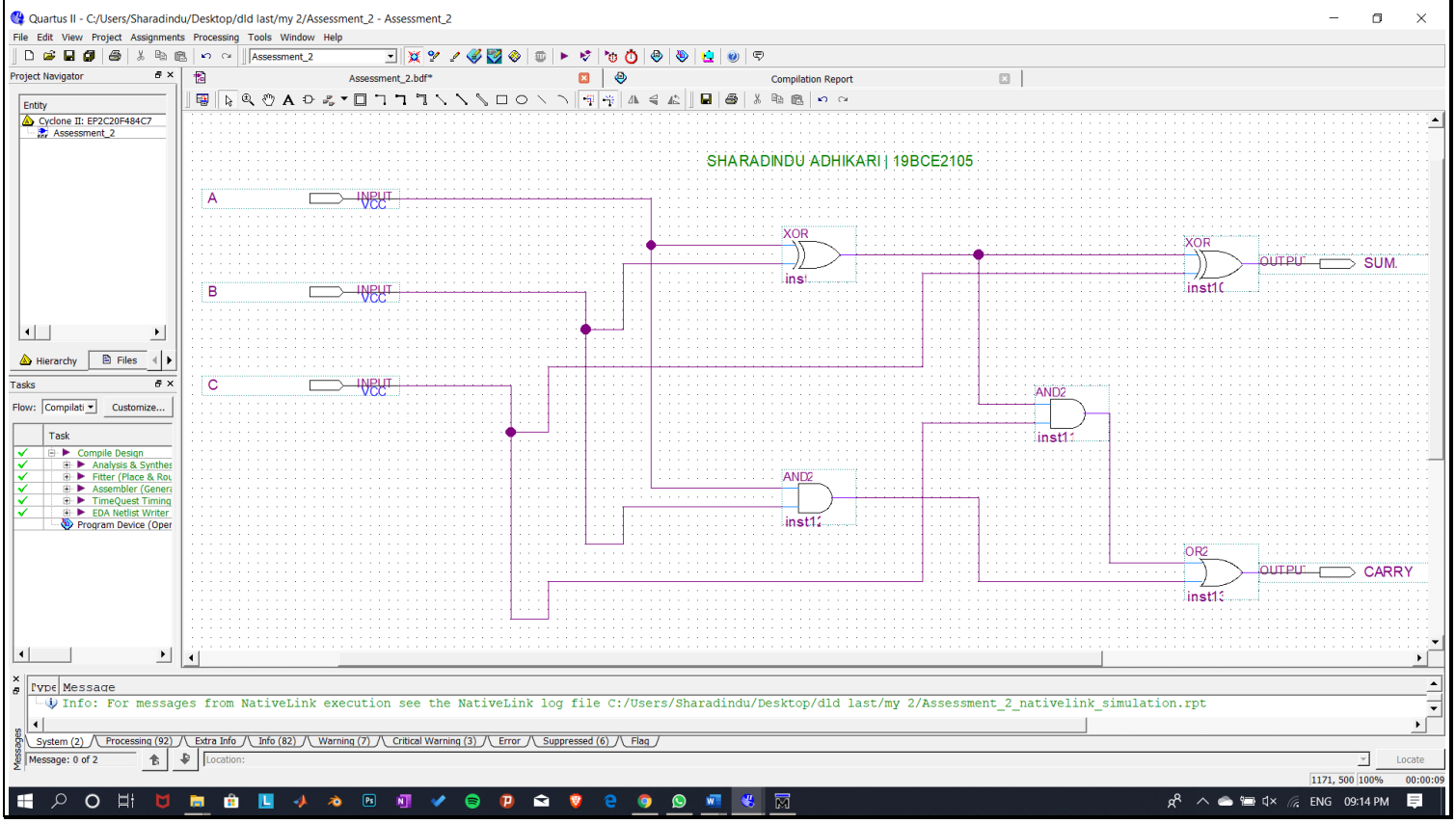
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean expression:

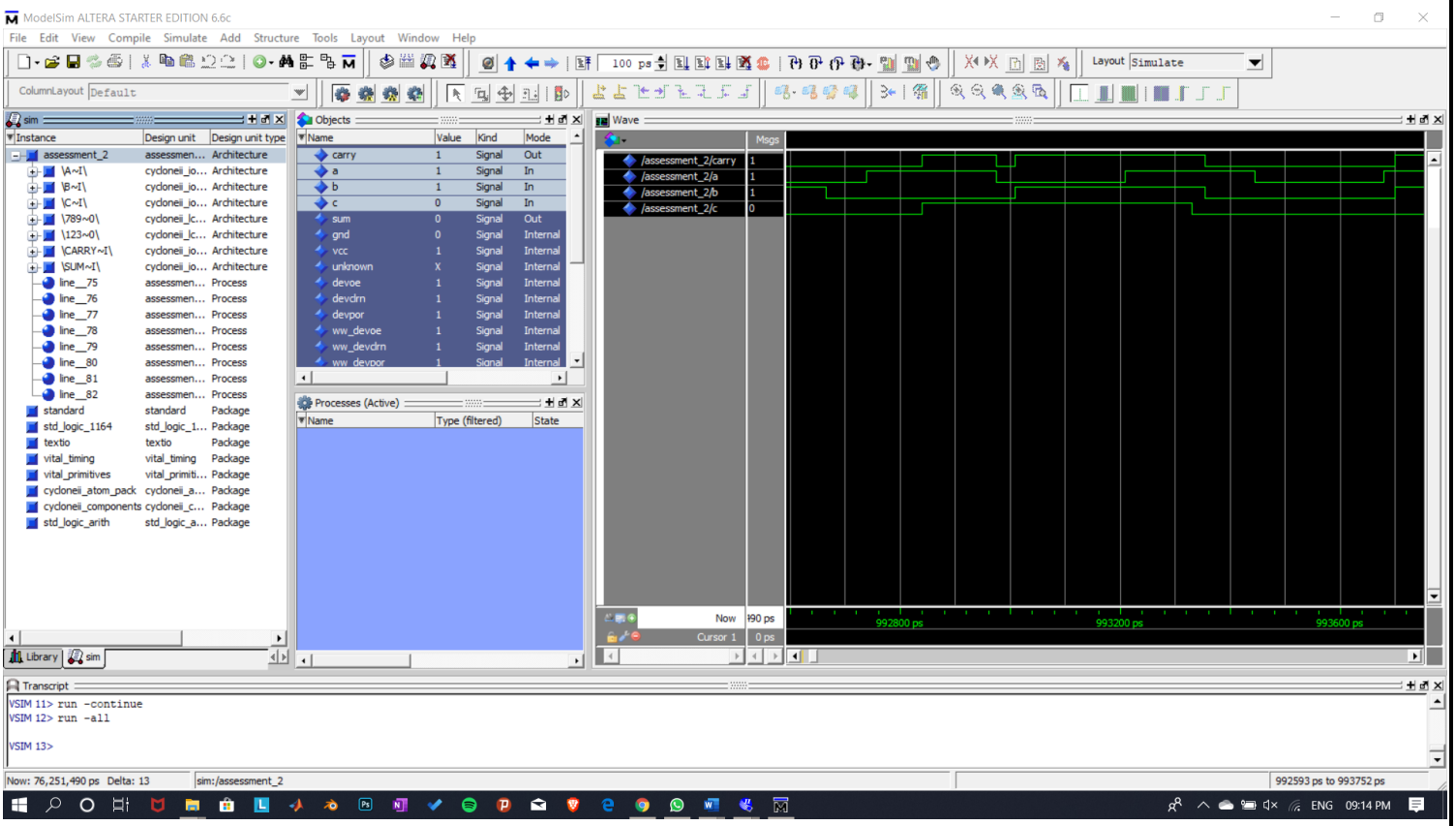
$$\text{Sum} = A \oplus B \oplus C$$

$$\text{Carry} = AB + (A \oplus B) \cdot C$$

Logic diagram:



Final output screen:



Test case: Forced the values of **a, b,** & **c** as **1, 1,** & **0** respectively.

Result: The full adder using two half adders has been verified in Quartus-II ModelSim Altera.

_____end_____