

CSE 1003

DLD



Assessment – 1

L27+L28

WINTER SEMESTER 2019–20

December 20, 2019

by

SHARADINDU ADHIKARI

19BCE2105

Verification of Logic gates

1. AND gate:

Quartus II - C:/19BCE2105/NEW/Day2 - Day2

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Day2.bdf

Entity Cyclone II: EP2C20F484C7 Day2

Hierarchy Files Design Units

Tasks Flow: Compilation Customize...

Task

- ✓ ▶ Compile Design 0
- ✓ ▶ Analysis & Synthesis 0
- ✓ ▶ Fitter (Place & Route) 0
- ✓ ▶ Assembler (Generate programming files) 0
- ✓ ▶ TimeQuest Timing Analysis 0
- ✓ ▶ EDA Netlist Writer 0
- Program Device (Open Programmer)

Type Message

Info: Quartus II Full Compilation was successful. 0 errors, 20 warnings

System Processing (135) Extra Info (118) Warning (14) Critical Warning (3) Error Suppressed (6) Flag

Messages: 0 of 199

ModelSim ALTERA STARTER EDITION 6.6c

File Edit View Compile Simulate Add Wave Tools Layout Window Help

ColumnLayout Default

sim Objects Processes (Active)

Name	Value
z	0
a	1
b	0
gnd	0
vcc	1
unknown	X
devoe	1
devdrn	1
devpor	1
ww_devoe	1
ww_devdrn	1

Wave

Now 700 ps Cursor 1 0 ps

Transcript

VSIM 23> run
VSIM 24> run
VSIM 25>

Now: 1,700 ps Delta: 0 sim:/practice2

86 ps to 1415 ps

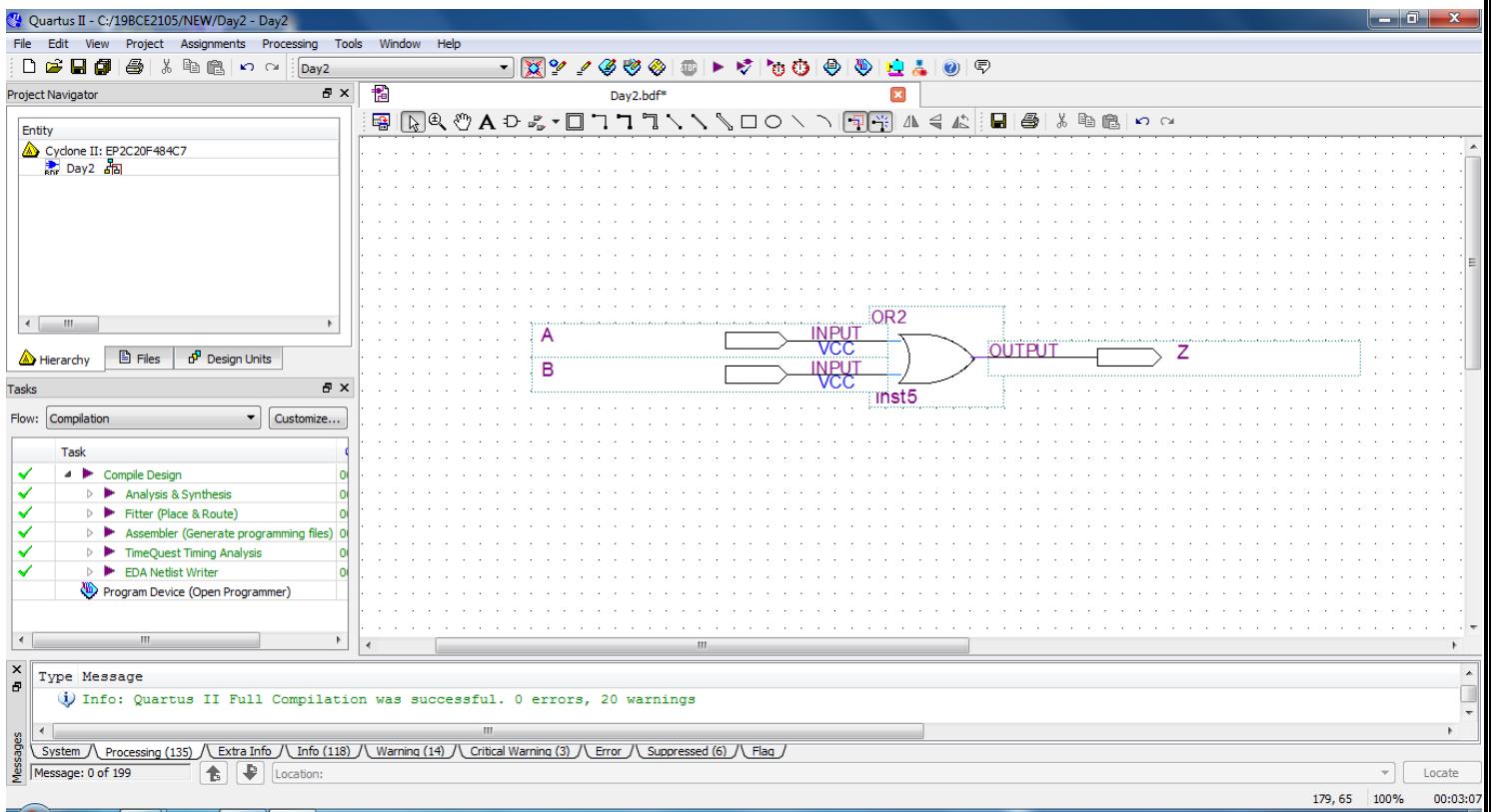
10:47 AM

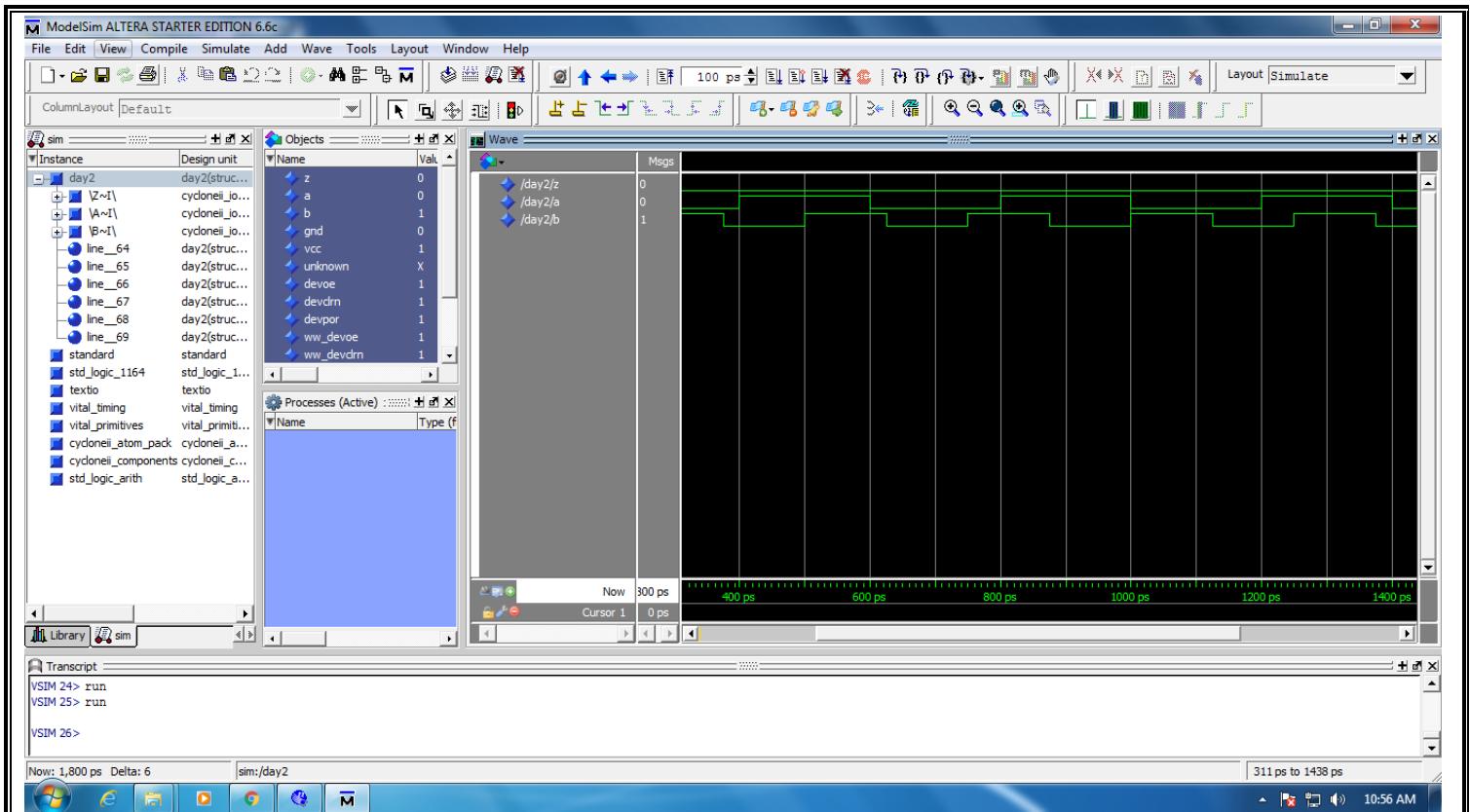
Boolean algebraic expression: $Z = A \cdot B$

Truth Table:

Input		Output
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

2. OR gate:



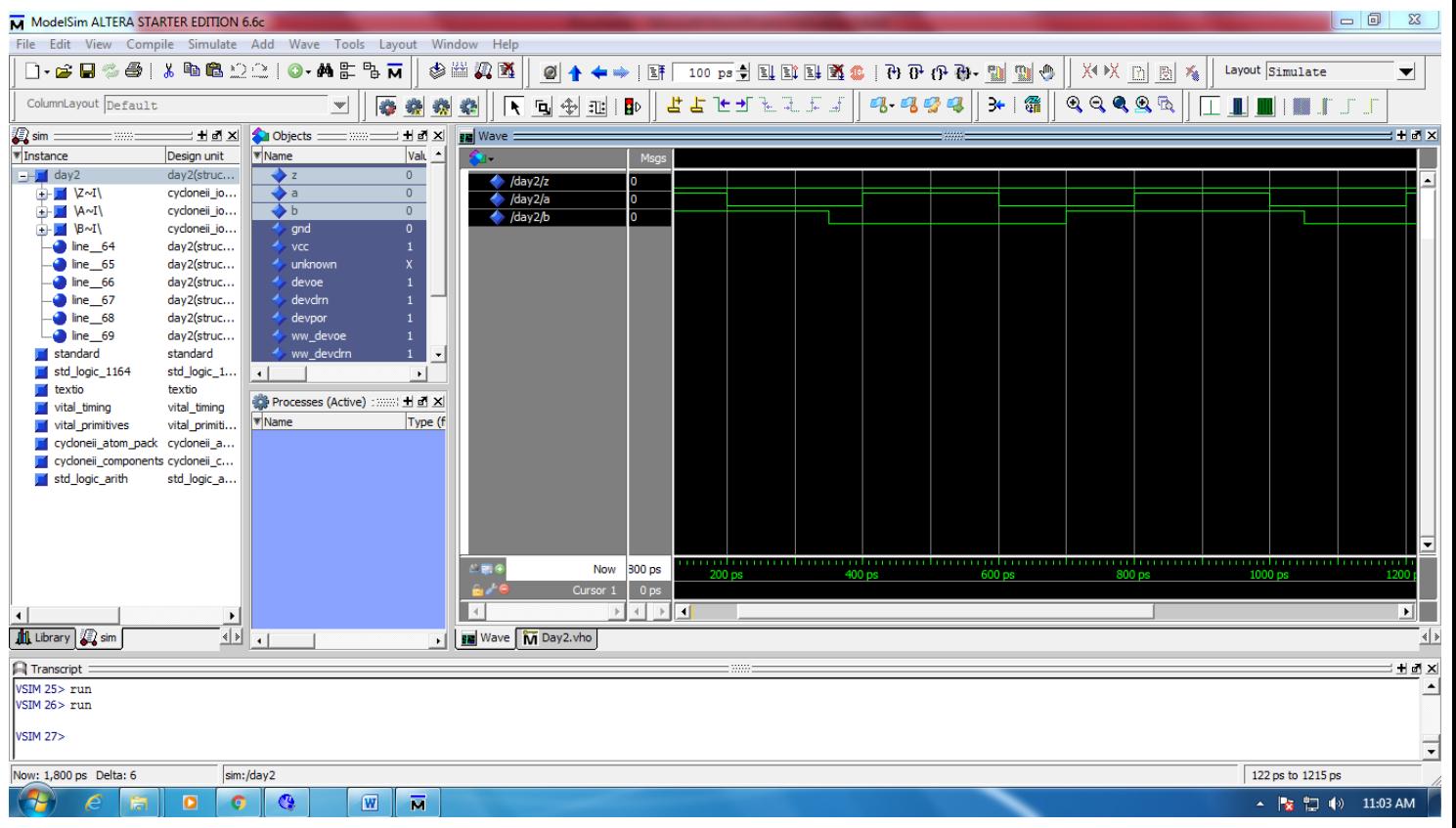
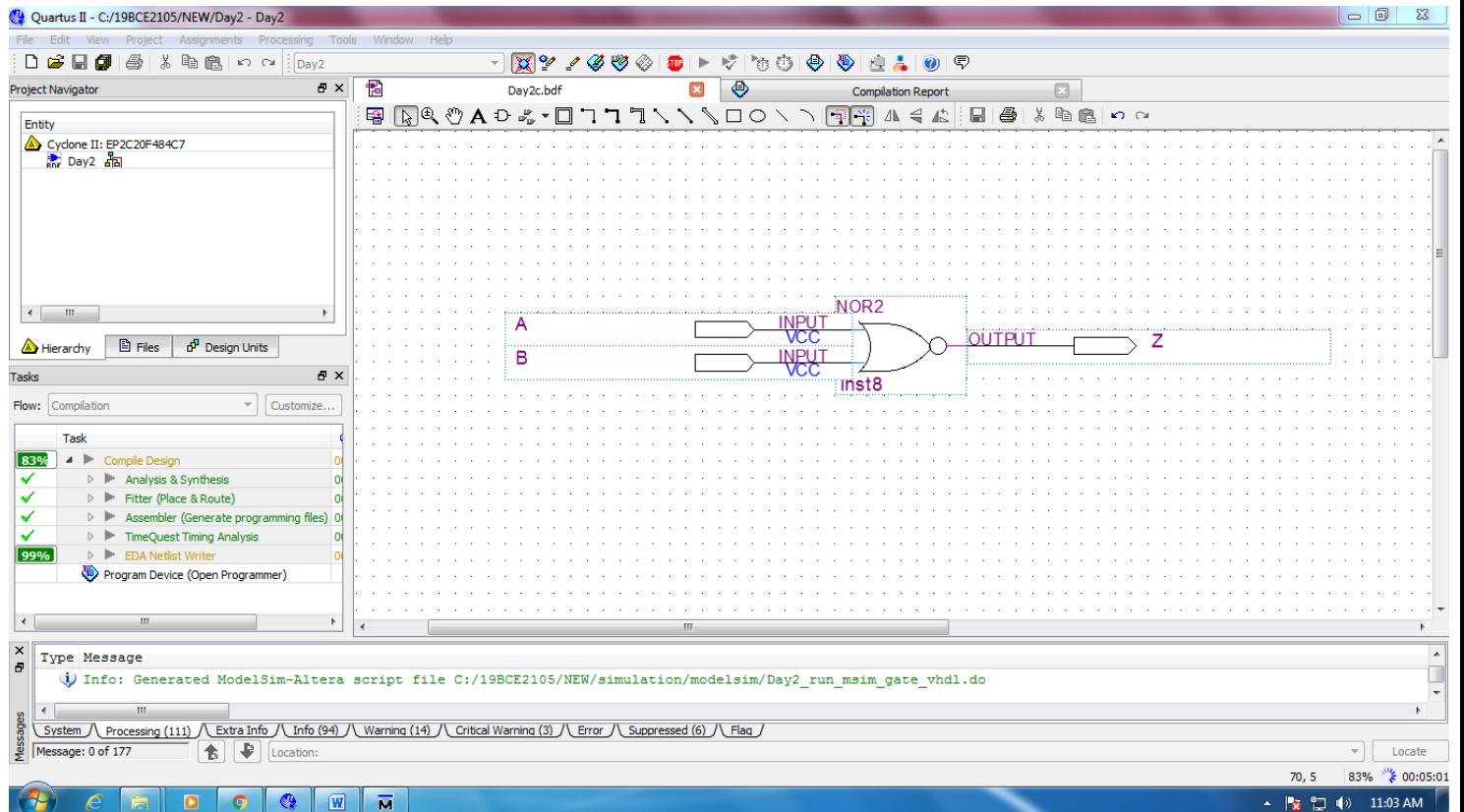


Boolean algebraic expression: $Z = A + B$

Truth Table:

Input		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

3. NOR gate:

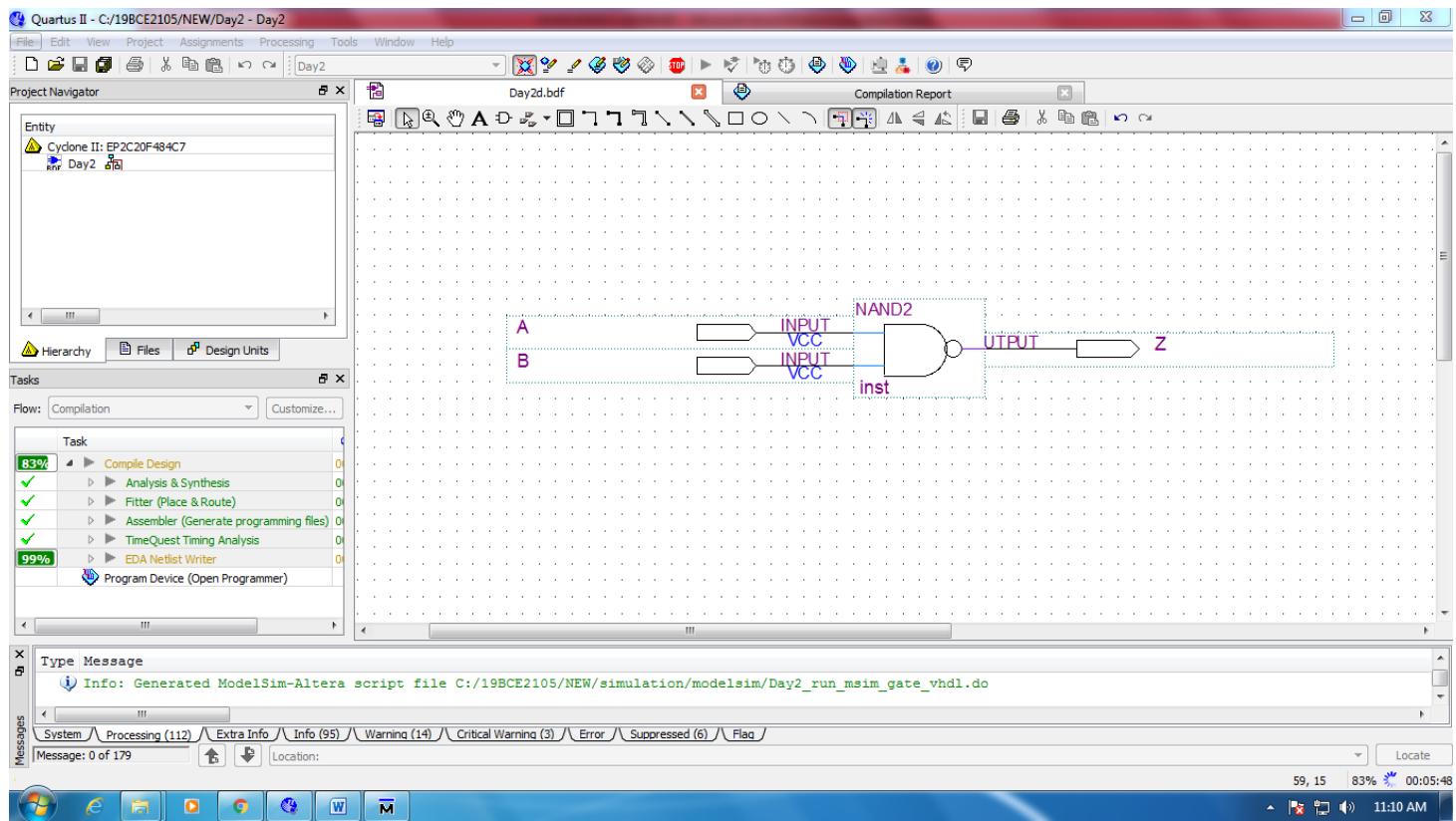


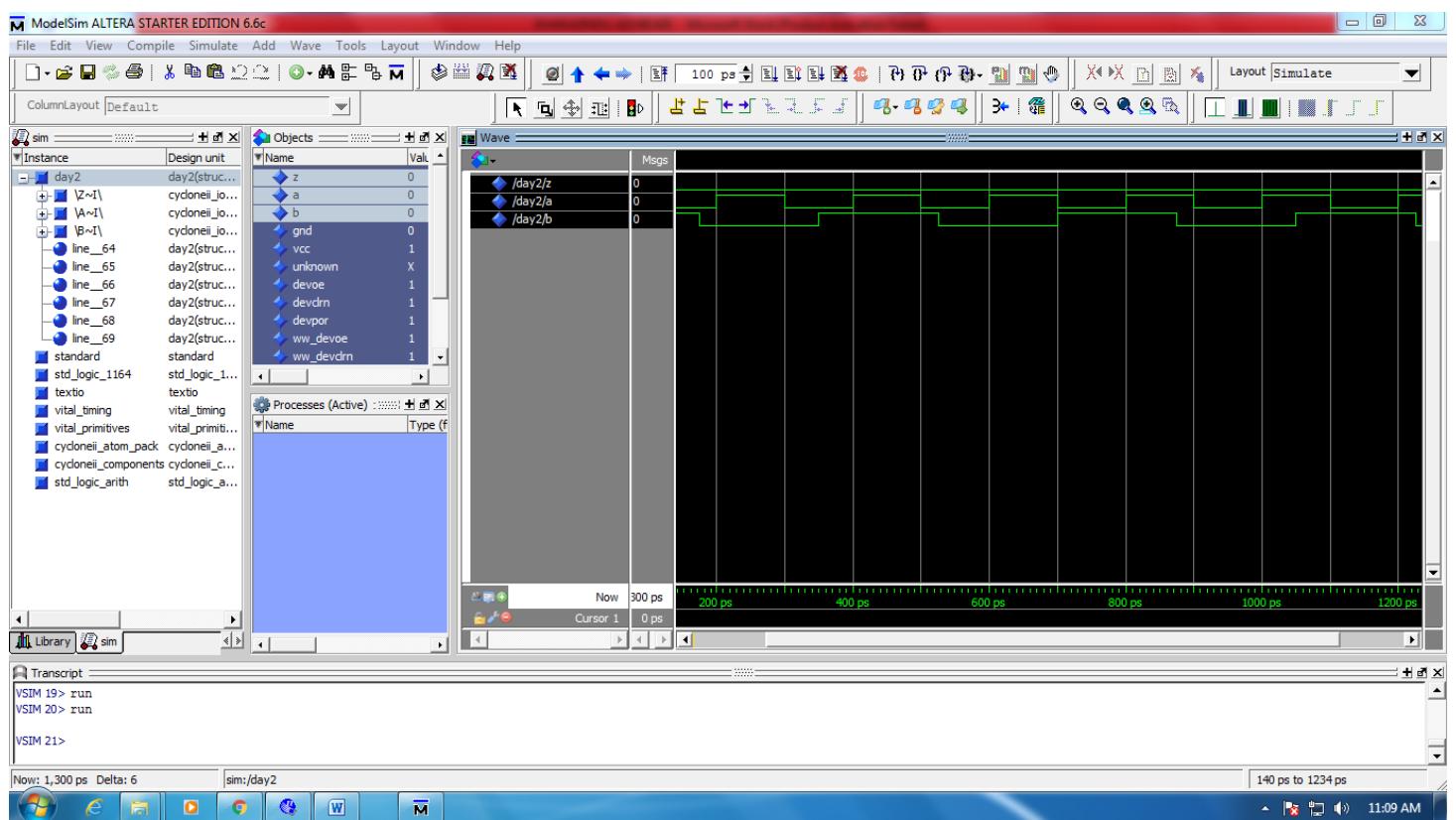
Boolean algebraic expression: $Z = \overline{A + B} = \overline{A} \cdot \overline{B}$

Truth Table:

Input		Output
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

4. NAND gate:



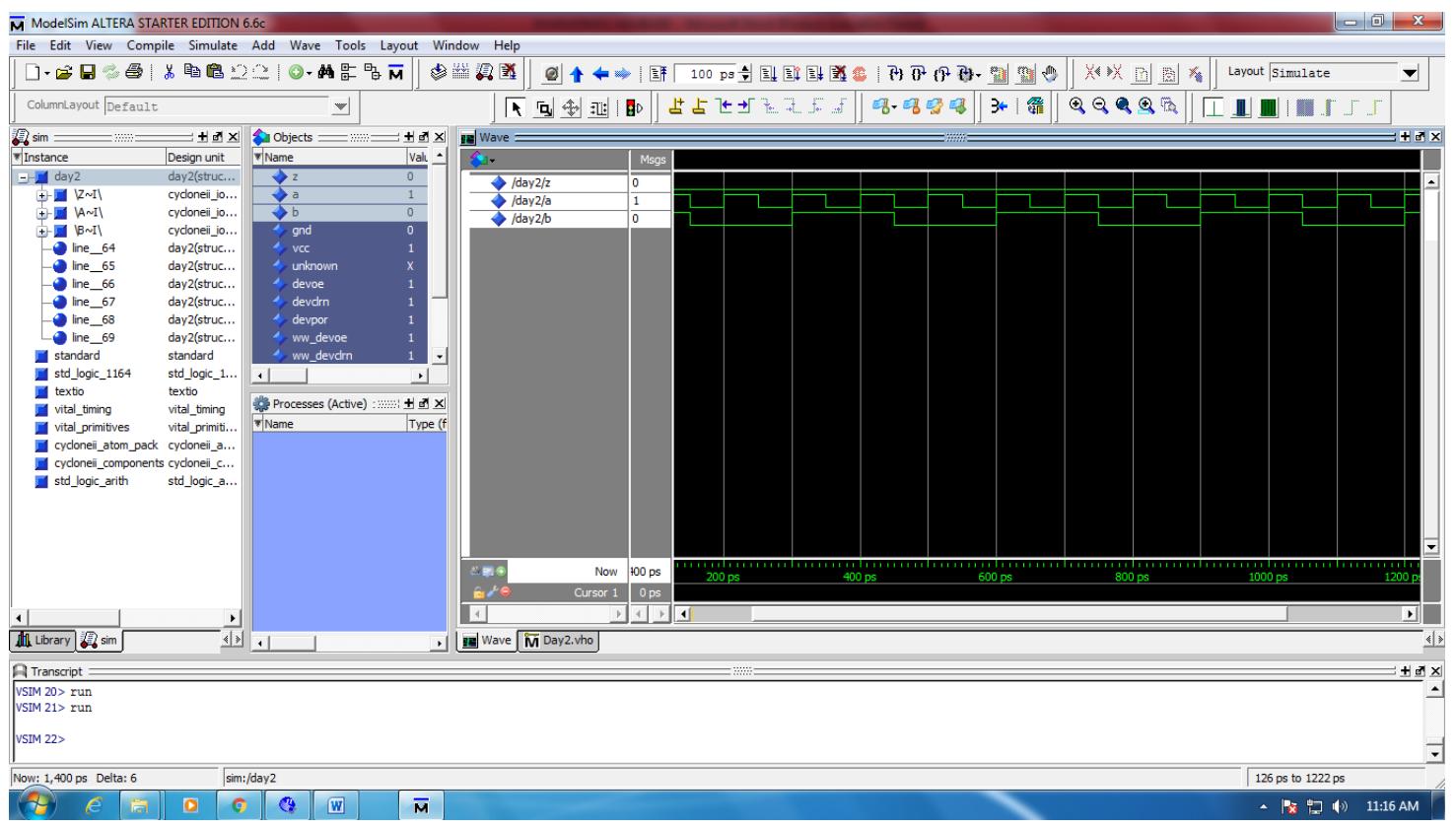
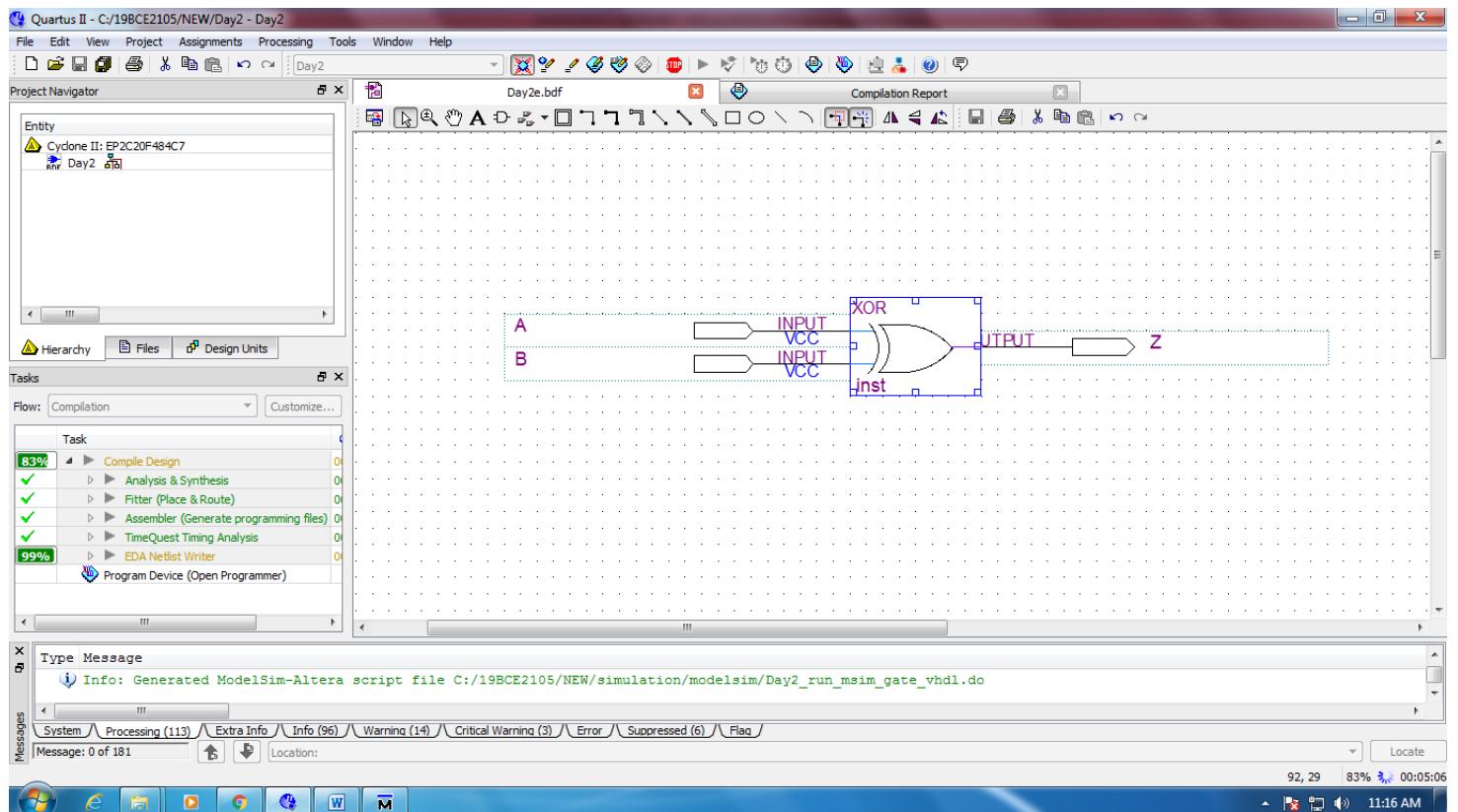


Boolean algebraic expression: $Z = \overline{A} \cdot \overline{B} = \overline{A} + \overline{B}$

Truth Table:

Input		Output
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

5. XOR gate:

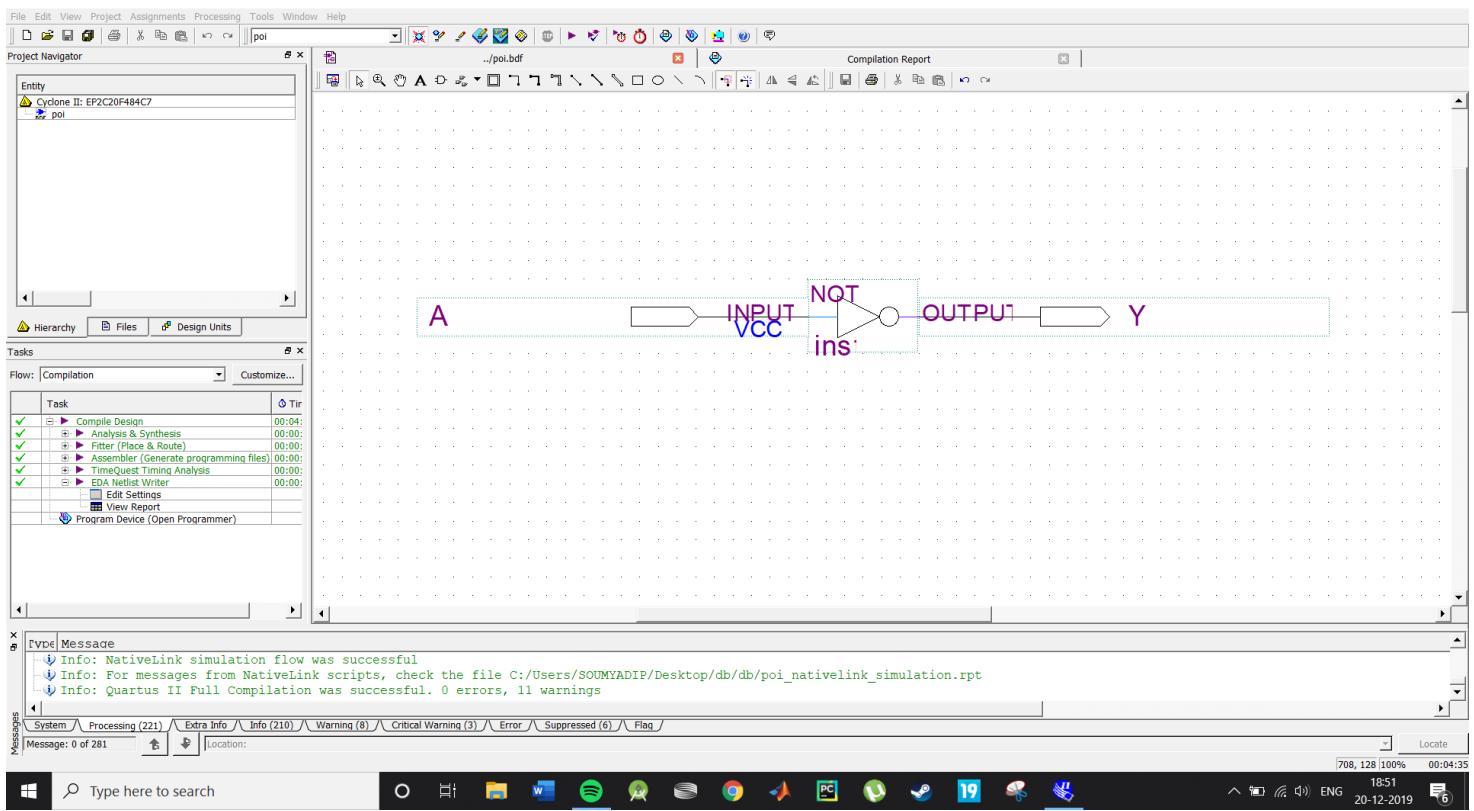


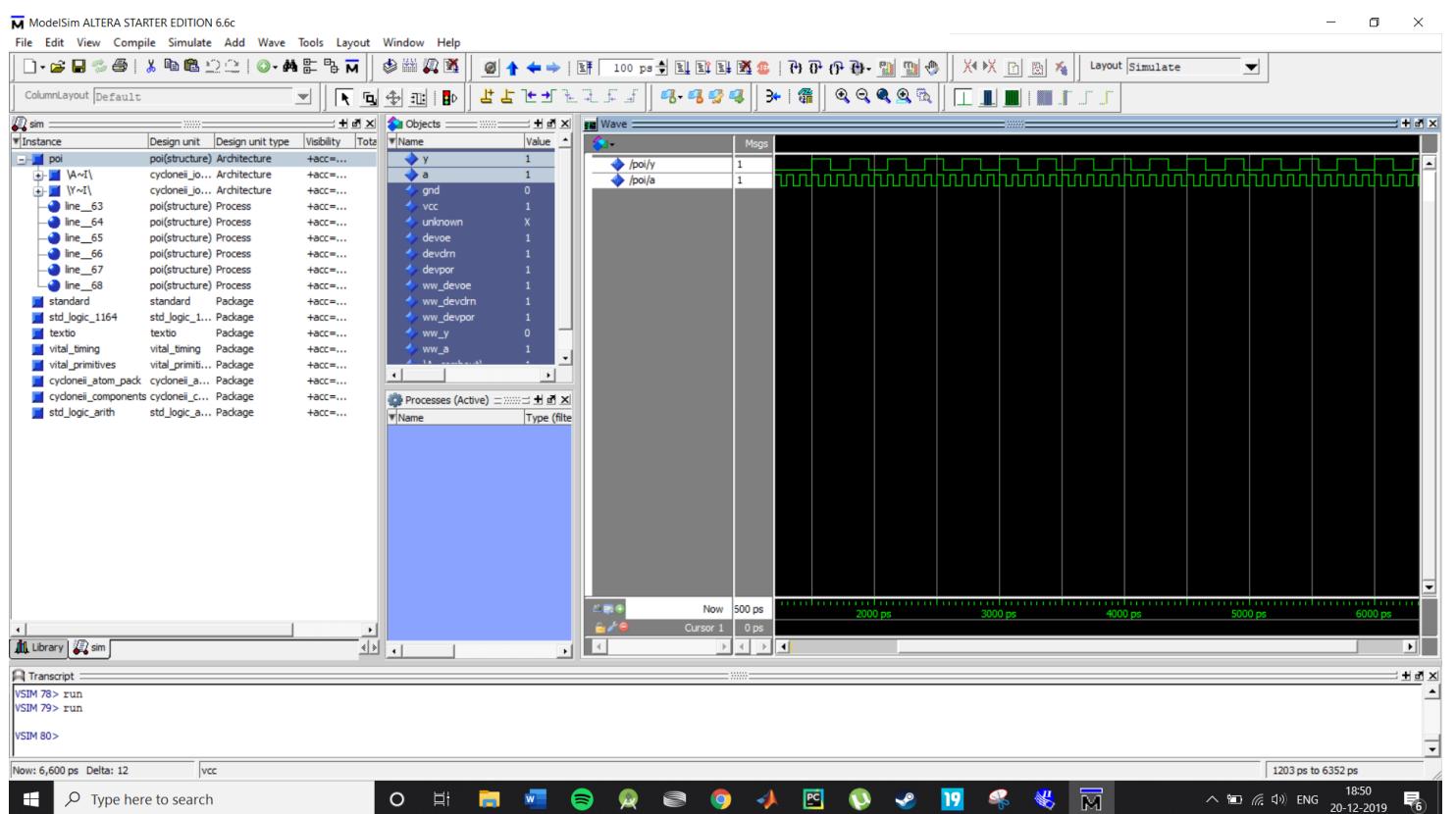
Boolean algebraic expression: $Z = A \oplus B$

Truth Table:

Input		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

6. NOT gate:





Boolean algebraic expression: $Z = \bar{A}$

Truth Table:

Input	Output
A	Y
0	1
1	0

Verification of de Morgan's laws for 2 variables

- deMorgan's 1st theorem:** It states that a NOR gate is equivalent to a bubbled AND gate.

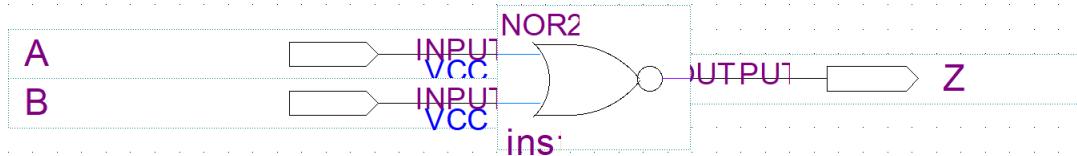
Boolean algebraic expression: $\overline{A \cdot B} = \overline{A} + \overline{B}$

Truth Table:

Input		Output				
A	B	$A \cdot B$	$\overline{A \cdot B}$	\overline{A}	\overline{B}	$\overline{A} + \overline{B}$
0	0	0	1	1	1	1
1	0	0	1	0	1	1
0	1	0	1	1	0	1
1	1	1	0	0	0	0

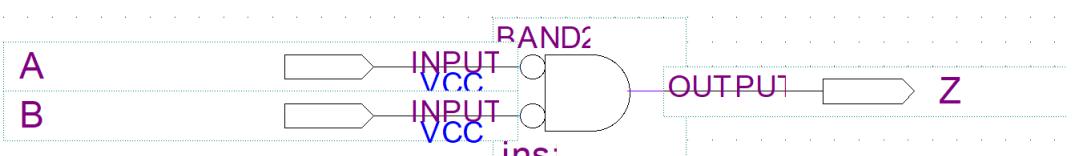
Logic Diagram:

NOR gate:

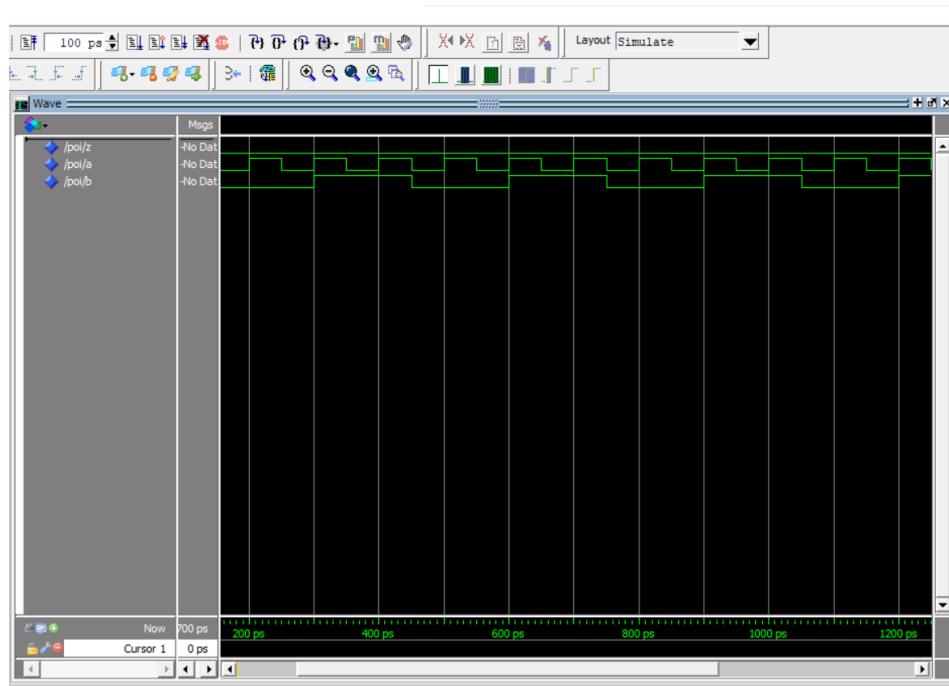


≡

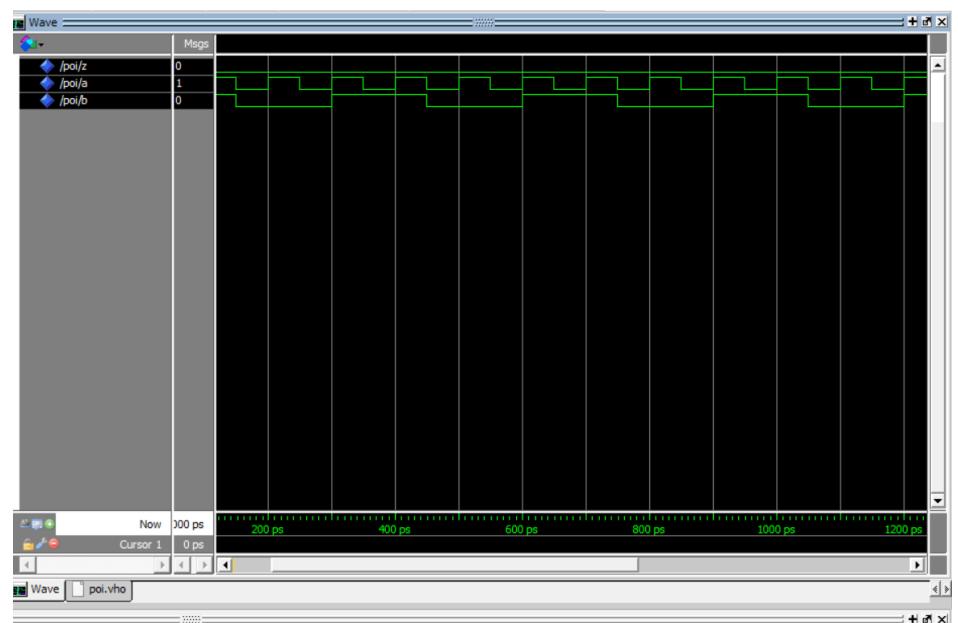
bubbled NAND gate:



Outputs:



is equivalent to:



2. **deMorgan's 2nd theorem:** It states that NAND gate is equivalent to bubbled OR gate.

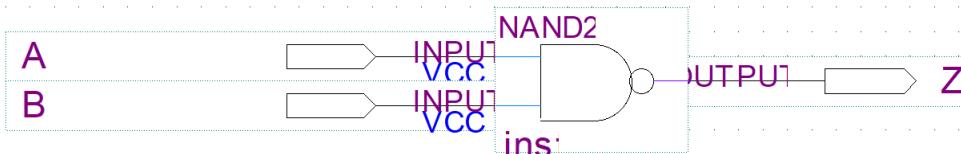
Boolean algebraic expression: $\overline{A + B} = \overline{A} \cdot \overline{B}$

Truth table:

Input		Output				
A	B	A+B	$\overline{A + B}$	\overline{A}	\overline{B}	$\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1
1	0	1	0	0	1	0
0	1	1	0	1	0	0
1	1	1	0	0	0	0

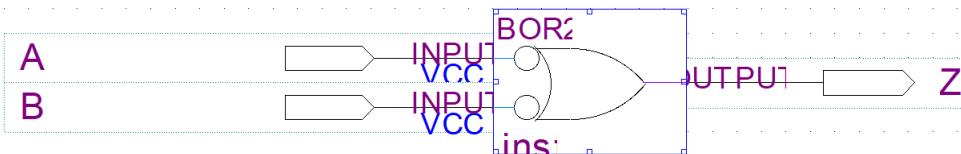
Logic diagram:

NAND gate:

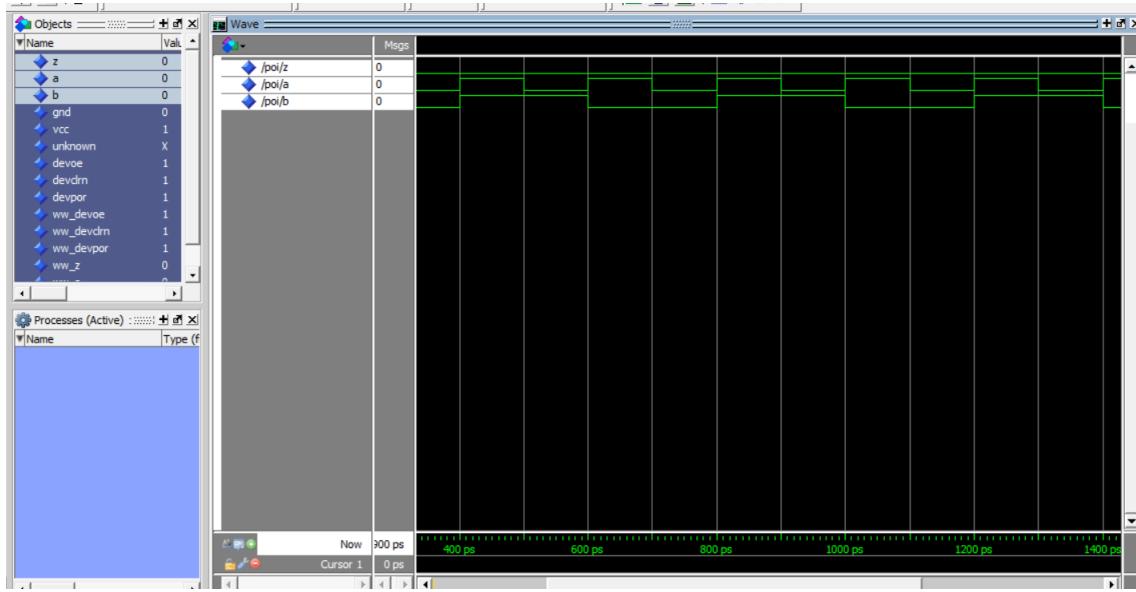


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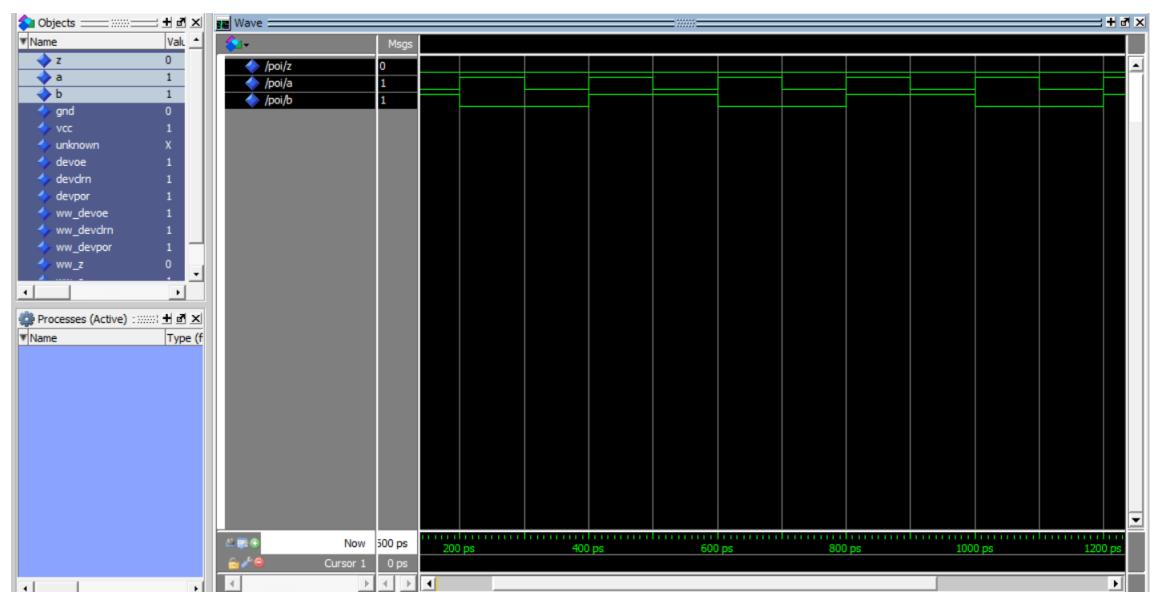
bubbled OR gate:



Outputs:



is equivalent to:



Digital Logic & Design

GSE1003

DIGITAL ASSIGNMENT - I / ELA

Winter Semester : 2019-20

Name : Sharadindu Adhikari

Reg. No. : 19 BCE 2105

slot : E2/TE2 . L27/L28

1. Verification of Logic Gates :-

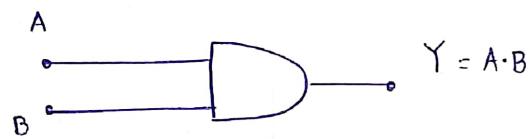
① AND gate :

② Aim : To verify the expression of AND gate using Truth table

③ Truth Table :

input		output
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

④ Logic diagram :



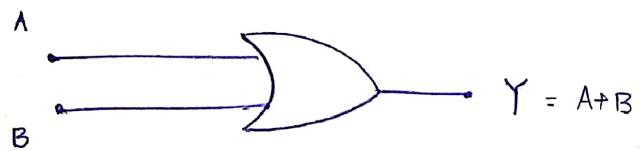
⑤ Boolean Algebraic expression :

$$Y = A \cdot B$$

② OR gate :

⑥ Aim : To verify the expression of OR gate using Truth Table.

⑦ Logic diagram :



② Truth Table :

Input		Output
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

③ Boolean Algebraic Expression :

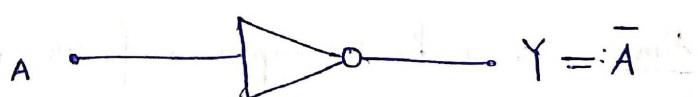
$$Y = A + B$$

③ NOT Gate :

- ① Aim : To verify the expression of NOT gate using Truth Table.
- ② Truth Table :

input	output
A	Y
0	1
1	0

④ Logic Diagram :



- ④ Boolean algebraic expression :

$$Y = \text{NOT } A \\ = \bar{A}$$

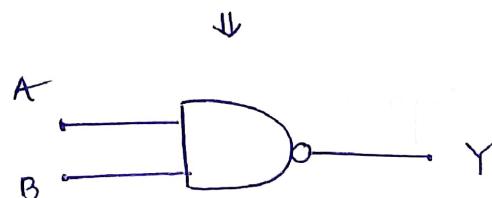
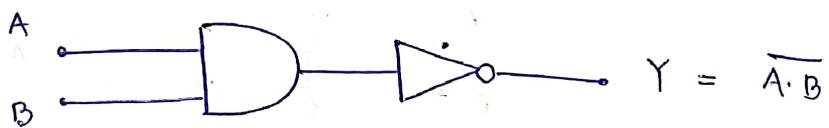
- ④ NAND Gate :

① Aim : To verify the expression of NAND gate using Truth Table

② Truth table :

input		output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

- ③ Logic diagram :



- ④ Boolean algebraic expression :

$$Y = \overline{A \cdot B} = \bar{A} + \bar{B}$$

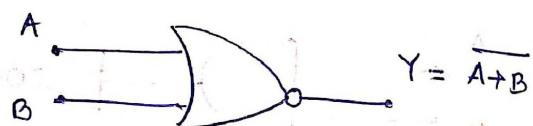
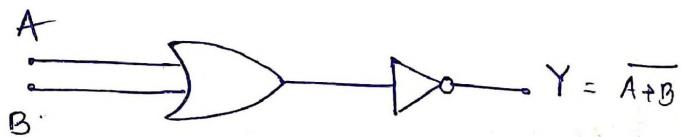
⑤ NOR gate:

⑥ Aim: To verify the expression of NOR gate using Truth Table.

⑦ Truth Table:

input		output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

⑧ Logic diagram:



⑨ Boolean algebraic expression:

$$Y = \overline{A+B} = \overline{A} \cdot \overline{B}$$

Algebraic * graphical

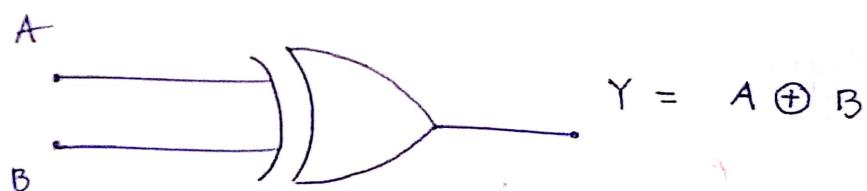
⑥ XOR Gate :

① Aim : To verify the expression of XOR gate using Truth Table.

② Truth table :

input		output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

③ Logic diagram :



④ Boolean algebraic expression :

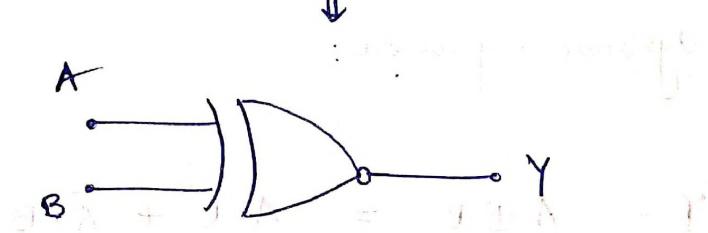
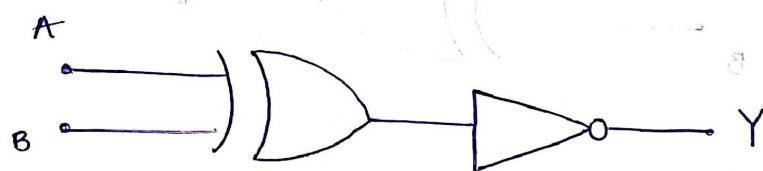
$$Y = A \oplus B = A \cdot \bar{B} + \bar{A} \cdot B$$

⑦ XNOR gate:

- ① Aim: To verify the expression of XNOR gate using Truth table.
- ② Truth Table:

input		output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

③ Logic diagram:



④ Boolean algebraic expression:

$$Y = A \oplus B = \bar{A} \cdot \bar{B} + A \cdot B$$

2. Verification of de Morgan's Laws for 2 variables :-

① de Morgan's 1st Theorem :

② Statement :

This Law proves that when two or more input variables are AND'ed and negated, they are equivalent to OR of the complements of individual variables.

③ Aim :

To prove the expression $\overline{A \cdot B} = \overline{A} + \overline{B}$ using Truth table.

④ Truth table :

inputs		outputs				
A	B	$A \cdot B$	$\overline{A \cdot B}$	\overline{A}	\overline{B}	$\overline{A} + \overline{B}$
0	0	0	1	1	1	1
1	0	0	1	0	1	1
0	1	0	1	1	0	1
1	1	1	0	0	0	0

Hence,

$$\boxed{\overline{A \cdot B} = \overline{A} + \overline{B}}$$

Also, deMorgan's 1st theorem states that a NOR gate is equivalent to a bubbled AND gate.

④ Boolean algebraic expressions for:

- NOR gate: $Z = \overline{A+B}$

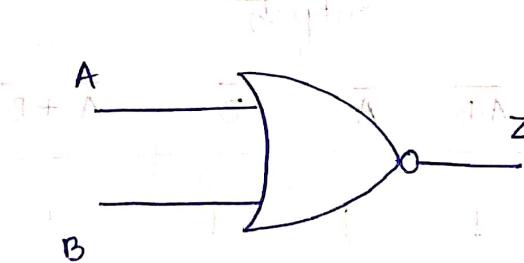
- bubbled AND gate: $Z = \overline{\overline{A} \cdot \overline{B}}$

∴ Just from the Truth table what we've deduced; from this expression as well, it can be written as:

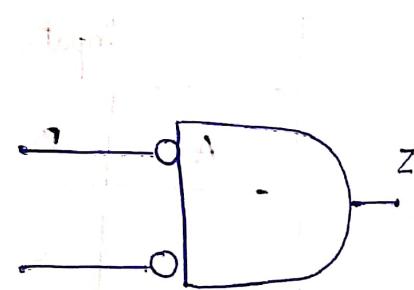
$$\overline{A+B} = \overline{\overline{A} \cdot \overline{B}}$$

Since both gates have identical outputs for same set of inputs.

⑤ Logic diagrams:



NOR gate



bubbled AND gate

$$\overline{A+B} = \overline{\overline{A} \cdot \overline{B}}$$

Q2

de Morgan's 2nd Theorem :

④ Statement : [~~Top 10 Theorems of Boolean Algebra~~]

This law states that when two or more input variables are OR'ed and negated, they are equivalent to AND of the complements of individual variables.

⑤ Aim : To prove the expression $\overline{A+B} = \overline{A} \cdot \overline{B}$ using Truth table.

⑥ Truth table :

inputs		outputs				
A	B	$A+B$	$\overline{A+B}$	\overline{A}	\overline{B}	$\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1
1	0	1	0	0	1	0
0	1	1	0	1	0	0
1	1	1	0	0	0	0

Hence,

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

Also, de Morgan's 2nd theorem states that the NAND gate is equivalent to a bubbled OR gate.

② Boolean expression for:

- NAND gate: $Z = \overline{A \cdot B}$

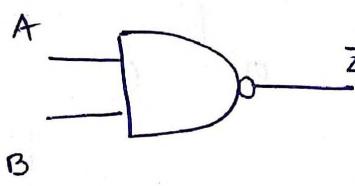
- bubbled OR gate: $Z = \overline{\overline{A} + \overline{B}}$

- From the truth table and the expression we've deduced from above, it can well be written as:

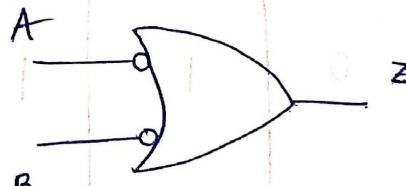
$$\overline{A \cdot B} = \overline{\overline{A} + \overline{B}}$$

- since both gates have identical outputs for same set of inputs.

③ Logic diagrams:



NAND gate



bubbled OR gate

... END ...