Ex. No.:4

Date: 29/8/2019

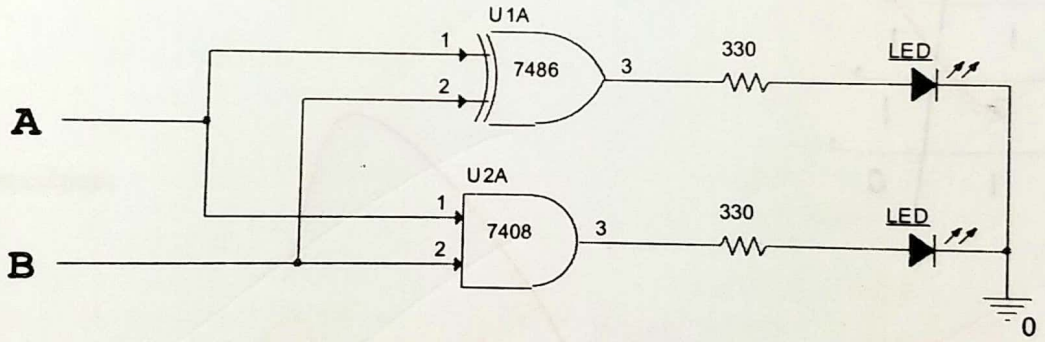
Design of Half Adder Circuit using gates

Aim: To verify the truth tables for Half-Adder Circuit using Logic gates

Apparatus Required:

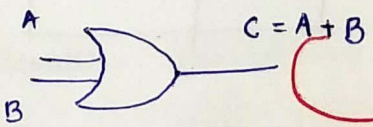
S. No.	Name of the apparatus	Range / Type	Quantity
1	7486 gate	-	1 No.
2	7408 gate	-	1 No.
3	LED	-	2 Nos.
4	RPS	0 – 15 V	1 No.
5	Resistor	330 Ω	2 Nos.
6	Breadboard	-	1 No.
7	Wires	-	Few

Circuit Diagram:



Theory: Logic gates :-

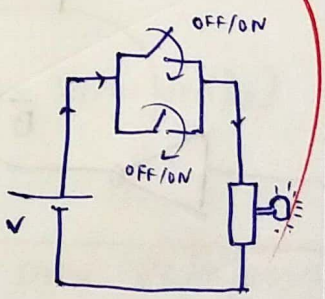
OR-gate :



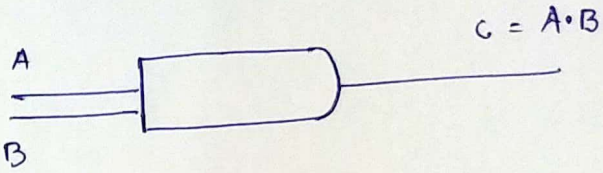
A	B	C
0	0	0
0	1	1
1	0	0
1	1	1

0 → off

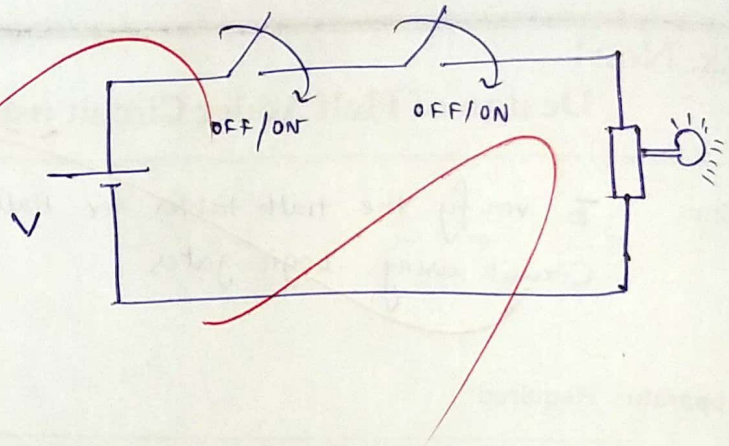
1 → ON



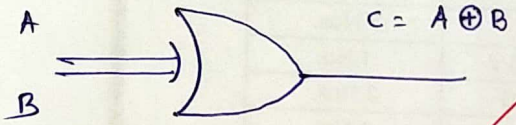
AND gate :-

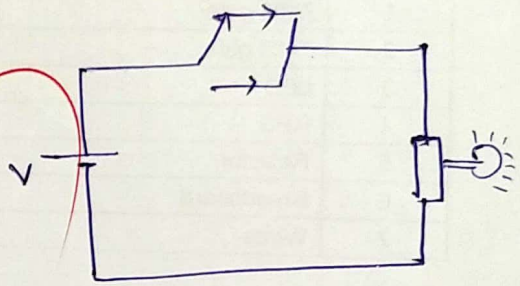


A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



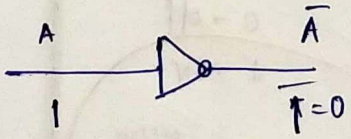
XOR gate :-

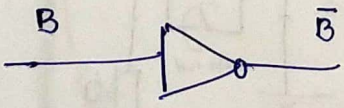




A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

NOT gate :-





$\bar{1} = 0$

$\bar{0} = 1$

A	$\bar{A}$
B	$\bar{B}$

Truth Table

A	B	S=A⊕B	C=A.B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Observation:

Procedure:

Result: The design of Half Adder Circuit have been verified with Truth tables.

Reg. No: 19BCE2105 **Name:** SHARADINDU ADHIKARI **Date:** 29/8/2019