Digital Logic and Design

EXAM-2 / part-B

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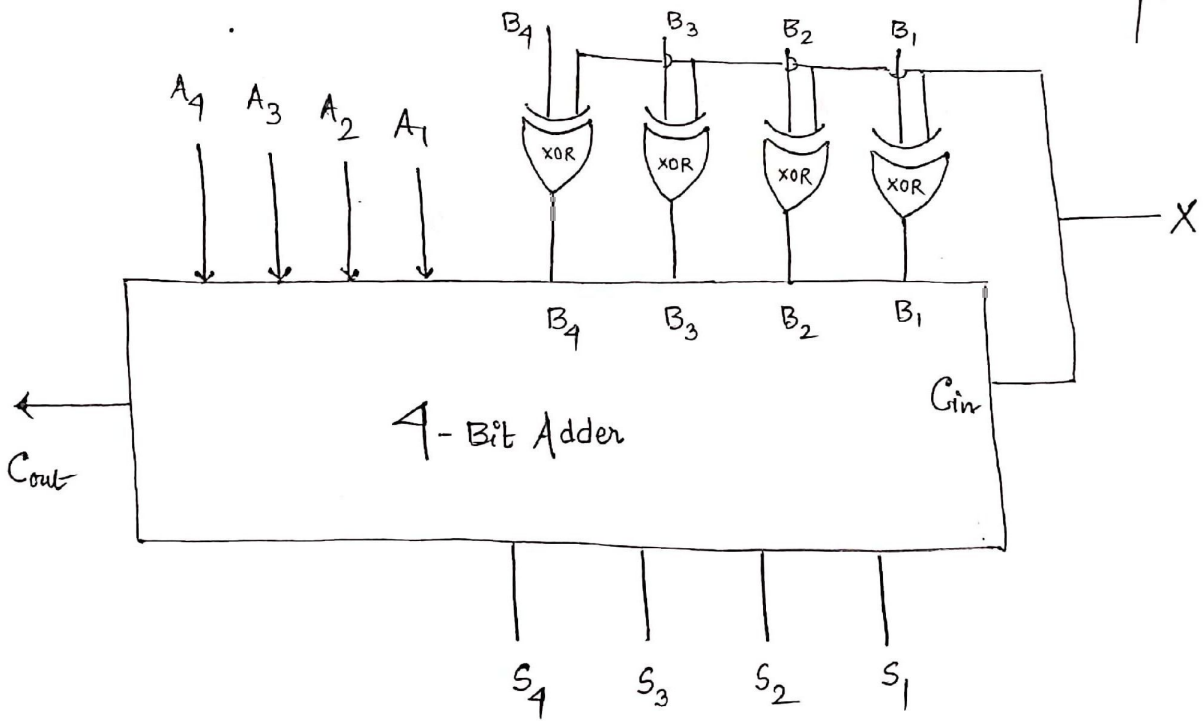
Q. Design and compare 4-bit adder/subtractor circuit using two's and one's complement for subtraction. Show your design for deducing the correct result (positive or negative) on subtraction.

Soln →

Let's consider a 4-bit adder/subtractor which uses one's complement:



If $X = 0$, sum $= A + B + C_{in} = A + B + 0 = A + B$

If $X = 1$, sum $= A +$ (one's complement of B) $+ C_{in}$

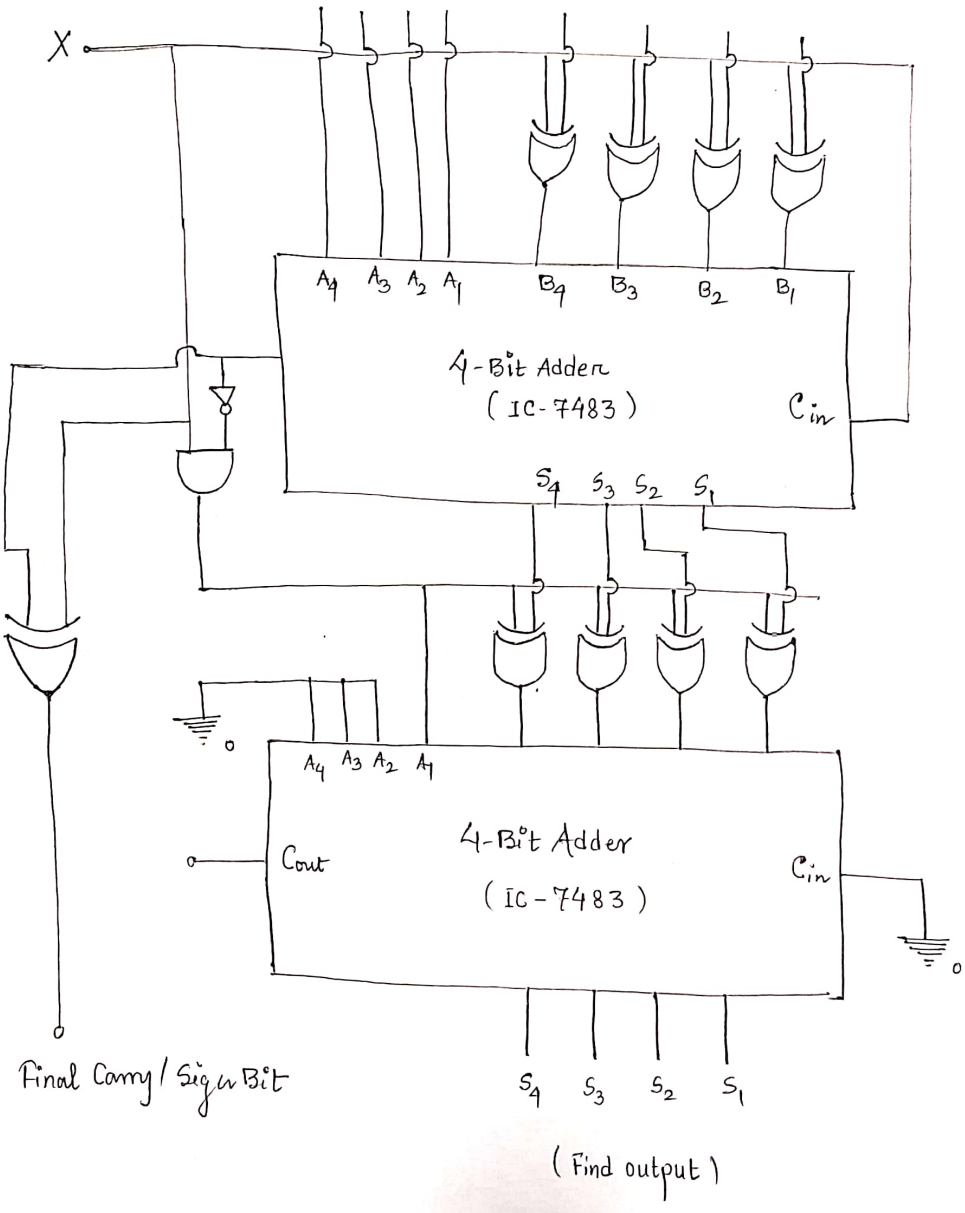
$= A +$ (one's complement of B) $+ 1$

$= A - B$

In the above circuit, when the 4th addition operation takes place, and the sum output exceeds the 4-bit, then the carry-out bit is considered as the MSB of the output. In subtraction operation, if the carry-out bit is 1, the sum output is considered to be positive and the carry-out bit is neglected.

But in subtraction operation when the carry-out becomes Zero, the actual answer is considered to be negative and the sum output has to be calculated further in two's complement method, it means when a 4-bit subtraction operation produces a negative value, it gives a half-calculated output which has to be further deduced.

To solve the problem, we can design the following circuit :-



Ω Truth-table of XOR gate which produces final carry :—

X	Cout	Final Carry / Signal Bit
0	0	0
0	1	1
1	0	1
1	1	0

Ω Explanation of the changed design which uses two's complement :—

In this circuit, NOT gate is inverting the carry-out result of 1st adder chip and the AND gate is passing active high signal only when the bit X is 1 (i.e. subtraction operation is operated) and carry-out bit is zero (i.e. the actual answer becomes negative). Thus when the subtraction operation produces the negative result, an active high signal is passed to the XOR gates of the 2nd controlled inverter and it passes one's complement of the sum, output of the 1st adder chip (i.e. S_1, S_2, S_3, S_4). The same signal is passed to the LSB of A bit (i.e. A_1); the remaining A bits (i.e. A_2, A_3, A_4) and carry-in bit of the 2nd adder chip are set to ground (i.e. 0). This produces the two's complement of the previous sum output and generates final output along with the sign bit.

In case of addition & subtraction (where $X=0$). which produces positive result, the result of AND gate becomes zero and the sum output of the 1st adder chip remains unchanged, because the controlled inverter directly passes the inputs to the outputs than the previous sum output. In case of 4-bit addition which produces 4-bit sum with zero in carry-out bit, is represented in sign magnitude form in the final result, because there the sign bit is also zero.

In case of 4-bit addition producing 4-bit sum with a carry-out bit 1, the final result implements the 5-bit sum result, no-sign bit in there's needed as the number must be positive. when the subtraction takes place where the answer is positive, the sign bit is positive, i.e., Zero.

Hence, the accurate result of addition and subtraction comes out at once by using "Adder / subtractor using two's complement".
