CSE 1003

DLD

Assessment – 4

L27+L28

WINTER SEMESTER 2019–20

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by

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Question 1

Aim: To design the BCD to seven segment circuit (use seven segment display to show the output)

Truth Table:

	A	B	C	D	E	F	G	H	I	J	K
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	1	0	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1

Boolean expression:

E = A+CD+BD+B'D'

F = B'+C'D'+CD

G = B+C'+D

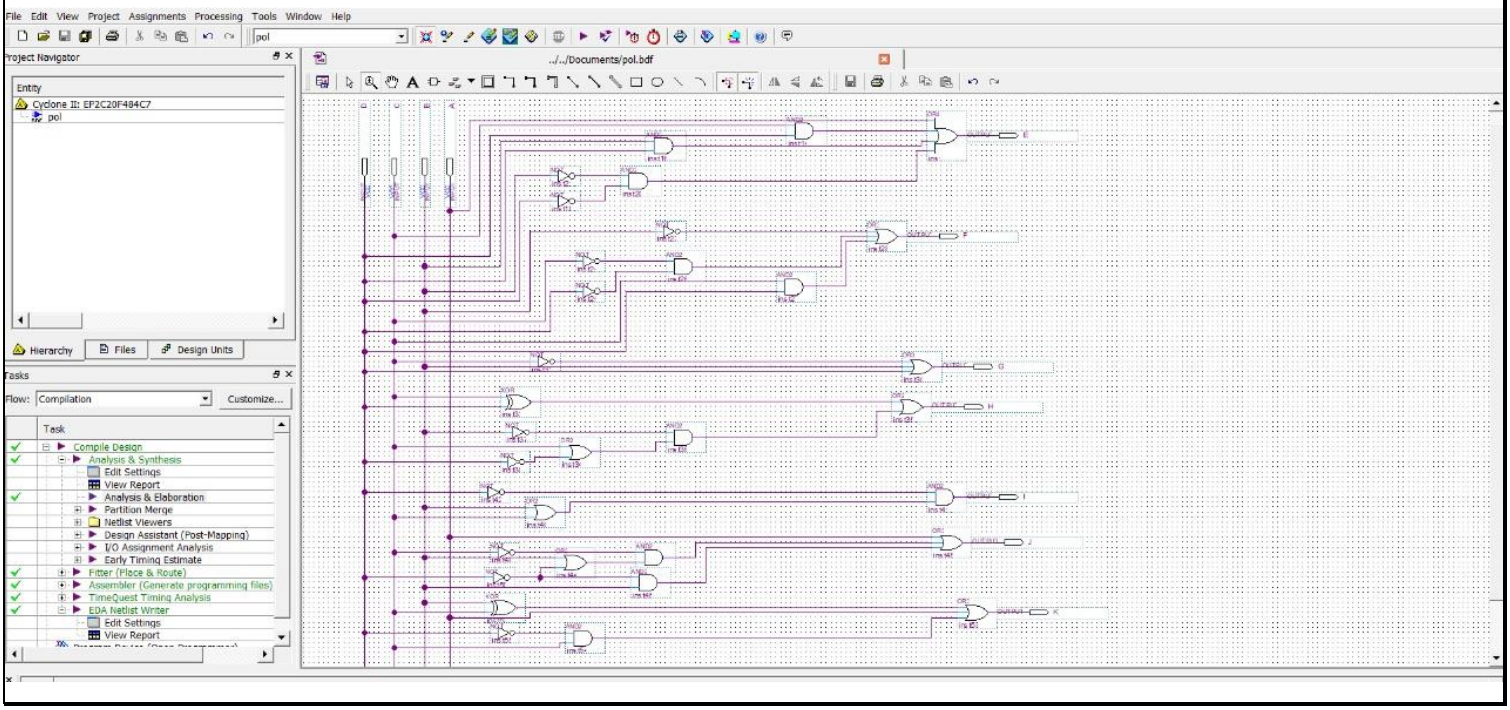
H = B'D'+CD'+B'C+BC'D

I = B'D'+CD'

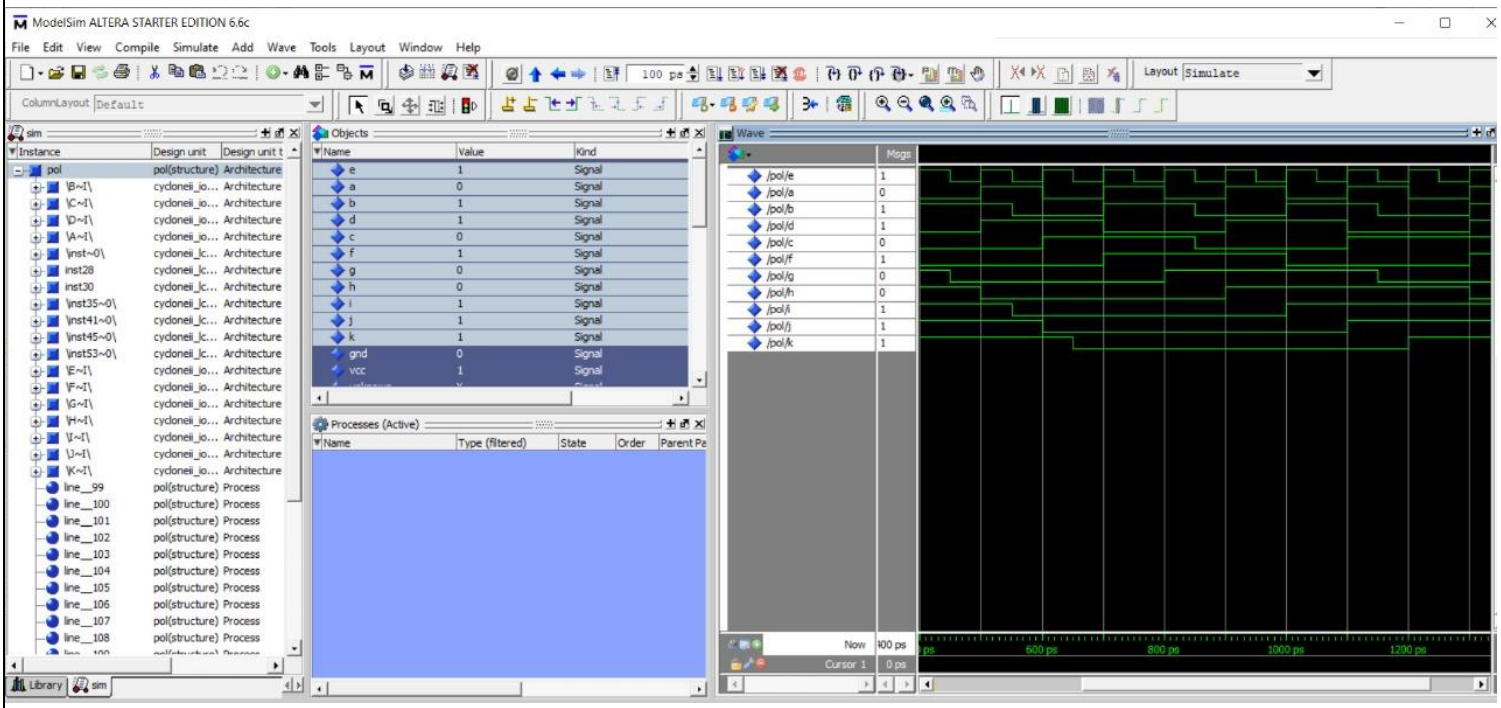
J = A+C'D'+BC'+BD'

K = A+BC'+CD'+B'C

Logic diagram:



Final output screen:



Test case: a=0, b=1, c=0, d=1, e=1, f=1, g=0, h=0, i=1, j=1, k=1

Result: The BCD to seven segment circuit has been verified in Quartus-II ModelSim Altera.

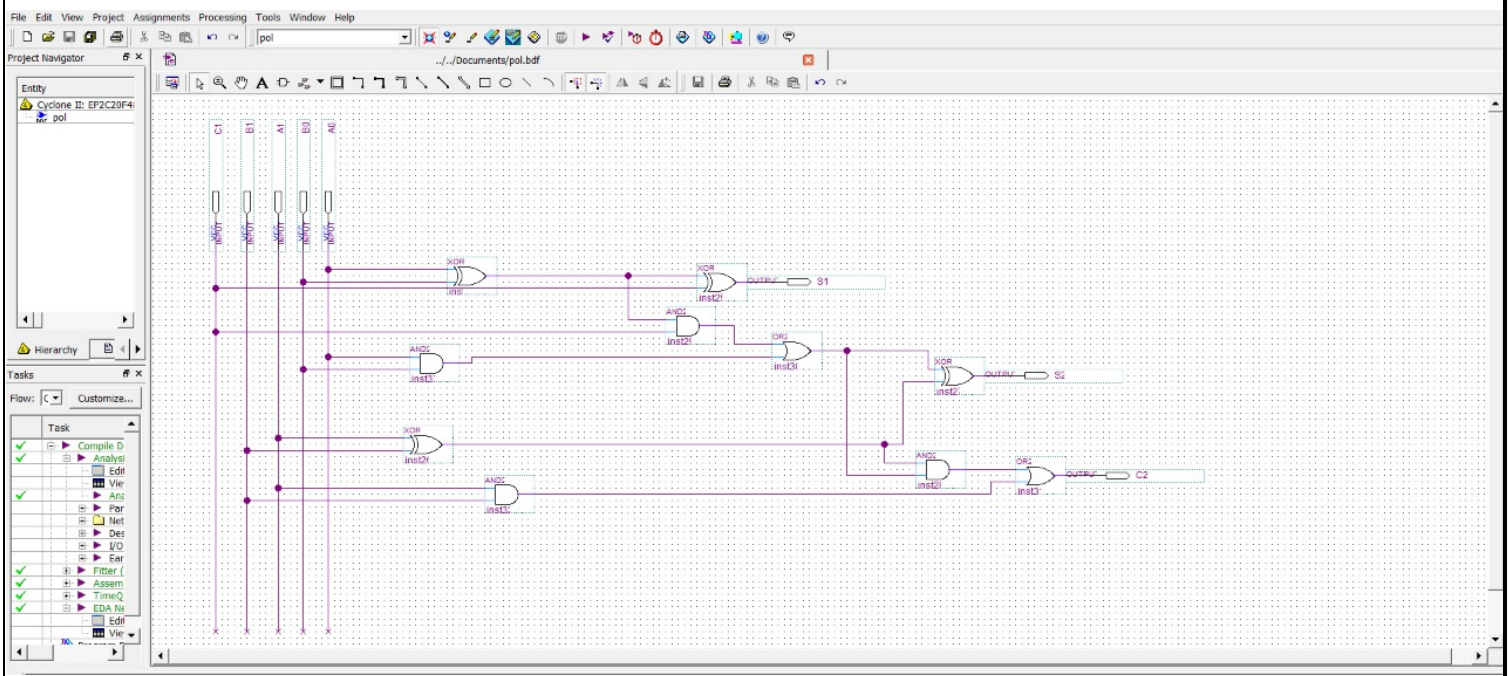
Question 2

Aim: To design a 2-bit parallel adder/subtractor circuit.

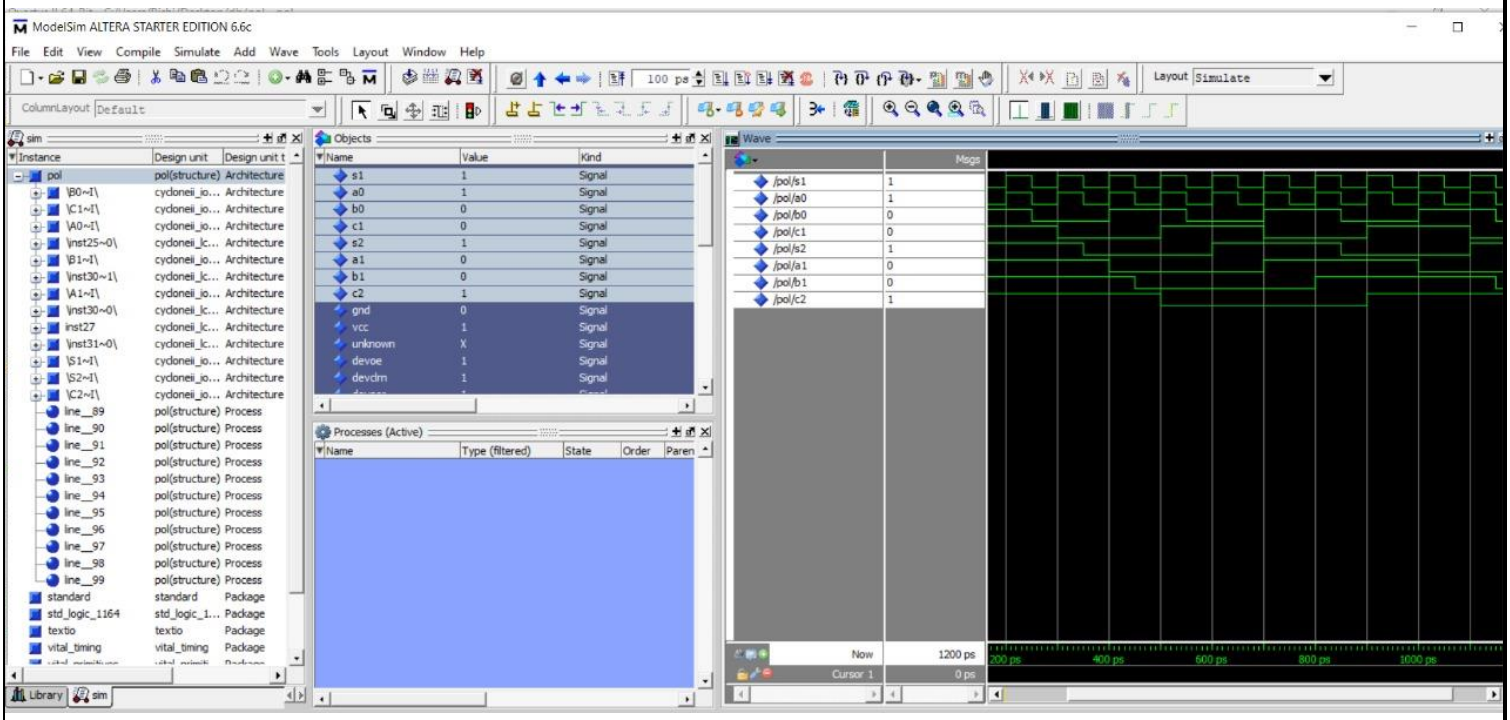
Truth Table:

A0	A1	B0	B1	C1	S0	S1	C2
0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0
0	1	0	0	0	0	1	0
1	0	1	0	0	0	1	0
0	1	0	1	0	0	0	1
0	1	0	0	1	1	1	0
1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1

Logic diagram:



Final output screen:



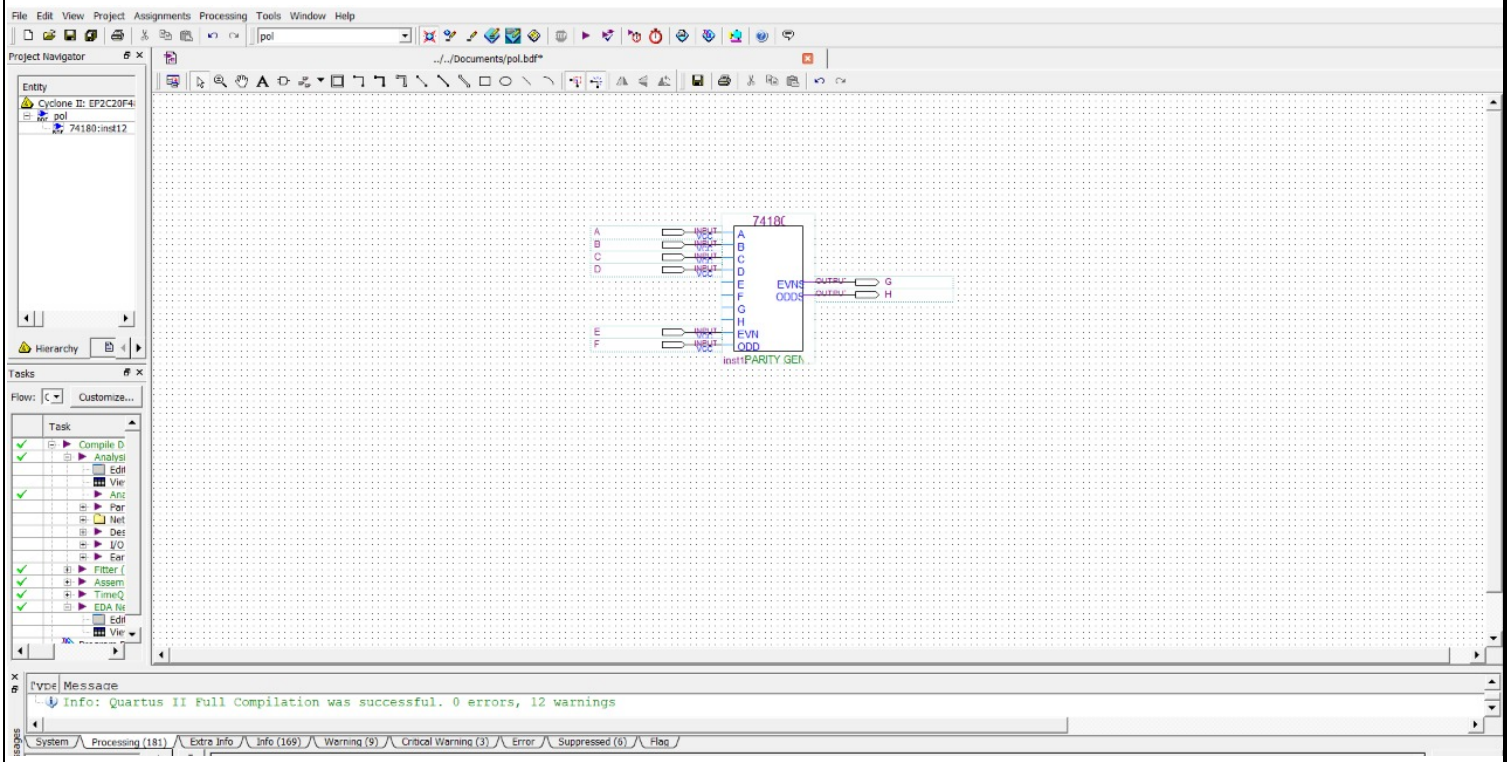
Test case: s1=1, a0=1, b0=0, c1=0, s2=1, a1=0, b1=0, c2=1

Result: The design and implement 4 line to 2 line priority encoder has been verified in Quartus-II ModelSim Altera.

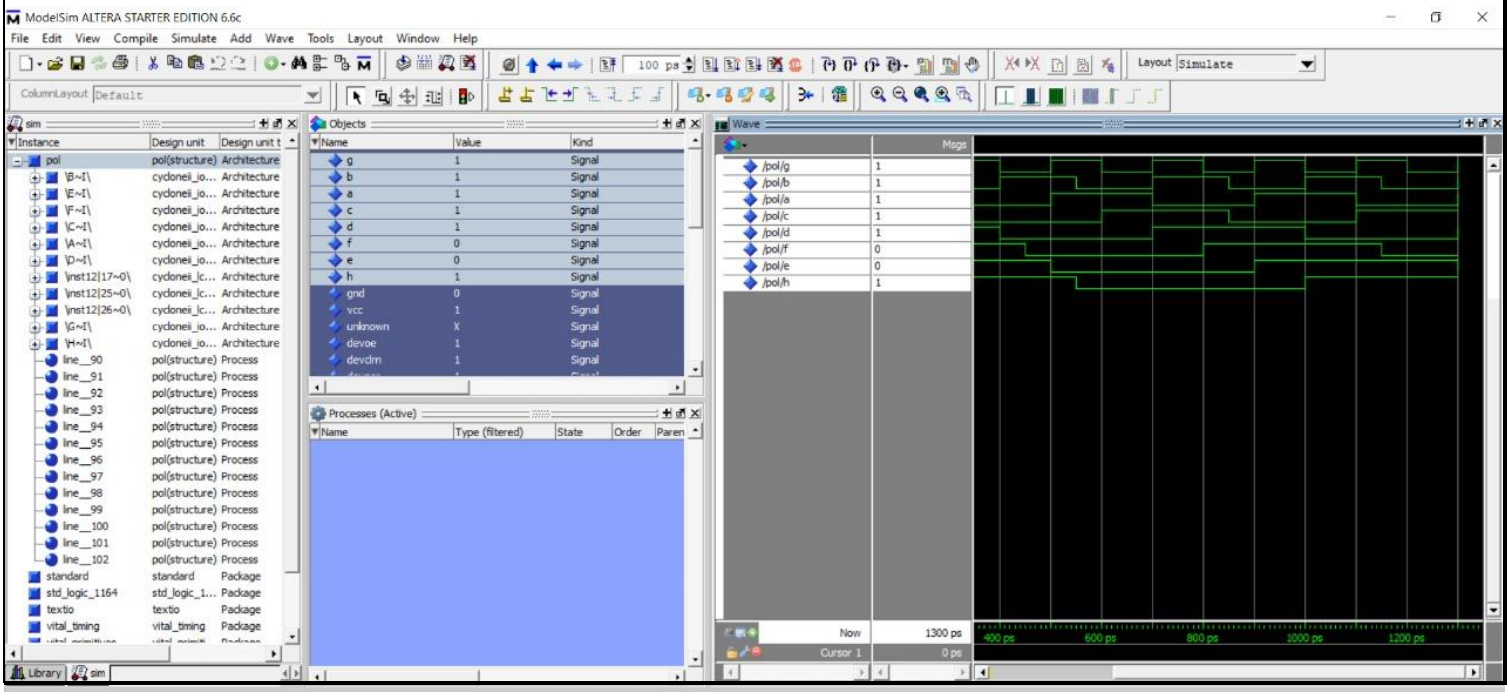
Question 5

Aim: To design a 4-bit odd parity generator using a multiplexer.

Logic diagram:



Final output screen:



Test case: a=1, b=1, c=1, d=1, e=0, f=0, g=1, h=1

Result: The 4-bit odd parity generator has been verified in Quartus-II ModelSim Altera.

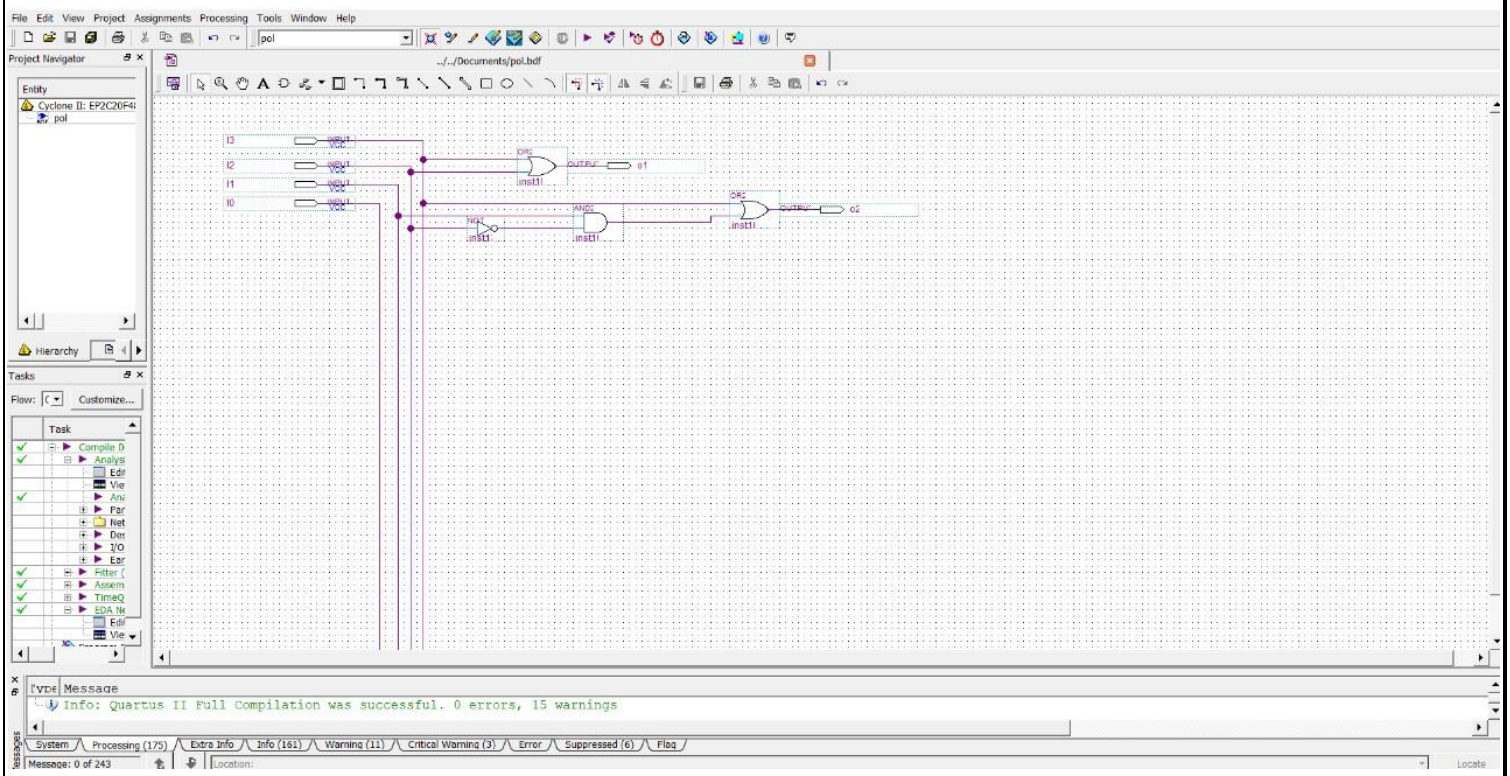
Question 7

Aim: To design and implement 4 line to 2 line priority encoder.

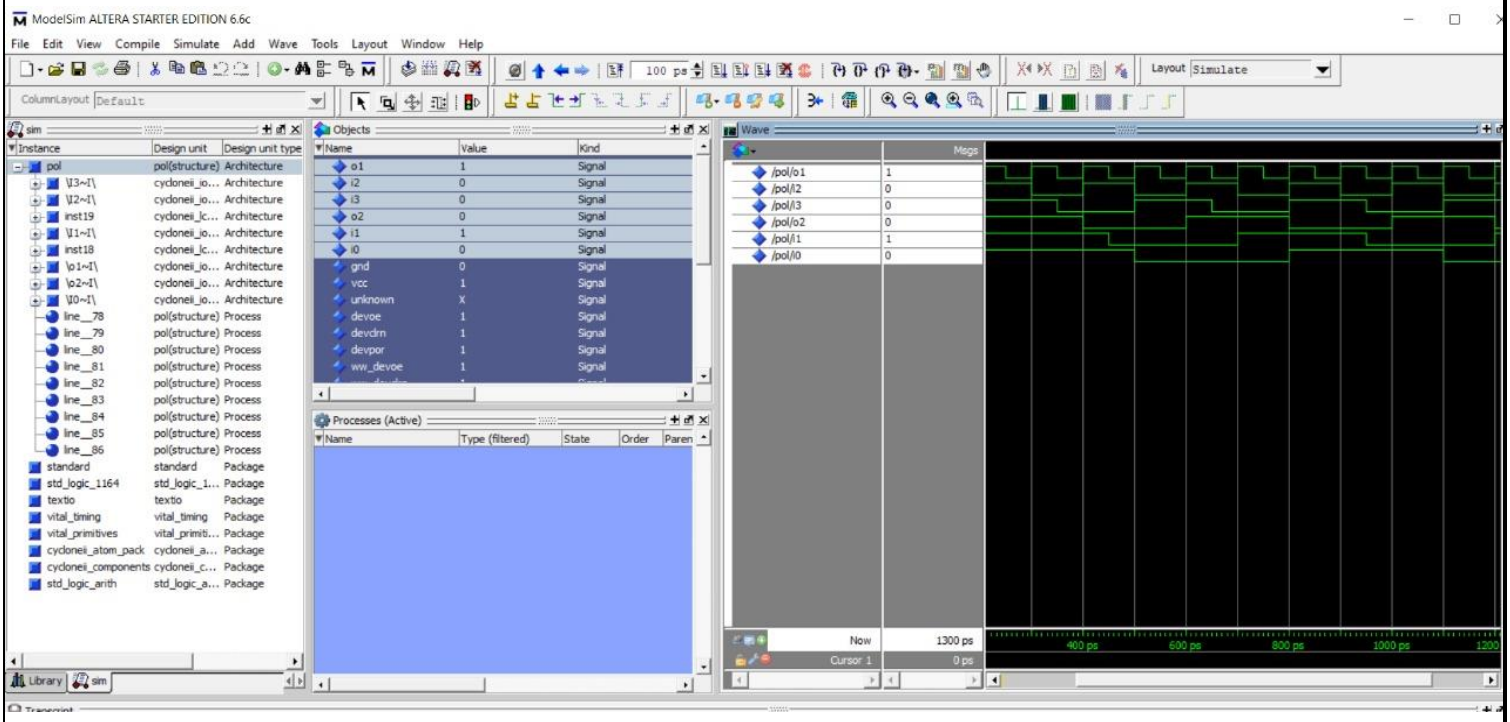
Truth Table:

	I_3	I_2	I_1	I_0	O_1	O_2
0	0	0	0	0	0	0
1	0	0	0	1	0	0
2	0	0	1	0	0	1
3	0	0	1	1	0	1
4	0	1	0	0	1	0
5	0	1	0	1	1	0
6	0	1	1	0	1	0
7	0	1	1	1	1	0
8	1	0	0	0	1	1
9	1	0	0	1	1	1
10	1	0	1	0	1	1
11	1	0	1	1	1	1
12	1	1	0	0	1	1
13	1	1	0	1	1	1
14	1	1	1	0	1	1
15	1	1	1	1	1	1

Logic diagram:



Final output screen:



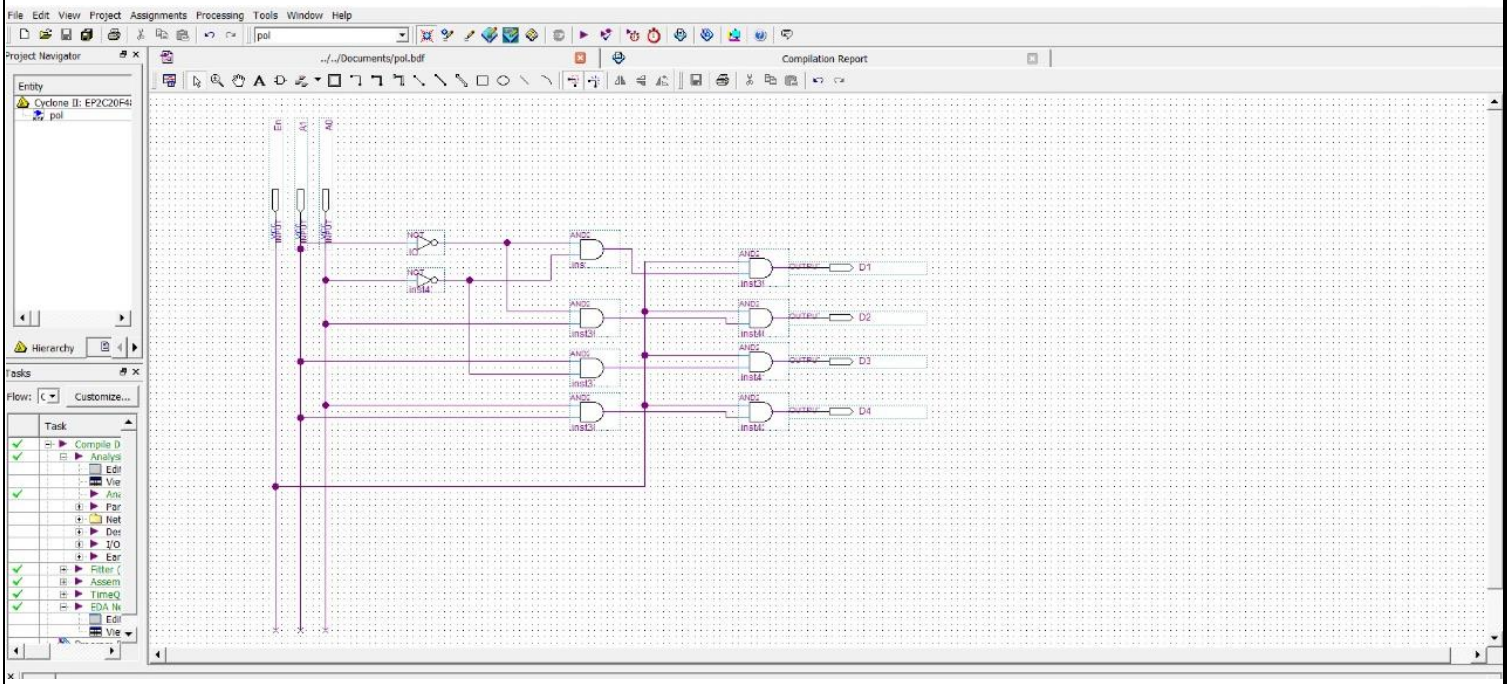
Test case: $i_0=0$, $i_1=1$, $i_2=0$, $i_3=0$, $o_1=1$, $o_2=0$

Result: The design and implement 4 line to 2 line priority encoder has been verified in Quartus-II ModelSim Altera.

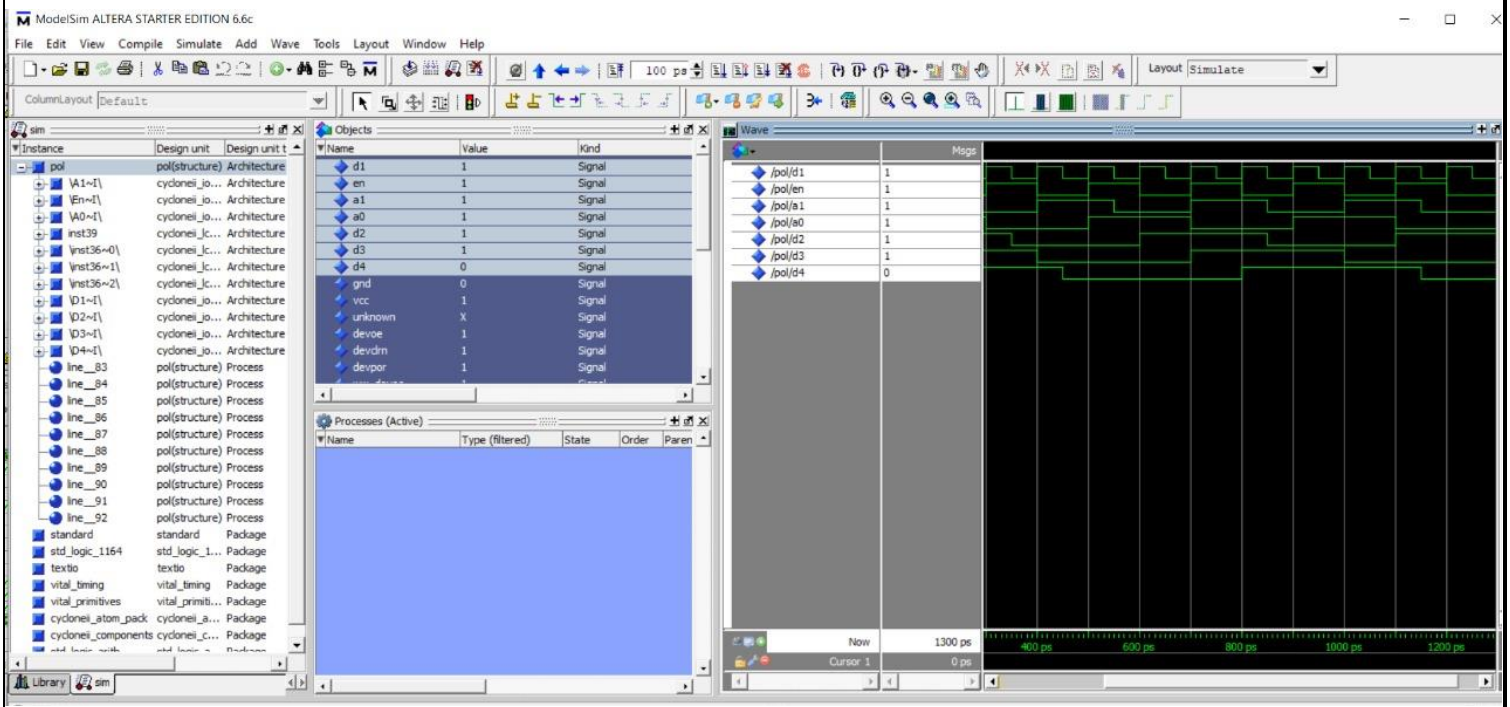
Question 8

Aim: To design a 2 to 4 line decoder.

Logic diagram:



Final output screen:



Test case: d1=1, en=1, a1=1, a0=1, d2=1, d3=1, d4=0

Result: The 2 to 4 line decoder has been verified in Quartus-II ModelSim Altera.

_____end_____