Ex. No.: 4 **Date:** 17/10/19

Design of Half Adder and Full Adder circuits

Aim: To verify the truth tables of Half Adder and Full Adder circuit and its corresponding output waveforms in Capture CIS.

Apparatus/Tool required:

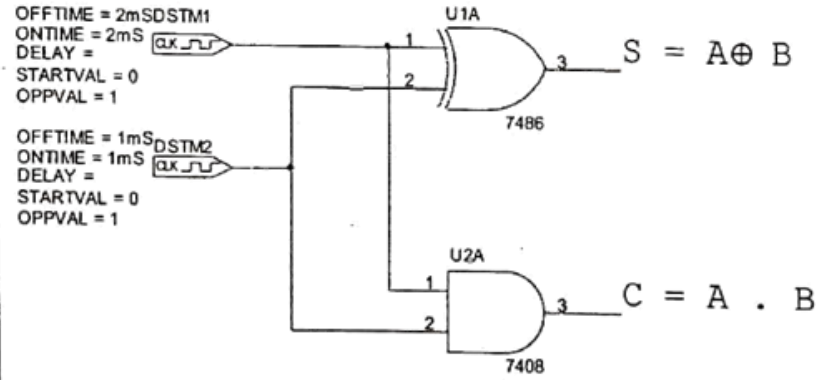
ORCAD / PSpice simulator - > **7400 Library – 7408, 7432 & 7486**
Source Library - Digclock

Simulation Settings: **Analysis Type - Time Domain**

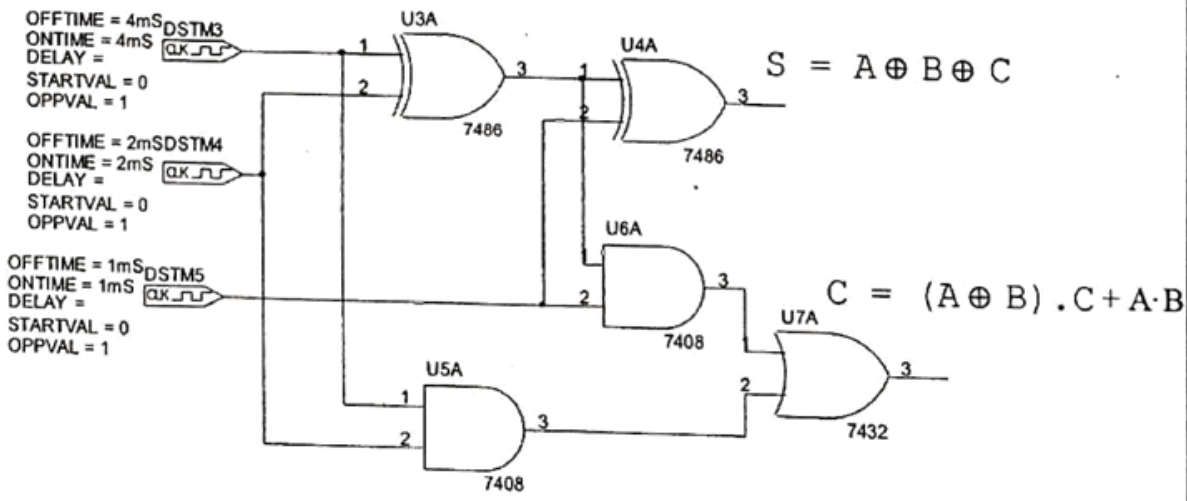
Run to time: 4ms (for Half Adder)
Run to time: 8ms (for Full Adder)

Circuit Diagram:

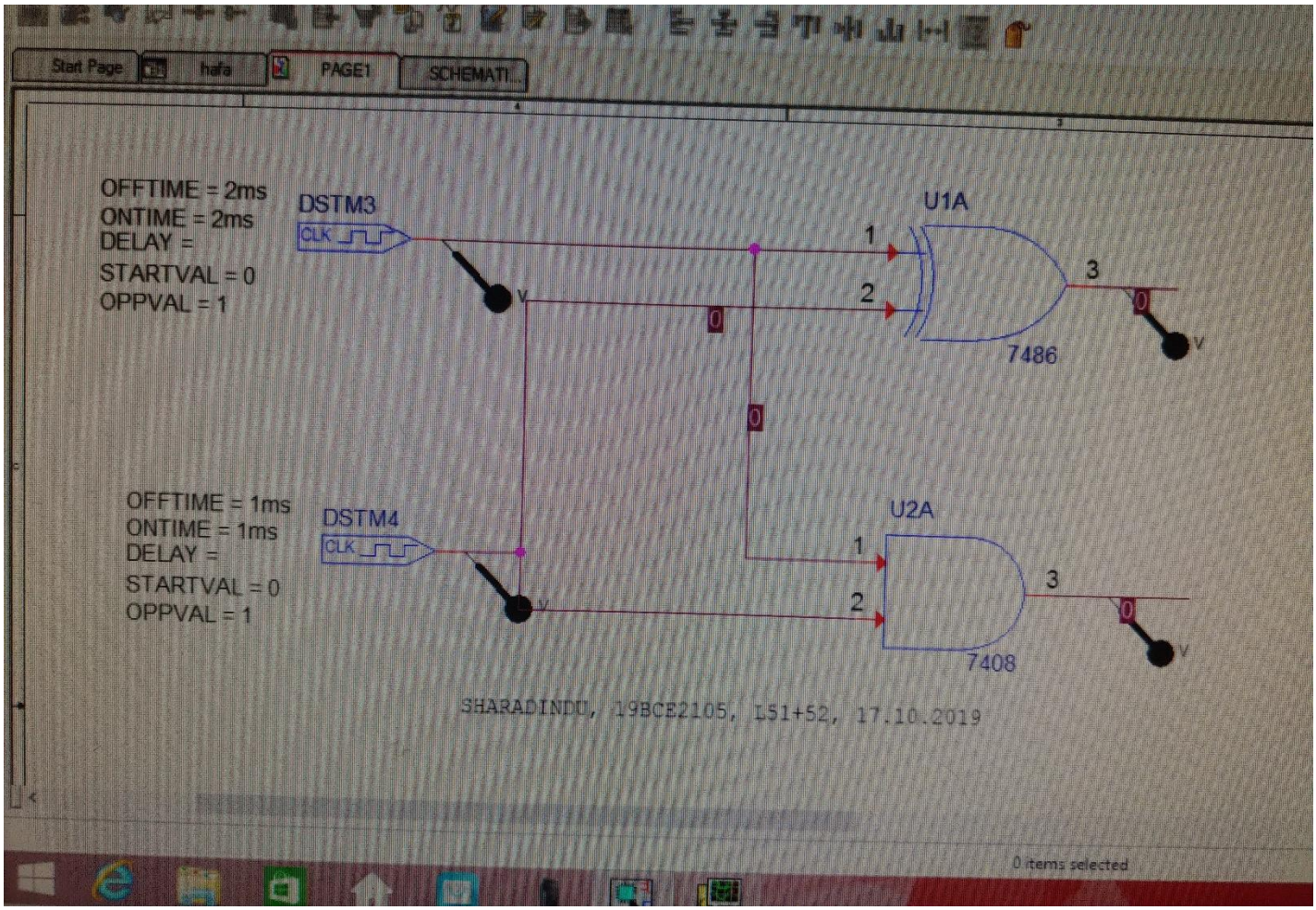
Half – Adder Circuit

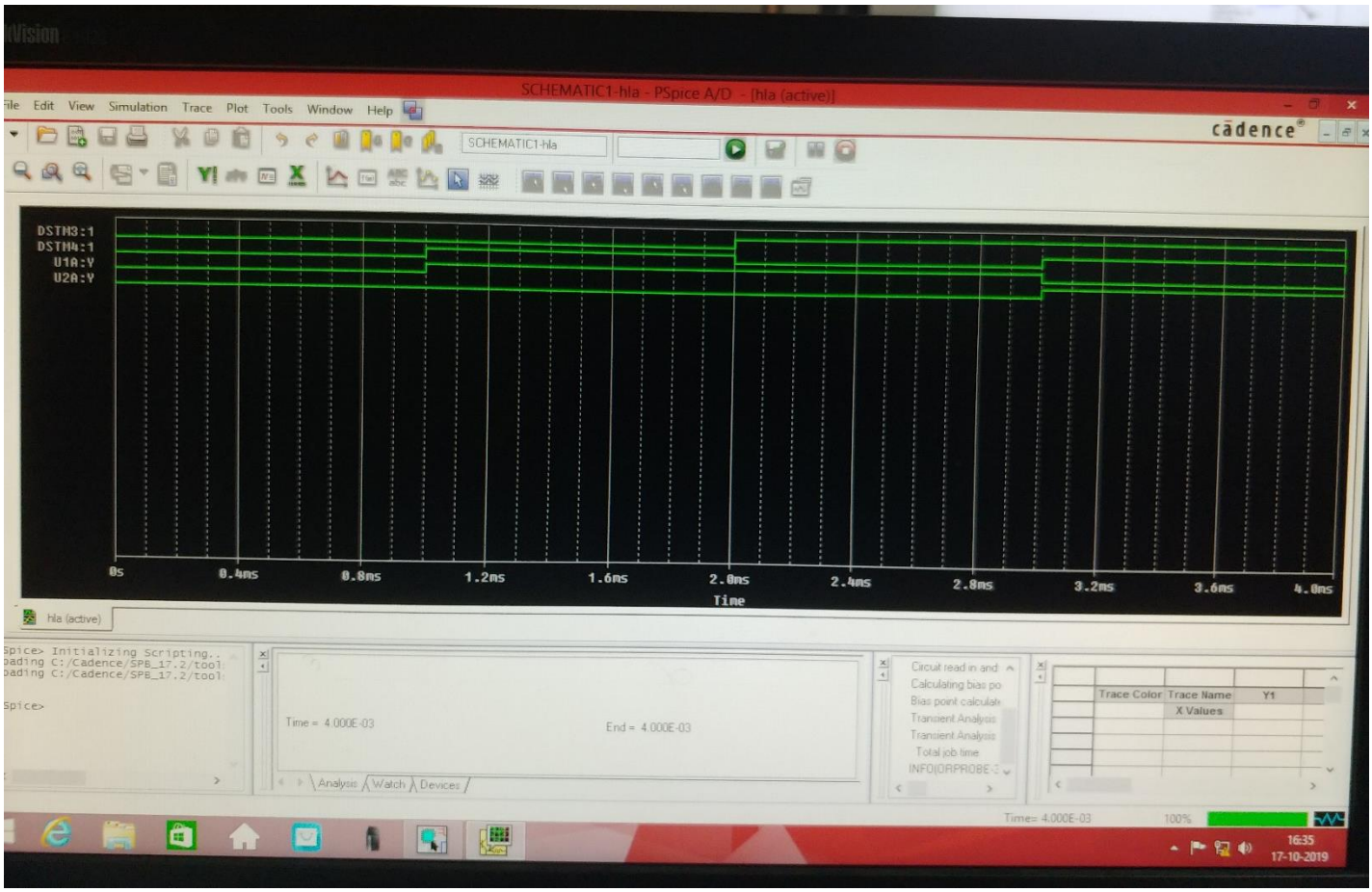


Full – Adder Circuit

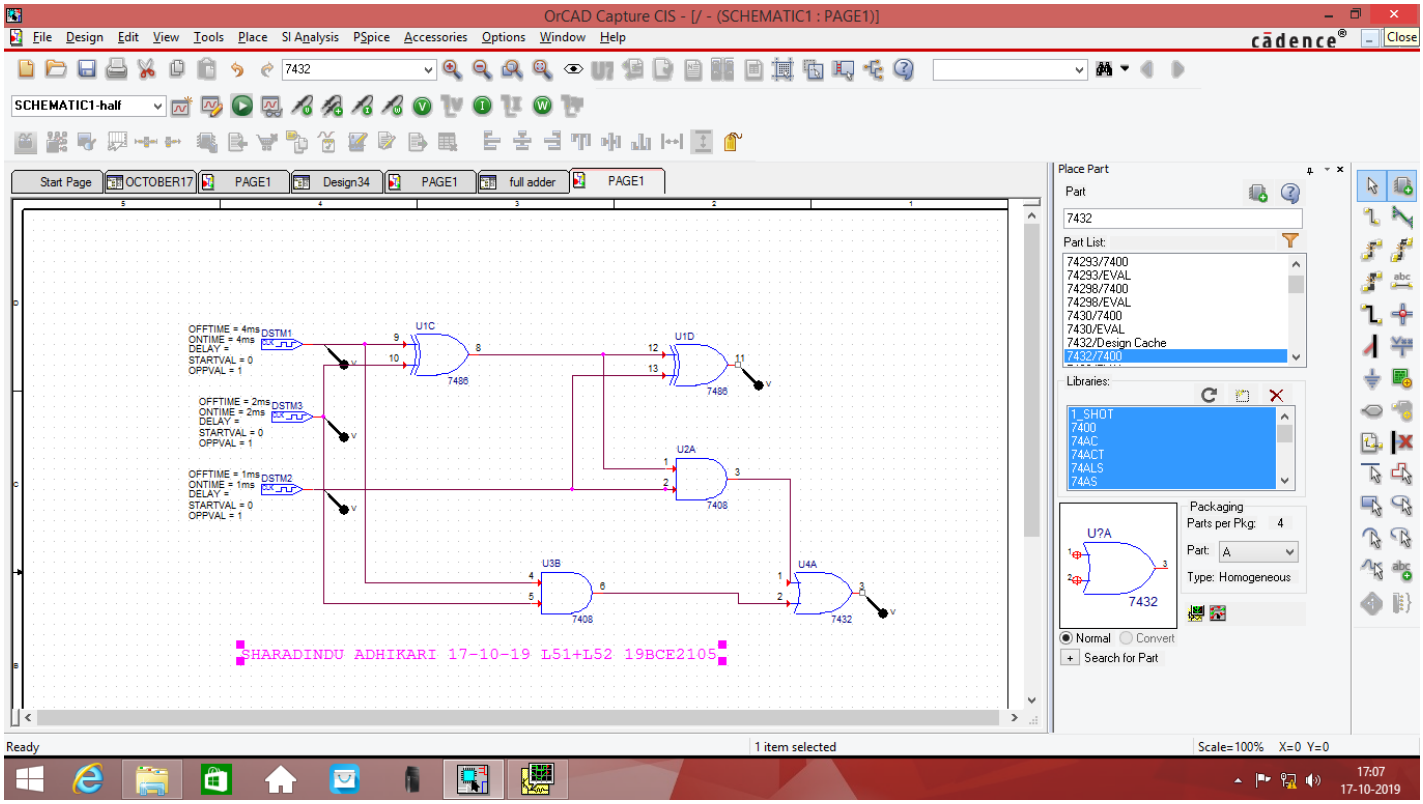


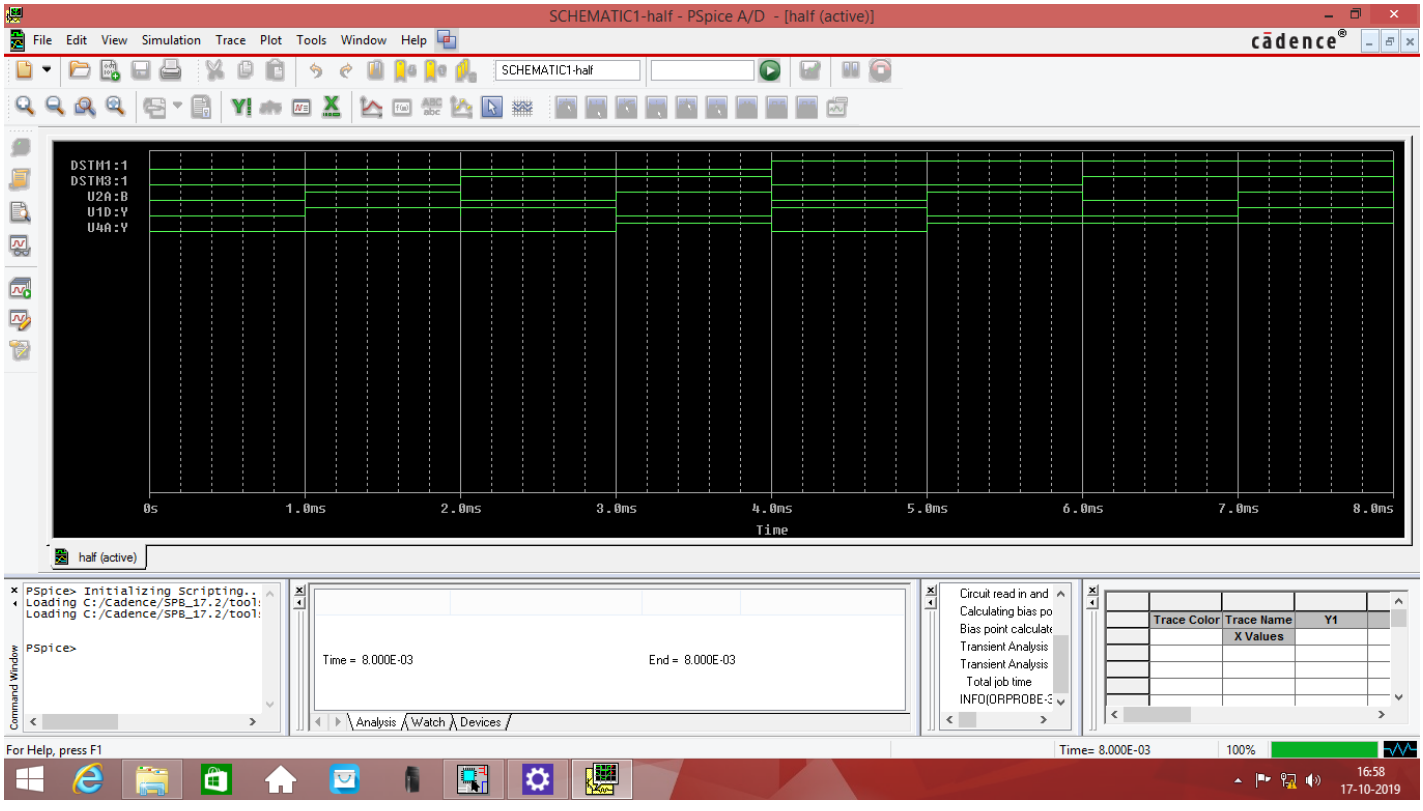
Half-Adder Circuit:





Full-Adder Circuit:





Theory:

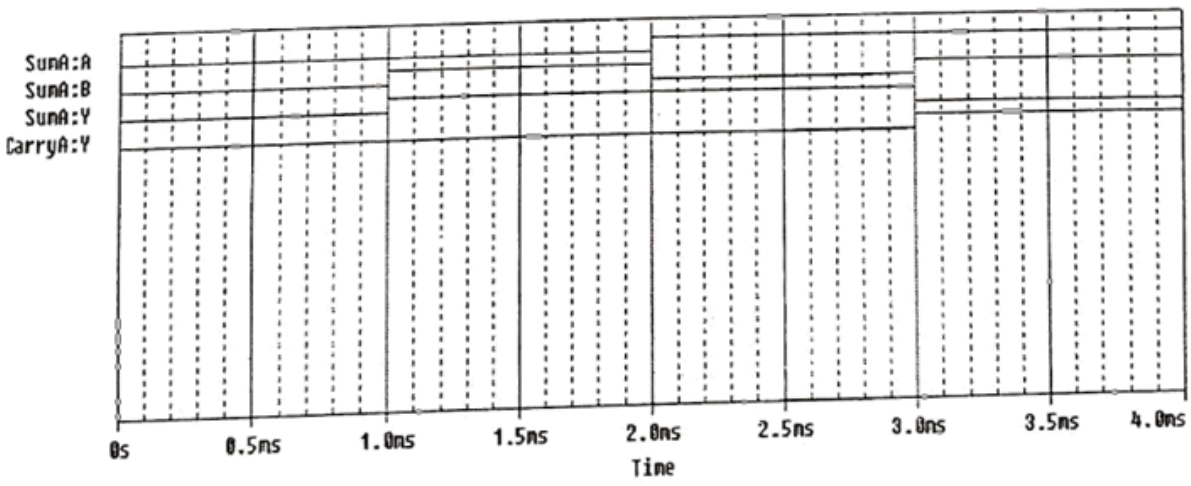
Half Adder Circuit:

Truth Table

A	B	S=A⊕B	C=A.B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Model Timing Diagram:

Half – Adder



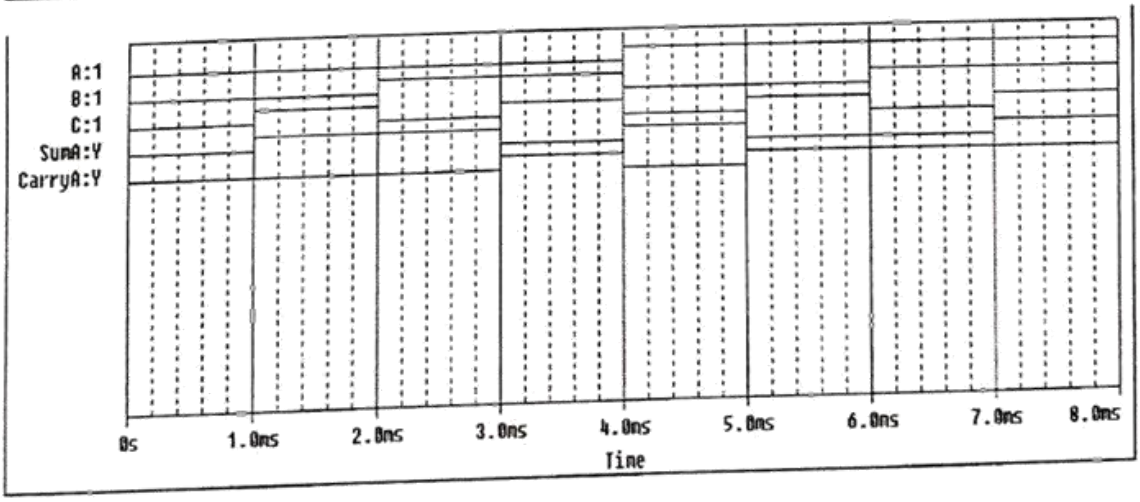
Full Adder Circuit

Truth Table

A	B	C	S=A⊕B⊕C	C= (A⊕B).C+A.B
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Model Timing Diagram:

Full – Adder



Procedure:

Result: ~~The half adder and full adder circuit truth tables and output wave forms have been verified in simulation waveforms~~

The half adder and full adder experiments have been performed using Capture CIS.

~~Inference~~

The truth table and its corresponding waveforms have been verified.

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