CS5222 Advanced Computer Architecture

Assignment 2.1: FPGA Programming

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B: Pipelining in HLS

Design latency: 16 194 cycles

Device utilisation:

Name	BRAM_18K	DSP48E	FF	LUT
Total	16	10	25405	30526

Floating point adders and multipliers used:

Instance	**Module**	BRAM_18K	DSP48E	FF	LUT
mmult_hw_fadd_32nbkb_U0	mmult_hw_fadd_32nbkb	0	2	205	390
mmult_hw_fadd_32nbkb_U1	mmult_hw_fadd_32nbkb	0	2	205	390
mmult_hw_fmul_32ncud_U2	mmult_hw_fmul_32ncud	0	3	143	321
mmult_hw_fmul_32ncud_U3	mmult_hw_fmul_32ncud	0	3	143	321
Total		**0**	**10**	**732**	**1462**

Initiation Interval achieved: 128 (target 1)

C: Increasing Pipeline Parallelism by Repartitioning Memories

Note that the target 42× speed-up could *not* be achieved; however, a speedup of $\frac{230331}{9018} = 25.5\times$ speed-up was attempted.

Design latency: 9018 cycles

Device utilisation:

Name	BRAM_18K	DSP48E	FF	LUT
Total	12	10	41339	21024

Floating point adders and multipliers used: 32 each

D: Amortizing Iteration Latency with Batching

Previous normalised latency = $\frac{9018}{8} = 1127.25$

Design latency with batch size **256**: 149 274 cycles

Normalised latency: $\frac{149\,274}{256} = 583.10$ cycles

Device utilisation:

Name	BRAM_18K	DSP48E	FF	LUT
Total	524	10	234738	57036

E: Extending Batch Size with Tiling

Previous normalised latency: $\frac{149\,274}{256} = 583.10$ cycles

Design latency with tile size 128, and batch size **512**: 162 573 cycles

Normalised latency: $\frac{162\,573}{512} = 317$ cycles

F: Hardware compilation and FPGA testing on the PYNQ

FPGA accuracy: 70.36 % validation error CPU accuracy: 13.04 % validation error

FPGA speed-up: 24.13×