CS5222 Advanced Computer Architecture

Assignment 2.2: Fixed-Point Optimisations on FPGA

Sharadh Rajaraman
A0189906L

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1. Fixed-point validation accuracy: 18.96 %
2. Design latency: 418984 cycles
3. Speedup over naïve floating-point implementation: $\frac{230332/8}{418984/8192} = 1024\times\frac{230332}{418984} \approx 563\times$ batch-normalised speedup
4. Overall device utilisation:

Name	BRAM_18K	DSP48E	FF	LUT
Total	262	129	19799	22049

5. FPGA Speedup: 51.89×
6. Classification accuracy: 20.00 % validation error
7. Number of multipliers: **127**
8. Initiation interval of pipelined loop: 1287 cycles
9. The design is bandwidth-limited.