Write-Up:

Question:

Write and HDL implementation for a 4:1 Demultiplexer. Simulate the same using structural model and depict the timing diagram for valid inputs:

CODE:
Main Module:

```
module demux4to1(input a,sel1,sel2,output y0,y1,y2,y3);
    and g1(y3,a,~sel1,~sel2);
    and g2(y2,a,~sel1,sel2);
    and g3(y1,a,sel1,~sel2);
    and g4(y0,a,sel1,sel2);
endmodule
```

Test Module:

```
module demux_tb;
    reg a,sel1,sel2;
    wire y0,y1,y2,y3;
    demux4to1 de(a,sel1,sel2,y0,y1,y2,y3);
    initial
   begin
        $dumpfile("demux.vcd");
        $dumpvars(0,demux_tb);
        a = 0;sel1 = 0;sel2 = 0;
        #20
        a = 1;sel1 = 0;sel2 = 0;
        #20
        a = 0;sel1 = 0;sel2 = 1;
```

```
        #20
        a = 1;sel1 = 0;sel2 = 1;
        #20
        a = 0;sel1 = 1;sel2 = 0;
        #20
        a = 1;sel1 = 1;sel2 = 0;
        #20
        a = 0;sel1 = 1;sel2 = 1;
        #20
        a = 1;sel1 = 1;sel2 = 1;
        #20
        $finish;
    end
endmodule
```

Execution:

Output: