Scalable High Performance Main Memory System Using Phase-Change Memory Technology

Summary:

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This paper looks at a novel memory hierarchy organization including Phase Change Memory. The authors look at PCM to see if it is feasible to use as a replacement to one of the existing memory hierarchy layers.

There is a minor problem in totally replacing DRAM with PCM.

- PCM is a lot slower (around 4x slower) than DRAM.
- PCM has lesser endurance compared to DRAM.

The authors solve the 2 issues in the paper.

- Solution to issue 1: Put a smaller DRAM before the larger PCM. The small DRAM acts similar to a cache. it returns read data much faster than PCM alone would have. Ideally if the hot pages are always available in the smaller DRAM, the application would suffer no performance loss.
- Solution to issue 2: Try and write uniformly over the entire PCM. We don't want a small portion to be written a lot compared to other parts. Thereby, keep rotating data throughout the PCM such that all parts of the PCM chip get written more-or-less uniformly, thereby maximizing lifetime. Try to avoid writes to PCM wherever possible, and write to the PCM memory in smaller chunks instead of a page.

Some optimisations proposed are:

- **Lazy Write:** A page is written to the PCM only when it is evicted from the DRAM storage, and it is not already present in PCM, or the dirty bit is set.
- **Line Level Write-back:** When a dirty page is evicted from the DRAM, if the page is already present in the PCM, only the dirty lines of the page are written to the PCM.
- **Page Level Bypass:** When a page is evicted from DRAM, PLB invalidates the Page Table Entry associated with the page, and does not install the page in PCM.
- **Fine Grained Wear Leveling (FGWL):** The lines in each page are stored in the PCM in a rotated manner.

Questions:

1. If we utilise the non-volatility of PCM, would it give better results?
2. It is not explained how the hybrid models have better performance than models without flash-disc caches?