Design of Telescopic Opamp

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***Abstract*—This paper presents the design and simulation of a two-stage telescopic operational amplifier in SCL $180\,\mathrm{nm}$ CMOS technology, optimized for low-power and moderate-voltage analog applications. The proposed amplifier operates from a $1.8\,\mathrm{V}$ supply and employs a telescopic cascode architecture to achieve high intrinsic gain and wide bandwidth while maintaining low power dissipation. A dedicated biasing circuit is used to generate stable bias voltages, and Miller compensation is applied to ensure closed-loop stability. Comprehensive AC, DC, and transient simulations are performed with a load capacitance of $1\,\mathrm{pF}$. The amplifier achieves a differential gain of $102\,\mathrm{dB}$, a common-mode gain of $-4\,\mathrm{dB}$, and a CMRR of $106\,\mathrm{dB}$. The unity-gain bandwidth is $610.2\,\mathrm{kHz}$ with a phase margin of 58°. The PSRR is $71\,\mathrm{dB}$, and the slew rate is $0.44\,\mathrm{V}/\mu\mathrm{s}$. The input and output common-mode ranges are also validated through DC analysis, while the total power dissipation is $58.482\,\mu\mathrm{W}$. The obtained results demonstrate that the proposed telescopic op-amp offers a good trade-off between gain, speed, stability, and power efficiency.**

***Index Terms*—Telescopic operational amplifier, CMOS analog design, SCL 180 nm technology, low-power op-amp, unity-gain bandwidth, phase margin, CMRR, PSRR.**

I. Introduction

The telescopic cascode operational amplifier is a widely used topology in high-performance analog integrated circuits due to its ability to achieve high voltage gain, wide bandwidth, and low power consumption. By employing cascoded transistors in a single signal path, the telescopic architecture significantly increases output resistance, thereby enhancing the intrinsic gain while maintaining a relatively simple structure. These characteristics make telescopic op-amps particularly attractive for applications requiring high speed and low noise, such as data converters, sample-and-hold circuits, and precision analog front ends.[1]

Despite its advantages, the telescopic topology is inherently constrained by limited voltage headroom, which restricts both the input common-mode range (ICMR) and output voltage swing. This limitation becomes more pronounced in low-voltage CMOS technologies, where reduced supply voltages further limit the allowable stacking of transistors. As a result, the design of telescopic op-amps demands careful trade-offs between gain, swing, stability, and power dissipation. Proper biasing, device sizing, and compensation techniques are essential to ensure reliable operation under these constraints.[2]

In this work, a two-stage telescopic operational amplifier designed for a $1.8\,\mathrm{V}$ supply voltage is presented and analyzed. The amplifier is optimized to achieve high differential gain and common-mode rejection while maintaining adequate phase margin and low power dissipation. Comprehensive AC, transient, and DC simulations are carried out to evaluate the frequency response, stability, large-signal behavior, and operating ranges of the proposed design. The results demonstrate that, with careful design considerations, the telescopic op-amp remains a viable and efficient solution for low-power and moderate-voltage analog applications.

II. Design Methodology

The schematic of the proposed telescopic operational amplifier along with its biasing circuit is shown in Fig. 1 and Fig. 2, respectively. The amplifier is designed to operate from a $1.8\,\mathrm{V}$ supply while achieving high gain, adequate stability, and low power dissipation.

The transistor dimensions are carefully selected to satisfy gain, speed, and voltage headroom constraints. The input differential pair transistors M_1 and M_2 are sized with a width-to-length ratio of $0.42/4\,\mu\mathrm{m}$ to obtain sufficient transconductance and good device matching. The cascode transistors M_3 and M_4 use dimensions of $0.42/2\,\mu\mathrm{m}$ to increase output resistance and improve voltage gain while preserving adequate headroom. Transistors M_5–M_8, forming the load and bias branches, are sized at $0.42/1\,\mu\mathrm{m}$ to ensure stable bias currents across the amplifier.

Transistor M_9 is designed with dimensions of $0.42/0.2\,\mu\mathrm{m}$ to support a higher current density where required. The bias generator transistors M_{10} and M_{11} are sized at $5/2\,\mu\mathrm{m}$ to establish well-defined bias voltages, while transistors M_{12}–M_{15} employ dimensions of $0.42/0.54\,\mu\mathrm{m}$ to provide reliable current mirroring within the biasing network. The input DC common-mode voltage is set to $500\,\mathrm{mV}$ to maintain all transistors in saturation over the operating range.

To ensure stable operation of the two-stage amplifier, Miller compensation is implemented by placing a capacitor of $1\,\mathrm{pF}$ between the first and second stages. This compensation technique introduces a dominant pole at low frequency and achieves an adequate phase margin for stable closed-loop operation.

III. Simulation Results

The proposed two-stage telescopic operational amplifier was designed for a single-ended supply voltage of $1.8\,\mathrm{V}$ and a load capacitance of $1\,\mathrm{pF}$. Post-layout AC, transient, and DC simulations were carried out to evaluate the small-signal and large-signal performance.

The amplifier achieves a low-frequency differential-mode gain of $102\,\mathrm{dB}$ and a common-mode gain of $-4\,\mathrm{dB}$, resulting

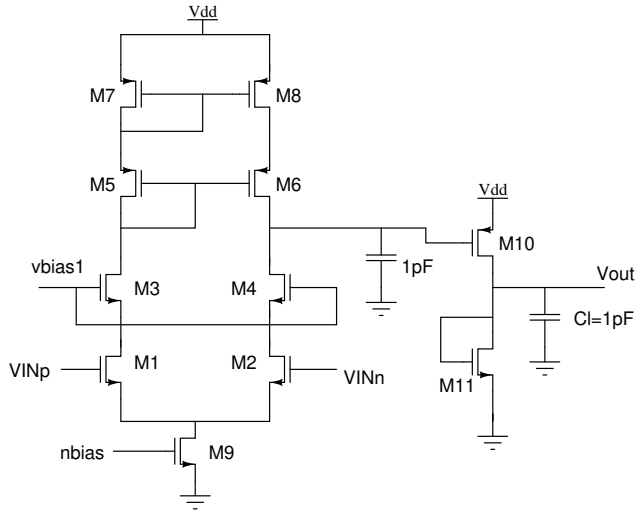

Fig. 1: Schematic of the proposed telescopic operational amplifier with labeled transistors and device dimensions (W/L in μm).

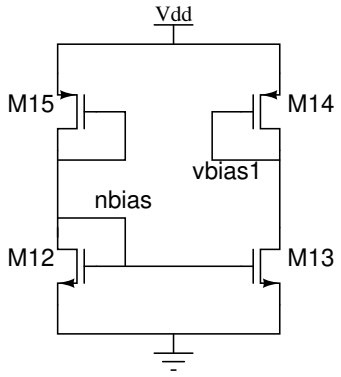

Fig. 2: Biasing circuit used to generate the required bias voltages and currents for the telescopic op-amp, ensuring stable operation across process and voltage variations.

in a CMRR of $106\,\mathrm{dB}$. The unity-gain bandwidth (UGBW) is $610.2\,\mathrm{kHz}$ with a phase margin of $58°$, ensuring stable closed-loop operation. The power-supply rejection ratio (PSRR) at low frequency is $71\,\mathrm{dB}$. From the large-signal transient response in unity-gain configuration, the output slew rate is obtained as $0.44\,\mathrm{V}/\mu\mathrm{s}$.

The input common-mode range (ICMR) extends from $0.499\,\mathrm{V}$ to $0.873\,\mathrm{V}$, while the output common-mode range (OCMR) varies between $0.553\,\mathrm{V}$ and $0.833\,\mathrm{V}$ for the specified load and supply conditions. A concise performance summary of the designed amplifier is given in Table I.

IV. Simulation Plots and Analysis

This section presents the simulated performance plots of the designed two-stage telescopic operational amplifier obtained from AC, transient, and DC analyses. All simulations are carried out at a supply voltage of $1.8\,\mathrm{V}$ with a load capacitance of $1\,\mathrm{pF}$.

TABLE I: Performance Summary of the Designed Telescopic Op-Amp

Parameter	Value
Supply voltage, V_{DD}	$1.8\,\mathrm{V}$
Load capacitance, C_{L}	$1\,\mathrm{pF}$
Differential gain	$102\,\mathrm{dB}$
Common-mode gain	$-4\,\mathrm{dB}$
CMRR	$106\,\mathrm{dB}$
Phase margin	$58°$
UGBW	$610.2\,\mathrm{kHz}$
PSRR	$71\,\mathrm{dB}$
Slew rate	$0.44\,\mathrm{V}/\mu\mathrm{s}$
ICMR (min–max)	0.499–$0.810\,\mathrm{V}$
OCMR (min–max)	0.553–$0.873\,\mathrm{V}$
Power dissipation	$58.482\,\mu\mathrm{W}$

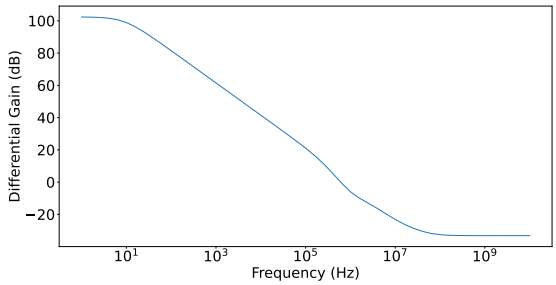

Fig. 3: Differential gain versus frequency of the proposed telescopic op-amp. A low-frequency gain of $102\,\mathrm{dB}$ is achieved, and the unity-gain bandwidth (UGBW) is observed at $610.2\,\mathrm{kHz}$, indicated by the 0-dB crossover.

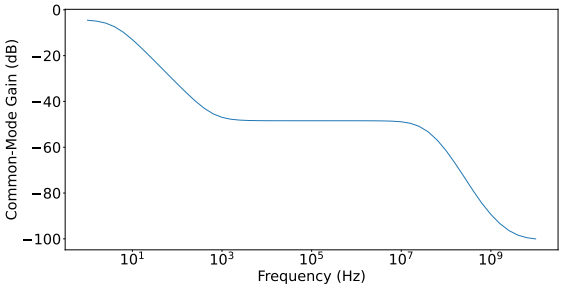

Fig. 4: Common-mode gain versus frequency plot. The common-mode gain remains low across the frequency range, confirming effective suppression of common-mode signals.

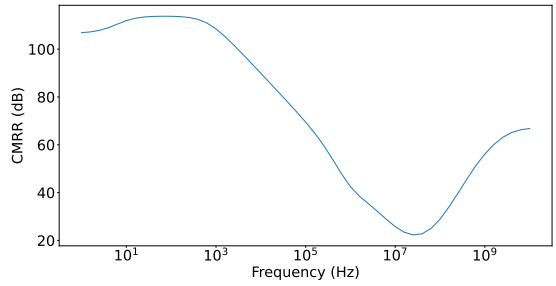

Fig. 5: CMRR as a function of frequency. A high low-frequency CMRR of $106\,\mathrm{dB}$ is achieved, indicating excellent differential-to-common-mode signal rejection.

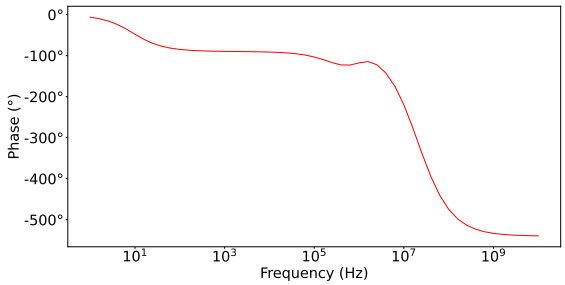

Fig. 6: Phase response of the telescopic op-amp. The phase margin measured at the unity-gain frequency is $58°$, ensuring stable closed-loop operation.

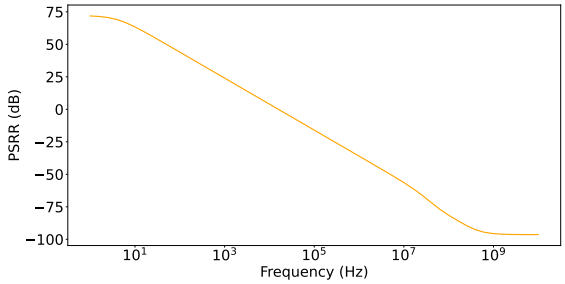

Fig. 7: Power Supply Rejection Ratio (PSRR) versus frequency. A low-frequency PSRR of $71\,\mathrm{dB}$ is obtained, demonstrating good immunity to supply voltage variations.

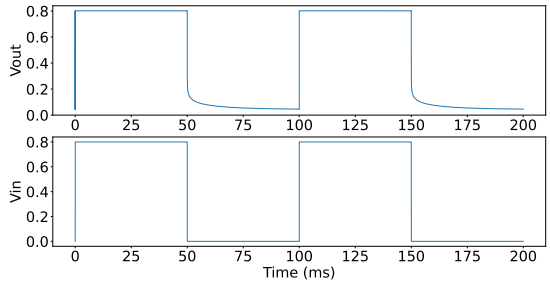

Fig. 8: Transient response of the op-amp under unity-gain feedback. The applied square-wave input (V_{in}) and the corresponding output response (V_{out}) are shown. The linear rising segment of the output waveform is used to estimate a slew rate of $0.44\,\mathrm{V}/\mu\mathrm{s}$.

V. Conclusion

A two-stage telescopic operational amplifier has been designed and analyzed for low-power analog applications using a $1.8\,\mathrm{V}$ supply voltage. The telescopic cascode topology, together with a carefully designed biasing network and Miller compensation, enables high gain and stable operation under limited voltage headroom. Simulation results confirm that the proposed amplifier achieves a high differential gain of $102\,\mathrm{dB}$, a CMRR of $106\,\mathrm{dB}$, and a unity-gain bandwidth of $610.2\,\mathrm{kHz}$ with a phase margin of $58°$. The amplifier also exhibits good power-supply rejection, acceptable slew-rate performance, and validated input and output common-mode ranges while dissipating only $58.482\,\mu\mathrm{W}$.

The results demonstrate that, despite the inherent swing limitations of the telescopic architecture, careful device sizing, biasing, and compensation allow it to remain a viable and efficient solution for low-power and moderate-voltage analog integrated circuits. The proposed design is therefore well suited for applications such as sensor interfaces, data converters, and analog front-end circuits.

References

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[2] Behzad Razavi, “Design of Analog CMOS Integrated Circuits,” McGraw Hill, 2001.

[3] Jan M. Rabaey, “Digital Integrated Circuits: A Design Perspective,” 2nd Edition, Prentice Hall, 2002.