**VISVESVARAYA TECHNOLOGICAL UNIVERSITY**

# JNANASANGAMA, BELAGAVI-590018



**Lab Report on**

**“Digital Design & Computer Organization” Subject code: BCS302**

# 3rd sem “CS&E(AI & ML)”

**Submitted by**

## SHARATH



**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**

**K.V.G. COLLEGE OF ENGINEERING SULLIA, D.K.-574327**

# 2023-24



**LABORATORY CERTIFICATE**

This is to certify that Mr./Ms SHARATH USN has satisfactorily completed course of experiments in Digital Design & Computer Organization prescribed by the Visvesvaraya technological University(VTU) for the 3RD Sem B.E course during the year 2023-24.

|  |  |
| --- | --- |
| ***Practical session assessment*** | |
| ***Max. Marks:*** | ***Marks Awarded:*** |

**Signature of staff in charge Signature of HOD**



## Particulars of the experiments performed

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **SL.**  **NO** | **DATE** | **TITLE OF THE EXPERIMENT** | **PAGE**  **NO** | **MARKS** |
| **1** |  | Given a 4-variable logic expression, simplify  it using appropriate technique and simulate the same using basic gates. | **1-3** |  |
| **2** |  | Design a 4 bit full adder and subtractor and  simulate the same using basic gates. | **4** |  |
| **3** |  | Design Verilog HDL to implement simple circuits using structural, Data flow and  Behavioural model. | **5-7** |  |
| **4** |  | Design Verilog HDL to implement Binary Adder-Subtractor – Half and Full Adder,  Half and Full Subtractor. | **8-11** |  |
| **5** |  | Design Verilog HDL to implement Decimal  adder. | **12-13** |  |
| **6** |  | Design Verilog program to implement Different types of multiplexer like 2:1, 4:1  and 8:1. | **14-20** |  |
| **7** |  | Design Verilog program to implement types  of De-Multiplexer. | **21-22** |  |
| **8** |  | Design Verilog program for implementing various types of Flip-Flops such as SR, JK and D. | **23-26** |  |
|  |  | **TOTAL MARKS** |  |  |
|  |  | **AVERAGE MARKS** |  |  |

|  |  |  |
| --- | --- | --- |
| ***Average marks for***  ***conduction and report:*** | ***Test:*** | ***Viva-voce:*** |