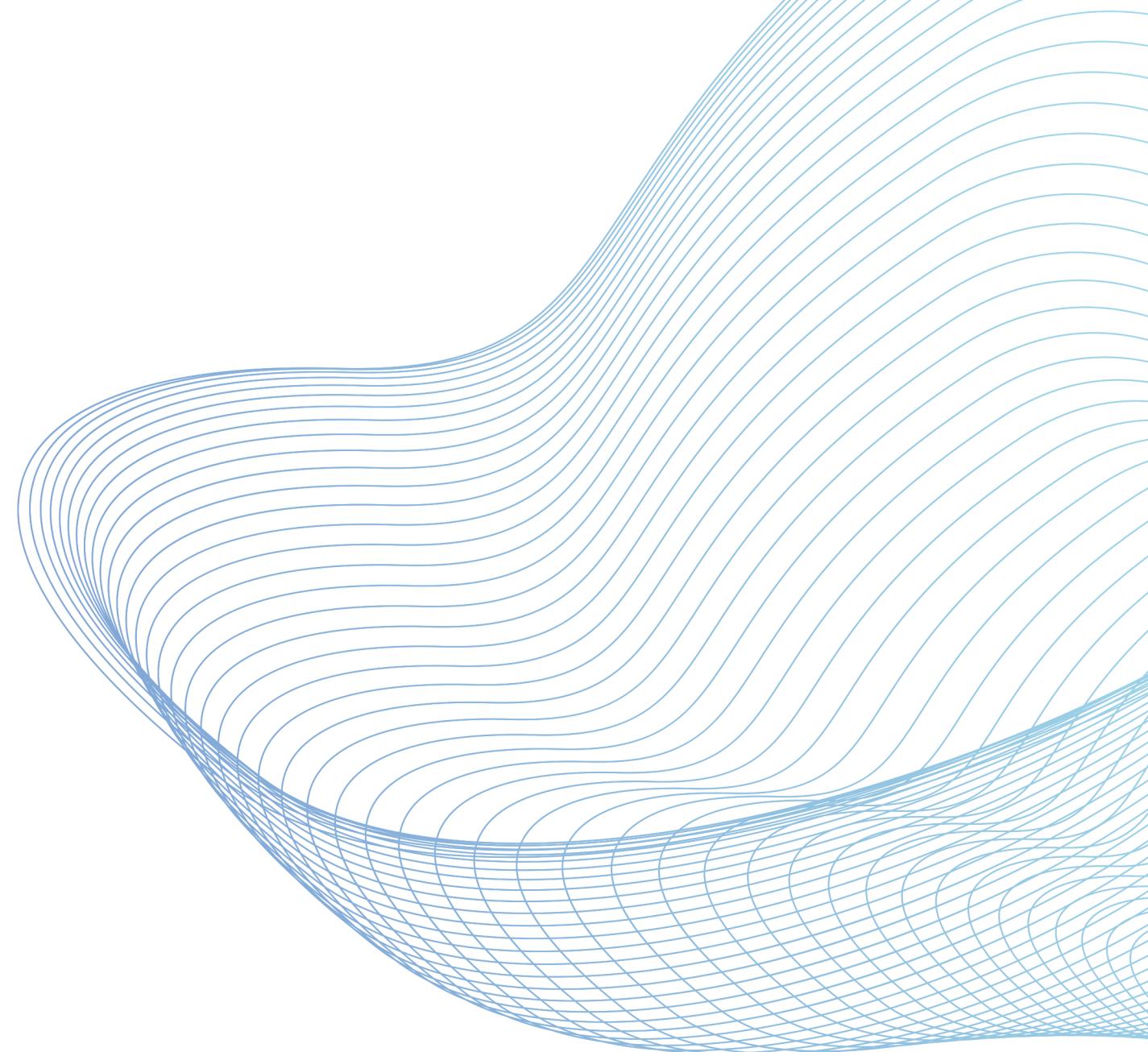


RELIABILITY ANALYSIS IN DIGITAL CIRCUITS



Mentor :

Dr.Pushpa Raikwal

Presented by:

B. Rakesh(20BEC026)

B. Sharath Naik(20BEC028)

R. Narahari(20BEC088)

V S S Sainath

Sanapala(20BME061)

INTRODUCTION

Lifetime Reliability is a significant concern with downscaling of CMOS technology. There are many phenomenon that degrades the circuit performance. As time passes and temperature vary, these phenomenon come into effect. We study the effects and propose a efficient circuit which performs well.

RELIABILITY PARAMETERS

TIME DELAY

Time delay is defined as the time taken to a signal to propagate through the input to output. For a circuit to be more reliable, it should have the least time delay.

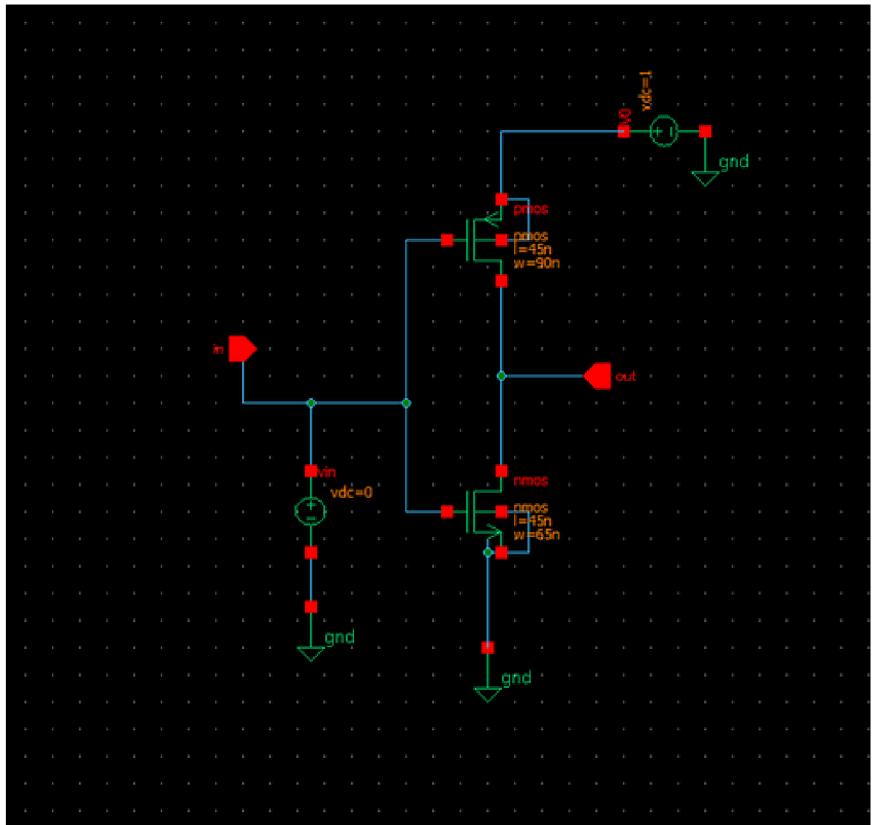
LEAKAGE CURRENT

Leakage current is the current that flows through the circuit even when it is in off state. It can also be defined as off state current of a circuit. Leakage current should be less for a circuit to be more reliable.

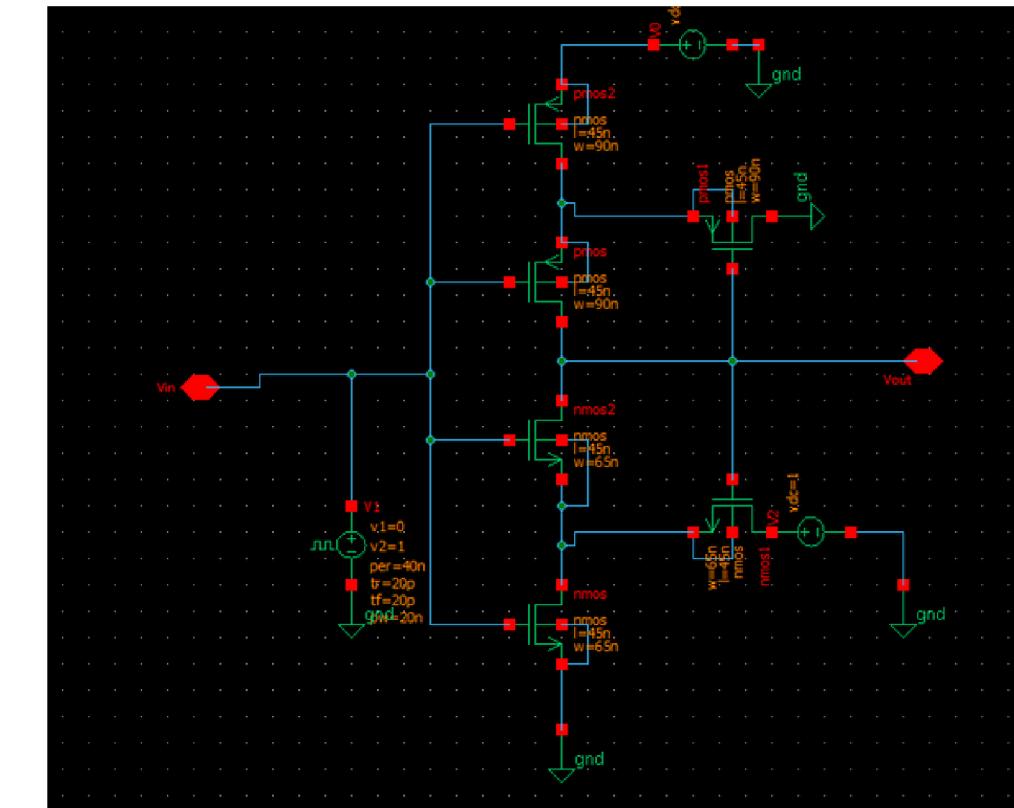
CRITICAL CHARGE

Critical charge is the minimum amount of charge that must be deposited by a particle strike to cause a circuit to malfunction. More the critical charge more is the circuit reliability

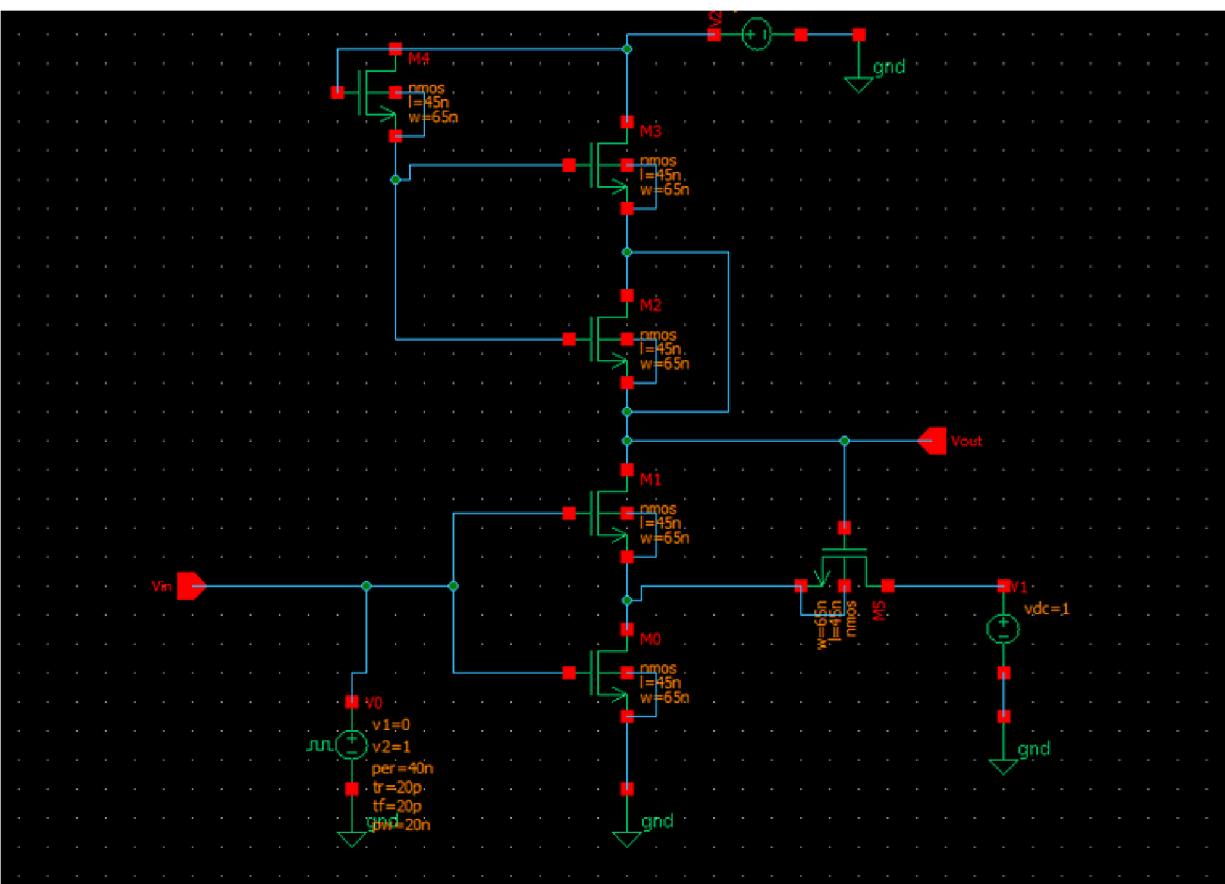
CIRCUIT DIAGRAMS



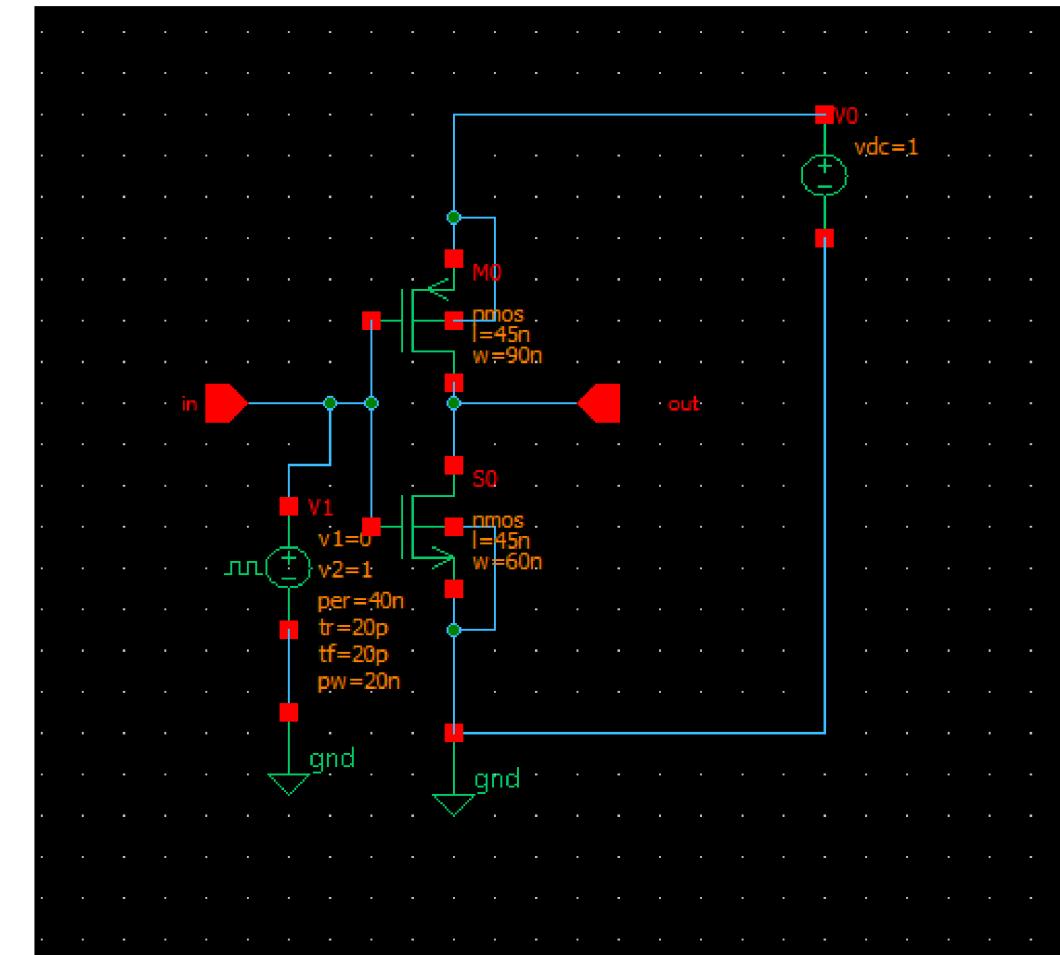
CMOS INVERTER



SCHMITT TRIGGER

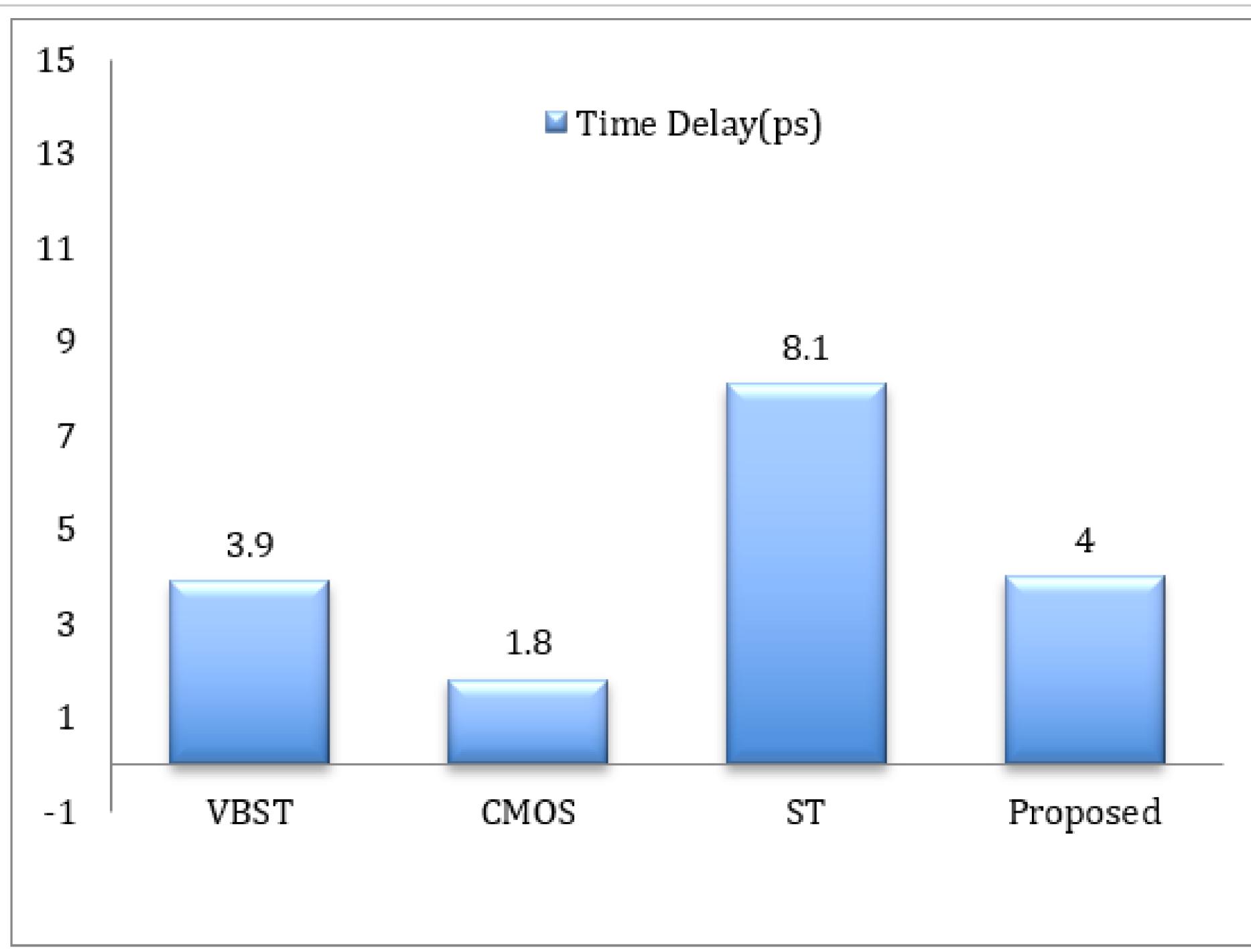


VOLTAGE BOOTSTRAPPING SCHMITT TRIGGER

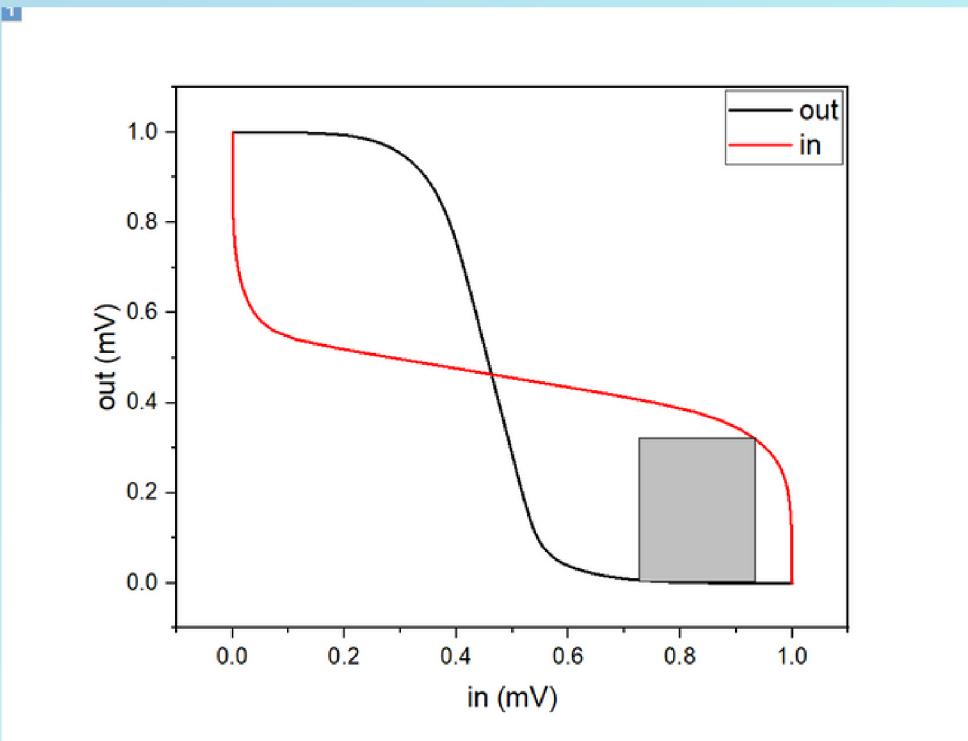


FINFET BASED INVERTER

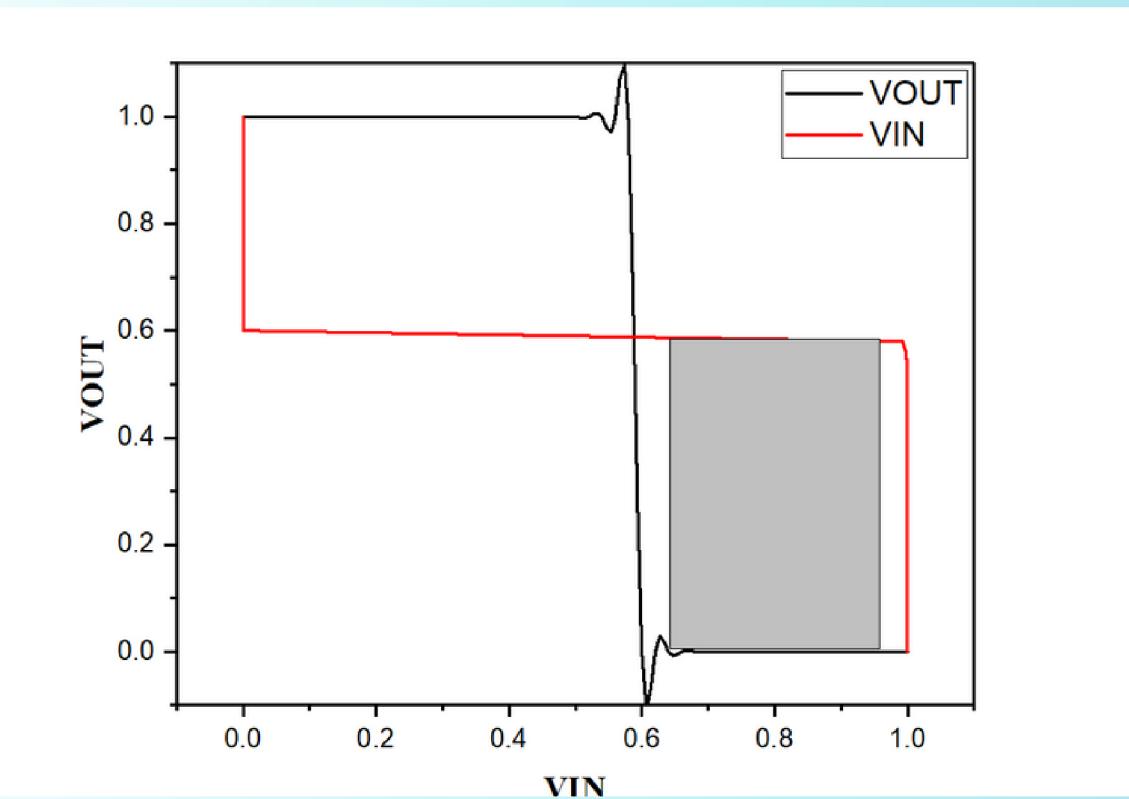
Time Delay Comparison Graph



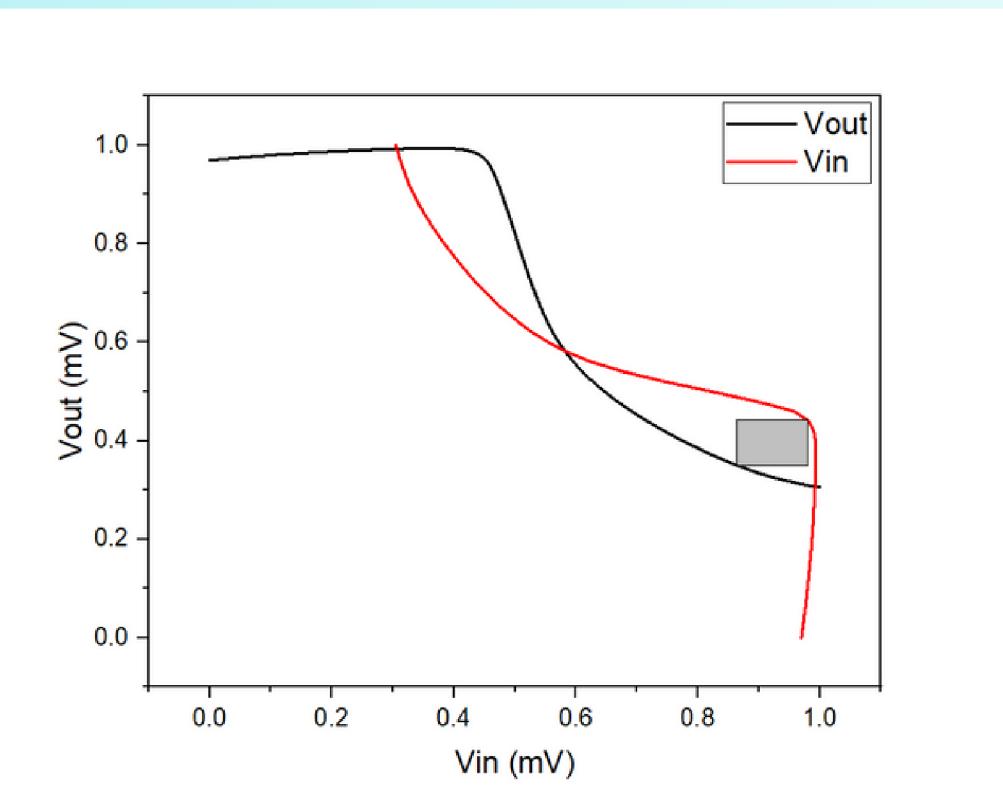
STATIC NOISE MARGIN(SNM)



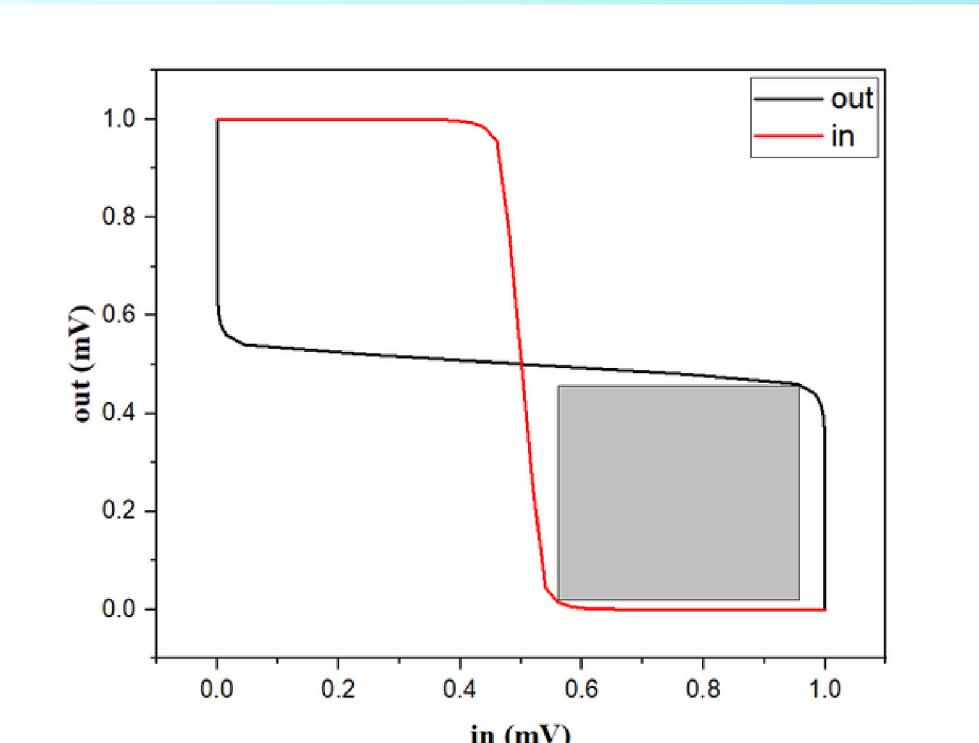
CMOS Inverter



Schmitt Trigger

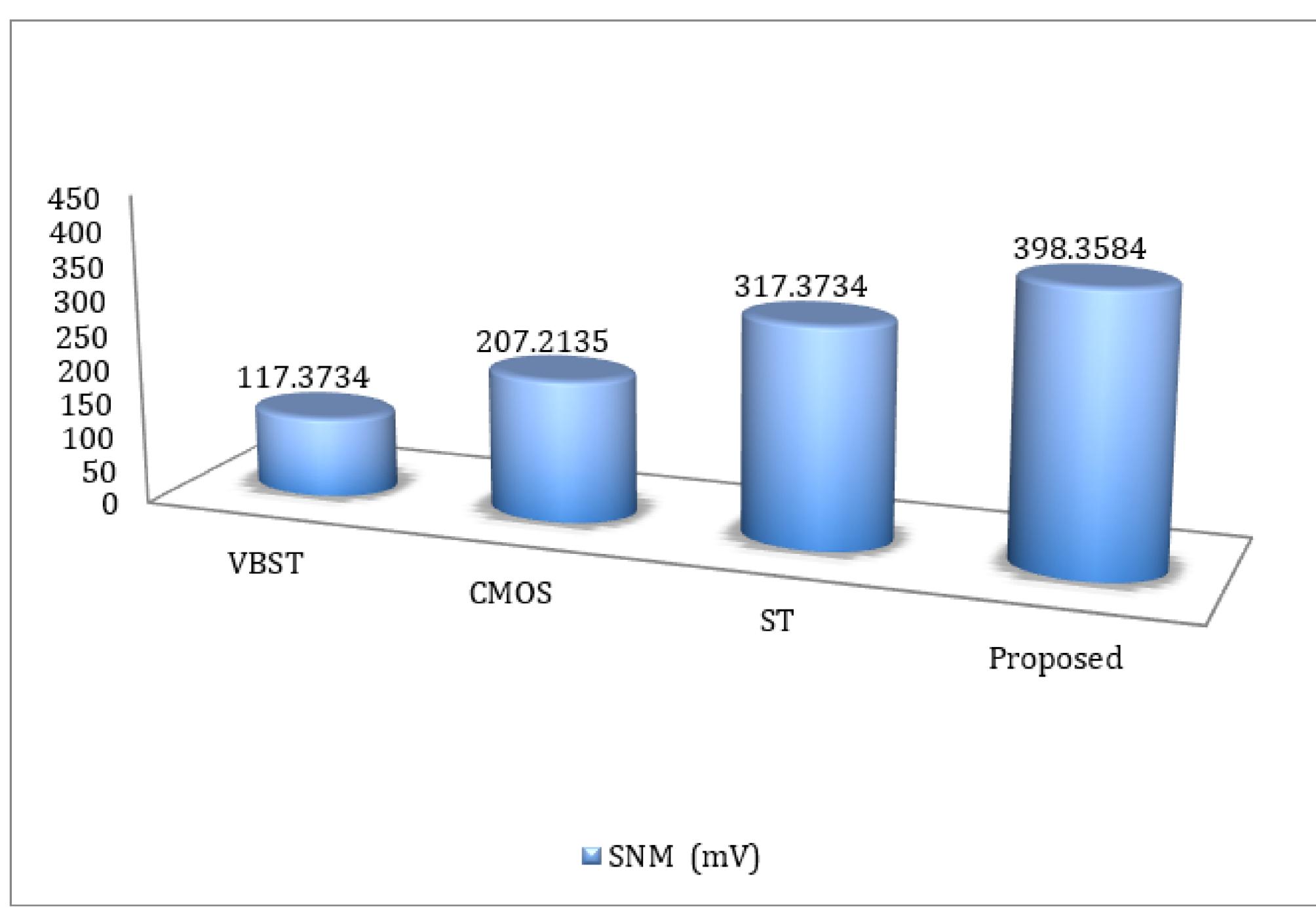


VBST



FinFET based Inverter

Static Noise Margin(SNM) comparison

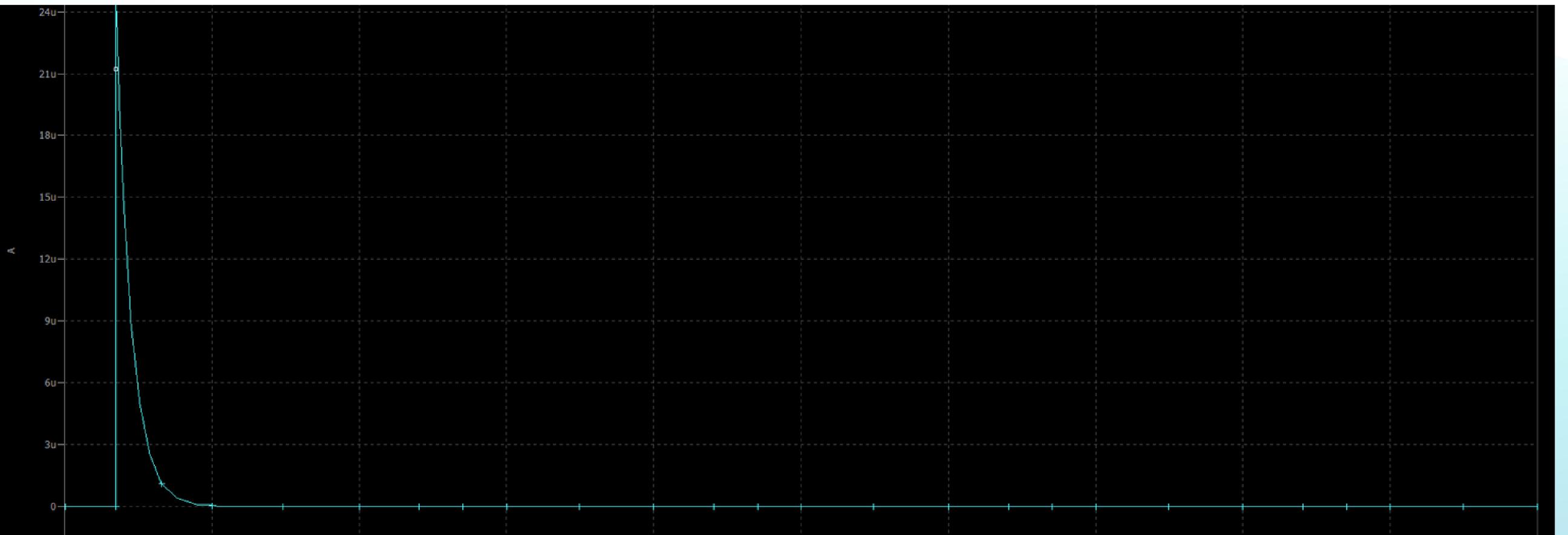


Critical Charge

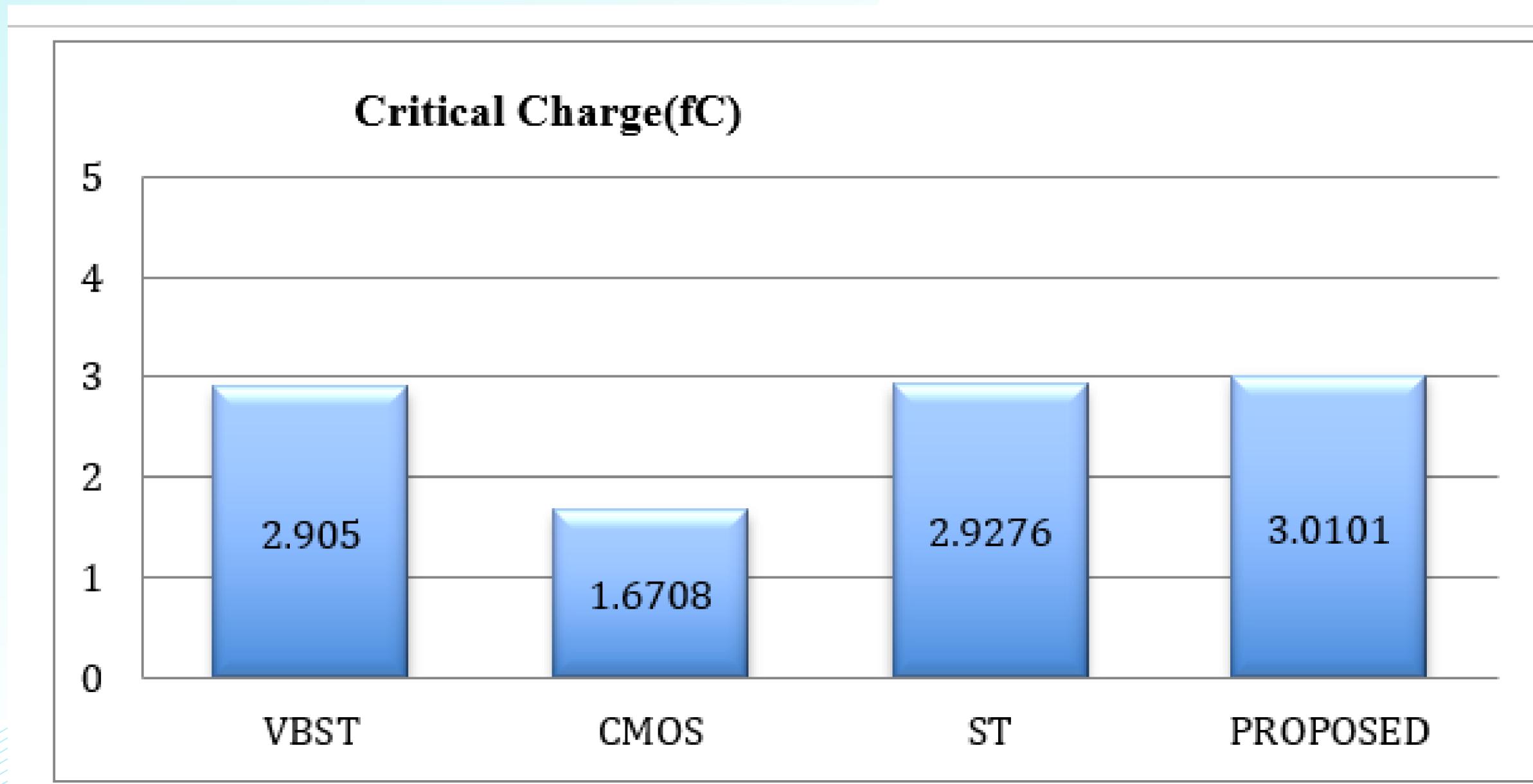
$$I_{inj}(t) = I_{peak} \times \left(e^{-\frac{t}{Tf}} - e^{-\frac{t}{Tr}} \right)$$

Tr = Rise Time, Tf = Fall Time

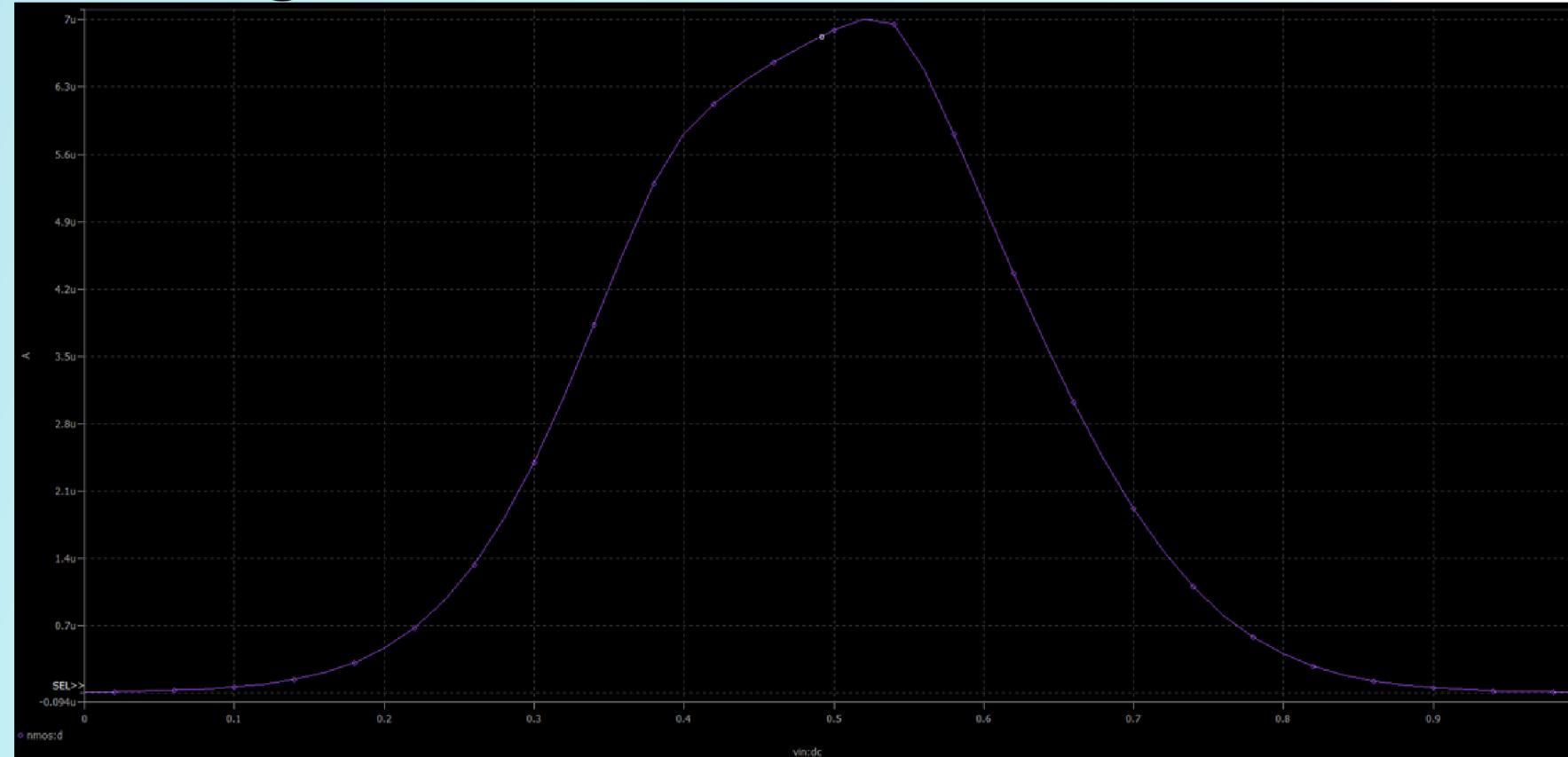
$$Q = \int_0^{T_{crit}} I_{inj}(t) dt$$



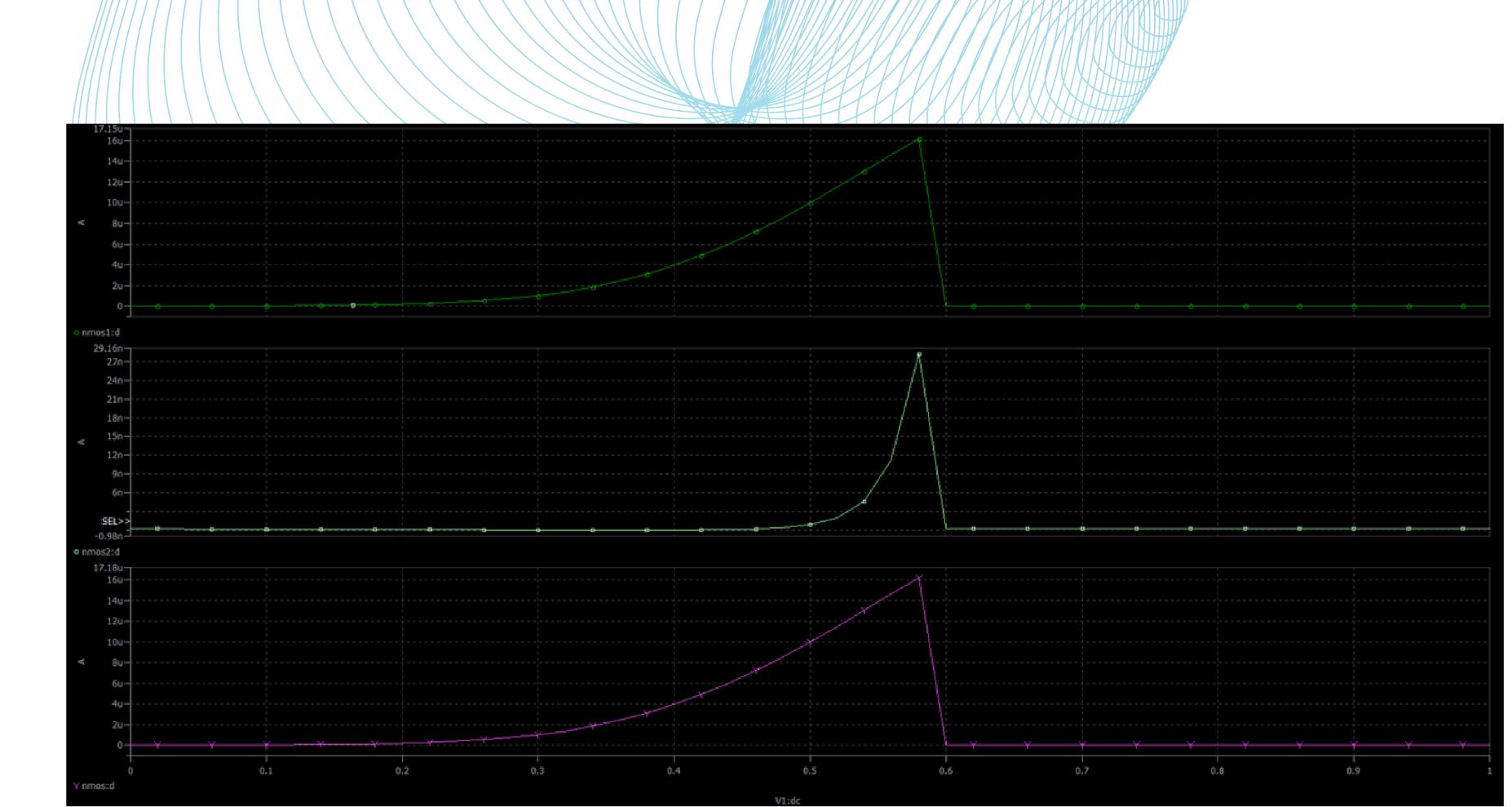
Critical Charge comparison



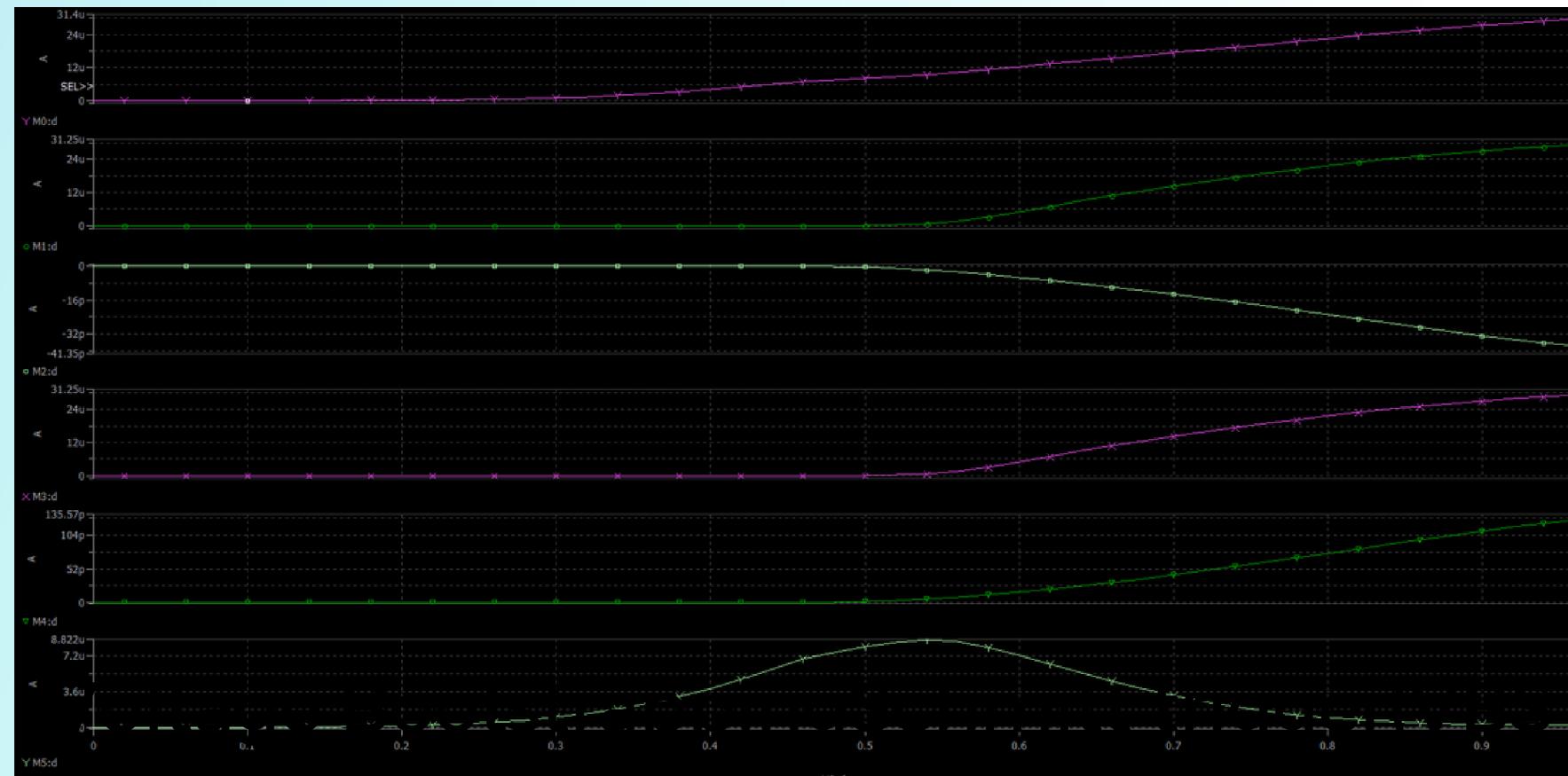
Leakage Current



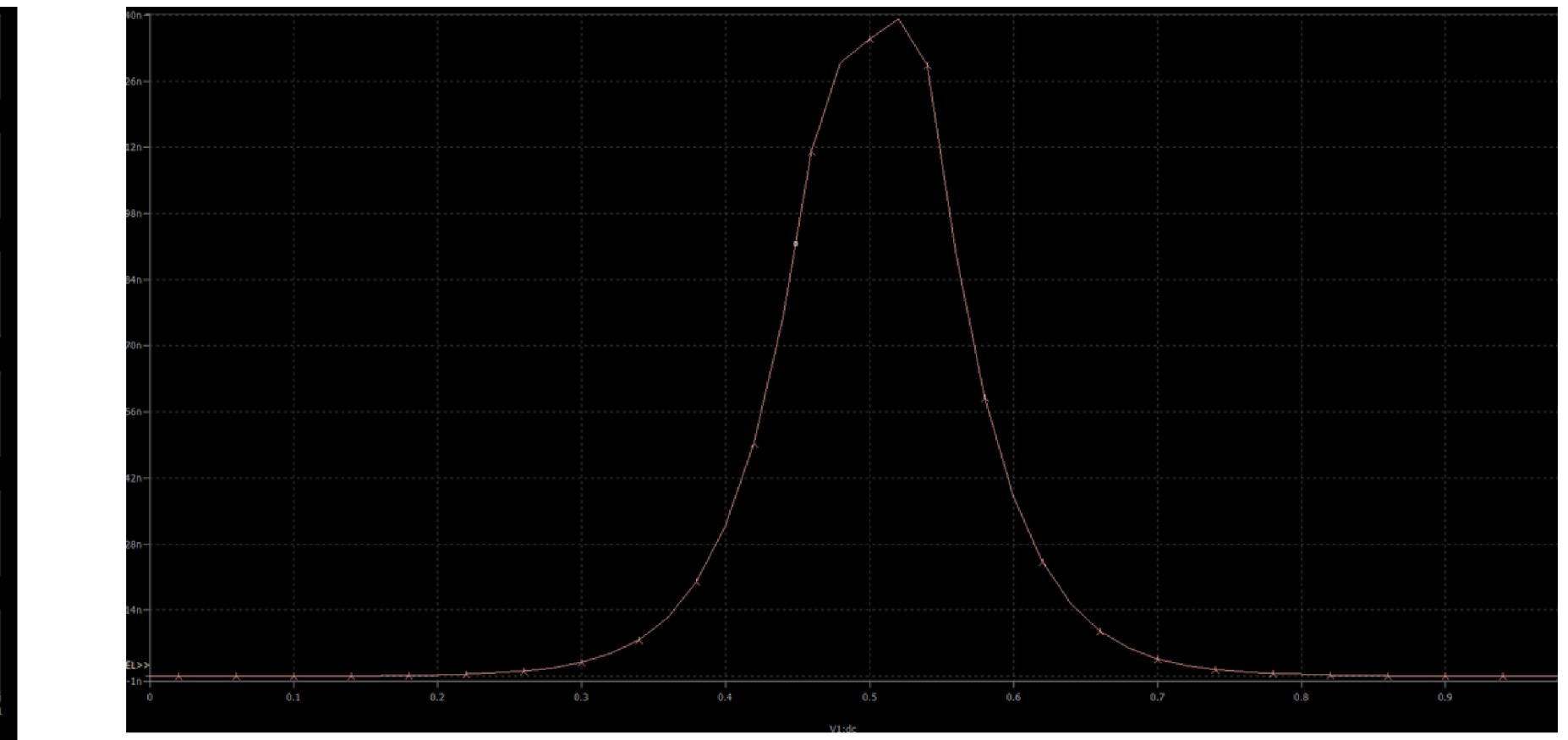
CMOS Inverter



Schmitt Trigger(ST)

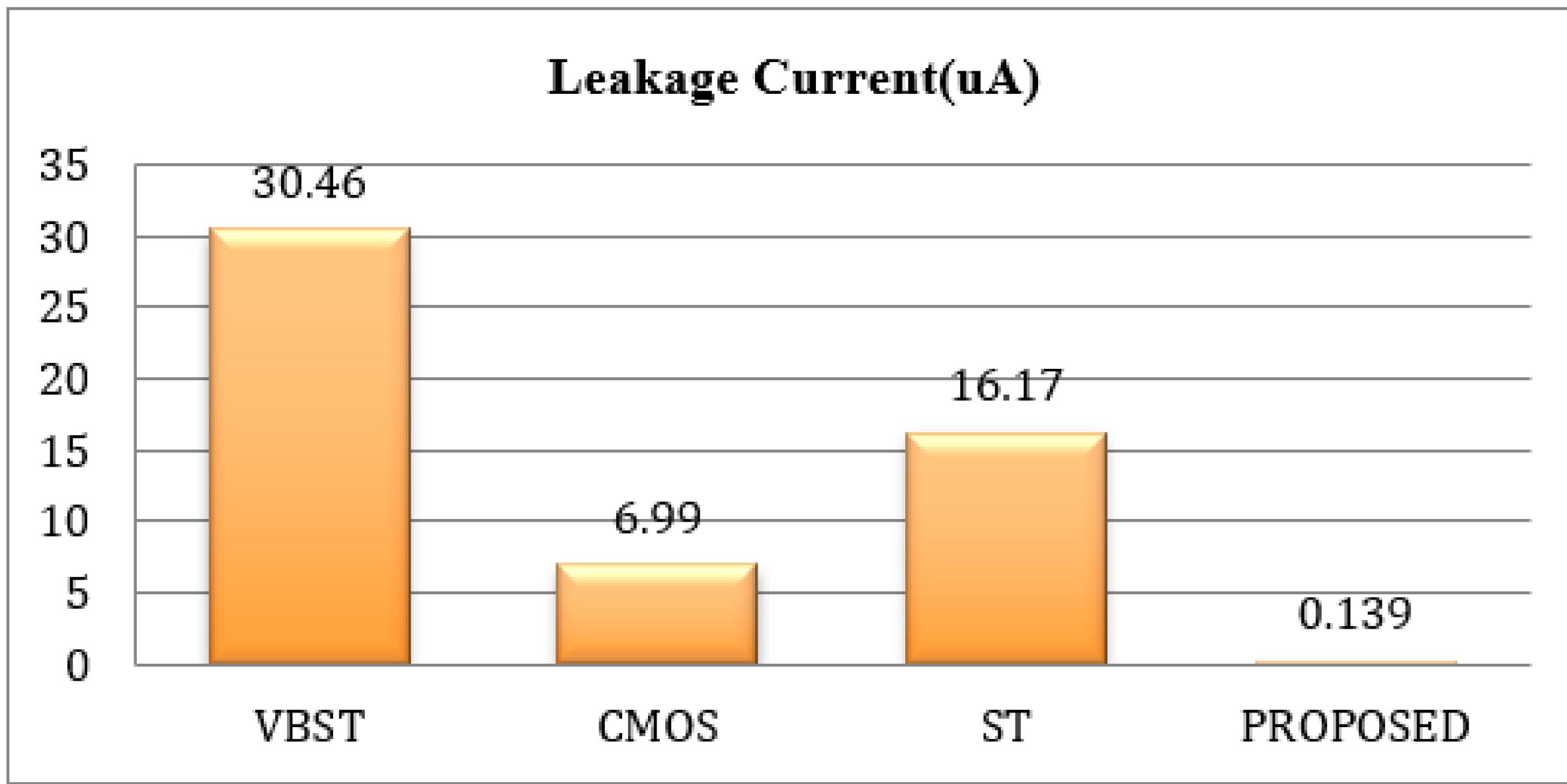


Voltage Bootstrapping Schmitt Trigger(VBST)



FinFET based Inverter

Leakage Current Comparison Graph



Conclusion:

	CMOS INVERTER	SCHMITT TRIGGER	VOLTAGE BOOTSTRAPPING SCHMITT TRIGGER	FinFET based Inverter
Time Delay(ps)	1.8	8.1	1.1	4
SNM(mV)	207.2135	317.3734	117.3734	398.3584
Critical Charge(fC)	1.6708	2.9276	2.9050	3.0101
Leakage Current(uA)	6.99	16.17	30.46	0.139

References:

1. Neha Gupta, A P Shah, R S Kumar, Gopal Raut, Soft error hardened voltage bootstrapped Schmitt trigger design for reliable circuits, microelectronics reliability
2. Sumio Tanaka, Theory of drain leakage current in silicon MOSFETs
3. Critical charge, Architecture Design for soft errors

THANK YOU