Reliability Analysis in Digital Circuits

(END TERM REPORT)

By
B. Rakesh(20BEC026)
B. Sharath Naik(20BEC028)
R. Narahari(20BEC088)
V S S Sainath Sanapala(20BME061)

Supervised by:
Dr. Pushpa Raikwal
ECE Department

Electronics and Communication Engineering
PDPM INDIAN INSTITUTE OF INFORMATION TECHNOLOGY
DESIGN AND MANUFACTURING JABALPUR

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Introduction:

In the majority of semiconductor industries, ensuring lifetime reliability poses a significant challenge, particularly given the aggressive downscaling of CMOS technology. Throughout the lifespan of a system, the transistor I-V characteristics may undergo alterations due to phenomena like Bias Temperature Instability (BTI), Hot carrier effects, Soft error, Single Event Effect(SEE). At elevated temperatures (125°C), NBTI emerges as the predominant aging phenomenon over PBTI in PMOS transistors. Consequently, BTI reduces the carrier mobility and transconductance, leading to an elevation in the threshold voltage. This increase in threshold voltage minimizes the leakage current and increases the circuit delay.

With the technology scaling down, the CMOS devices also become sensitive to radiation-induced Single Event Effects which degrade the noise immunity of the circuit.Reliability is the major concern in technology scaling down.In the digital devices, SEU flip the logic states, which causes the failure of systems.Single Event Transient(SET) effects are caused by alpha particles and cosmic neutrons generated, especially in terrestrial and space environment.The particle strikes causes a logical error, such errors are called as Soft errors. Critical charge(Qcrt) measures the Soft Error Rate at the most sensitive node and it should be as small as possible for a fault tolerant circuit. Critical charge is the amount of charge accumulated at sensitive node at the time of particle strike, which is sufficient to flip the output state of the circuit. So, critical charge should as high as possible to minimize the SER in the circuit. In this we going to study about the journey from a planar MOS to a three dimensional FINFET circuit which is more reliable than our traditional MOS based circuit.

Literature Review:

Inverter is the basic building block for most digital circuits. Hence the inverter itself should be tolerant to the effects of BTI and SEE. To understand the effects of above mentioned phenomena, Cadence is used. Using different types of inverter models, we examined the VTC curves, delay, critical charge and leakage analysis. The conventional CMOS inverter provides full swing from high to low according to the supply voltage. But it has reduced noise margin and due to presence of PMOS and NMOS in CMOS we can observe NBTI and PBTI respectively. For better stability, Schmitt Trigger(ST) circuit is proposed. It contains two feedback loops in the pull up and pull down network. ST has better noise margin and hysteresis loops are the fast transition. But due to the presence of PMOS and NMOS in the circuit(6 MOS transistors), NBTI and PBTI effects respectively can be observed. However, the PBTI has not caught much attention, mainly due to their ignorable impact on the thin gate oxide. Thus NBTI may impact more on the circuit performance than the PBTI. To overcome the issue of NBTI, a new Voltage Bootstrapping(VB) is proposed which is designed using only NMOS transistors. This removes the problem of aging

specially NBTI but also reduced the Noise margin and rail-to-rail voltage. PBTI is present in VB due to NMOS transistors but PBTI has less impact when compared to NBTI in PMOS devices. Hence we consider BTI(NBTI+PBTI) for reliability analysis. The VB circuit is less aging insensitive because of using NMOS transistor but has many complications like less noise margin, distorted voltage transfer characteristic curve (VTC).So a Voltage Bootstrapping Schmitt Trigger(VBST) is proposed which is combination of both VB and ST. Schmitt trigger circuit resolves the distorted VTC curve and improves the noise margin. But the ST circuit faces the NBTI aging problem due to the three PMOS transistors in the pull-up network.VBST is designed using only NMOS with bootstrapping in pull up network and a feedback loop in the pull down network.

Leakage current:

Leakage current is one of the major issues in a circuit. The leakage current has three major components namely Sub threshold leakage current(Isub), Junction Leakage current(Ijn), and gate leakage current(Ig). From the circuits we can segregate in which transistor the leakage current is present. We can observe errors in a circuit at elevated temperatures. So the circuit should be radiation tolerant.For this analysis, the critical charge should be high with less soft error rate and excellent sensitivity

Critical charge:

Critical charge is the minimum charge that must be deposited by a particle strike to cause a circuit to malfunction.Here, the charge accumulated at the node which is sufficient to shift the logic state of the circuit is called Critical charge. Critical charge can be calculated as:

$$I_{inj}\left(t\right) = \frac{Q_{inj}}{\tau_f - \tau_r} \times \left(e^{-t/\tau_f} - e^{-t/\tau_r}\right)$$

$$I_{inj}(t) = I_{peak} \times \left(e^{-t/\tau_f} - e^{-t/\tau_r}\right)$$

Here, Tf = Fall time, Tr = Rise time, Ipeak = Peak current

Soft error rate determines the probability of flipping the input and output voltage due to particle strike and is a function of critical charge. We can extend this to study the Soft error rate ratio which is defined as the ratio of soft error rate after some years to soft error rate for fresh time.

Vth is the major variable to investigate the effects of various parameters on transistors due to aging. The threshold voltage depends on temperature and see the effects on different stress time conditions. Thus Vth sensitivity is defined as the change in threshold voltage(Vth) to temperature and change in threshold voltage to stress time.

Time Delay:

Circuit delay or Time delay is defined as the time taken to a signal to propagate through the input to output. Mathematically we can say the time difference between 50% of output to 50% of input.

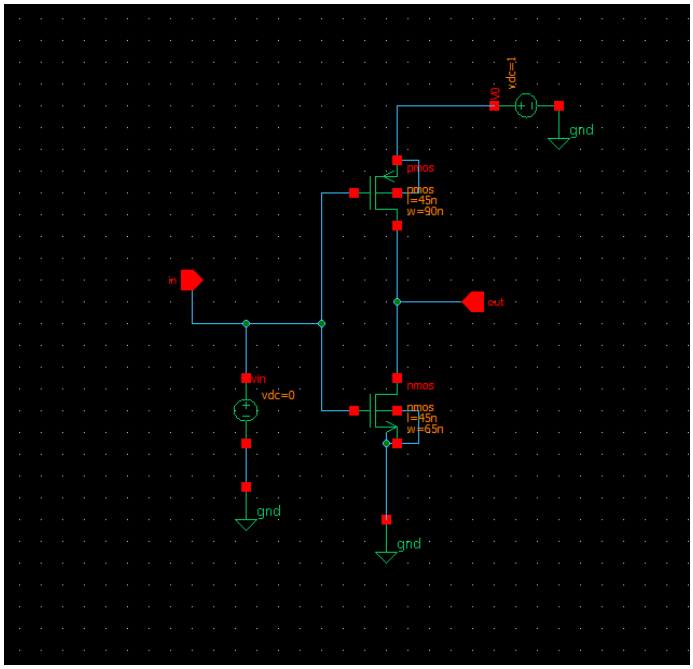
The static noise margin is defined as the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell. For a reliable circuit SNM ratio should be more.

By comparing all these above parameters like critical charge, leakage current, time delay and SNM ratio among the circuits(CMOS inverter, ST, VB, VBST), it was concluded that VBST is a better alternative for conventional CMOS inverter since it is more reliable.
CMOS inverter is designed with one PMOS and one NMOS.

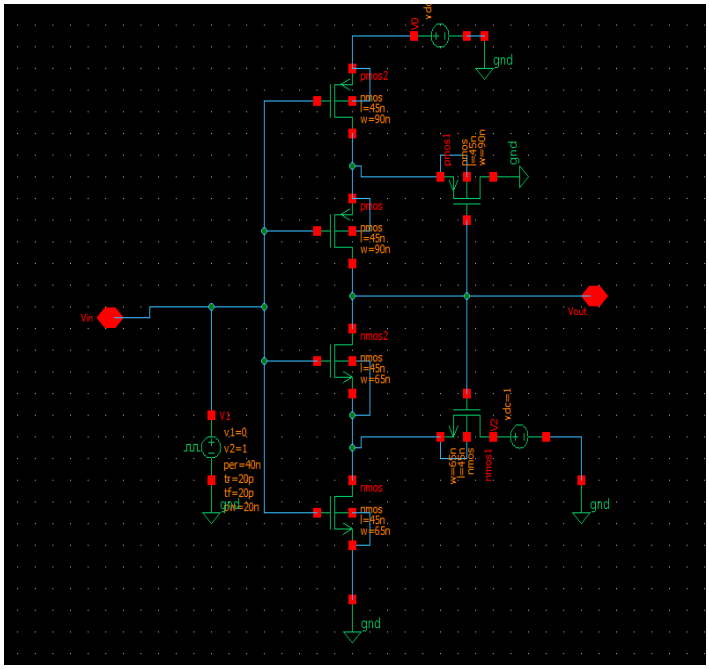
FinFET:

A FinFET is a type of field-effect transistor (FET) that has a thin vertical fin instead of being completely planar. The gate is fully "wrapped" around the channel on three sides formed between the source and the drain. The greater surface area created between the gate and channel provides better control of the electric state and reduces leakage compared to planar FETs. Using FinFETs, results in much better electrostatic control of the channel and thus better electrical characteristics than planar FETs. FINFET works as MOSFET in a much more efficient way.

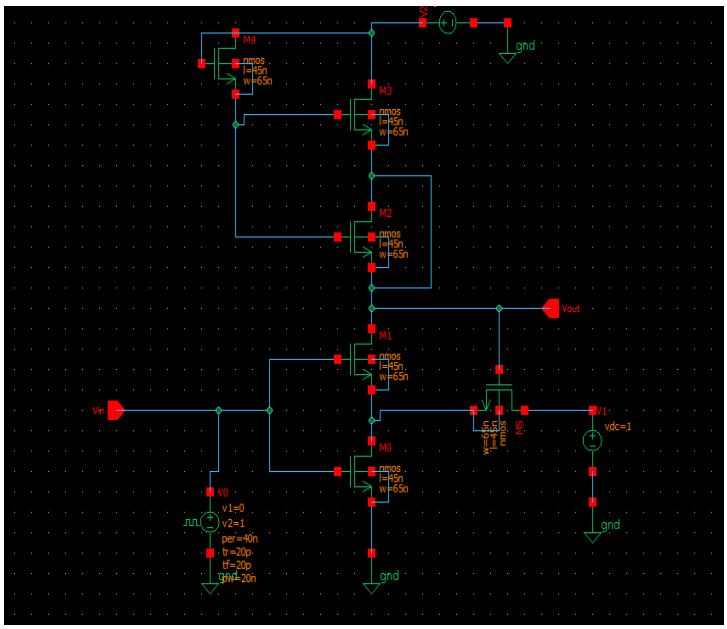
In [2], it was concluded that VBST is the best circuit which is reliable and more efficient than the other inverter circuits that are compared. Upon further study we would like to propose an inverter circuit designed with FinFET which is better than the proposed VBST in [2]. In VBST, 6 NMOS are used which need more area compared to FinFET based inverter. Also reliability parameters like critical charge, time delay, SNM ratio are better for FinFET when compared to VBST. In the following sections we discuss about the designing of the circuits, simulation results and discussion followed by conclusion.



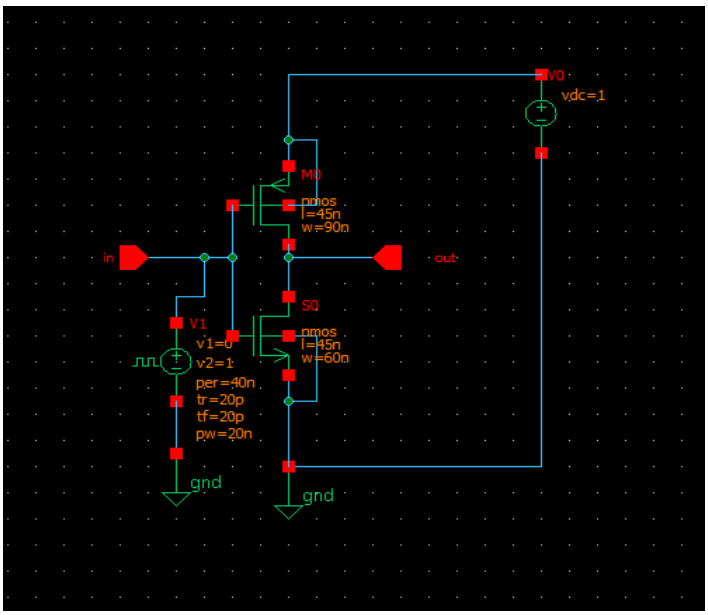
CMOS Inverter



Schmitt Trigger



VBST



FinFET based Inverter

Methodology:

For analysis of digital circuits, we used the Symicade platform in which we can design and simulate the circuits. CMOS inverter, Schmitt trigger, Voltage Bootstrapping Schmitt Trigger and FinFET are designed and the parameters are calculated. For every technology there are different model libraries which contain the device parameters. All our circuit components are based on 45nm technology. In the cellview we designed the schematic of the circuit. We have to set the input and output terminals and set them up for simulation. Select the appropriate model library, select the mode of analysis like DC analysis or Transient analysis etc., select the parameters which are required to be plotted. Click on netlist and run, we get the graphs with the parameters we selected for plotting. In the software, we can change the temperature where the output will be based on the behavior of the circuit at the given temperature. Voltage Transfer Characteristics(VTC), Transient analysis, leakage current are plotted on the graph.

Using the tool we can calculate the Time delay, average power. For calculating critical charge we use the double exponential current source which will act as a particle strike at a given period of time. Using the graph tools and the critical charge formula we can find the critical charge of the circuit. By exporting the values of the graph to a csv file and using originpro software we can plot Static Noise Margin(SNM). The schematic circuits that we designed can be converted into symbols which can be used in other cellviews. The software is user friendly. It is more flexible and compatible such that we are free to give all the parameters like time constants, delay, length, width etc., We can generate our own model library.

Progress Update:

FinFET based inverter is designed using Symicade software. The parameters Time delay, Static Noise Margin, Leakage current, Critical charge are calculated with the help of the tools of Symicade and originpro. Compared the results of FinFET based inverter with the results of CMOS inverter, Schmitt trigger and Voltage Bootstrapping Schmitt trigger(VBST) and concluded an efficient and reliable inverter circuit among them.

Results and Discussions:

DC analysis of all the four inverters can be seen in Fig1. From Fig1 we can observe how fast is the transition from low state to high state in Schmitt Trigger(ST). Also we can observe distorted curve of VB(Voltage Bootstrapping)

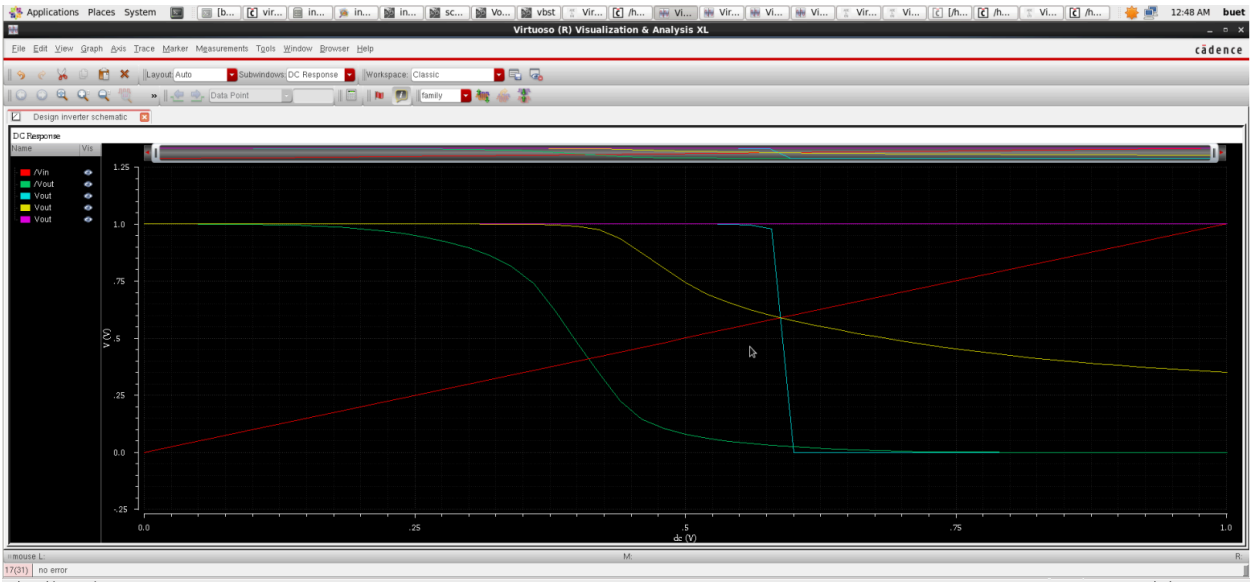


Fig1: Voltage Transfer Characteristics(VTC) of the inverters

From the Fig2a, 2b,2c, 2d Static Noise Margin of the circuits CMOS,ST,VBST and FinFET based inverter can be observed. In Fig3 we can observe the SNM values of all the circuits. SNM value of FinFET based inverter is 398.35mV, CMOS inverter is 207.21mV, of ST is 317.37mV and of VBST is 117.37mV. From this it is clear that FinFET based inverter has more SNM.

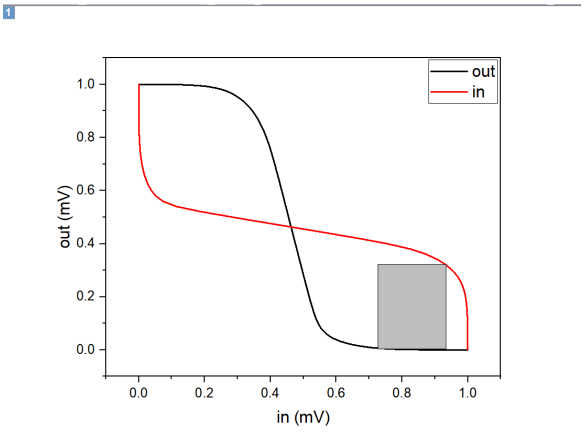


Fig2a: SNM of CMOS

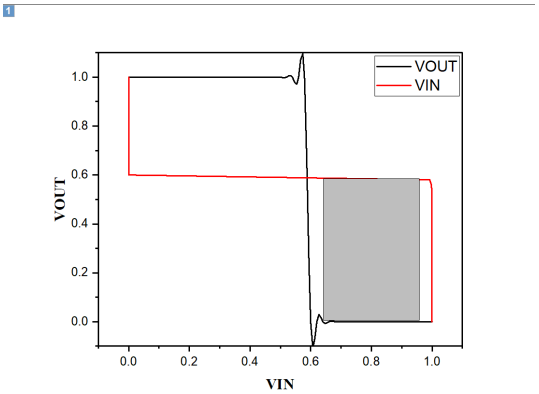


Fig2b: SNM of ST

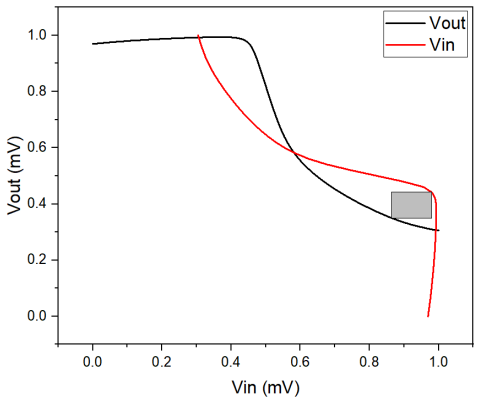


Fig2c: SNM of VBST

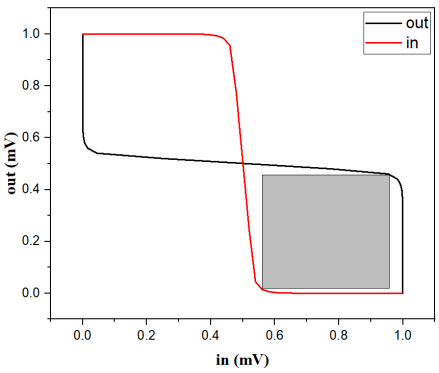


Fig2d: SNM of FinFET based Inverter

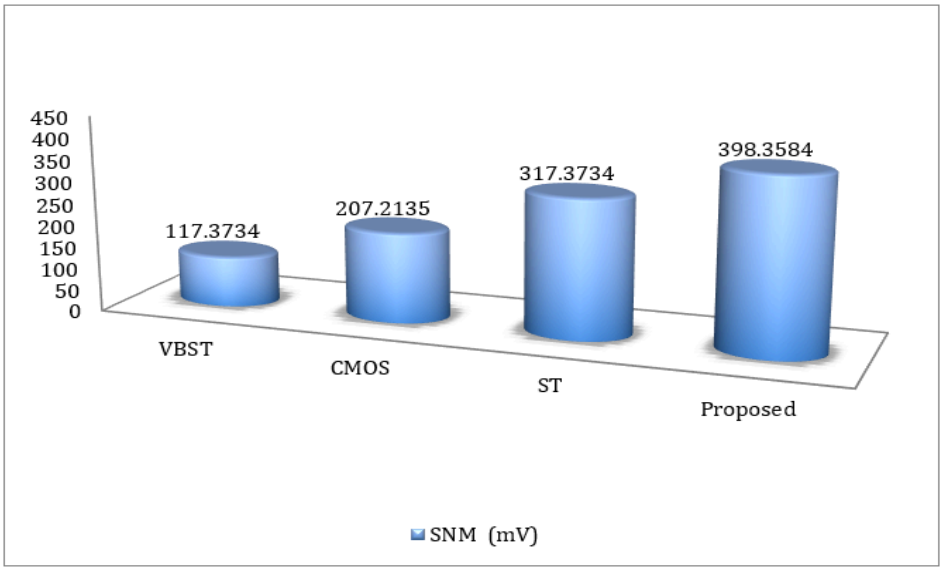


Fig3: SNM comparison graph of circuits

From Fig4 Time delay of the circuits can be analyzed. Time Delay of our FinFET based inverter(4ps) is less than that of ST(8.1ps) but is more than VBST(3.9ps) and CMOS(1.8ps).

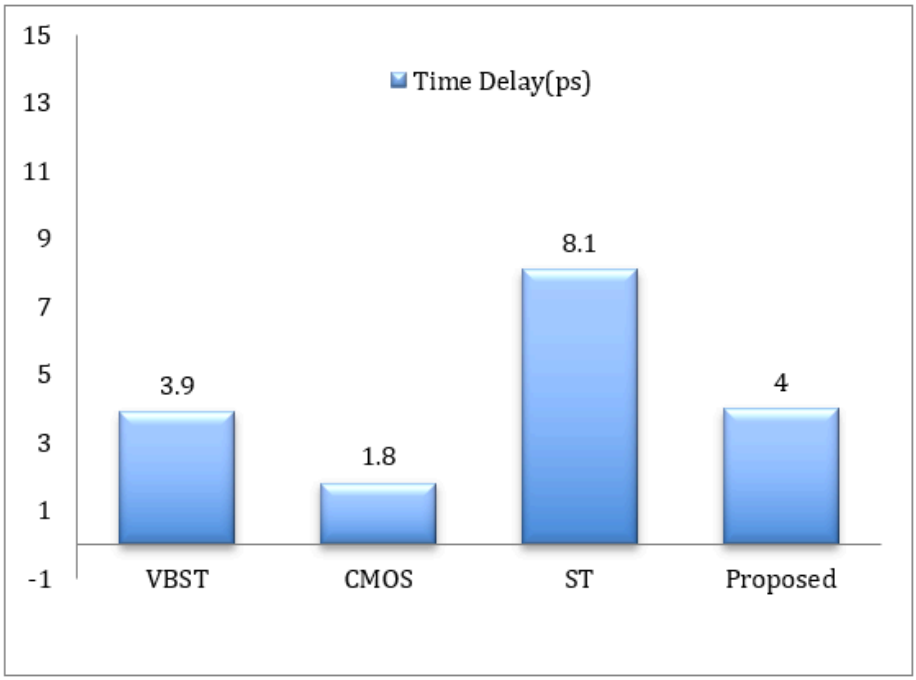


Fig4: Time Delay of digital circuits

Figures 5a,5b,5c,5d are the plots of Leakage currents of the CMOS, ST, VBST and FinFET based inverter circuits respectively. Since Leakage current is off state current, it should be as little as possible or we can say the circuit with less leakage current is more reliable. We can see the values of leakage current of all our circuits from Fig6

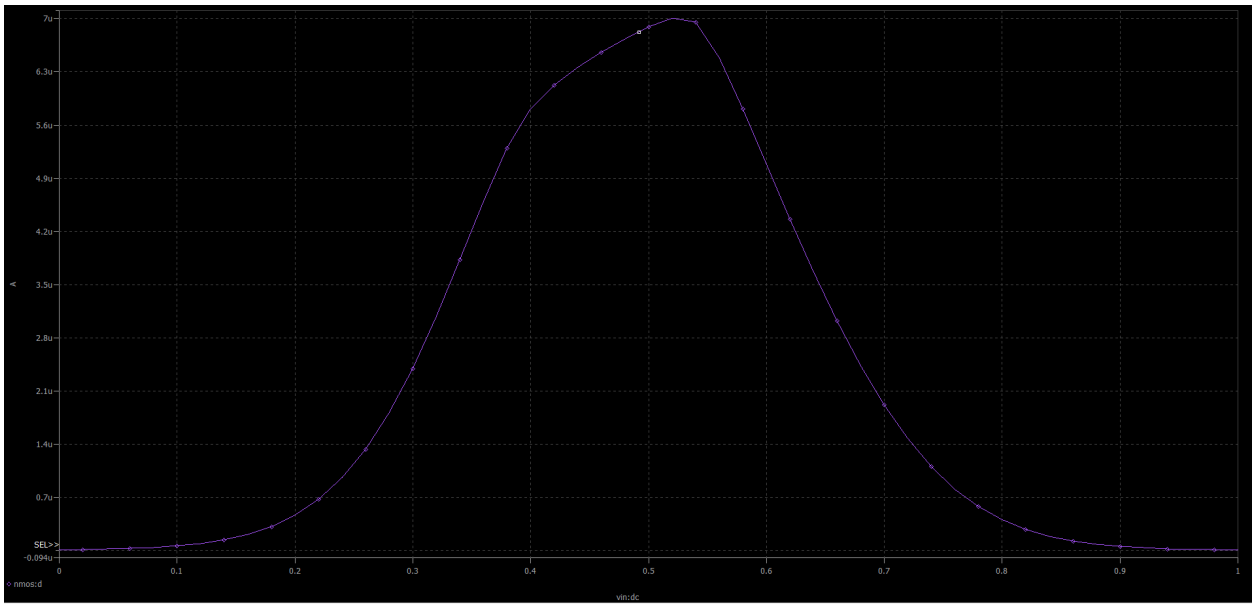


Fig5a:CMOS leakage current

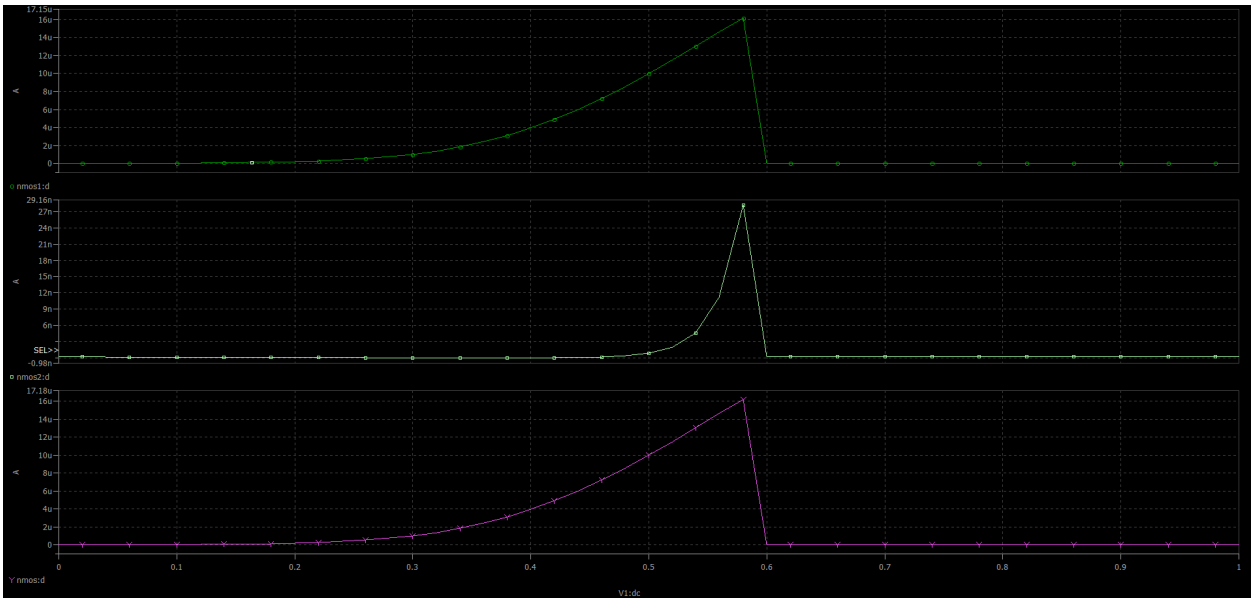


Fig5b:Schmitt Trigger Leakage Current

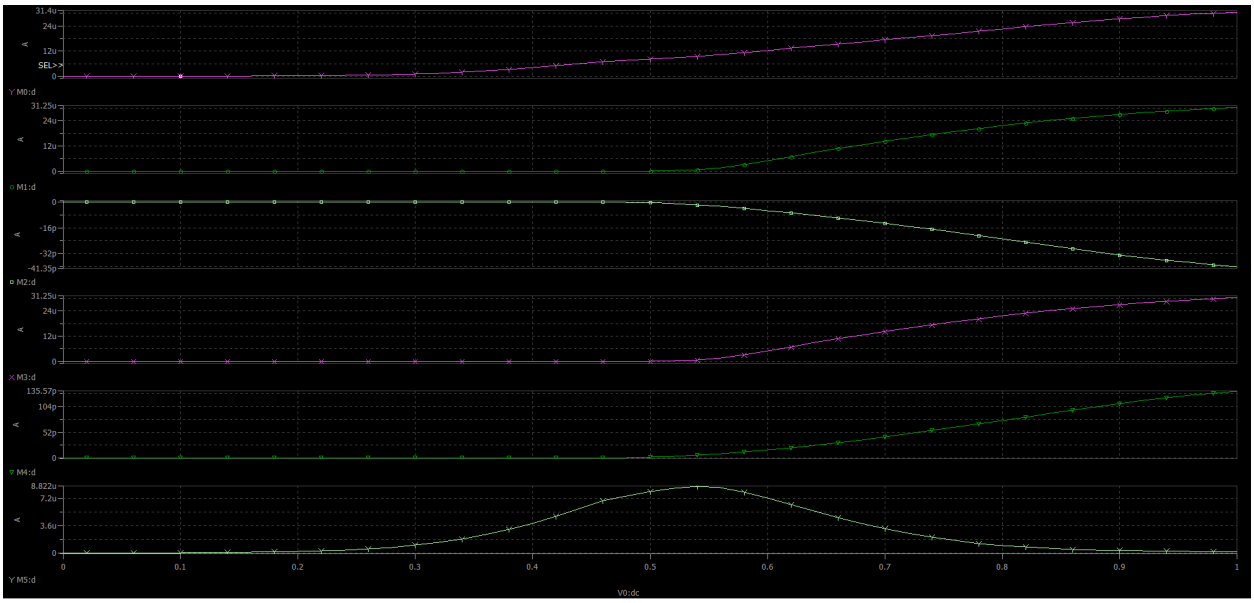


Fig5c:Voltage Bootstrapping Schmitt Trigger(VBST) Leakage Current

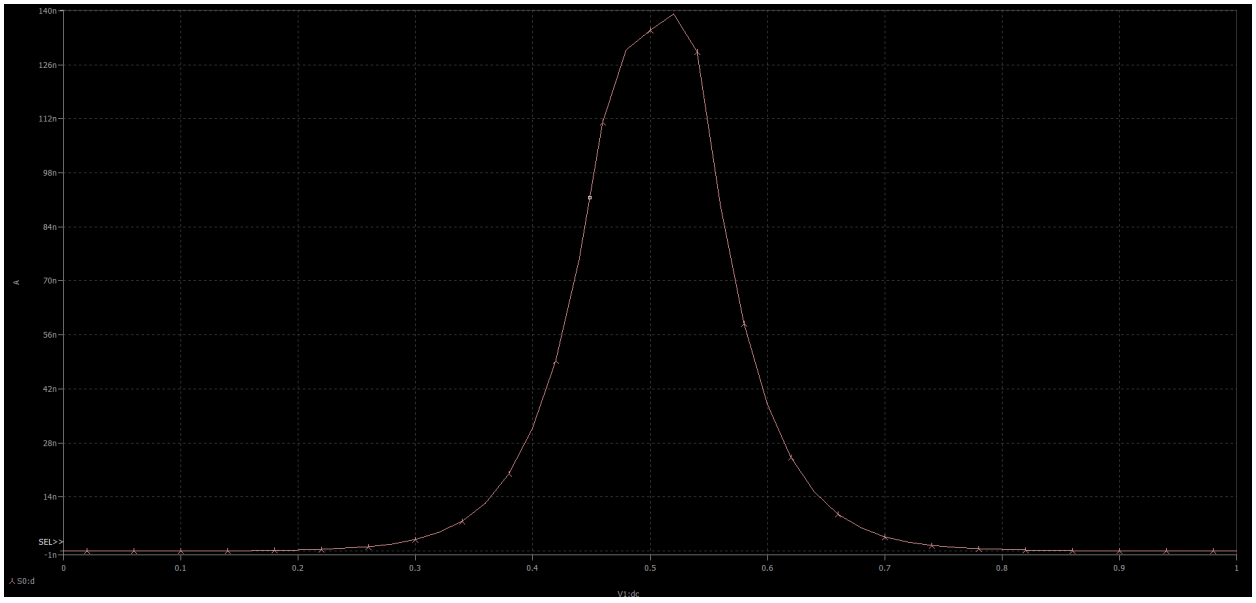


Fig5d:FinFET based Inverter Leakage Current

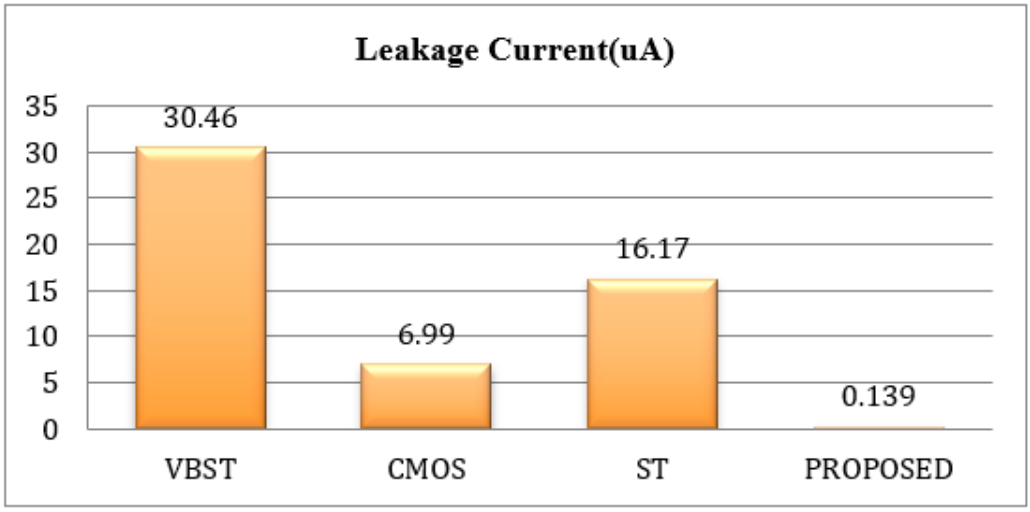


Fig6: Leakage current comparison

Fig7 indicates the critical charge of all the circuits. Critical charge of the proposed FinFET based inverter(3.0101 fC) is more than VBST, CMOS and ST. For a reliable circuit critical charge should be more so that the probability of flipping of bit will be less.

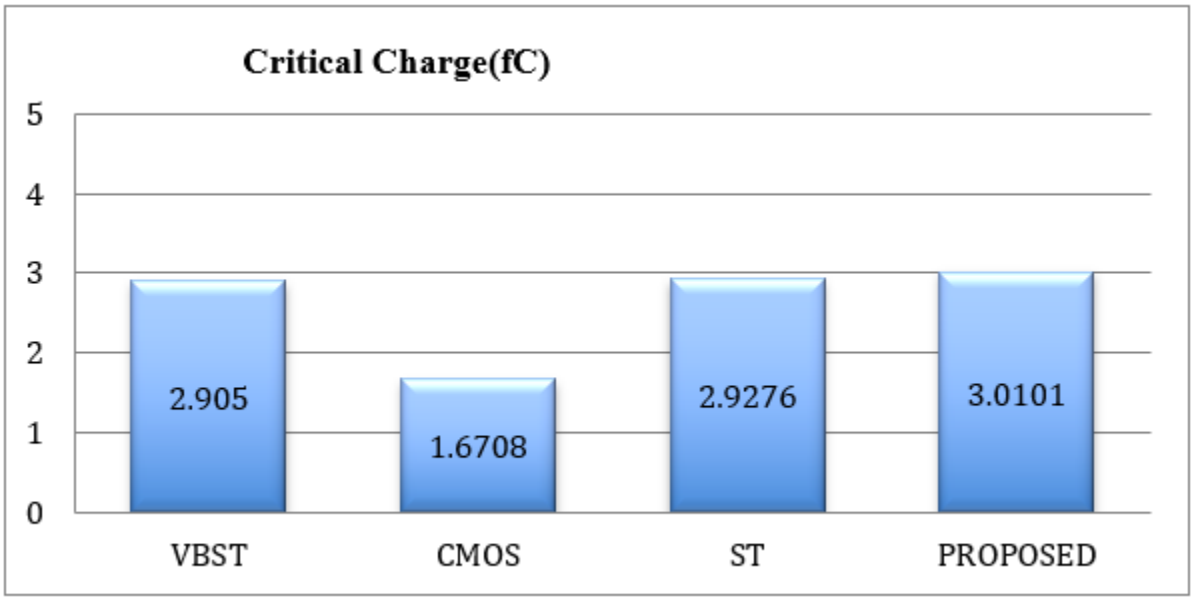


Fig7: Critical charge

Table1 contains all the parameter values of each circuit we studied. From Table1 we can compare all the parameters among the circuits and can conclude which circuit is more efficient and reliable.

	CMOS INVERTER	SCHMITT TRIGGER	VOLTAGE BOOTSTRAPPING SCHMITT TRIGGER	FinFET based Inverter
Time Delay(ps)	1.8	8.1	1.1	4
SNM(mV)	207.2135	317.3734	117.3734	398.3584
Critical Charge(fC)	1.6708	2.9276	2.9050	3.0101
Leakage Current(uA)	6.99	16.17	30.46	0.139

Table1: Reliable parameter values of the circuits

Conclusion:

In [1], it was concluded that the VBST circuit is more reliable than CMOS and Schmitt Trigger. We designed a FinFET based inverter and compared it with the circuits VBST, CMOS and Schmitt Trigger. From Fig1 VTC of the circuits can be compared. The Static Noise Margin can be compared and understood from Fig3. From Fig3 it is clear that the SNM of the proposed FinFET based inverter circuit is more than the others. For a circuit to be considered as reliable than others it should have more SNM. For a reliable circuit, Time delay should be minimum. Time delays of the circuits can be compared from Fig4. We can observe that the time delay of a FinFET circuit is less than ST but is more than VBST and CMOS. The off state current also called Leakage current should be less for a circuit to be reliable. From Fig6 it is clear that FinFET based inverter has less leakage current than the rest of the circuits. Critical charge has direct effect on the malfunctioning of a circuit. Critical charge should be more for a reliable circuit. The values of critical charges of the circuits can be observed from Fig7. Our proposed FinFET based inverter circuit has more critical charge among the circuits.

Table1 comprises the values of all the parameters of all the circuits. From Table1 we can conclude that a FinFET based inverter circuit is more reliable than all other circuits. Many of the reliable parameters are better for a FinFET based inverter than VBST and

other circuits. So from [1] and above study we can finally conclude that FinFET based Inverter is more efficient and reliable than VBST.

References:

[1]. Neha Gupta, A P Shah, R S Kumar, Gopal Raut, Soft error hardened voltage bootstrapped Schmmit trigger design for reliable circuits, microelectronics reliability

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[3]. Usman Khalid,A Mastrandrea,Effect of NBTI/PBTI aging and process variations on write failures in MOSFET and FinFET flip-flops

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