

# Sharath Hebbur Shivakumar

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## Education

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**Master's in Electrical and Computer Engineering at Purdue University, USA** Aug 2022 - May 2024  
**Courses:** VLSI Design, SoC Design, GPU Arch, Advanced Computer Architecture, Parallel Systems **GPA:** 3.7/4.0

**Bachelor's Degree at PES University, India** Aug 2016 - Sept 2020  
Electrical and Electronics Engineering, Graduated with Medal, Honors and Rank **GPA:** 9.07/10.0

## Skills

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- **Programming languages:** C, C++, Python, System Verilog, Regex, Makefiles, ARM, RISC-V, MIPS assembly
- **Tools:** Gem5, Cadence Virtuoso, Eagle CAD, VS code, Vim, Git, Perforce, GDB
- **Parallel Comp Arch:** MOESI, MSIF, Update based protocols (Firefly, Dragon), Memory Consistency Models
- **SoC Arch:** Distributed Shared Memory, Interconnect Networks & Topologies, CUMA, NUMA, COMA Arch
- **Parallel Programming:** CUDA, MPI, Pthreads

## Work Experience

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**AMD (Intern)** Boxborough, MA May 2023 - Aug 2023

- Designed singlecycle RISC processor with xDRAM integration in SystemVerilog for streamlined testing of emulators.
- Created a Python-based Build Differentiator to efficiently compare emulation builds and diagnose failures.
- Tool performs a precise comparison of **70k** build files, identifying version and configuration discrepancies.

**Purdue University (Graduate Teaching Assistant)** West Lafayette, IN Aug 2022 - May 2024

- Taught Code Quality, Test-Driven Development, GDB, Valgrind, Vim for **Advanced C Programming** class.
- Instructed students on designing multicore, L1 split cache coherent CPU in RTL for **Computer Architecture** class.

**Volvo Trucks (Embedded Application Engineer)** Bangalore, India Sept 2020 - Jul 2022

- Worked on verifying and developing software components in C++ using AUTOSAR architecture.
- Developed a testing application using python scripting and Digital IO box hardware prototype to test IC.

## Projects

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**AlexNET - Convolutional Neural Network implementation** Jan 2024 - Present

- Acceleration of convolution, gemm and max pool operations with optimization for run time in CUDA.

**Load Value Predictor Performance Modelling (Alpha 21264)** [git] Aug 2023 - Dec 2023

- Improving data access time by exploiting data value locality in cycle-accurate microarchitectural **Gem5 simulation**.
- Implemented Load Value Prediction Table, Load Classification Table, Constant Verification Unit in C++.
- Achieved **25%** speedup in **bzip** and **15%** speedup in **gcc** benchmarks for OoO CPU compared to baseline O3 model.

**Vortex GPU Coupled Scalar Core Design** [git] [git] Aug 2023 - Dec 2023

- Integrating latency-sensitive RiscV scalar core into the Vortex GPU core, with shared L1 cache in System Verilog.
- Implemented high priority kernel scheduler for assigning priority tasks to custom scalar processor for better performance.
- Tightly coupled Vortex GPGPU core with scalar core for achieving speedup of **1.3x** on control flow divergence tasks.

**Multi Core Processor design** [git] Jan 2023 - May 2023

- Constructed multicore, split cache, pipelined MIPS processor with cache coherence in System Verilog.
- Incorporated MSI protocol, Branch Predictor with BTB and achieved speed of around **60 MHz** after Synthesis.
- Designed cache coherency, bus controller & Read-Modify-Write functionality for multithreading.

**Hardware Acceleration of Neural Network Inference** [git] Aug 2022 - Dec 2022

- Classified image numerical data from MNIST dataset using KANN API, a lightweight neural network library.
- Enhanced sw performance through optimized vector dot product implementation and custom instructions in hardware.
- Interfaced DMA/burst transfers with pipelined computation, resulting in **6.4x(CNN)** and **16.86x(MLP)** speedup.