Sharath Hebbur Shivakumar

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Education

Master's in Electrical and Computer Engineering at Purdue University, USA — Aug 2022 - present
Courses: MOS VLSI Design, SoC Design, GPU, Computer Architecture and Design ASIC Design, Digital Design — GPA: 3.77/4.0

Bachelor's Degree at PES University, India — Aug 2016 - Sept 2020
Electrical and Electronics Engineering, Graduated with Medal, Honors and Rank — GPA: 9.07/10.0

Skills

- **Programming languages:** C, C++, Python and Bash scripting, Regex, Makefiles, SystemVerilog, MIPS assembly
- **Software:** Gem5, Cadence Virtuoso, Eagle CAD, MATLAB, Labview, VS code, Vim, Git, Perforce, GDB
- **FPGA tools**: Altera Cyclone (Intel Quartus prime sw), Xilinx KRIA (Vivado sw), experience in Emulation Build flow

Work Experience

AMD (Virtual Bring Up Intern) Boxborough, MA — May 2023 - Aug 2023
- Created a Python-based Build Differentiator to efficiently compare emulation builds and diagnose failures.
- Tool performs a precise comparison of **70k** build files, identifying version and configuration discrepancies.
- Designed singlecycle RISC processor with xDRAM integration in SystemVerilog for streamlined testing of emulators.
- Contributed to debugging integration for X2 emulator, build optimization, jenkins configuration for regression build.

Purdue University (Teaching Assistant) West Lafayette, IN — Aug 2022 - Dec 2023
- Taught Code Quality, Test-Driven Development, GDB , Valgrind, Vim for **Advanced C Programming** class.
- Helped students develop embedded applications on esp32 using micropython in **Software for Embedded Systems**.
- Instructed students on designing multicore L2 split cache coherent CPU in **Computer Design** lab.

Volvo Trucks (Embedded Application Engineer) Banglore, India — Sept 2020 - Jul 2022
- Worked on verifying and developing software components using AUTOSAR architecture.
- Developed a testing application using python scripting and Digital IO box hardware prototype to test IC.

Projects

GPU Coupled Scalar Core Design
- Integrating latency-sensitive scalar core into the GPU core, with shared data scratch pad.
- Implementing thread arbitration for higher-priority warps, to scalar core's instruction scratch pad.
- Coupling Vortex GPU core with a RISC-V pipelined core for parallel processing capabilities.

Multi Core Processor design
- Constructed multicore pipelined processor with cache coherence, adhering to MIPS architecture standards.
- Incorporated MSI protocol, Branch Predictor with BTB and achieved speed of around **60 MHz** after Synthesis.
- Designed split cache with cache coherence, bus control & Read-Modify-Write functionality for multithreading.

Modelling Piecewise-Linear Branch Predictor
- Improving prediction accuracy by learning the behavior of certain linearly Inseparable branches.
- Performance evaluation by simulating predictor with a CPU capable of dynamic execution in Gem5 simulator.

Hardware Acceleration of Neural Network Inference [git link]
- Classified image numerical data from MNIST dataset using KANN API, a lightweight neural network library.
- Enhanced sw performance through optimized vector dot product implementation and custom instructions in hardware.
- Interfaced DMA/burst transfers with pipelined computation, resulting in a **6.4x(CNN)** and **16.86x(MLP)** speedup.

STRAM design
- Implemented 8T SRAM Array Design layout**(128 words of 16 Bit length)** for data access in Cadence Virtuoso.