Sharath Hebbur Shivakumar

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Education

Master's in Electrical and Computer Engineering at Purdue University, USA — Aug 2022 - May 2024
Courses: VLSI Design, SoC Design, GPU Arch, Advanced Computer Architecture, Parallel Systems — GPA: 3.7/4.0

Bachelor's Degree at PES University, India — Aug 2016 - Sept 2020
Electrical and Electronics Engineering, Graduated with Medal, Honors and Rank — GPA: 9.07/10.0

Skills

- **Programming languages**: C, C++, Python, System Verilog, Regex, Makefiles, ARM, RISC-V, MIPS assembly
- **Tools**: Gem5, Cadence Virtuoso, Eagle CAD, VS code, Vim, Git, Perforce, GDB
- **Parallel Comp Arch**: MOESI, MSIF, Update based protocols (Firefly, Dragon), Memory Consistency Models
- **SoC Arch**: Distributed Shared Memory, Interconnect Networks & Topologies, CUMA, NUMA, COMA Arch
- **Parallel Programming**: CUDA, MPI, Pthreads

Work Experience

AMD (Memory Subsystem Engineer) Santa Clara, CA — June 2024 - Present
- RTL performance analysis & microbenchmarking for Infinity Fabric composed of Interconnect NW, Memory Controller.
- Theoretical analysis of mem system optimizations, develop-maintain IP debug tools for performance bottleneck debug.
- Worked on AMD's cutting edge products like EPYC, MI400's memory subsystem IP's driving innovation.

AMD (Intern) Boxborough, MA — May 2023 - Aug 2023
- Designed singlecycle RISC processor with xDRAM integration in SystemVerilog for streamlined testing of emulators.
- Created a Python-based Build Differentiator to efficiently compare emulation builds and diagnose failures.
- Tool performs a precise comparison of **70k** build files, identifying version and configuration discrepancies.

Purdue University (Graduate Teaching Assistant) West Lafayette, IN — Aug 2022 - May 2024
- Taught Code Quality, Test-Driven Development, GDB , Valgrind, Vim for **Advanced C Programming** class.
- Instructed students on designing multicore, L1 split cache coherent CPU in RTL for **Computer Architecture** class.

Volvo Trucks (Embedded Application Engineer) Banglore, India — Sept 2020 - Jul 2022
- Worked on verifying and developing software components in C++ using AUTOSAR architecture.
- Developed a testing application using python scripting and Digital IO box hardware prototype to test IC.

Projects

Speculative Coherency Modelling in Distributed Shared Memory — Jan 2024 - Present
- Performance modelling of **Dynamic Self Invalidation** and **Last Touch Prediction** protocols in cache architecture.
- Implemented with DSM **MOESI directory protocol** for scalable nodes in Gem5 using ruby framework in C++.
- Benchmarked Splash3 applications and achieved an average **speedup of 28% in DSI and 32% in LTP**.

Load Value Predictor Performance Modelling (Alpha 21264) [git] — Aug 2023 - Dec 2023
- Improving data access time by exploiting data value locality in cycle-accurate microarchitectural **Gem5 simulation**.
- Implemented Load Value Prediction Table, Load Classification Table, Constant Verification Unit in C++.
- Achieved **25%** speedup in **bzip** and **15%** speedup in **gcc** benchmarks for OoO CPU compared to baseline O3 model.

Vortex GPU Coupled Scalar Core Design [git] [git] — Aug 2023 - Dec 2023
- Integrating latency-sensitive RiscV scalar core into the Vortex GPU core, with shared L1 cache in System Verilog.
- Implemented high priority kernel scheduler for assigning priority tasks to custom scalar processor for better performance.
- Tightly coupled Vortex GPGPU core with scalar core for achieving speedup of **1.3x** on control flow divergence tasks.

Hardware Acceleration of Neural Network Inference [git] — Aug 2022 - Dec 2022
- Classified image numerical data from MNIST dataset using KANN API, a lightweight neural network library.
- Enhanced sw performance through optimized vector dot product implementation and custom instructions in hardware.
- Interfaced DMA/burst transfers with pipelined computation, resulting in **6.4x(CNN)** and **16.86x(MLP)** speedup.