Sharath Hebbur Shivakumar

sharathat45 | Sharath Hebbur Shivakumar | shebburs@purdue.edu | +1 765-767-3705

Education

Master's in Electrical and Computer Engineering at Purdue University, USA — Aug 2022 - May 2024
Courses: VLSI Design, SoC Design, GPU Architecture, Advanced Computer Architecture and Design — GPA: 3.77/4.0

Bachelor's Degree at PES University, India — Aug 2016 - Sept 2020
Electrical and Electronics Engineering, Graduated with Medal, Honors and Rank — GPA: 9.07/10.0

Skills

- **Programming languages:** C, C++, Python, System Verilog, Regex, Makefiles, Bash scripting, MIPS asm
- **Tools:** Gem5, Cadence Virtuoso, Eagle CAD, MATLAB, VS code, Vim, Git, Perforce, GDB
- **Parallel programming**: MPI, Pthreads, CUDA

Work Experience

AMD (Intern) Boxborough, MA — May 2023 - Aug 2023
- Designed singlecycle RISC processor with xDRAM integration in SystemVerilog for streamlined testing of emulators.
- Created a Python-based Build Differentiator to efficiently compare emulation builds and diagnose failures.
- Tool performs a precise comparison of **70k** build files, identifying version and configuration discrepancies.

Purdue University (Graduate Teaching Assistant) West Lafayette, IN — Aug 2022 - May 2024
- Taught Code Quality, Test-Driven Development, GDB , Valgrind, Vim for **Advanced C Programming** class.
- Supported students develop embedded applications on esp32 using micropython in **Software for Embedded Systems**.
- Instructed students on designing multicore, L1 split cache coherent CPU in RTL for **Computer Architecture** class.

Volvo Trucks (Embedded Application Engineer) Banglore, India — Sept 2020 - Jul 2022
- Worked on verifying and developing software components using AUTOSAR architecture.
- Developed a testing application using python scripting and Digital IO box hardware prototype to test IC.

Projects

Load Value Predictor Performance Modelling (Alpha 21264) [git] — Aug 2023 - Dec 2023
- Improving data access time by exploiting data value locality in cycle-accurate microarchitectural **Gem5 simulation**.
- Implemented Load Value Prediction Table, Load Classification Table, Constant Verification Unit in C++.
- Achieved **25%** speedup in **bzip** and **15%** speedup in **gcc** benchmarks for OoO CPU compared to baseline O3 model.

GPU Coupled Scalar Core Design [git] [git] — Aug 2023 - Dec 2023
- Integrating latency-sensitive RiscV scalar core into the GPU core, with shared L1 cache in system verilog design.
- Implemented high priority kernel scheduler for assigning priority tasks to custom scalar processor for better performance.
- Tightly coupled Vortex GPGPU core with scalar core for achieving speedup of **1.3x** on control flow divergence tasks.

Multi Core Processor design [git] — Jan 2023 - May 2023
- Constructed multicore, split cache, pipelined MIPS processor with cache coherence in System Verilog.
- Incorporated MSI protocol, Branch Predictor with BTB and achieved speed of around **60 MHz** after Synthesis.
- Designed cache coherency, bus controller & Read-Modify-Write functionality for multithreading.
- Built from scratch, starting with ALU using interfaces, testbench, packages, and functional units.

Hardware Acceleration of Neural Network Inference [git] — Aug 2022 - Dec 2022
- Classified image numerical data from MNIST dataset using KANN API, a lightweight neural network library.
- Enhanced sw performance through optimized vector dot product implementation and custom instructions in hardware.
- Interfaced DMA/burst transfers with pipelined computation, resulting in **6.4x(CNN)** and **16.86x(MLP)** speedup.

STRAM design — Aug 2022 - Dec 2022
- Implemented 8T SRAM Array Design layout**(128 words of 16 Bit length)** for data access in Cadence Virtuoso.