DIGITAL LOGIC DESIGN

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EXPERIMENT 12

EXPERIMENT – 12

AIM: -

Design of modulo-4 counter using J K flip flop.

APPARATUS REQUIRED:-

Logic trainer kit, J-K Flip-flop IC - 7476 wires.

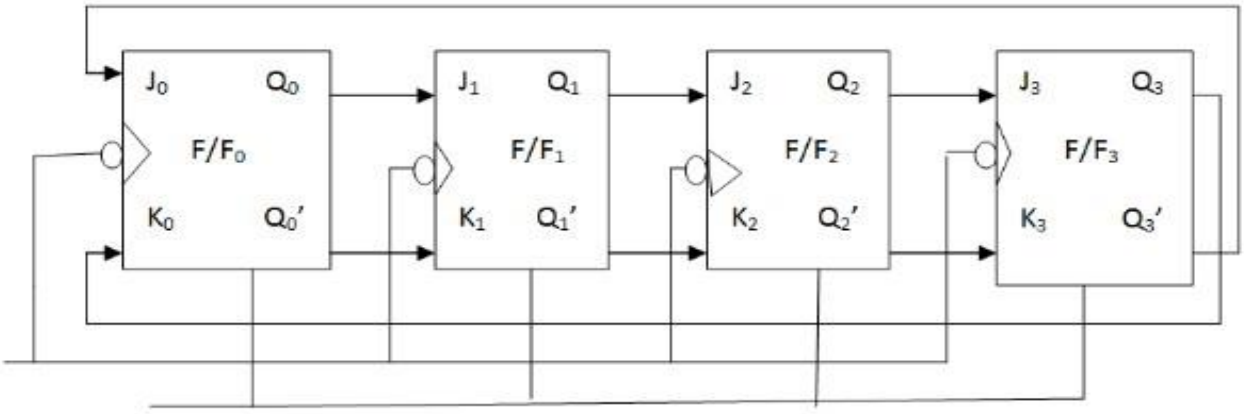
THEORY:

The Johnson counter is a modification of ring counter. In this the inverted output of the last stage flip flop is connected to the input of first flip flop. If we use n flip flops to design the Johnson counter, it is known as 2n bit Johnson counter or Mod 2n Johnson counter. This is an advantage of the Johnson counter that it requires only half number of flip flops that of a ring counter uses, to design the same Mod. The main difference between the 4 bit ring counter and the Johnson counter is that is in ring counter, we connect the output of last flip flop directly to the input of first flip flop. But in Johnson counter, we connect the inverted output of last stage to the first stage input. The Johnson counter is also known as Twisted Ring Counter, with a feedback. In Johnson counter the input of the first flip flop is connected from the inverted output of the last flip flop. The Johnson counter or switch trail ring counter is designed in such a way that it overcomes the limitations of ring counter. Mainly it reduces the number of flip flops required for designing the circuit.

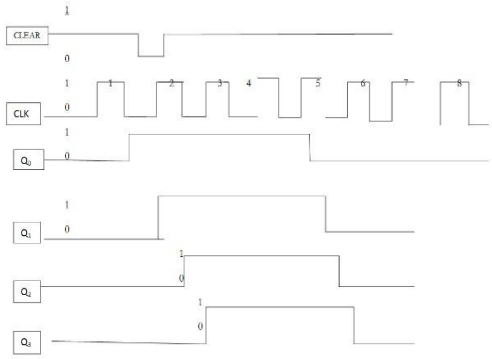
Operation

- Initially, a short negative going pulse is applied to the clear input of all flip-flops. This will reset all the flip-flops. Hence, initially the o/ps are $Q_3Q_2Q_1Q_0 = 0000$.
- But $Q'_3 = 1$ and since it is copied to J_0 it is also equal to 1.
- $J_0 = 1$ and $K = 1$.....initially.
- On the first negative edge of clock arrives at first f/f. o/p of $Q_0 = 1$.
- after 1st –ve edge clock the o/ps of f/fs will be, $Q_3Q_2Q_1Q_0 = 0001$
- On second –ve clock o/p of 2nd f/f will be 1 i.e $Q_1 = 1$.
- $Q_3Q_2Q_1Q_0 = 0011$
- Similarly for 3rd –ve edge clock, $Q_3Q_2Q_1Q_0 = 0111$
- For 4th –ve edge clock, $Q_3Q_2Q_1Q_0 = 1111$
- Now as soon as 5th –ve edge is arrived o/p of 1st f/f becomes 0 i.e $Q_0 = 1$ i.e $Q_3Q_2Q_1Q_0 = 1110$ - This operation continues till the o/p is reached to zero o/p state. i.e $Q_3Q_2Q_1Q_0 = 0000$

Logic diagram:-



Waveforms for Johnson's Counter



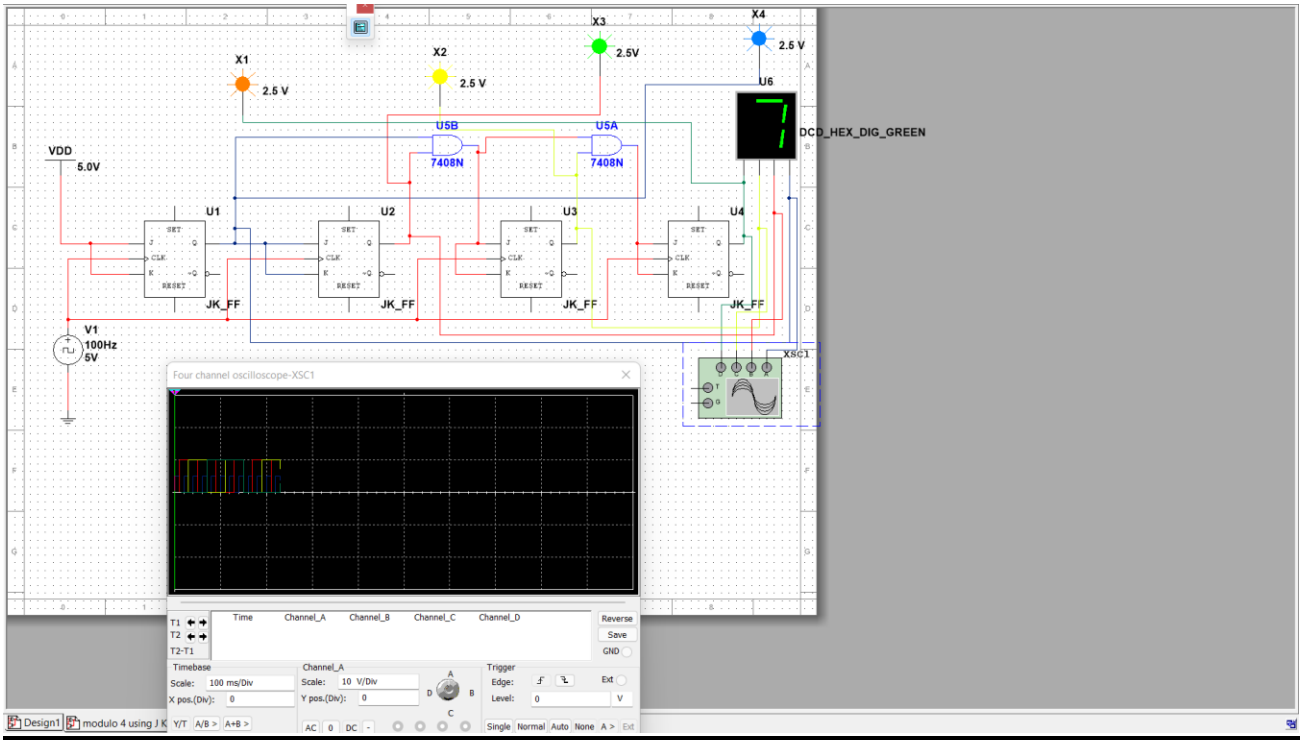
Truth Table for a 4-bit Johnson Ring Counter

Clock Pulse No	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

DESIGN:



RESULT:

Thus the Johnson counter was designed and their truth table is verified.

PRECATIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off. • Never touch live and naked wires.