DIGITAL LOGIC DESIGN

SHARDA KUMARI
BT20EC001
ELECTRONICS AND COMMUNICATION

EXPERIMENT 7

EXPERIMENT – 7

AIM: -

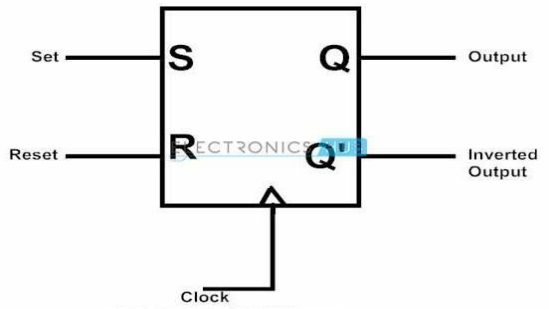
Design and test of an S-R flip-flop using NOR/NAND gates.

APPARATUS REQUIRED: -

Logic trainer kit, NAND gates ICs- 7400, NOR gates ICs-7402, wires.

THEORY:

The SR flip-flop is one of the fundamental parts of the sequential circuit logic. SR flip-flop is a memory device and a binary data of 1 – bit can be stored in it. SR flip-flop has two stable states in which it can store data in the form of either binary zero or binary one. Like all flip-flops, an SR flip-flop is also an edge sensitive device.
SR flip–flop is one of the most vital components in digital logic and it is also the most basic sequential circuit that is possible. The S and R in SR flip-flop means 'SET' and 'RESET' respectively. Hence it is also called Set–Reset flipflop. The symbolic representation of the SR Flip Flop is shown below.



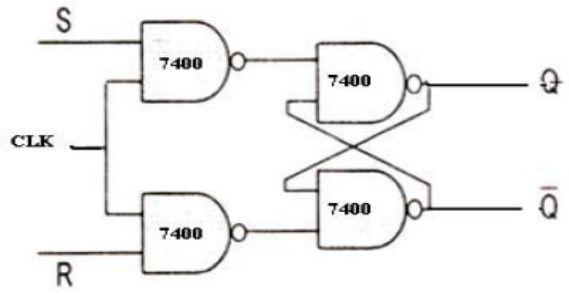
Working Principle:

SR flip-flop works during the transition of clock pulse either from low to high or from high to low (depending on the design) i.e. it can be either positive edge triggered or negative edge triggered.
For a positive edge triggered SR flip-flop, suppose, if S input is at high level (logic 1) and R input is at low level (logic 0) during a low to high transition on clock pulse, then the SR flip-flop is said to be in SET state and the output of the SR flip-flop is SET to
1. For the same clock situation, if the R input is at high level (logic 1) and S input is at low level (logic 0), then the SR flip-flop is said to be in RESET state and the output of the SR flip-flop is RESET to 0.
The SR flip-flops can be designed by using logic gates like NOR gates and NAND gates.

S-R Flip-Flop Using NAND Gate

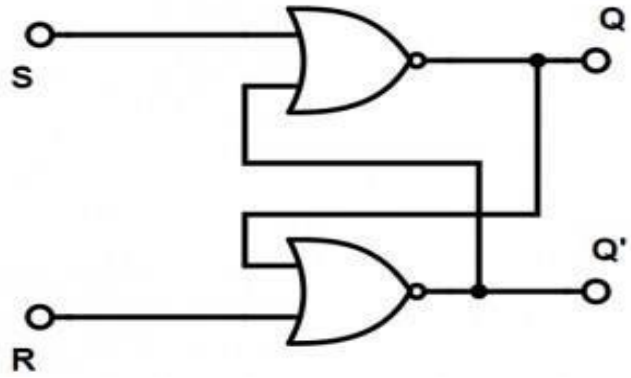
SR flip flop can be designed by cross coupling of two NAND gates. It is an active low input SR flip-flop. The circuit of SR flip-flop using NAND gates is shown in below figure:

R-S flip-flop using NAND gates



$\bar{S}$	$\bar{R}$	Q	State
1	1	Previous State	No change
1	0	0	Reset
0	1	1	Set
0	0	?	Forbidden

R – S flip-flop using NOR gates



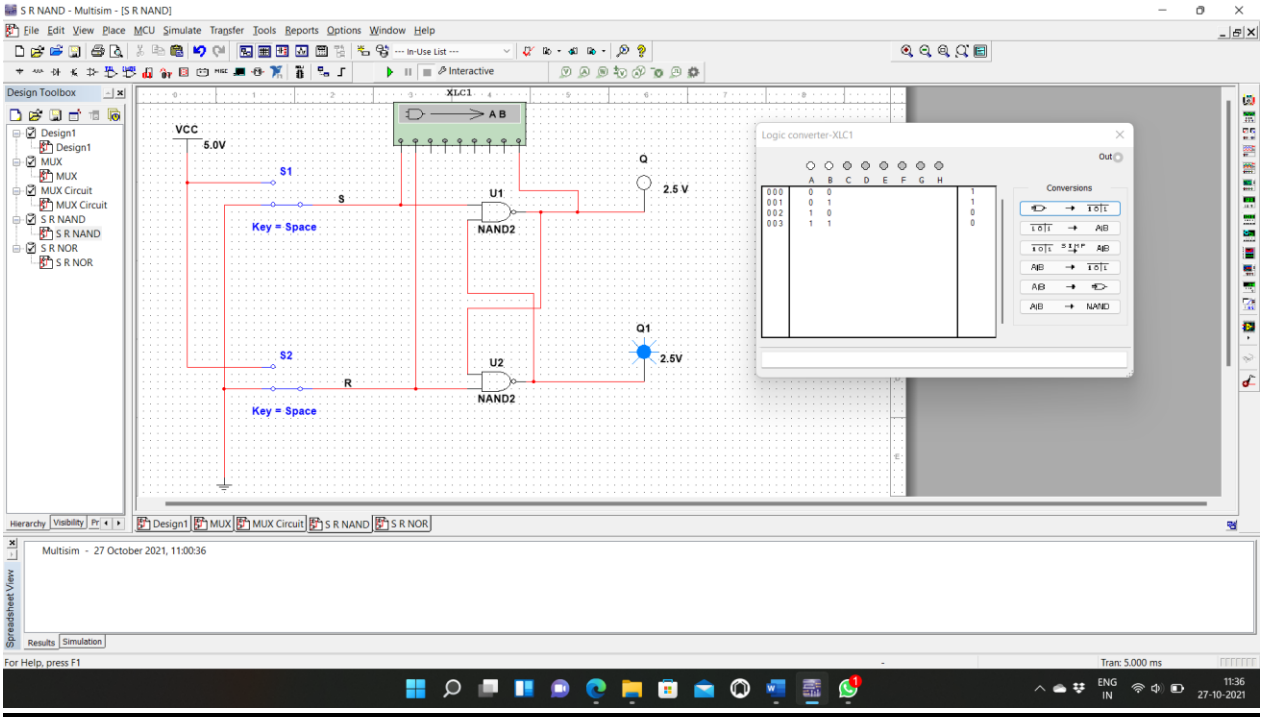
S	R	Q	State
0	0	Previous State	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Forbidden

PROCEDURE:

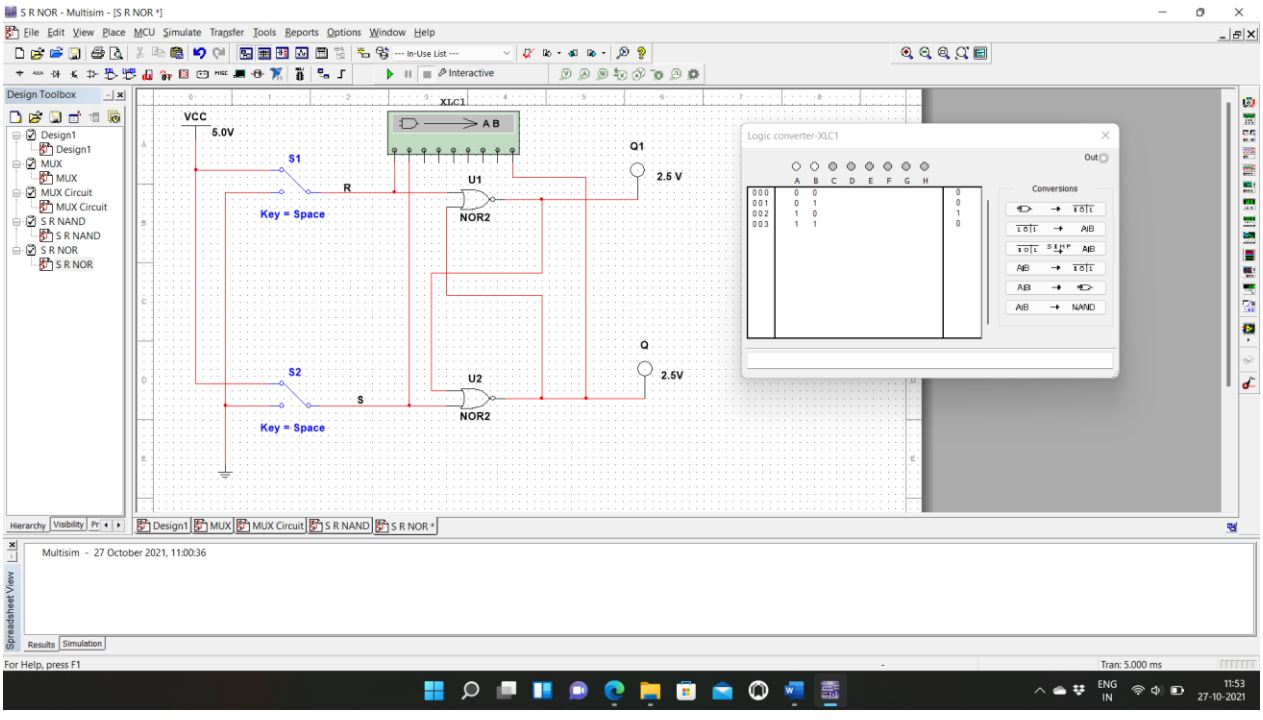
(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

TEST OF S R FLIP-FLOP :

USING NAND GATE:



USING NOR GATE:



RESULT:

Design of S-R Flip flop using NAND & NOR gates was verified successfully.

PRECAUTIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch live and naked wires.