DIGITAL LOGIC DESIGN

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EXPERIMENT 10

EXPERIMENT – 10

AIM: -

Operate the counters 7490, 7493.

APPARATUS REQUIRED:-

Logic trainer kit, Counter ICs- 7490, IC - 7493 wires.

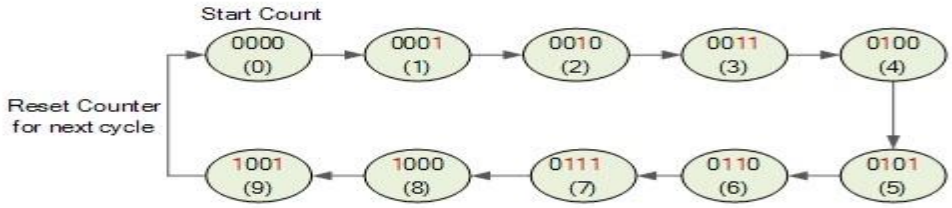
THEORY:

Asynchronous 74LS90 Decade Counter

Digital counters count upwards from zero to some pre-determined count value on the application of a clock signal. Once the count value is reached, resetting them returns the counter back to zero to start again.

A decade counter counts in a sequence of ten and then returns back to zero after the count of nine. Obviously to count up to a binary value of nine, the counter must have at least four flip-flops within its chain to represent each decimal digit as shown.

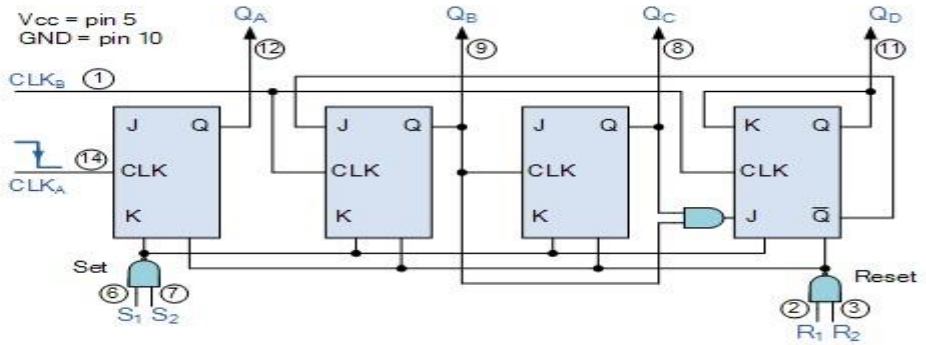
BCD Counter State Diagram



The 74LS90 BCD Counter

The 74LS90 integrated circuit is basically a MOD-10 decade counter that produces a BCD output code. The 74LS90 consists of four master-slave JK flip-flops internally connected to provide a MOD-2 (count-to-2) counter and a MOD-5 (count-to-5) counter. The 74LS90 has one independent toggle JK flip-flop driven by the CLK A input and three toggle JK flip-flops that form an asynchronous counter driven by the CLK B input as shown.

74LS90 BCD Counter



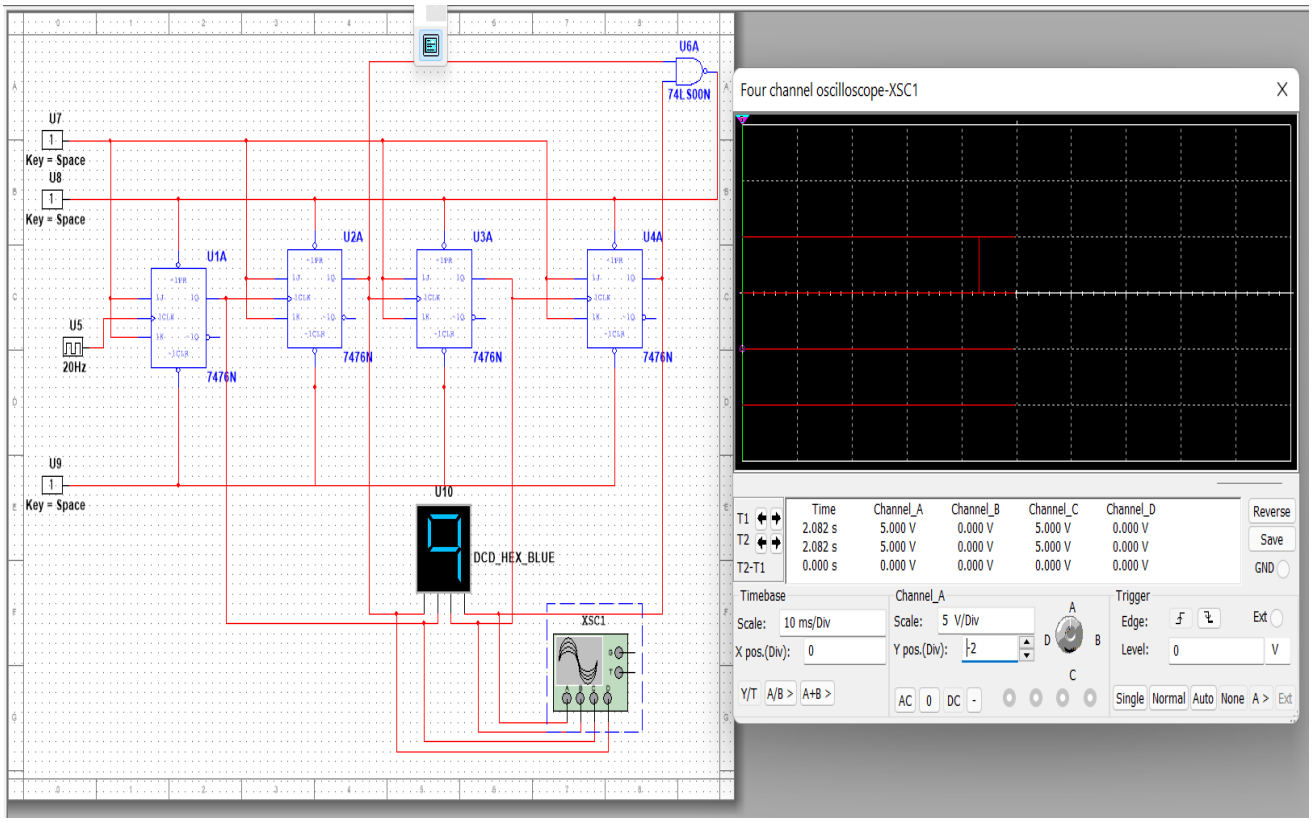
The counters four outputs are designated by the letter symbol Q with a numeric subscript equal to the binary weight of the corresponding bit in the BCD counter circuits code. So for example, Q_A, Q_B, Q_C and Q_D. The 74LS90 counting sequence is triggered on the negative going edge of the clock signal, that is when the clock signal CLK goes from logic 1 (HIGH) to logic 0 (LOW).
The additional input pins R_1 and R_2 are counter "reset" pins while inputs S_1 and S_2 are "set" pins. When connected to logic 1, the Reset inputs R_1 and R_2 reset the counter back to zero, 0 (0000), and when the Set inputs S_1 and S_2 are connected to logic 1, they Set the counter to maximum, or 9 (1001) regardless of the actual count number or position.

PROCEDURE:

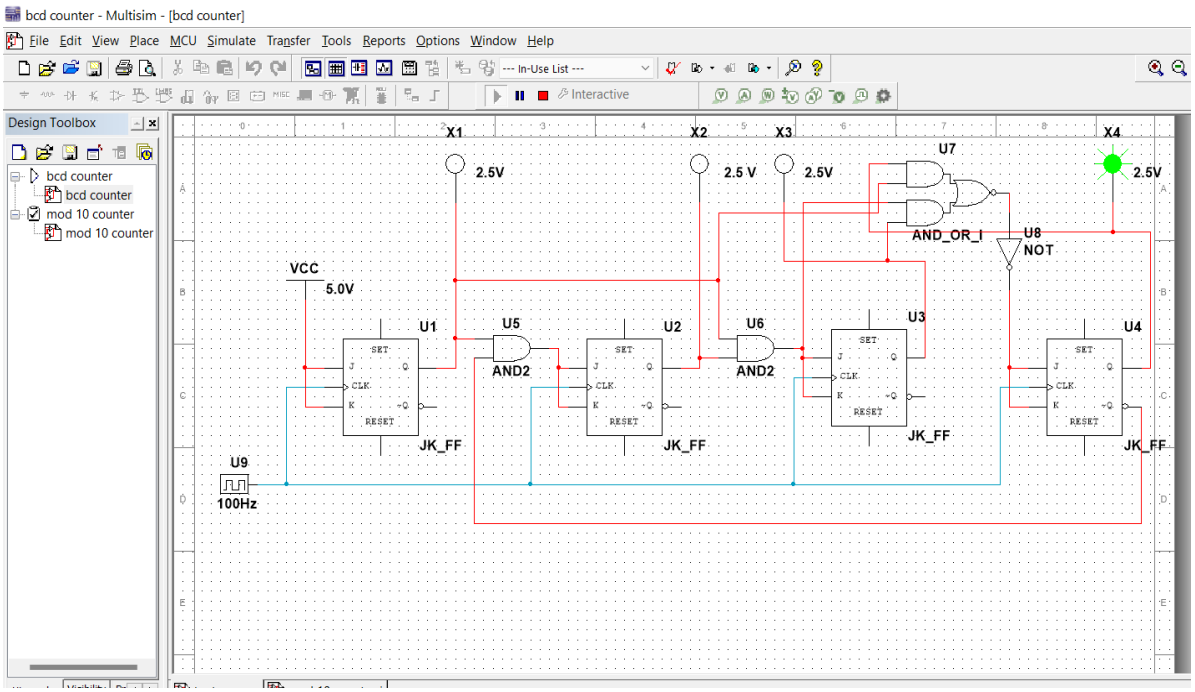
(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

CIRCUIT DESIGN:

ASYNCHRONOUS DECADE COUNTER



BCD COUNTER



RESULT:

Thus the Counters were designed and their truth table is verified.

PRECAUTIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch live and naked wires.