DIGITAL LOGIC DESIGN

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BT20EC001
ELECTRONICS AND COMMUNICATION
EXPERIMENT 2

EXPERIMENT – 2

AIM: -

Verify the NAND and NOR gates as universal logic gates.

APPARATUS REQUIRED: -

logic trainer kit, NAND gates (IC 7400), NOR gates (IC 7402), wires.

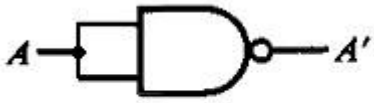
THEORY: -

NAND gate is actually a combination of two logic gates: AND gate followed by NOT gate. So its output is complement of the output of an AND gate.
This gate can have minimum two inputs; output is always one. By using only NAND gates, we can realize all logic functions: AND, OR, NOT, X-OR, X-NOR, NOR. So this gate is also called universal gate.

NAND gates as NOT gate:

A NOT produces complement of the input. It can have only one input, tie the inputs of a NAND gate together. Now it will work as a NOT gate. Its output is

$$Y = (A.A)'$$
$$Y = (A)'$$

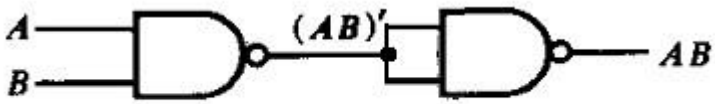


NOT (inverter)

NAND gates as AND gate:

A NAND produces complement of AND gate. So, if the output of a NAND gate is inverted, overall output will be that of an AND gate.

$$Y = ((A.B)')'$$
$$Y = (A.B)$$



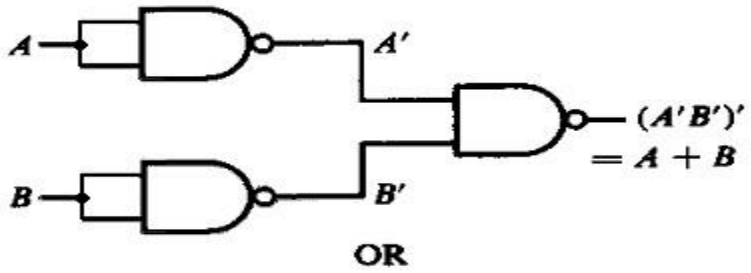
AND

NAND gates as OR gate:

From DeMorgan's theorems: (A.B)' = A' + B'

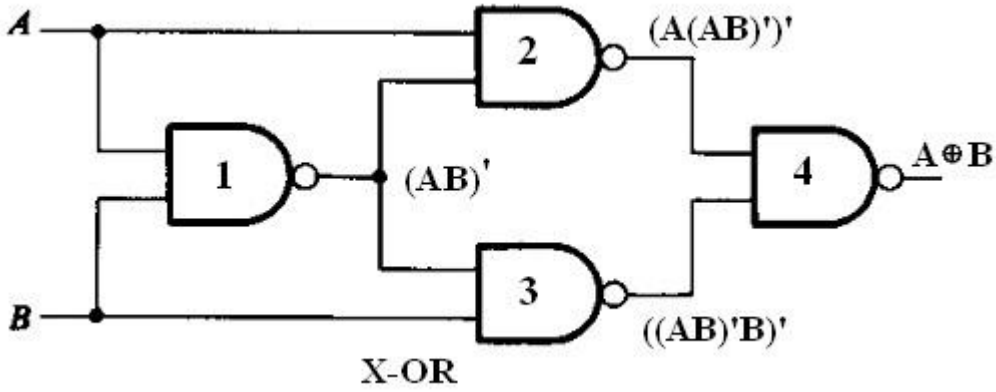
(A'.B')' = A'' + B'' = A + B

So, give the inverted inputs to a NAND gate, obtain OR operation at output.



NAND gates as X-OR gate:

The output of a two input X-OR gate is shown by: Y = A'B + AB'. This can be achieved with the logic diagram shown in the below.



Gate No.	Inputs	Output
1	A, B	(AB)'
2	A, (AB)'	(A (AB)')'
3	(AB)', B	(B (AB)')'
4	(A (AB)')', (B (AB)')'	A'B + AB'

Now the output from gate no. 4 is the overall output of the configuration.

Y = ((A (AB)')' (B (AB)')')'

= (A(AB)'')'' + (B(AB)'')''

= (A(AB)') + (B(AB)')

= (A(A' + B)') + (B(A' + B'))

= (AA' + AB') + (BA' + BB')

= (0 + AB' + BA' + 0)

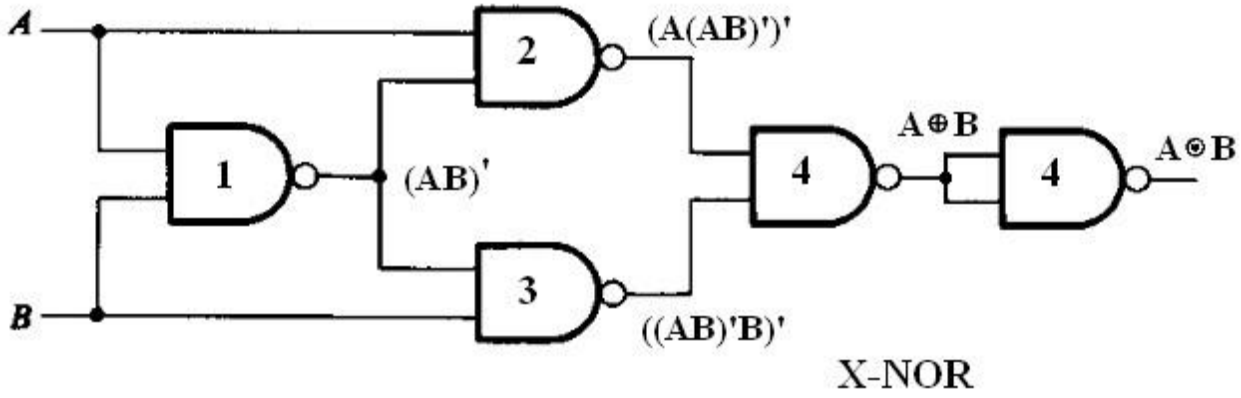
= AB' + BA'

Y = AB' + A'B

NAND gates as X-NOR gate:

X-NOR gate is actually X-OR gate followed by NOT gate. So give the output of X-OR gate to a NOT gate, overall output is that of an X-NOR gate.

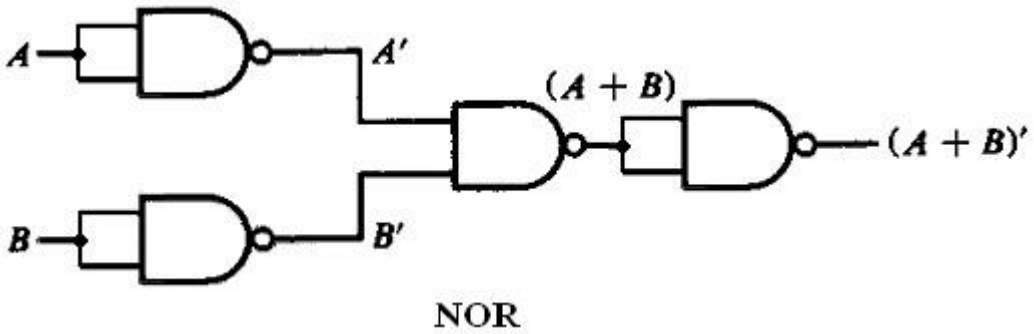
Y = AB+ A'B'



NAND gates as NOR gate

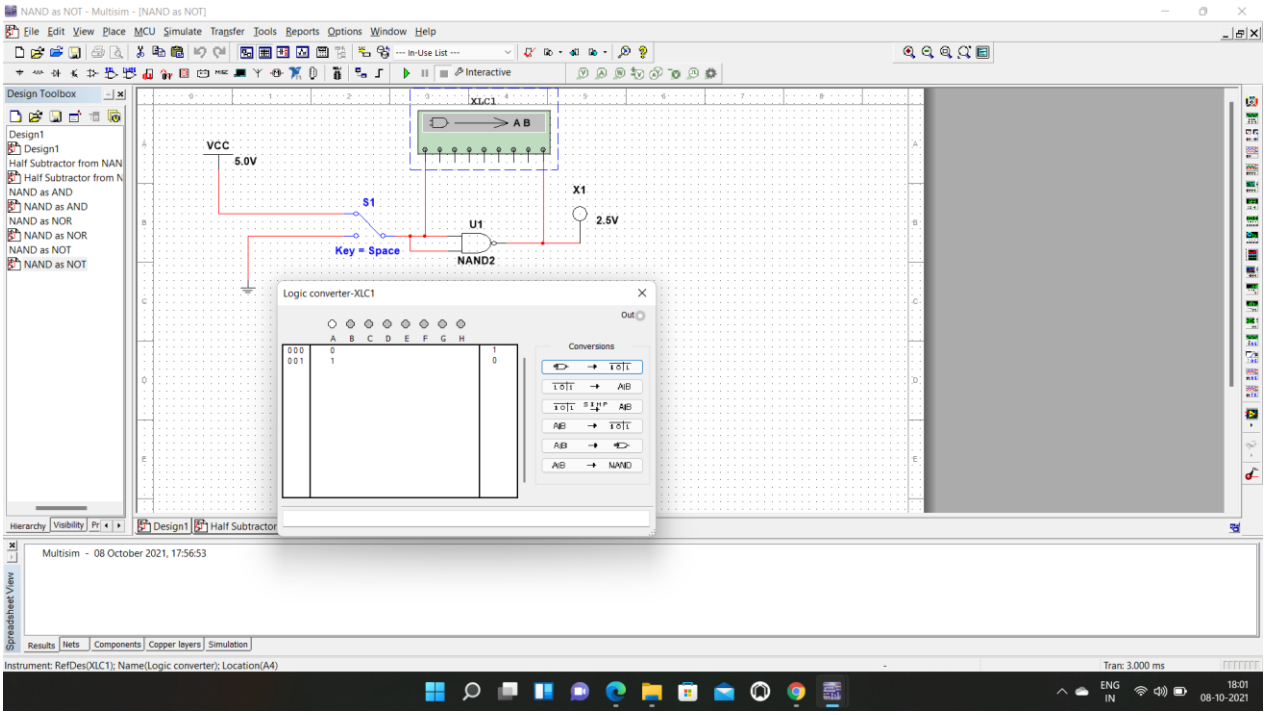
A NOR gate is an OR gate followed by NOT gate. So connect the output of OR gate to a NOT gate, overall output is that of a NOR gate.

Y = (A + B)'

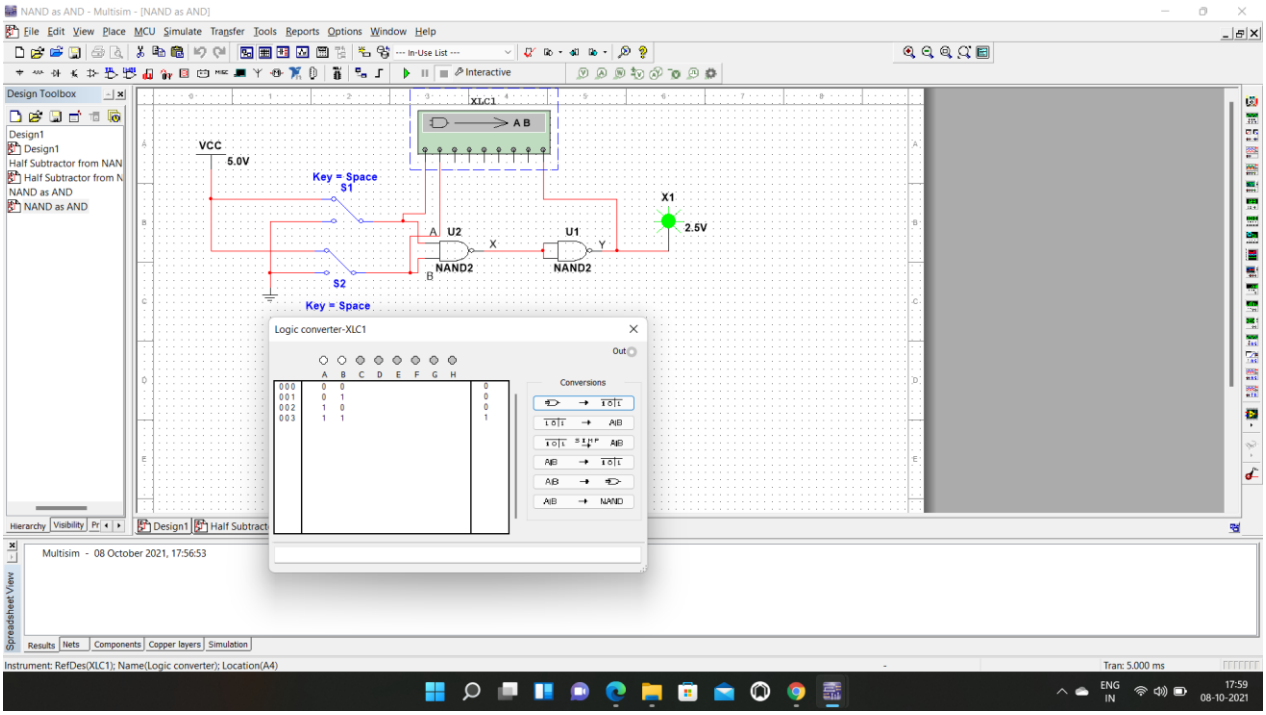


VERIFICATION FOR NAND GATE:

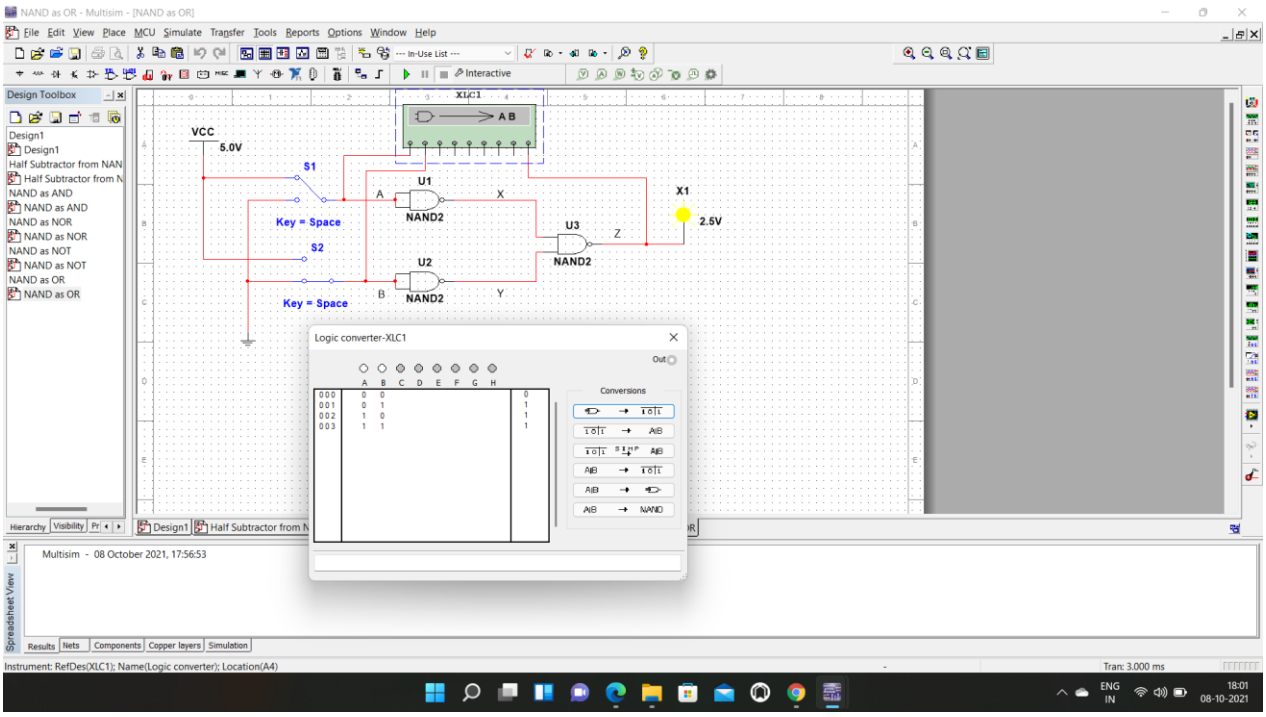
NAND gates as NOT gate:



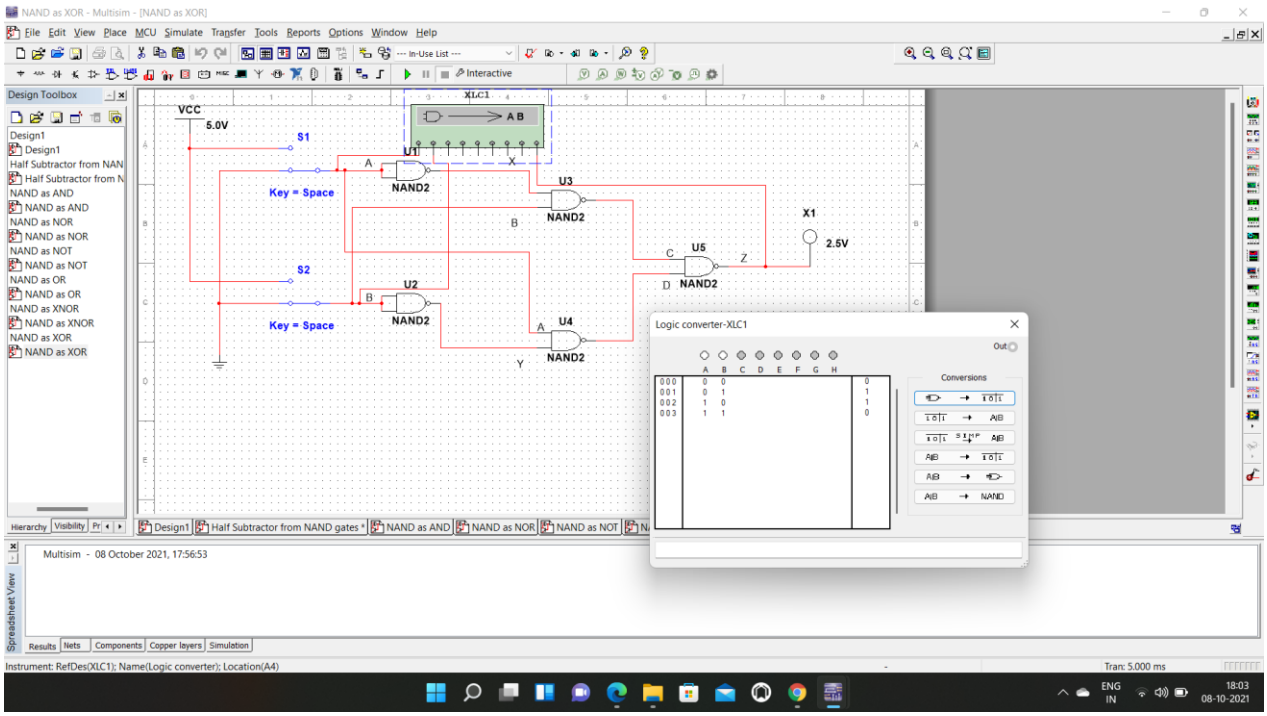
NAND gates as AND gate:



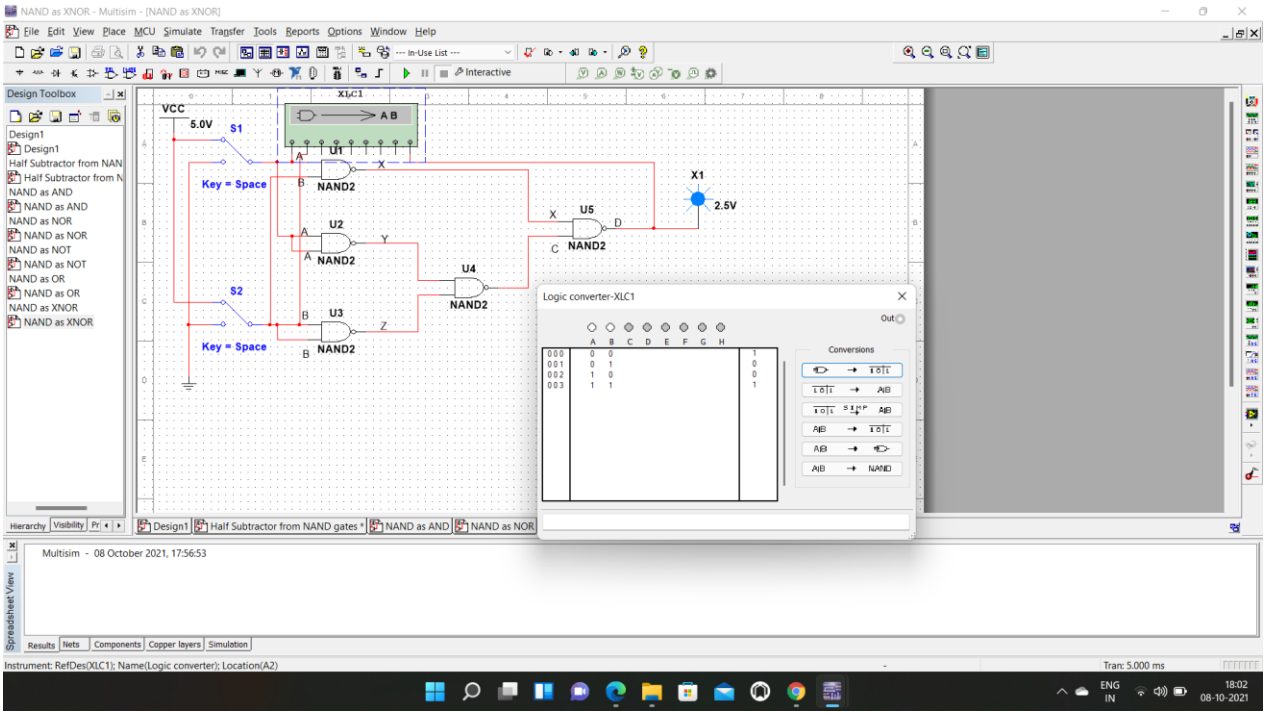
NAND gates as OR gate:



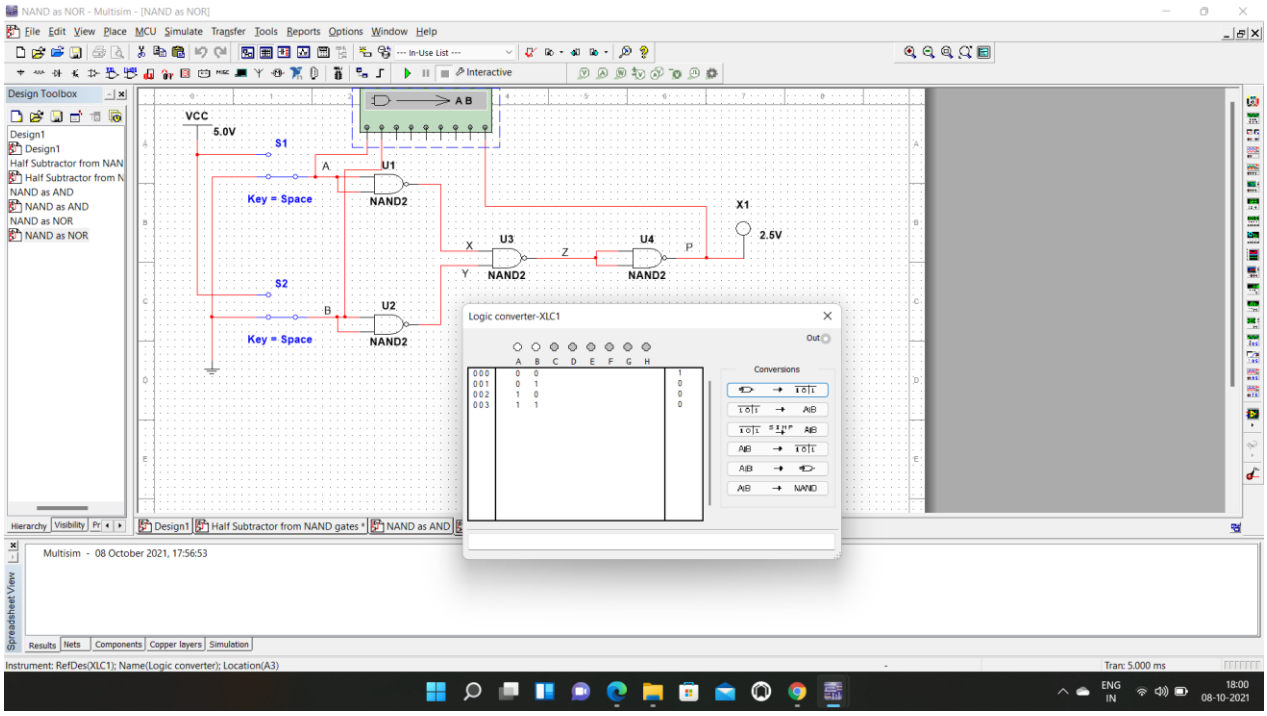
NAND gates as X-OR gate:



NAND gates as X-NOR gate:



NAND gates as NOR gate:



PROCEDURE:

1. Connect the trainer kit to ac power supply.
2. Connect the NAND gates for any of the logic functions to be realized.
3. Connect the inputs of first stage to logic sources and output of the last gate to logic indicator.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all logic functions.
7. Switch off the power supply.

THEORY:

NOR gate is actually a combination of two logic gates: OR gate followed by NOT gate. So its output is complement of the output of an OR gate.
This gate can have minimum two inputs; output is always one. By using only NOR gates, we can realize all logic functions: AND, OR, NOT, X-OR, X-NOR, NAND. So this gate is also called universal gate.

NOR gates as NOT gate:

A NOT produces complement of the input. It can have only one input, tie the inputs of a NOR gate together. Now it will work as a NOT gate. Its output is

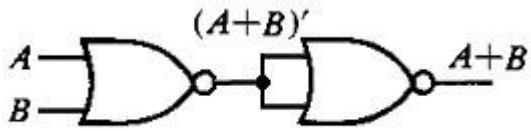
$$Y = (A+A)'$$
$$Y = (A)'$$

NOT

NOR gates as OR gate:

A NOR produces complement of OR gate. So, if the output of a NOR gate is inverted, overall output will be that of an OR gate.

$$Y = ((A+B)')'$$
$$Y = (A+B)$$



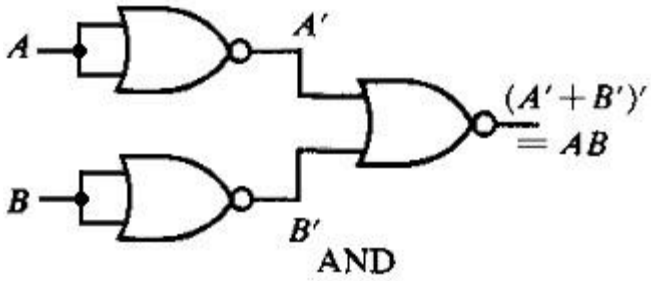
OR

NOR gates as AND gate:

From DeMorgan's theorems: $(A+B)' = A'B'$

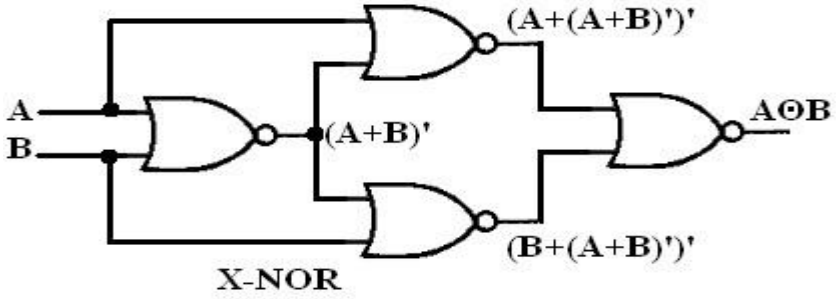
$$(A'+B')' = A''B'' = AB$$

So, give the inverted inputs to a NOR gate, obtain AND operation at output.



NOR gates as X-NOR gate:

The output of a two input X-NOR gate is shown by: Y = AB + A'B'. This can be achieved with the logic diagram shown in the left side.



Gate No.	Inputs	Output
1	A, B	(A + B)'
2	A, (A + B)'	(A + (A+B)')'
3	(A + B)', B	(B + (A+B)')'
4	(A + (A + B)')', (B + (A+B)')'	AB + A'B'

Now the output from gate no. 4is the overall output of the configuration.

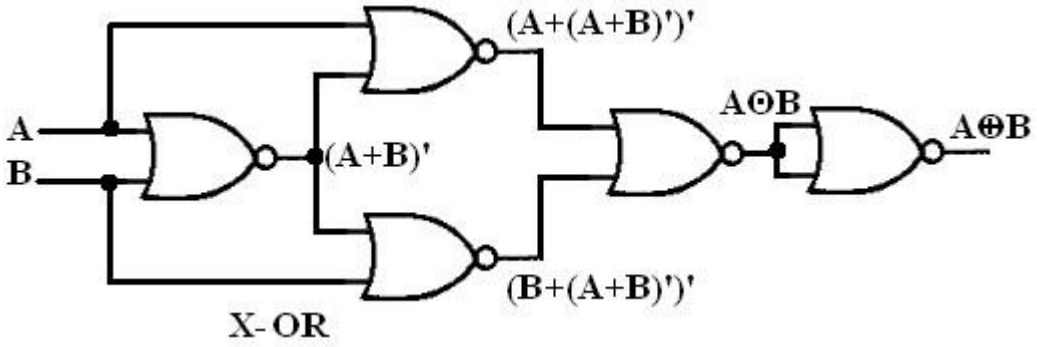
Y = ((A + (A+B)')' (B +(A+B)')')'
= (A+(A+B)'')'.(B+(A+B)')''
= (A+(A+B)').(B+(A+B)')
= (A+A'B').(B+A'B')
= (A + A').(A + B').(B+A')(B+B')
= 1.(A+B').(B+A').1
= (A+B').(B+A')
= A.(B + A') +B'.(B+A')
= AB + AA' +B'B+B'A'
= AB + 0 + 0 + B'A'
= AB + B'A'

Y = AB + A'B'

NOR gates as X-OR gate:

X-OR gate is actually X-NOR gate followed by NOT gate. So give the output of X-NOR gate to a NOT gate, overall output is that of an X-OR gate.

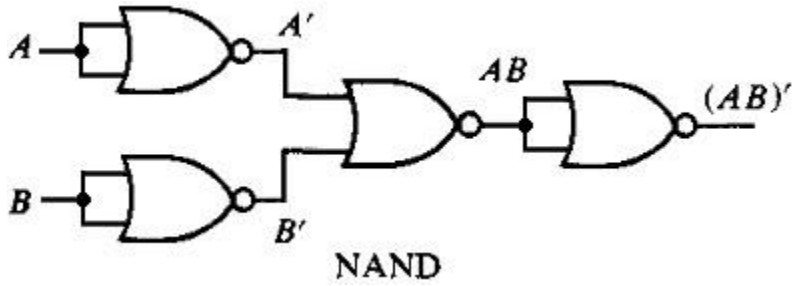
Y = A'B+ AB'



NOR gates as NAND gate:

A NAND gate is an AND gate followed by NOT gate. So connect the output of AND gate to a NOT gate, overall output is that of a NAND gate.

Y = (AB)'

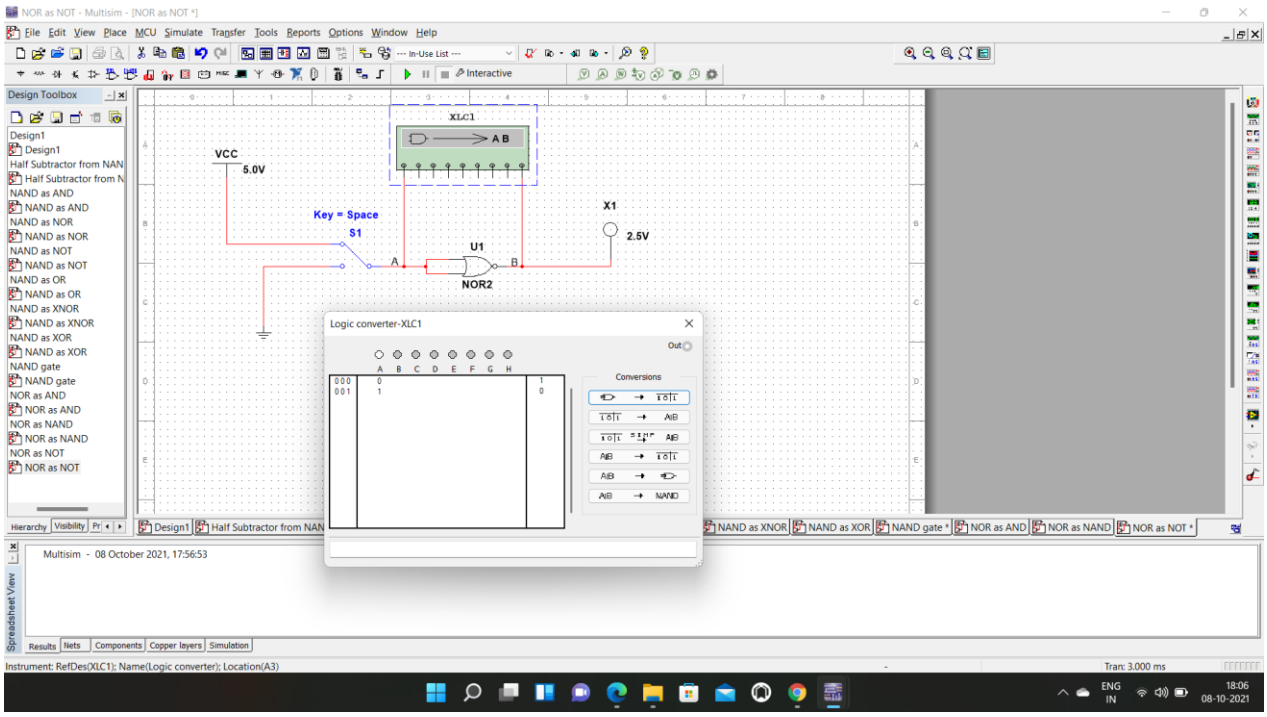


PROCEDURE:

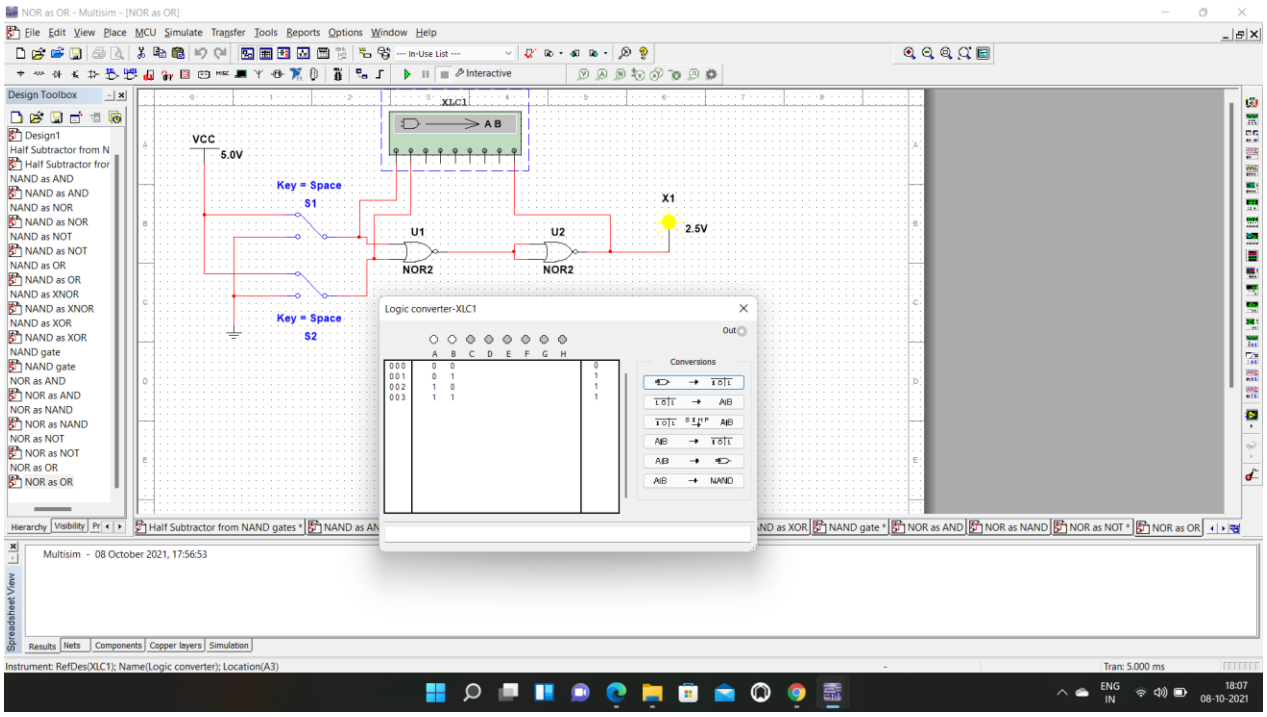
1. Connect the trainer kit to ac power supply.
2. Connect the NOR gates for any of the logic functions to be realised.
3. Connect the inputs of first stage to logic sources and output of the last gate to logic indicator.
4. Apply various input combinations and observe output for each one.
5. Verify the truth table for each input/ output combination.
6. Repeat the process for all logic functions.
7. Switch off the ac power supply.

VERIFICATION FOR NOR GATE:

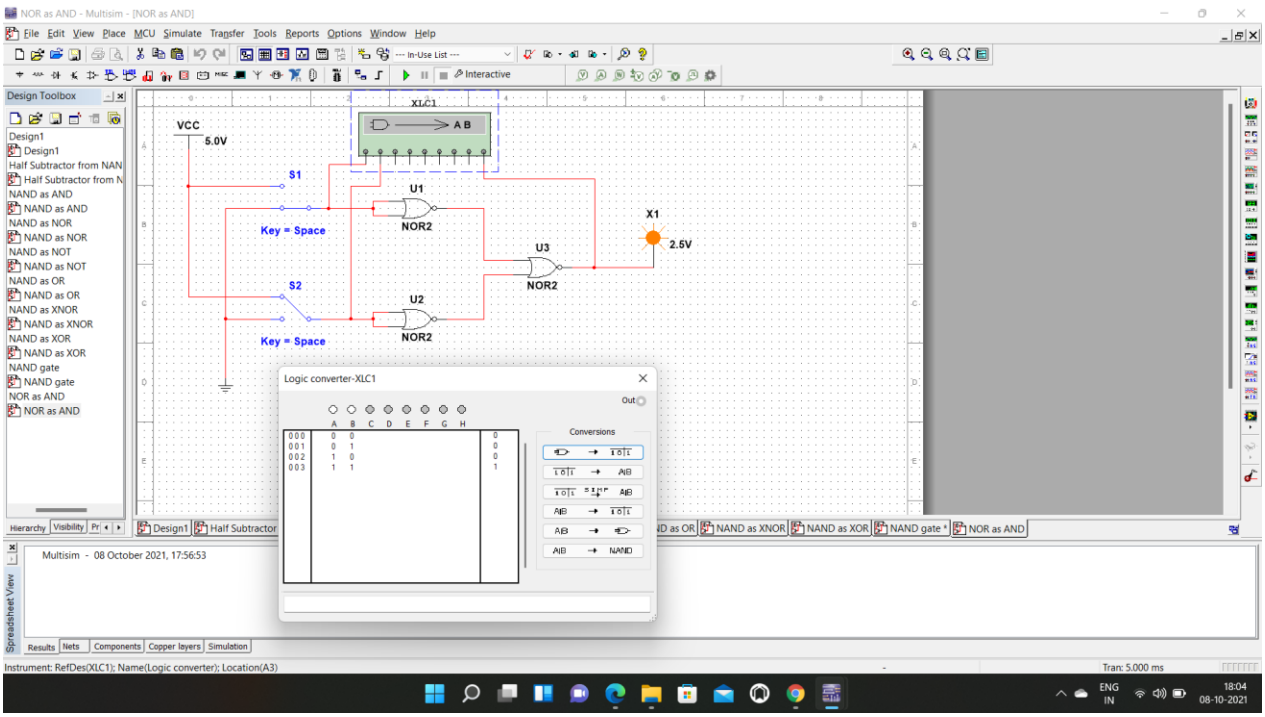
NOR gates as NOT gate:



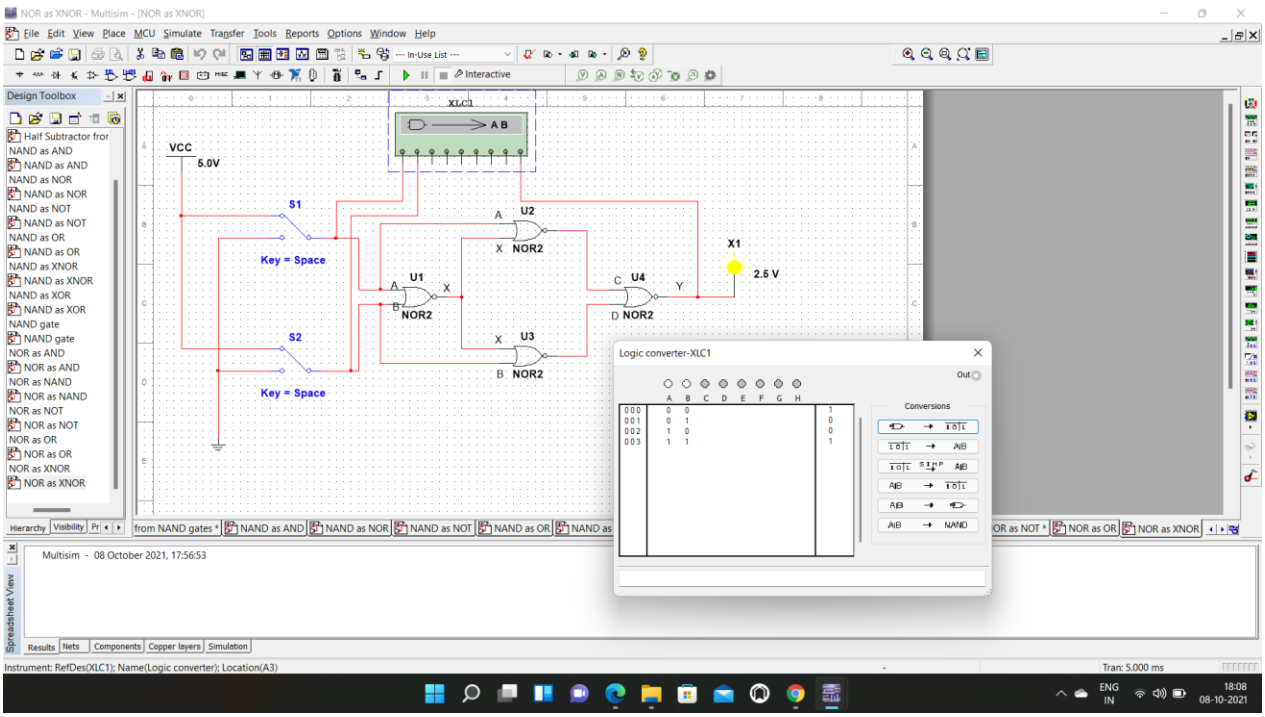
NOR gates as OR gate:



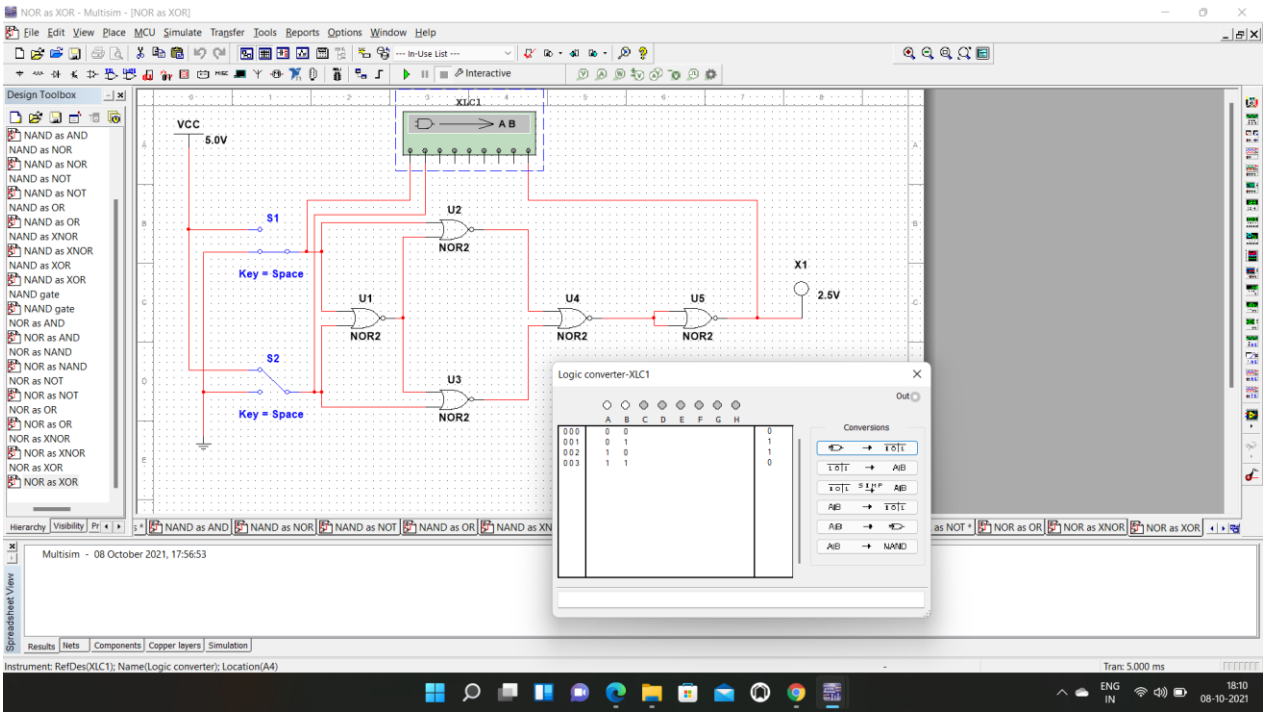
NOR gates as AND gate:



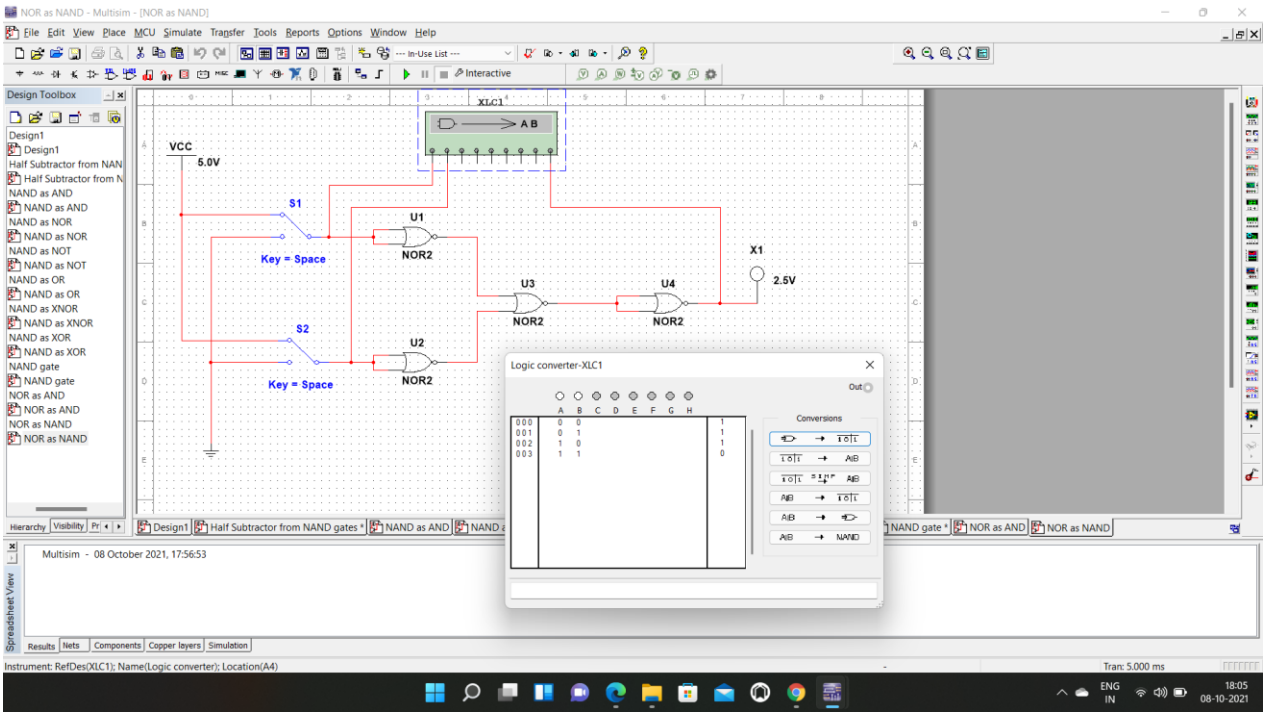
NOR gates as X-NOR gate:



NOR gates as X-OR gate:



NOR gates as NAND gate:



RESULT:

NAND & NOR are verified as universal gates successfully.

PRECAUTIONS:-

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch live and naked wires.