DIGITAL LOGIC DESIGN

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EXPERIMENT 4

EXPERIMENT – 4

AIM: -

Design and verification of the truth tables of Half and Full Subtractor circuits.

APPARATUS REQUIRED: -

logic trainer kit, NAND gates (IC 7400), XOR gates (IC 7486), AND gates (IC 7408), NOT gates (IC 7404), connecting wires.

THEORY:

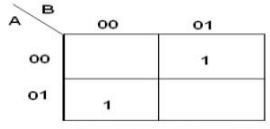
Half Subtractor:

The half subtractor is constructed using X-OR and AND Gate. The half subtractor has two input and two outputs. The outputs are difference and borrow. The difference can be applied using X-OR Gate, borrow output can be implemented using an AND Gate and an inverter.

Truth Table for Half Subtractor

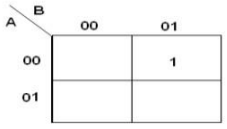
INPUT		OUTPUT	
A	**B**	**Bo**	**Diff**
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

K-Map for DIFFERENCE:



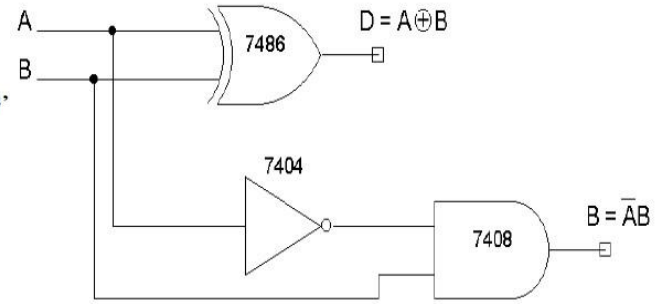
DIFFERENCE = A'B + AB'

K-Map for BORROW:

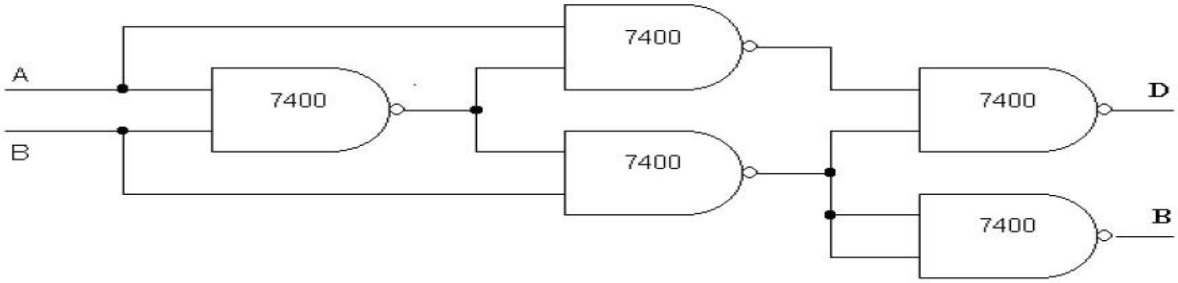


BORROW = A'B

Using X – OR and Basic Gates (a)Half Subtractor



(ii) Using only NAND gates (a) Half subtractor

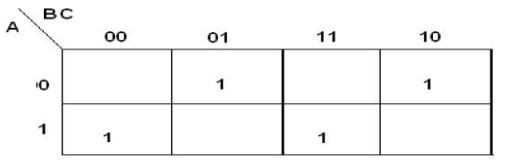


Full Subtractor:

The full subtractor is a combination of X-OR, AND, OR, NOT Gates. In a full subtractor the logic circuit should have three inputs and two outputs. The two half subtractor put together gives a full subtractor .The first half subtractor will be C and A B. The output will be difference output of full subtractor. The expression AB assembles the borrow output of the half subtractor and the second term is the inverted difference output of first X-OR. **Truth Table for Full Subtractor**

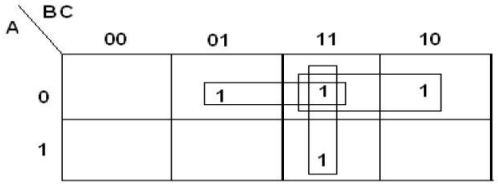
INPUT			OUTPUT	
A	**B**	**C**	**Bo**	**Diff**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-Map for Difference:



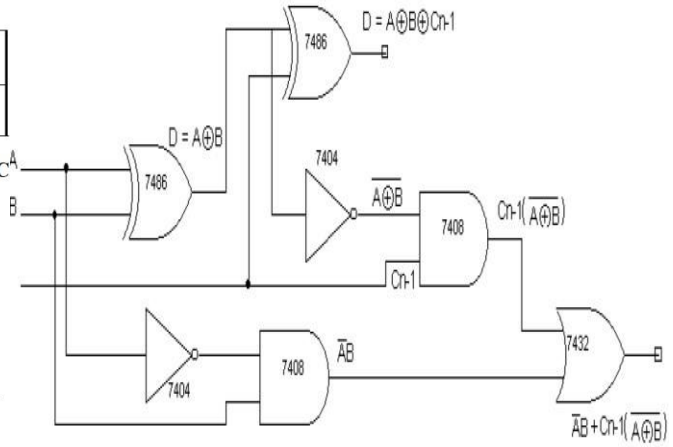
Difference = A'B'C + A'BC' + AB'C' + ABC

K-Map for Borrow:

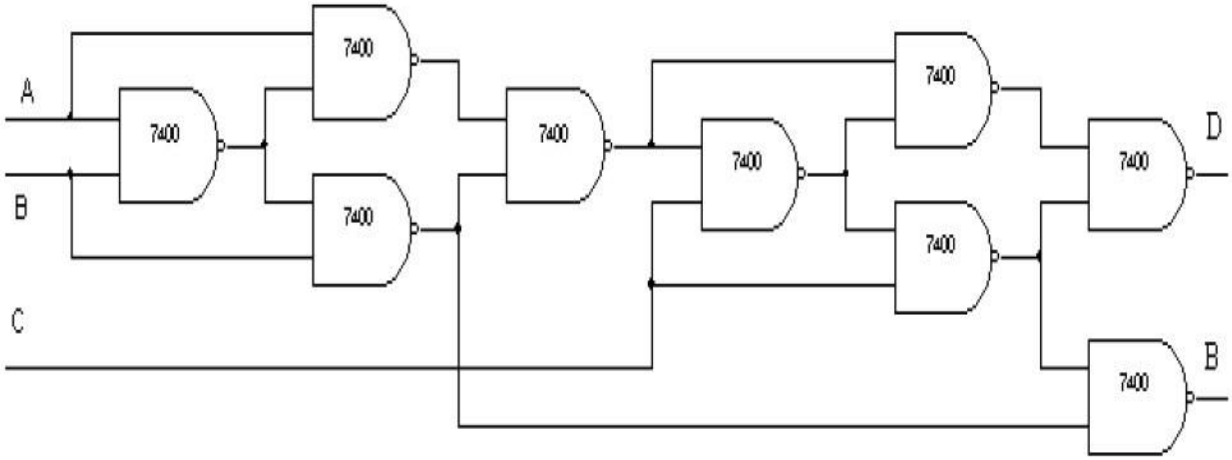


Borrow = A'B + BC + A'C

Full Subtractor



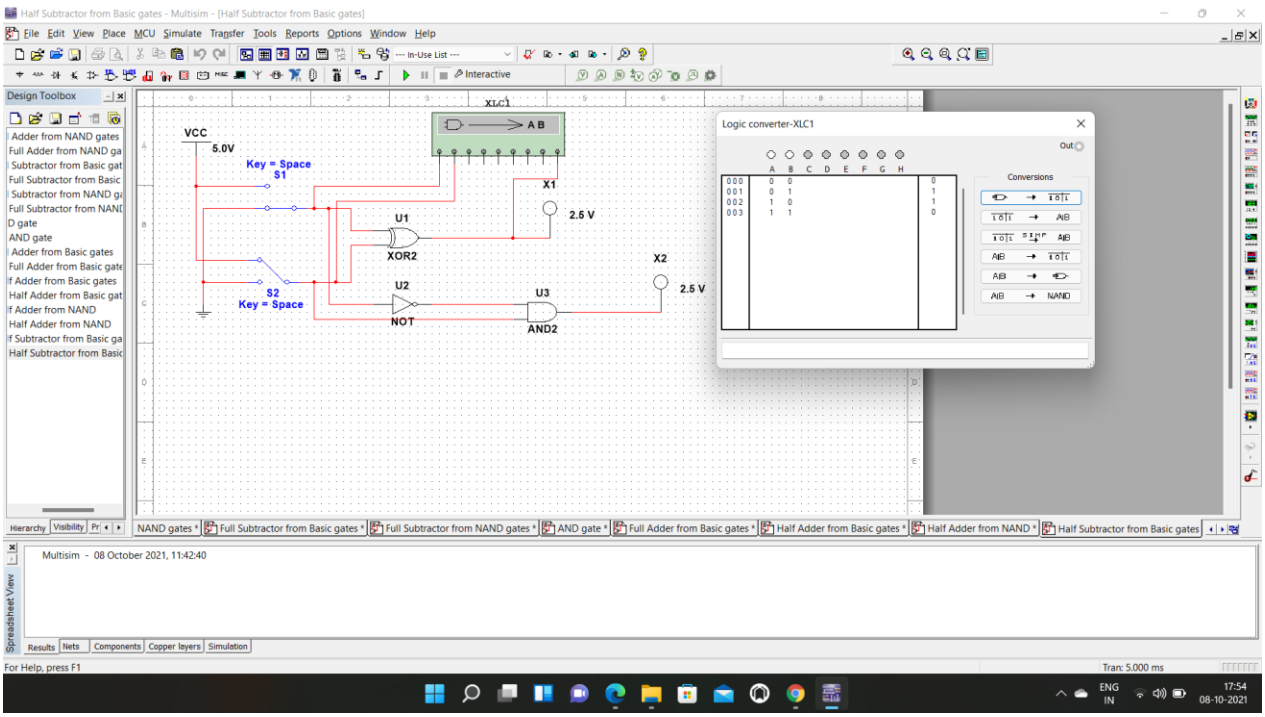
Using Only NAND Gates (Full Subtractor)



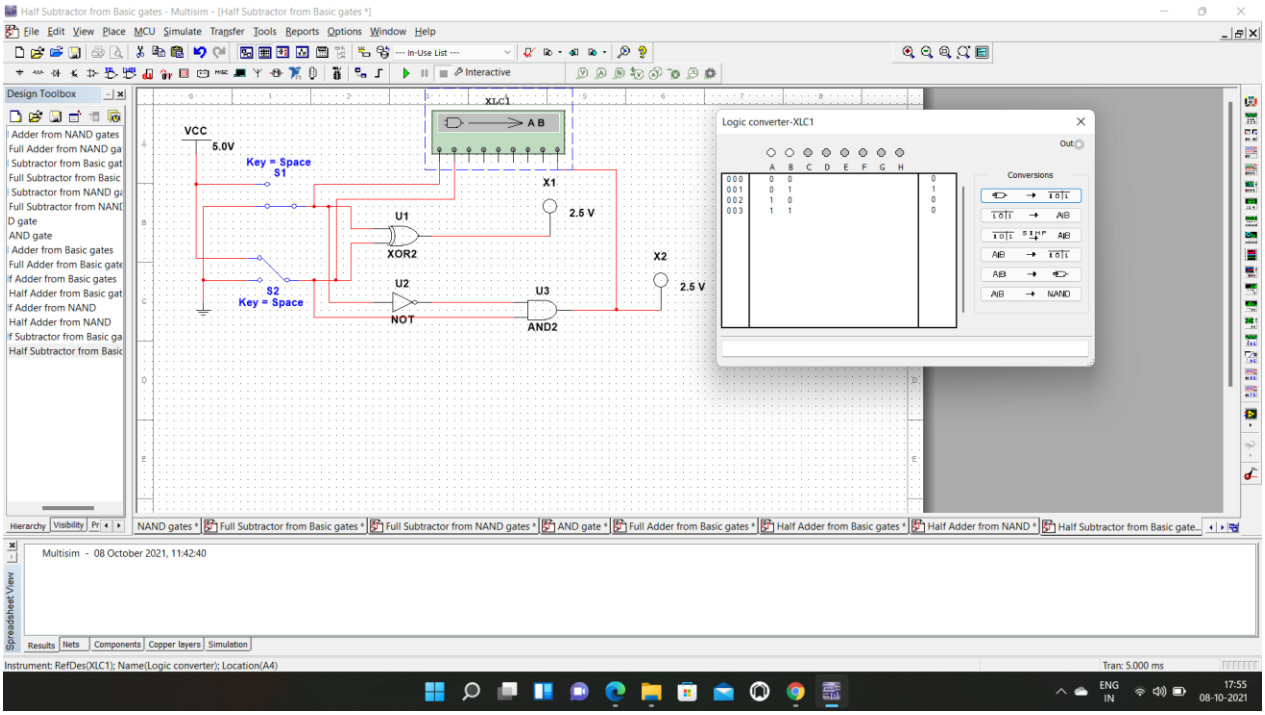
VERIFICATION OF HALF SUBTRACTOR:

HALF SUBTRACTOR USING BASIC GATES:

DIFFERENCE

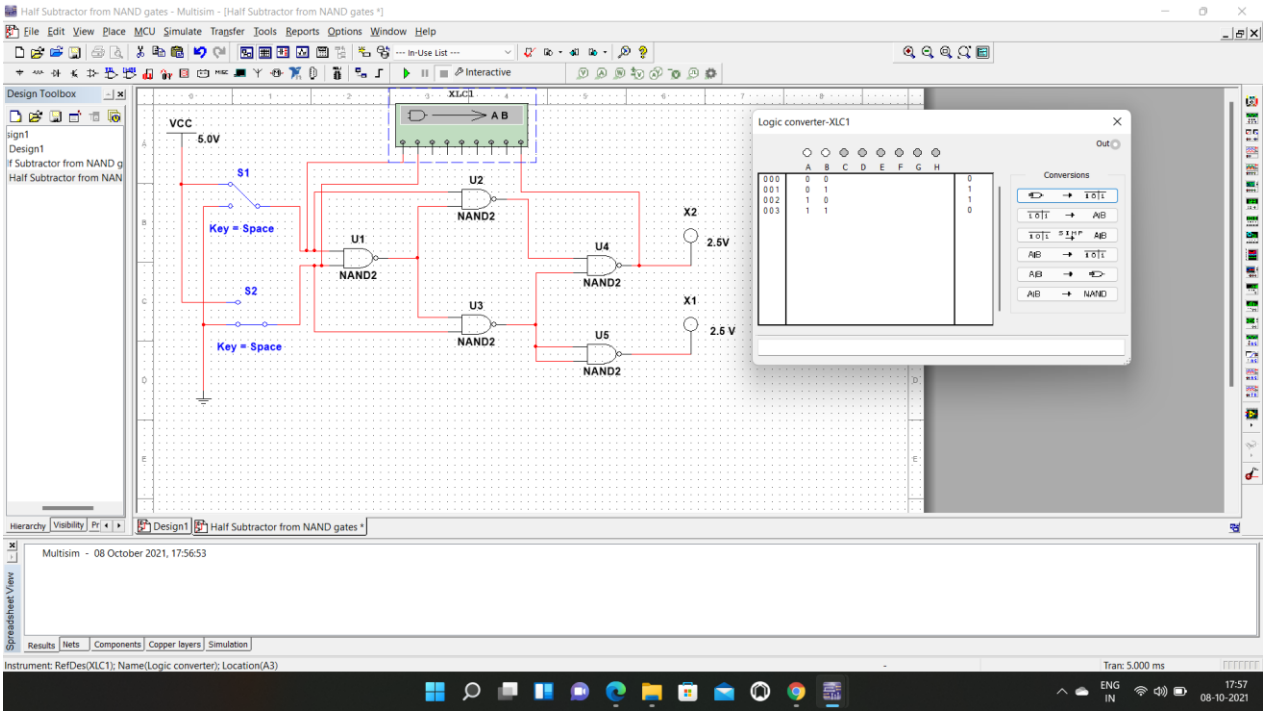


BORROW

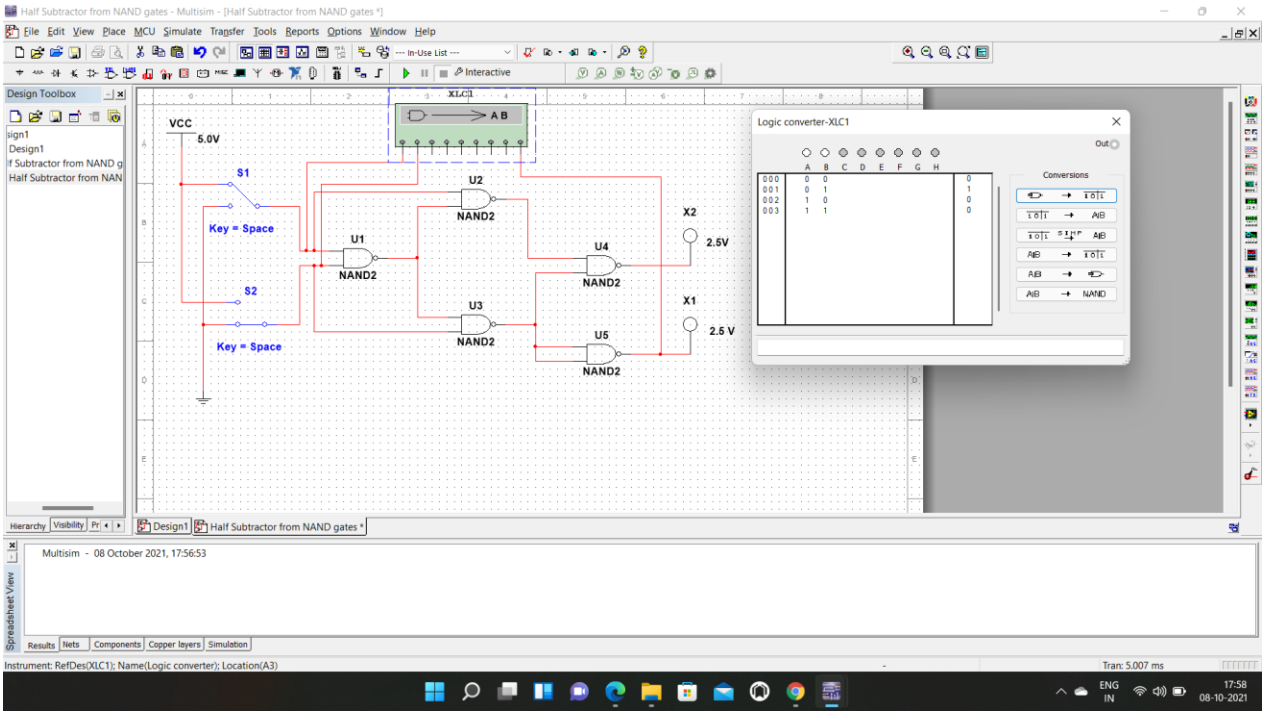


HALF SUBTRACTOR USING NAND GATES:

DIFFERENCE



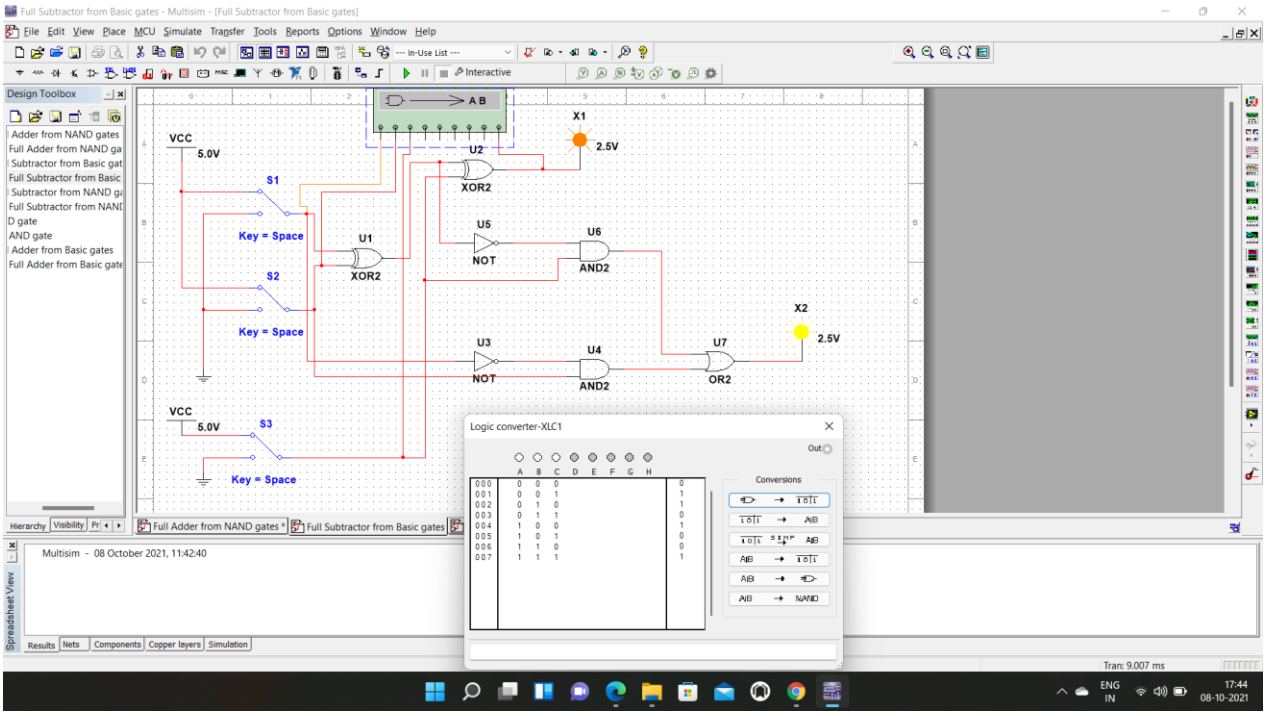
BORROW



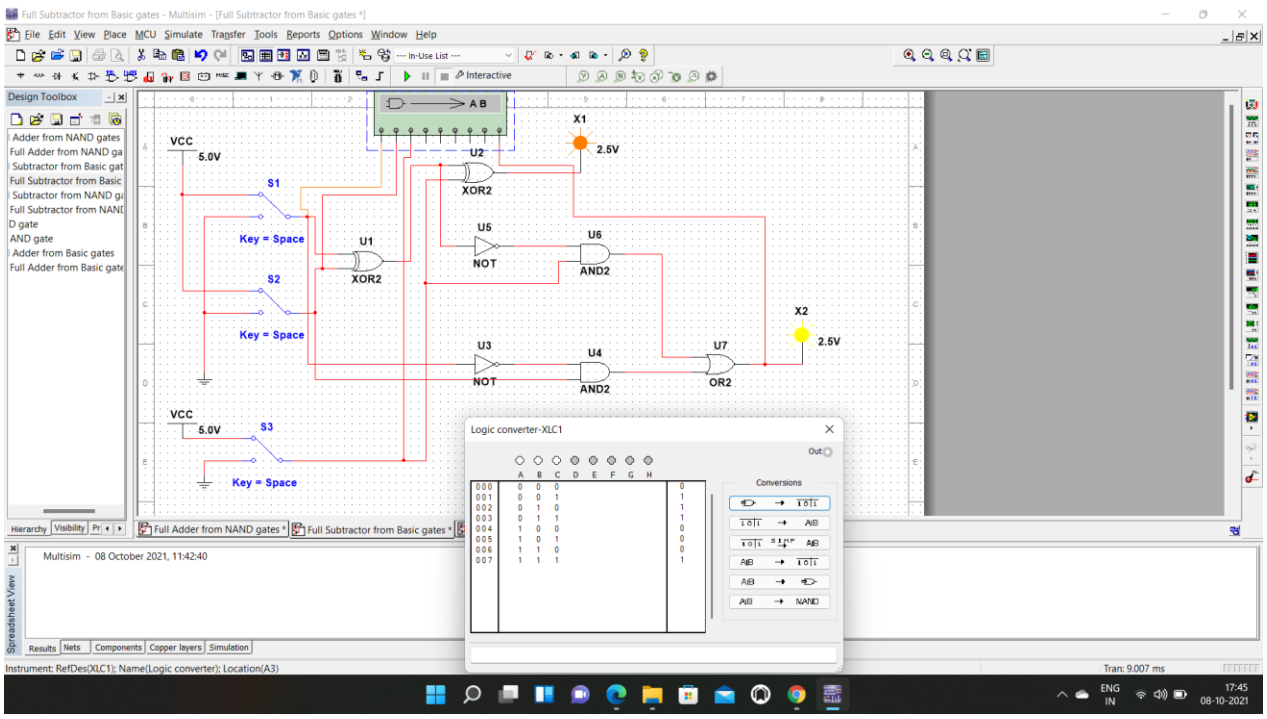
VERIFICATION OF FULL SUBTRACTOR:

FULL SUBTRACTOR USING BASIC GATES:

DIFFERENCE

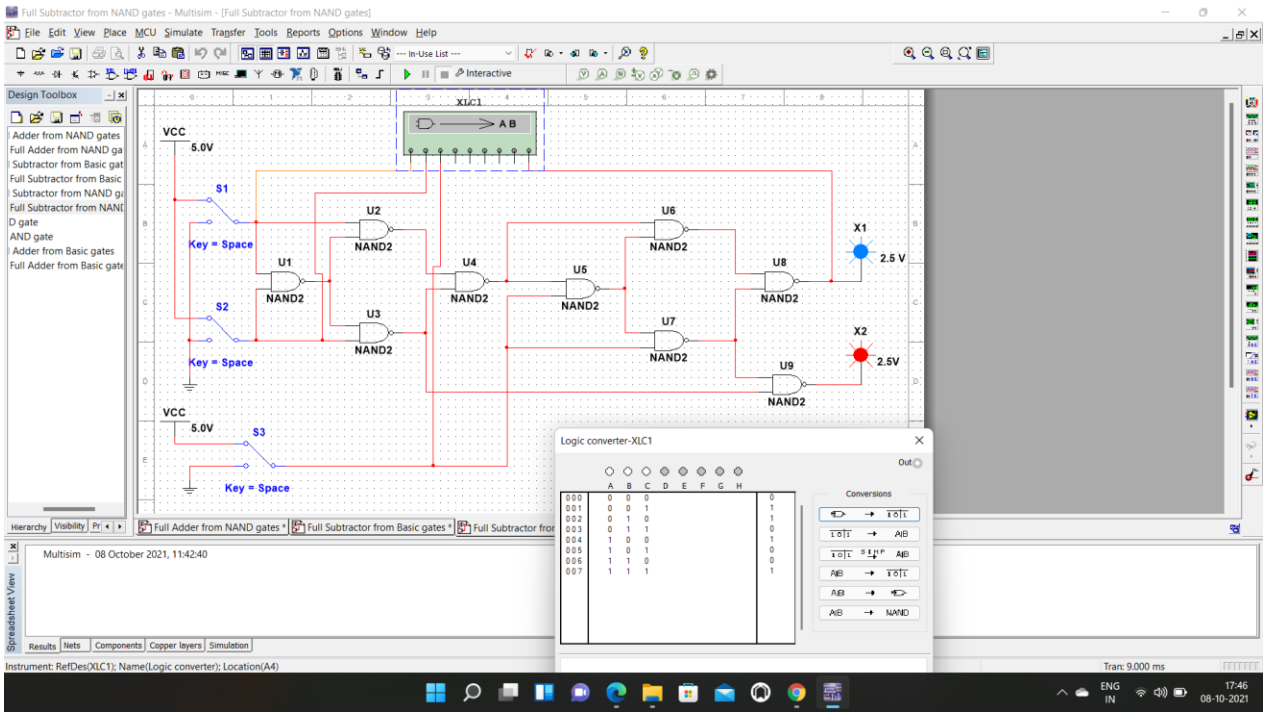


BORROW

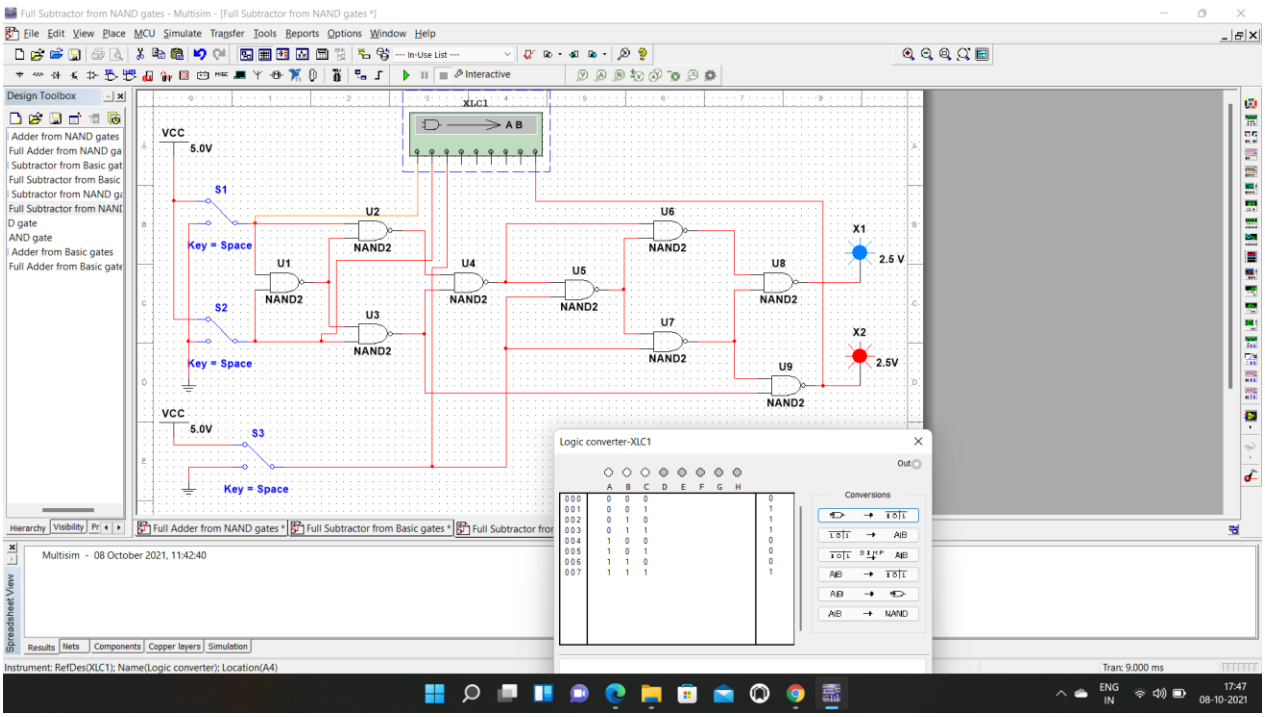


FULL SUBTRACTOR USING NAND GATES:

DIFFERENCE



BORROW



PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT:

Thus the half subtractor and full subtractor was designed and their truth table is verified.

PRECAUTIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off. • Never touch live and naked wires.