

**DIGITAL LOGIC DESIGN**  
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**ELECTRONICS AND COMMUNICATION**  
**EXPERIMENT 11**

## **EXPERIMENT – 11**

### **AIM: -**

Design of 4-bit shift register (shift right).

### **APPARATUS REQUIRED: -**

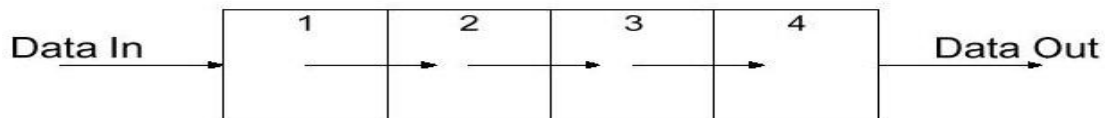
Logic trainer kit, D Flip-flop IC - 7474 wires.

### **THEORY:**

#### **Serial In/Shift Right/Serial Out Operation**

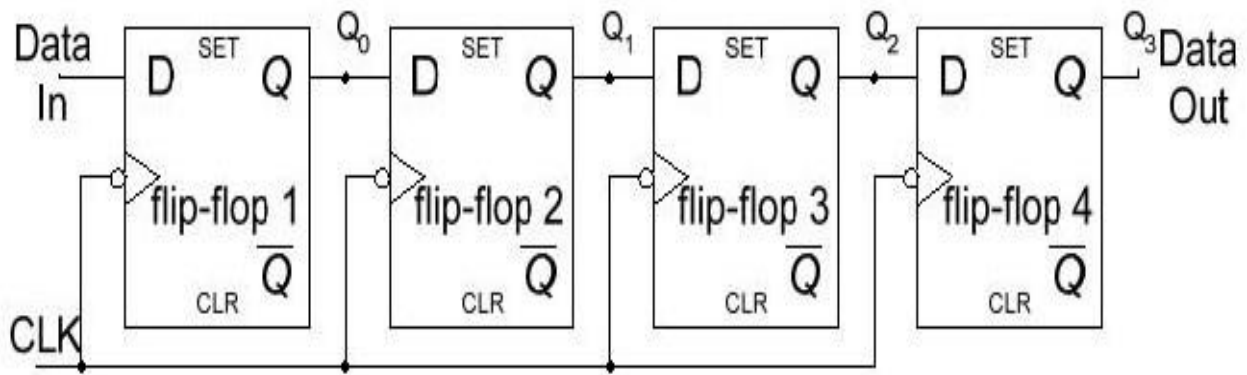
**Data** is shifted in the right hand direction one bit at a time with each transition of the clock signal. The data enters the shift register serially from the left hand side and after four clock transitions the 4-bit registers has 4-bbts of data. The data is shifted out serially one bit at a time from the right hand side of the register if clock signals are continuously applied. Thus after 8 clock signals the 4-bit data is completely shifted out of the shift register.

#### **Serial In/Serial Right/Serial Out Operation**

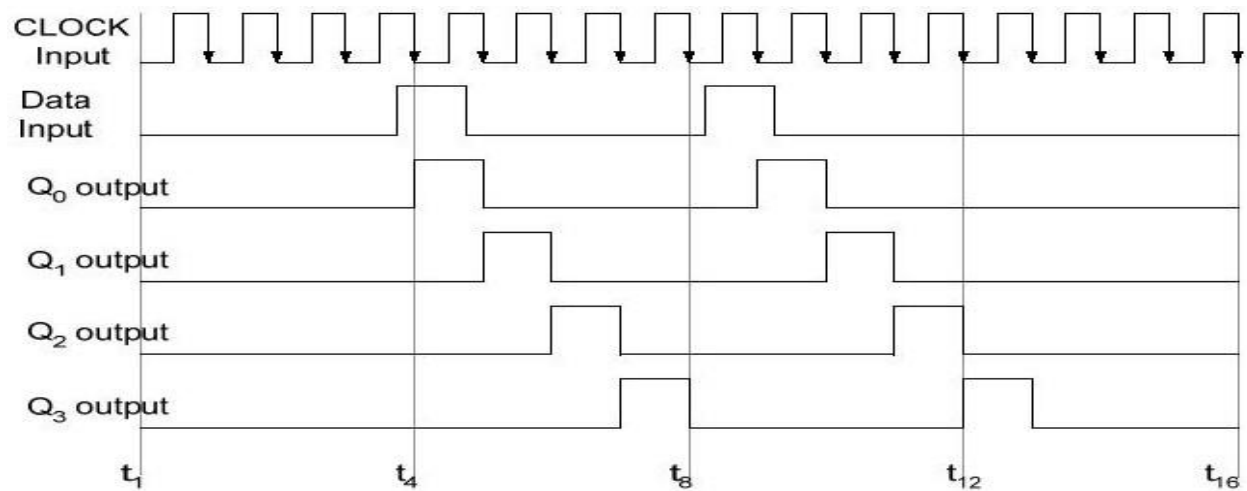


Serial shift registers can be implemented using any type of flip-flops. A serial shift register implemented using D flip-flops with the serial data applied at the D input of the first flip-flop and serial data out obtained at the Q output of the last flip-flop is shown in figure. At each clock transition 1 bit of serial data is shifted in and at the same instant 1-bit of serial data is shifted out. For a 4-bit shift register, 8 clock transitions are required to shift in 4-bit data and completely shift out the 4-bit data. As the data shifted out 1-bit at a time, a logic 0 value is usually shifted in to fill up the vacant bits in the shift register.

### Serial In/Shift Right/Serial Out Register



### Timing diagram of a Serial In/Shift Right/Serial Out Register



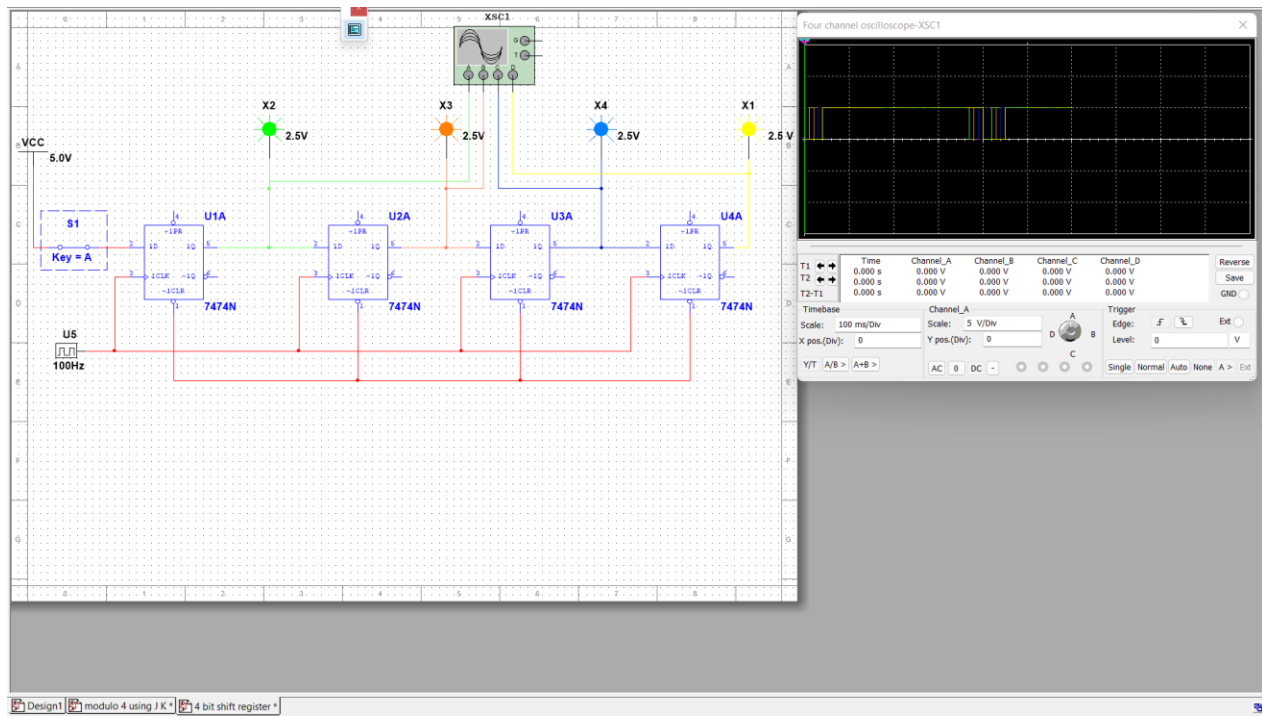
### Shift Register Truth Table

Outputs	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
Reset	0	0	0	0
CK Pulse 1	1	0	0	0
CK Pulse 2	0	1	0	0
CK Pulse 3	0	0	1	0
CK Pulse 4	0	0	0	1

## PROCEDURE:

- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table.

## DESIGN:



## RESULT:

Thus the Shift register was designed and their truth table is verified.

## PRECAUTIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch live and naked wires.