DIGITAL LOGIC DESIGN

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EXPERIMENT 3

EXPERIMENT – 3

AIM: -

Design and verification of the truth tables of Half and Full adder circuits.

APPARATUS REQUIRED: -

logic trainer kit, NAND gates (IC 7400), XOR gates (IC 7486), AND gates (IC 7408), wires.

THEORY:

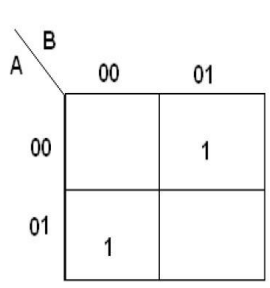
half adder:

A half adder has two inputs for the two bits to be added and two outputs one from the sum ' S' and other from the carry 'C' into the higher adder position. Above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND gate.

Truth Table for Half Adder

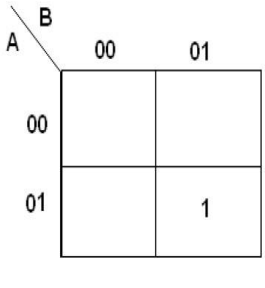
INPUT		OUTPUT	
A	**B**	**SUM**	**CARRY**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

K-Map for SUM:



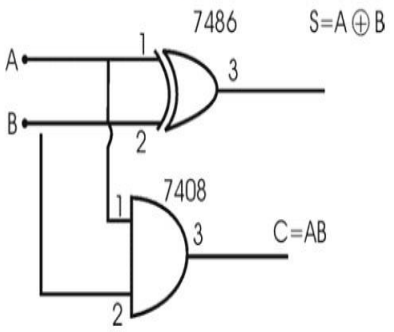
SUM = A'B + AB'

K-Map for CARRY:



CARRY = AB

Half Adder using basic gates:-

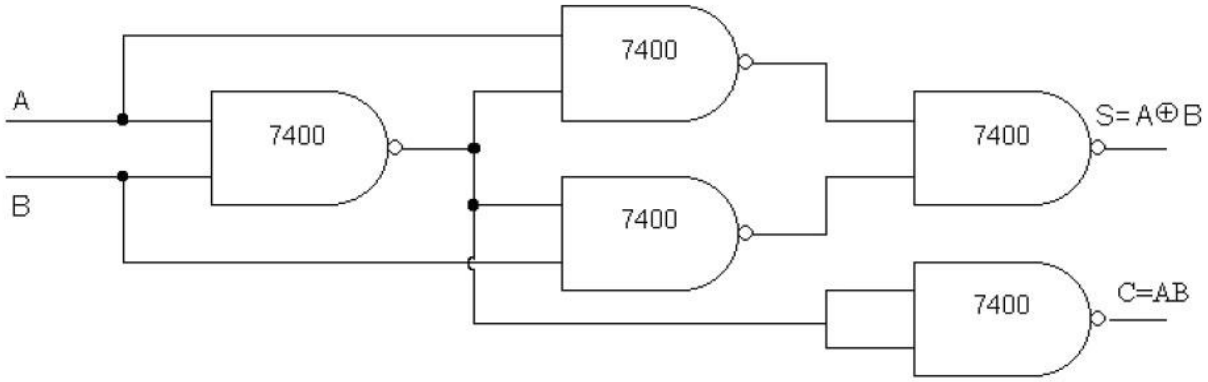


$S = \overline{A}B + A\overline{B}$

$S = A \oplus B$

$C = AB$

Half Adder using NAND gates only:-



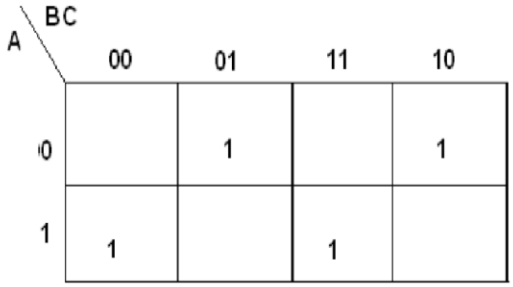
Full Adder:

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs. A full adder is useful to add three bits at a time but a half adder cannot do so. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

Truth Table for Full Adder

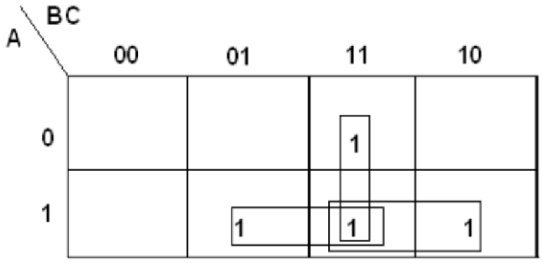
INPUT			OUTPUT	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-Map for SUM:



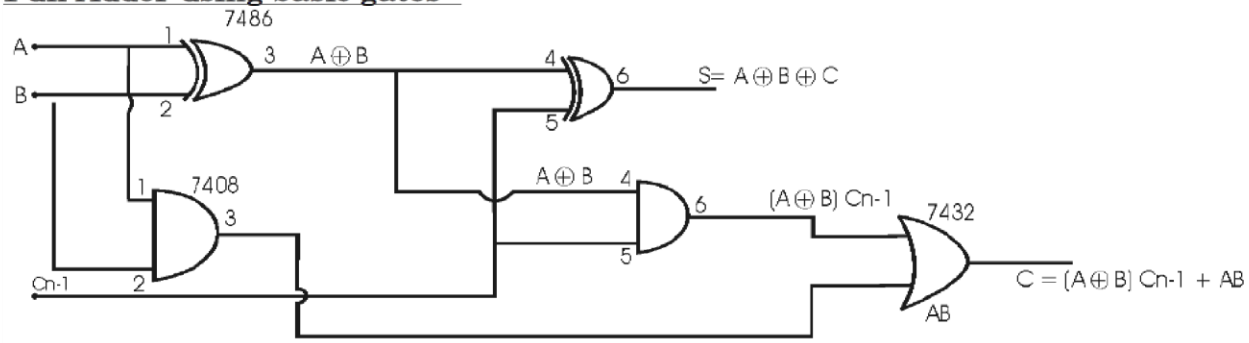
SUM = A'B'C + A'BC' + ABC' + ABC

K-Map for CARRY:

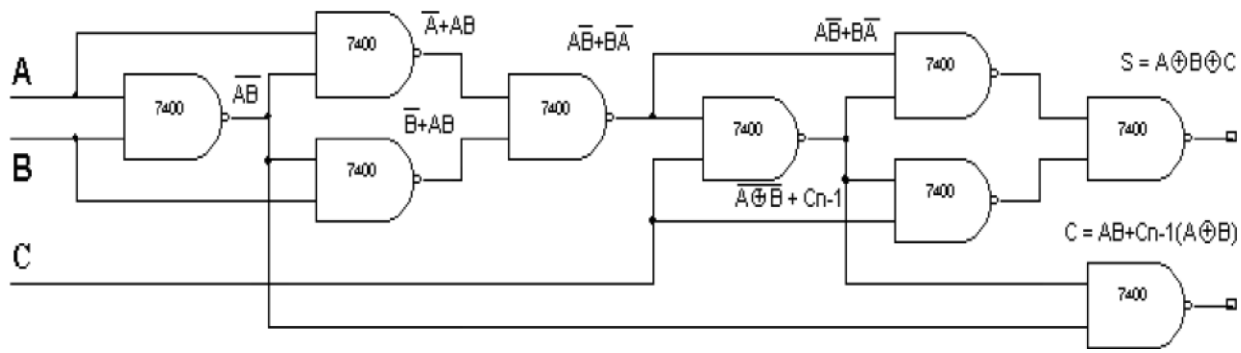


CARRY = AB + BC + AC

Full Adder using basic gates:-



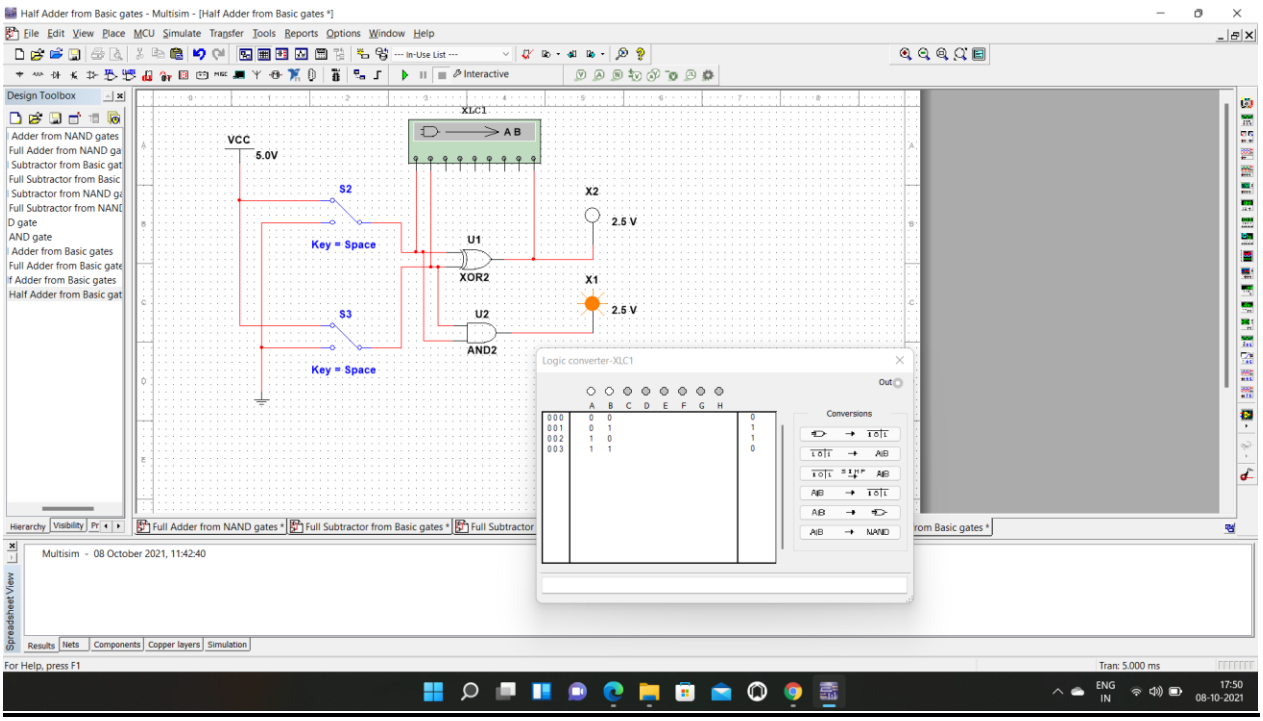
Full Adder using NAND gates only:-



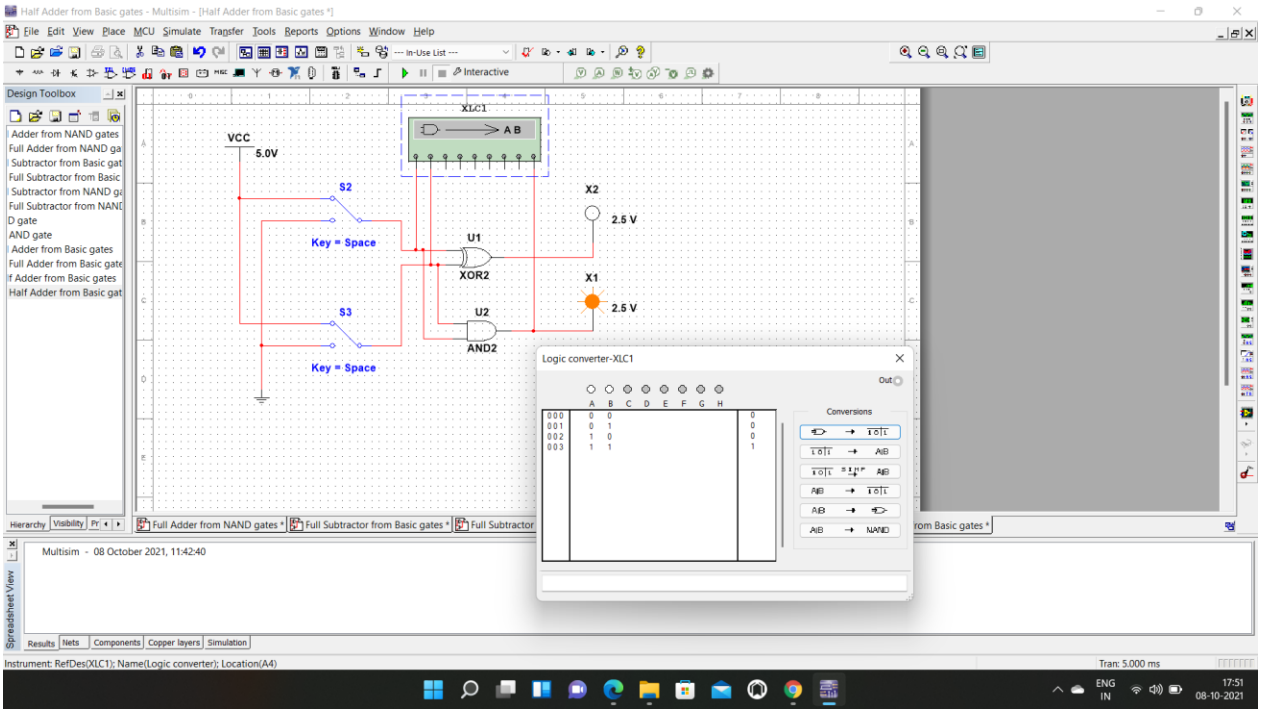
VERIFICATION OF HALF ADDER:

HALF ADDER USING BASIC GATES:

SUM

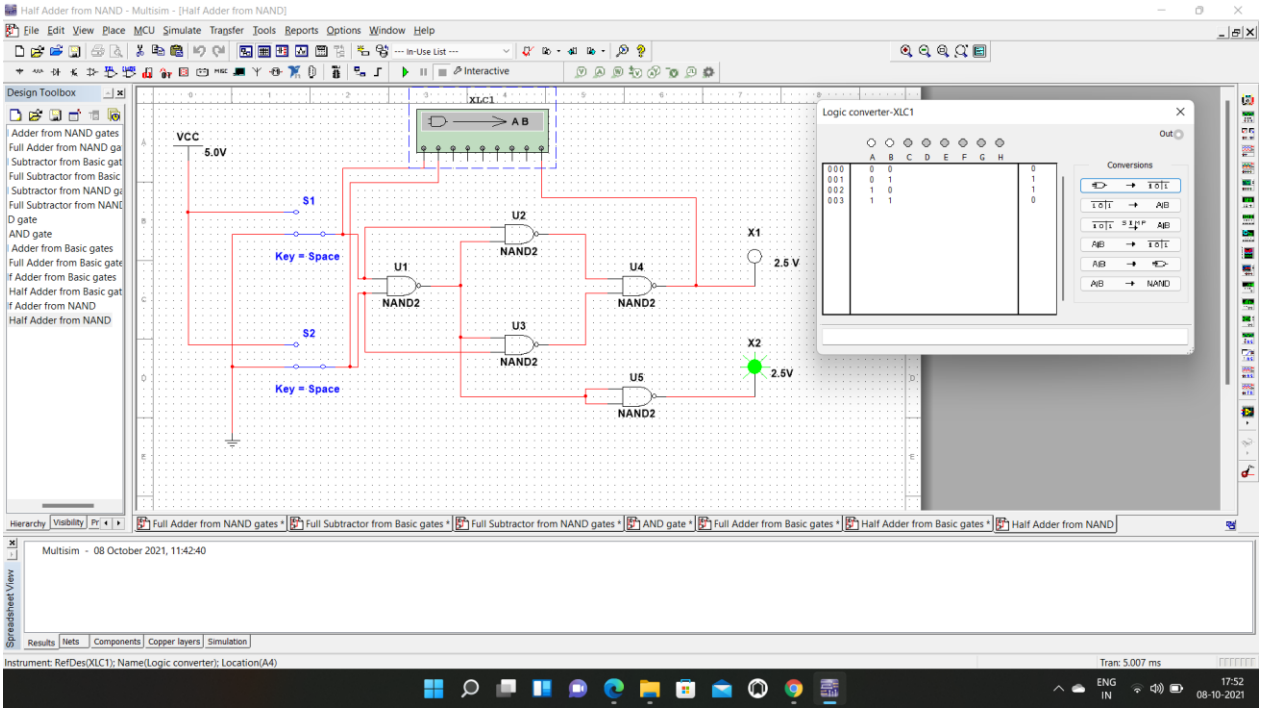


CARRY

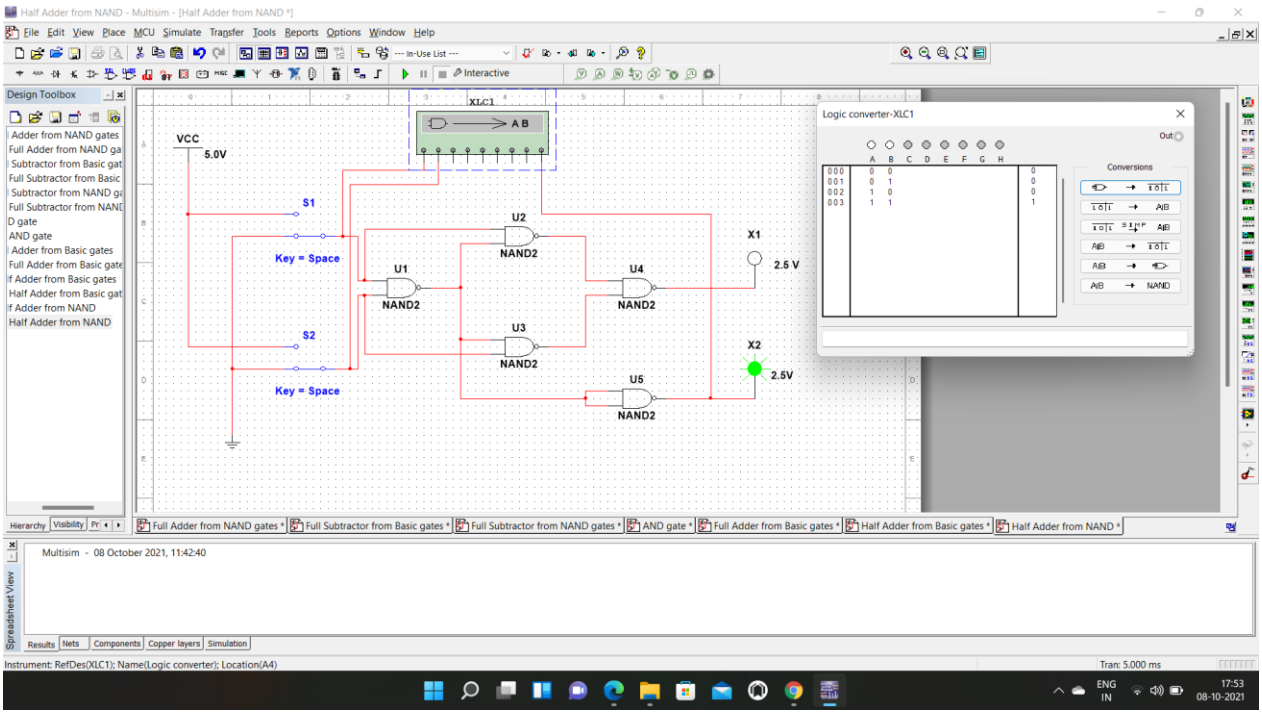


HALF ADDER USING NAND GATES:

SUM



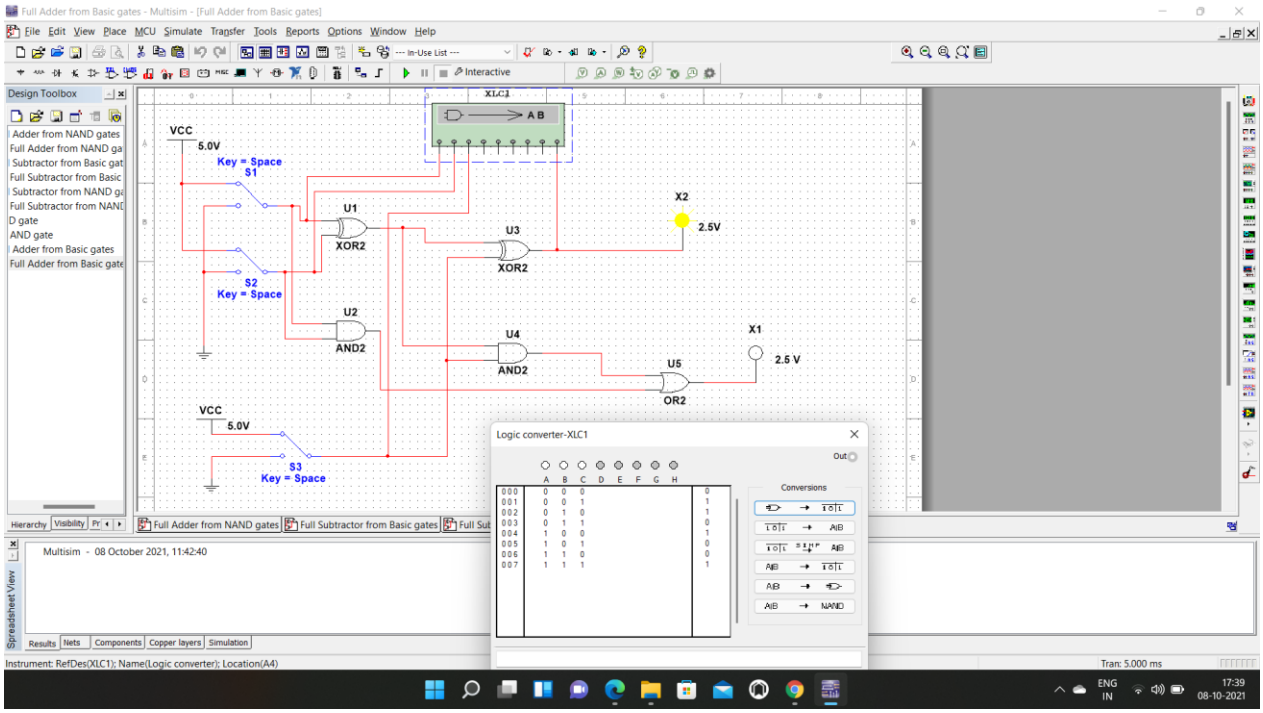
CARRY



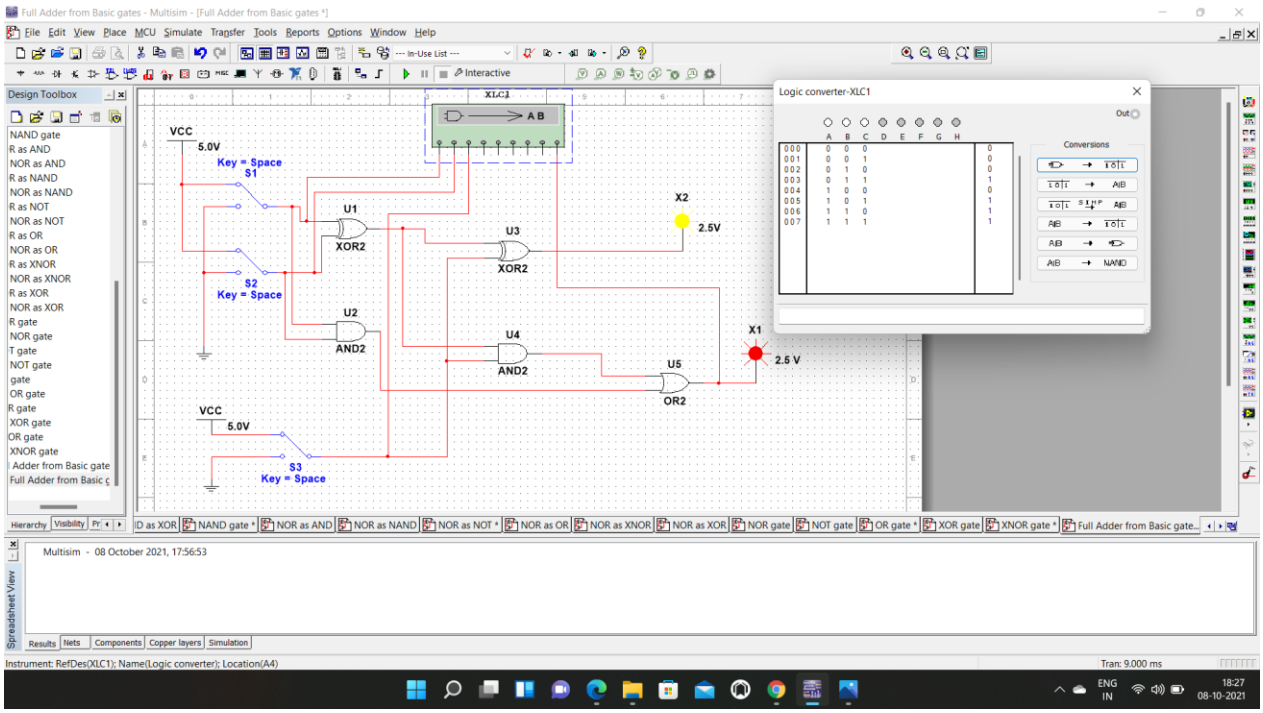
VERIFICATION OF FULL ADDER:

FULL ADDER USING BASIC GATES:

SUM

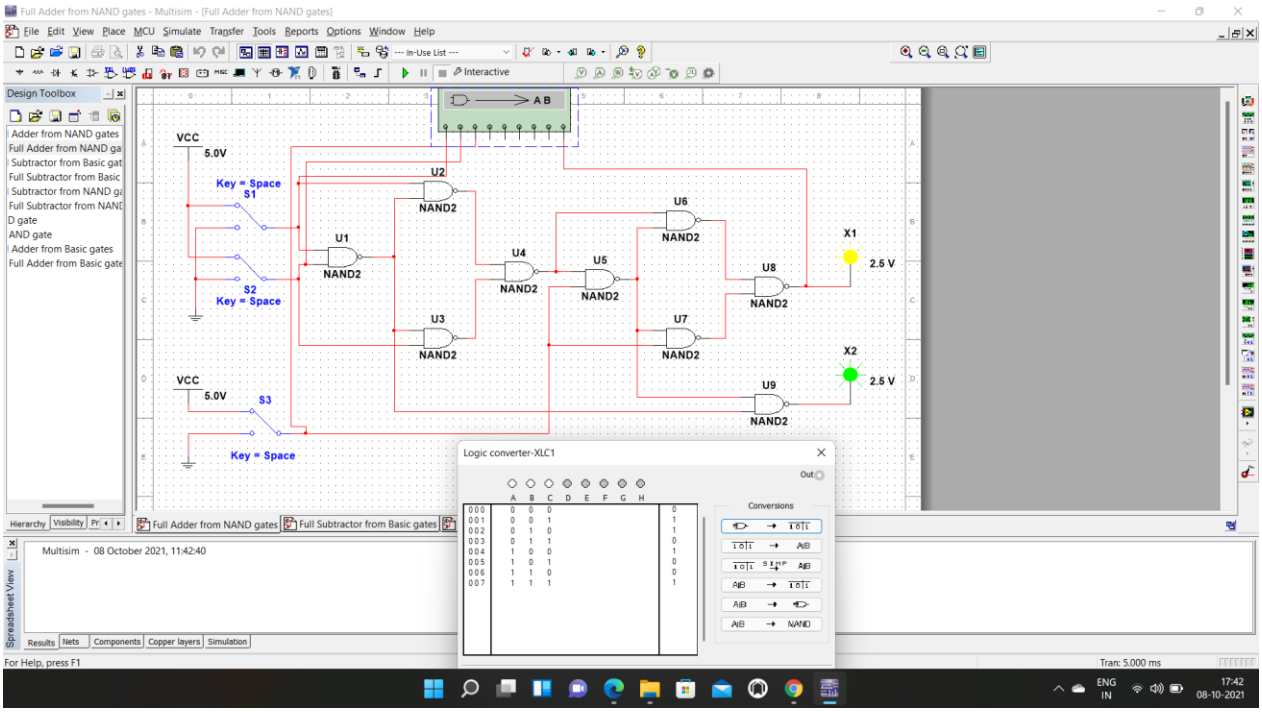


CARRY

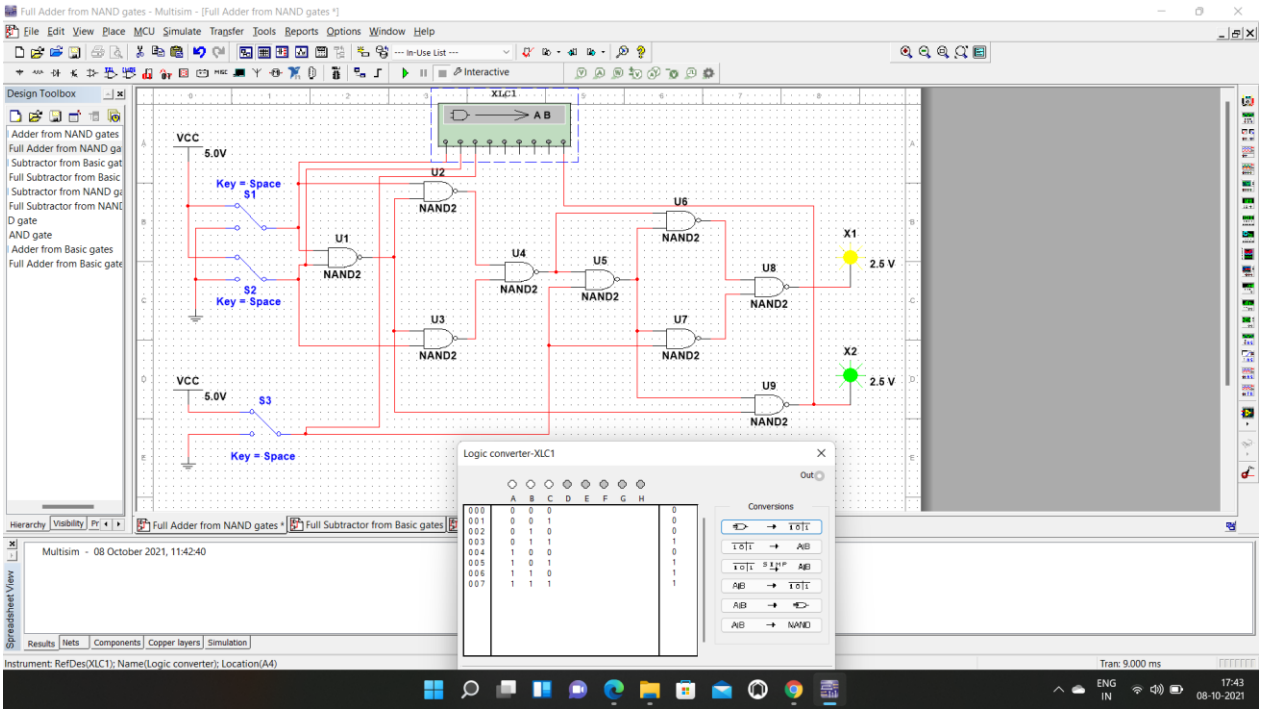


FULL ADDER USING NAND GATES:

SUM



CARRY



PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT:

Thus the half adder &full adder was designed and their truth table is verified.

PRECAUTIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off. • Never touch live and naked wires.