DIGITAL LOGIC DESIGN

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EXPERIMENT 8

EXPERIMENT – 8

AIM: -

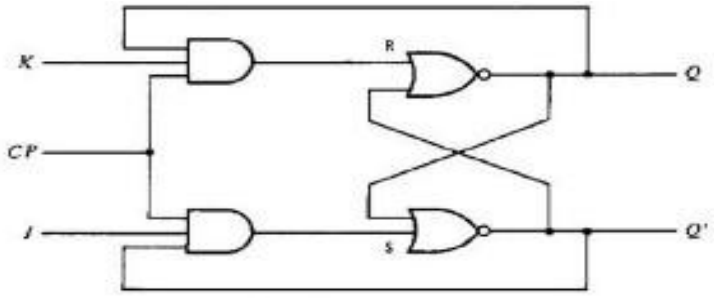
Verify the truth table of a J-K flip-flop (7476)

APPARATUS REQUIRED: -

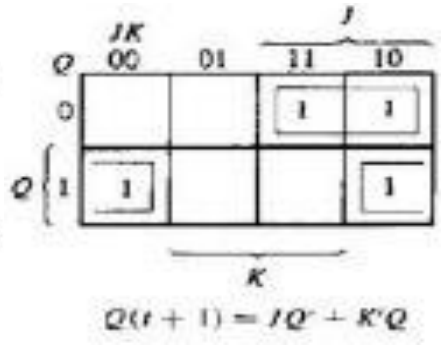
Logic trainer kit, Flip-flop ICs- 7476, wires.

THEORY:

The JK flip-flop is the modified version of SR flip-flop with no invalid state; i.e. the state J=K=1 is not forbidden. It works such that J serves as set input and K serves as reset. The only difference is that for the combination J=K=1 this flip-flop; now performs an action: it inverts its state.



(a) Logic diagram



Truth Table			
Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

The flip-flop is constructed in such a way that the output Q is ANDed with K and CP. This arrangement is made so that the flip-flop is cleared during a clock pulse only if Q was previously 1. Similarly, Q' is ANDed with J and CP, so that the flip-flop is cleared during a clock pulse only if Q' was previously 1.

When J = K = 0

When both J and K are 0, the clock pulse has no effect on the output and the output of the flip-flop is the same as its previous value. This is because when both the J and K are 0, the output of their respective AND gate becomes 0.

When J=0, K=1

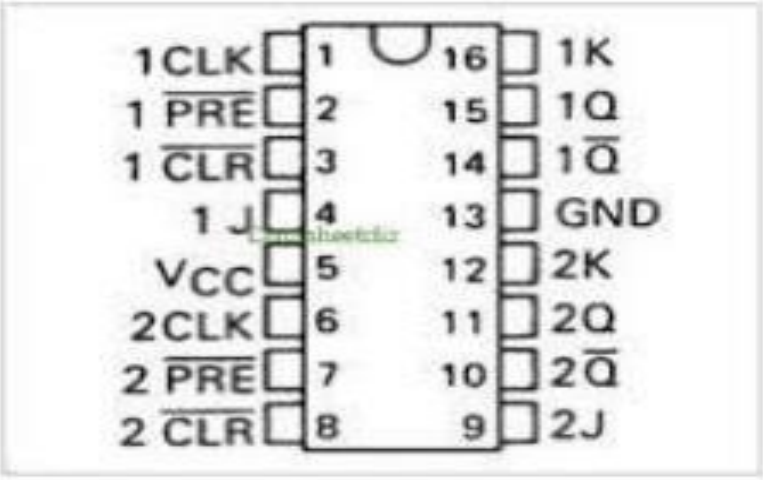
When J=0, the output of the AND gate corresponding to J becomes 0 (i.e.) S=0 and R=1. Therefore, Q' becomes 0. This condition will reset the flip-flop. This represents the RESET state of Flip-flop.

When J=1, K=0

In this case, the AND gate corresponding to K becomes 0(i.e.) S=1 and R=0. Therefore, Q becomes 0. This condition will set the Flip-flop. This represents the SET state of Flip-flop.

When J=K=1

Consider the condition of CP=1 and J=K=1. This will cause the output to complement again and again. This complement operation continues until the Clock pulse goes back to 0. Since this condition is undesirable, we have to find a way to eliminate this condition. This undesirable behavior can be eliminated by Edge triggering of JK flipflop or by using master slave JK Flip-flops.



Pin diagram of IC 7476

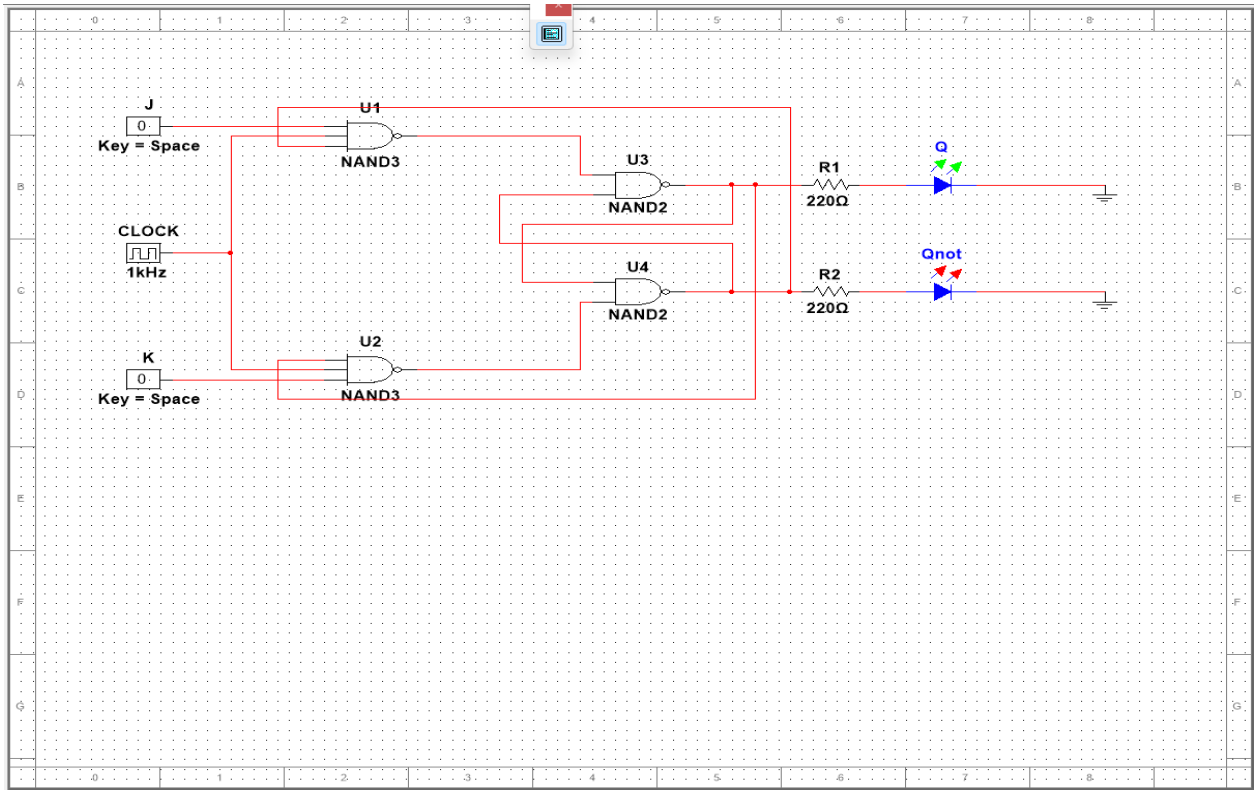
OBSERVATION TABLE:						
Inputs					Theoretical Outputs	Experimental Output
J	K	CLK	PRE	CLR	Q & Condition	Q & Condition
X	X	L	0	0		
X	X	L	0	1		
X	X	L	1	0		
X	X	L	1	1		
0	0	L	1	1		
0	1	L	1	1		
1	0	L	1	1		
1	1	L	1	1		

PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

VERIFICATION:



RESULT:

Thus the J-K Flip flop was designed and truth table is verified.

PRECAUTIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch live and naked wires.