DIGITAL LOGIC DESIGN

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EXPERIMENT 9

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AIM: -

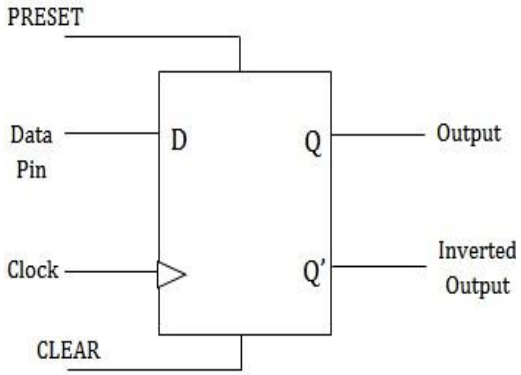
Verify the truth table of a D flip-flop (7474)

APPARATUS REQUIRED: -

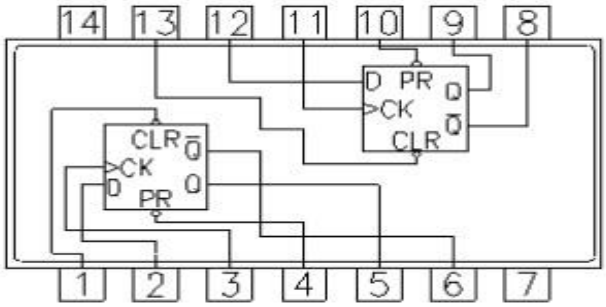
Logic trainer kit, Flip-flop ICs- 7474, wires.

THEORY:

D flip flop also called as delay flip flop where it can be used to introduce a delay in the digital circuit by changing the propagation delay of the flip flop. Here the input data bit at D will reflects at the output after a certain propagation delay.



Symbol: D Flip-flop



7474
Dual D Flip–Flop
with Preset and Clear

Truth Table of D Flip-Flop				Characteristic Table of D Flip-Flop		
Clock	**INPUT**	**OUTPUT**		**D**	**Q**	**Q'**
	D	**Q**	0	0	0	**0**
LOW	X	0	0	1	0	0
HIGH	0	0	1	0	1	1
HIGH	1	1	1	1	1	1

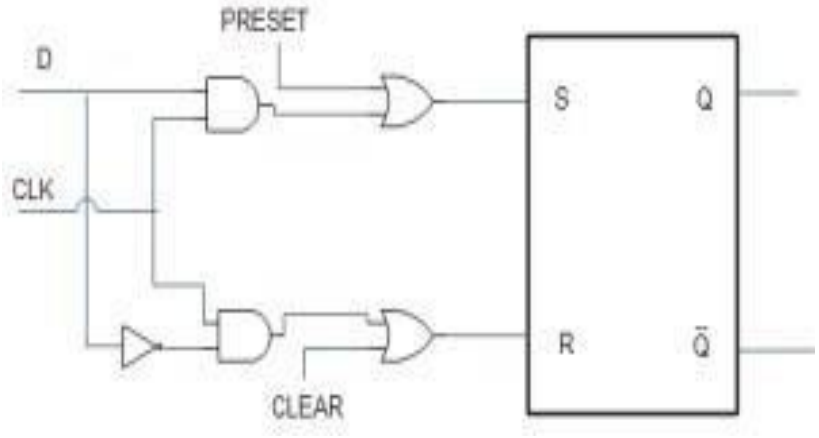
Characteristic Equation:

$$Q' = D\,Q' + D\,Q$$
$$Q' = D$$

D Flip Flop with PRESET and CLEAR

PRESET is the input to the D flip flop which sets the output data to High i.e. 1. and CLEAR is also an input which clears the output data or output state. A high PRESET forces Q to 1; a high CLEAR resets Q to 0. Figure shows clocked flip flop with PRESET and CLEAR inputs.

Clocked D Flip-Flop with PRESET and CLEAR

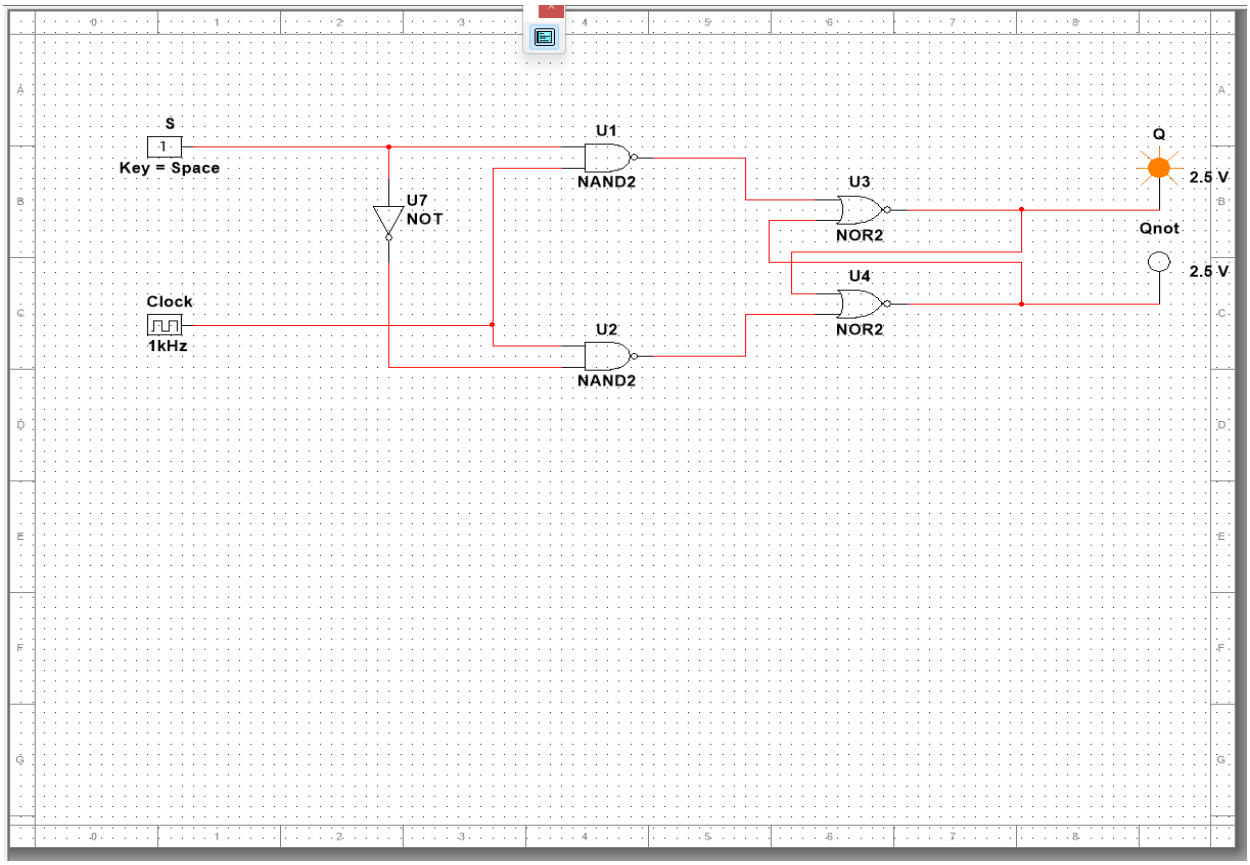


In the above circuit irrespective of the AND gates out, if the PRESET input is high the OR gate out directly sets the S input which makes Q to 1and in the same way if CLEAR input is high it resets the Q to 1.

PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

VERIFICATION:



RESULT:

Thus the D Flip flop was designed and their truth table is verified.

PRECATIONS:

- All connections should be made neat and tight.
- Digital lab kits and ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off.
- Never touch live and naked wires.