Curriculum Vitae (CV)

Umayia Mushtaq, **Guest Faculty**

Department of Electronics and Communication Engineering, Jamia Millia Islamia, (Central University) New Delhi 110025 Mob: +91 9682658300, umaiyamushtaq1247@gmail.com.

Research Interests:

Reliable circuit designs | Low-power circuit design using CMOS and FinFET technologies | Neuromorphic computing and brain-inspired circuit design | SRAM design for high-performance and energy-efficient memory architectures | In-memory computing for AI and edge applications

Teaching Experience:

Guest Faculty

Department of Electronics and Communication, [(JMI, New Delhi India)]

August 16, 2024 – Present

Courses taught at the undergraduate level:

- Embedded System Design
- Basics of Electronics and Communication.

Conducted lab sessions for:

- Electronic Devices and Circuits (EDC-I)
- Electronic Workshop
- Microwave Engineering Lab

- **Education and Qualifications**

School/College/University	Dates	Qualifications
Public Senior Secondary School Bijbehara	2009	10th Distinction with **86%**
Public Senior Secondary School Bijbehara	2011	12th Distinction with **88%**
IUST Awantipora j&K (State University)	2012-2016	B.Tech in Electronics and Communication Engineering with **90%**
Shri Mata Vaishno Devi University J&K (State University)	2017-2019	M.Tech in Electronics and Communication Engineering (VLSI) with **88%** **Award of Distinction for excelling in Academics, Co-curricular and Extracurricular Activities**
Jamia Millia Islamia New Delhi India (Central University)	Oct 2019-Feb 2025	PhD (Electronics and Communication Engineering)

- **Thesis Title**

M.Tech Thesis Title	Design of Low Power Circuits using FinFET
PhD. Thesis Title	Exploring Novel Techniques for Designing Energy-Efficient and Robust Nanoelectronic Circuits

- **Awards/Fellowships**

University/Research Award	Awards /Fellowship Name	Year
Reviewer Award	**IOP Trusted Reviewer**	2024
UGC NET Qualified	**Electronic Science**	2023
Best Paper Award at 6th International Conference on MICROELECTRONICS, ELECTROMAGNETICS AND TELECOMMUNICATIONS	For the paper titled "Design and Analysis of Energy Efficient Logic Gates Using INDEP Short Gate FinFETs at 10nm Technology Node"	2021
University Award (Shri Mata Vaishno Devi University J&K)	**Certificate of Distinction** for Excelling in Academics ,Co-Curricular and Extra Curricular Activities	2019
University Fellowship	**Student Merit Scholarship For top 3 position holders during M.Tech**	2017-2019
IIT Roorkee NPTEL	SILVER+ELITE in **CMOS Digital VLSI Design (Top 2%)**	2019
Essay writing competition Award under Swacch Bharat Summer internship at Shri Mata Vaishno Devi University J&K	3rd Position Award	2018

- **List of Publications**

JOURNAL PUBLICATIONS

1. **Umayia Mushtaq**, Akram, M.W., Prasad, D. and Islam, A., 2024. An energy and area-efficient spike frequency adaptable LIF neuron for spiking neural networks. **Computers and Electrical Engineering**, 119, p.109562.**(SCIE Listed, IF= 4.0)**

2. **Umayia Mushtaq**., Akram, M.W., Prasad, D., Islam, A, 2024. INDIDO: A novel low-power approach for domino logic circuits. **Physica Scripta**, 99(7), p.075914.**(SCIE Listed, IF= 2.9)**
3. **Umayia Mushtaq**, Md Waseem Akram, Dinesh Prasad, and Bal Chand Nagar. "LCINDEP: a novel technique for leakage reduction in FinFET based circuits." ***Semiconductor Science and Technology*** 38, no. 1 **(2022):** 015003. **(SCIE Listed, IF=1.9)**
4. **Umayia Mushtaq** and Vijay Kumar Sharma. "Design and analysis of INDEP FinFET SRAM cell at 7-nm technology." ***International journal of numerical Modelling: electronic networks, devices and fields*** 33, no. 5 **(2020):** e2730**. (SCIE Listed, IF=1.6)**
5. **Umayia Mushtaq** and Vijay Kumar Sharma. "Performance analysis for reliable nanoscaled FinFET logic circuits." ***Analog Integrated Circuits and Signal Processing*** 107, no. 3 **(2021**): 671-682. **(SCIE Listed, IF=1.4)**
6. **Umayia Mushtaq**., Akram, M.W., Prasad, D., Islam, A. and Nagar, B.C., **2024**. Impact of Variability on Novel Transistor Configurations in Adder Circuits at 7nm FinFET Technology. ***Journal of Circuits, Systems and Computers***. **(SCIE Listed, IF=1.2)**
7. **Umayia Mushtaq**, Md Akram, Dinesh Prasad, and Bal Chand Nagar. "A Novel Energy Efficient and Process Immune Schmitt Trigger Circuit Design Using FinFET Technology." **Indian Journal of Pure and Applied Physics. (2022) (SCIE Listed, IF=0.846)**
8. **Umayia Mushtaq**,, Md Waseem Akram and Dinesh Prasad. "Energy Efficient and Variability Immune Adder Circuits using Short Gate FinFET INDEP Technique at 10nm technology node**."** ***Australian Journal of Electrical and Electronics Engineering*** **(2022)**: 1-12. **(Scopus Indexed Taylor and Francis Journal)**

CONFERENCE PUBLICATIONS

1. **Umayia Mushtaq** and Vijay Kumar Sharma**."** Design of 6T FinFET SRAM cell at 7nm**"** **In** ***2019 International Conference on Communication and Electronics Systems*** *(ICCES)*, pp.104-108. **IEEE, 2019**
2. **Umayia Mushtaq**, Md Akram and Dinesh Prasad. **"**Design and Analysis of Energy-Efficient Logic Gates Using INDEP Short Gate FinFETs at 10 nm

Technology Node." **In *Advances in Micro-Electronics, Embedded Systems and IoT*, pp. 19-28. Springer, Singapore, 2022 (Best paper Award)**

3. **Umayia Mushtaq**, Md Waseem Akram and Dinesh Prasad**. "FinFET:** A Revolution in Nanometer Regime**."** ***Emerging Electronics and Automation****: Select Proceedings of E2A 2021*. **Singapore: Springer** Nature Singapore, 2022. 403-417.
4. **Umayia Mushtaq**, Md Akram and Dinesh Prasad and Bal Chand Nagar, 2022, December. A Novel D-Latch Design for Low-Power and Improved Immunity. In ***International Conference on Modeling, Simulation and Optimization (pp. 349-360). Singapore:*** **Springer Nature Singapore.**
5. Nazida Ansari**, Umayia Mushtaq,** Seema Erum and Md Waseem Akram. Design and Implementation of Multifunctional Logic Circuits Using SRAM Cells Utilizing In Memory Computing. ***Emerging Electronics and Automation****: Select Proceedings of E2A 2023*. **Singapore: Springer** Nature Singapore,2023

BOOK CHAPTERS

- **Umayia Mushtaq**, Md Akram and Dinesh Prasad. "Design and Analysis of Energy-Efficient Logic Gates Using INDEP Short Gate FinFETs at 10 nm Technology Node**."** **In *Advances in Micro-Electronics, Embedded Systems and IoT*, pp. 19-28. Springer, Singapore, 2022**
- **Umayia Mushtaq**, Md Waseem Akram and Dinesh Prasad**. "FinFET:** A Revolution in Nanometer Regime**."** ***Emerging Electronics and Automation****: Select Proceedings of E2A 2021*. **Singapore: Springer** Nature Singapore, 2022. 403-417.
- **Umayia Mushtaq**, Md Akram and Dinesh Prasad and Bal Chand Nagar, 2022, December. A Novel D-Latch Design for Low-Power and Improved Immunity. In International Conference on Modeling, Simulation and Optimization (pp. 349-360). Singapore: Springer Nature Singapore

ABSTRACT PUBLICATION

- **Umayia Mushtaq** , Vijay Kumar Sharma " Design of Low Power circuits using FinFET at 5th International Conference on Recent

Trends & Advancement in Engineering and Technology organized by Shri Mata Vaishno Devi University, Katra ,25-26 October,2018

- **Umayia Mushtaq** , Neeraj Tripati "MEMS Devices for Human Welfare and Upliftment: A critical Study" at 13th Session of Jammu and Kashmir Science Congress(JKSC-2018) organized by University of Kashmir in collaboration with the Jammu and Kashmir State Science, Technology, and Innovation Council,2nd-4th April 2018

Other Roles

Review Board Membership

Review Board Member
MC Engineering Themes
Reviewer Board Link

Scientific Committee Member
Annual International Congress on Electrical Engineering
March 6–7, 2025 | Oxford, United Kingdom / Online
Conference Link

Reviewer of International Journals:

- Scientific Reports (Springer Nature)
- Analog Integrated Circuits and Signal Processing (Springer)
- Physica Scripta (IOP Publishing)
- Journal of circuits systems and computers (World Scientific)
- Engineering Research Express(IOP Publishing)
- Australian Journal of Electrical and Electronics Engineering (Taylor and Francis)
- Journal of Autonomous Intelligence

Volunteer Roles

- 4th International Conference on Recent Trends and Advancements in Engineering And Technology organized by Shri Mata Vaishno Devi University Katra during 3-4 Nov,2017

NPTEL COURSES

- **Elite +silver** grade in NPTEL course organized **by IIT Roorkee** in **CMOS DIGITAL VLSI DESIGN** to be **among top 2%** in April 2019.
- **Elite** grade in NPTEL course organized by IIT Hyderabad in **Introduction to Semiconductor Devices** in Oct 2022

ATAL FDPs

- FDP on "**Neuronal Dynamics and Neuromorphic Computing"** from 08/12/2021 to 12/12/2021 **at Indian Institute of Technology Patna**.
- FDP on "**Reliability and Security of VLSI Circuits & Systems for IoT**" from 02/08/2021 to 06/08/2021 at **Indian Institute of Technology Jammu**.
- FDP on "**Devices And Circuits For Next-Generation Computing Architectures**" from 25/10/2021 to 29/10/2021 at Govind Ballabh Pant Institute of Engineering & Technology, Ghurdauri.

WORKSHOPS

- Indian Nanoelectronics Users' Programme - Idea to Innovation hands-on training of online TCAD – Circuit Simulation Workshop, dually organized by IIT Bombay and Synopsys during August 1-5, 2022.
- Workshop on VLSI to System Design: Silicon to End Application Approach organized by All India Council for Technical Education (AICTE), Arm Education and STMicroelectronics from 31st July to 4th August 2023.
- Microwind Workshop on "FinFET, Nano-Sheet Cell Design, Now& Road Ahead" An educational perspective by Dr. Etienne Sicard, organized by nidesigns Pvt. Ltd., Pune, from September 14-16, 2022.
- Microwind Workshop on "FinFET, Nano-Sheet Cell Design, Now& Road Ahead" An educational perspective by Dr. Etienne Sicard, organized by nidesigns Pvt. Ltd., Pune, from August 29-31, 2023.
- Workshop on Brain-inspired/Neuromorphic Computing for Responsible AI organized by Department of Electrical Engineering ,Indian Institute of Technology Patna from 20th-26th March 2023.

- One week short time course on Advanced Techniques for Next GEN Networks with focus on 5G, IOT and Aerially controlled HETNETS organized by School of Electronics and communication Engineering SMVDU Katra Jammu and Kashmir from 16th – 20th December 2018.
- Two week Refresher course on Introduction to MATLAB and Research Enhancement tools organized by School of Electronics and communication Engineering SMVDU Katra Jammu and Kashmir from 16th- 25th March 2018
- One Week Workshop on Modeling and Simulation in Ultra Low Power VLSI Design organized by School of Electronics and communication Engineering SMVDU Katra Jammu and Kashmir from 18th May-22nd May 2019.
- One Week National Workshop on Scientific Learning with Python organized by School of Electronics and communication Engineering SMVDU Katra Jammu and Kashmir from 25th -29th May 2019.

PROFESSIONAL SKILLS:

- CADENCE VIRTUOSO TOOL
- PSPICE, (EDA TOOLS)
- MICROWIND
- LTSPICE, MULTISIM
- SENTAURAS SYNOPSIS HSPICE
- CADFEKO,CST
- MATLAB, OPTISYSTEM, QUALNET