Curriculum Vitae (CV)

Dr. Sajad Ahmad Loan, Fellow IETE, Shastri Fellow, MIEEE,MIAENG UK
Professor
Department of Electronics and Communication Engineering, Jamia Millia Islamia, (Central University) New Delhi 110025
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Education and qualifications

School/College/University	Dates Attended	Qualifications gained.
National Institute of Tech. (NIT) Srinagar, Kashmir	1991-1995	B. E. Electronics Engineering. Class: Ist
Aligarh Muslim University (AMU) India	1998-2000	M.Tech. (VLSI) Class: Ist
Indian Institute of Technolog Kanpur (IITK)	**2005-2010**	**PhD in Elect. Engg (Nanoelectr-VLSI)**

M.Tech Thesis Title: Design, VHDL modelling and FPGA Implementation of an 8-bit processor

PhD. Thesis Title: Design and Simulation Studies of SELBOX MOSFET and Lateral Bipolar Junction Transistor (LBJT) on SOI with Selective or Modified Buried Oxide Structures

Work history

Dates	Name and address of employer & Position held
1996-97	Temporary job in J&K Electrical Engineering Department
2000 Nov-2001 Feb	Visiting faculty, Electronics Engineering Department, Jamia Millia Islamia (JMI) New Delhi-110025
2001-2007	Assistant Professor(GP:6000) Electronics Engineering Department, JMI New Delhi-110025
2007-2012	Assistant Professor (GP:7000) Electronics Engineering Department, JMI New Delhi-110025.
2012- 2015	Sr. Assistant Professor, (GP:8000) Electronics Engineering Department, JMI New Delhi-110025
2015-2018	Associate Professor, Electronics Engineering Department, JMI New Delhi-110025
September/ October 2017	**Visiting Associate Professor, University of Waterloo, Canada.**
15/2/2018---- CONTD.	**Professor, Electronics Engineering Department, JMI New Delhi-110025**
Sep /Nov 2018	**Visiting Professor, University of Waterloo, Canada.**

Awards and fellowships

S. NO	Name
1	JK State Board of School Education10th class school topper.
2	JK State Board of School Education12th class school topper.
3	QIP fellowship for PhD, MHRD Ministry (AICTE) New Delhi, INDIA (2005).
4	Nominated for Commonwealth (UK)(One in India) and Japanese Fellowship(2005).
5	**Best Student paper award in IEEE Int. Conf. on Semicon. Electr. (ICSE 2008), Malaysia**.
6	Erasmus Mundus (European Fellowship) fellowship (Not availed due to leave problem)
7	Nominated and represented IIT Kanpur in an International Collaborators Conference in Waseda University Japan (March 9-13, 2010)
8	Merit paper award in IAENG Int. Conf. on Electrical Engineering Hong Kong (Mar. 2014)

9	Visiting Professorship under VPP program, King Saud University, 2015
10	Nominated for Presidents Award for Innovation 2017, JMI New Delhi
11	Indo-Canadian Shastri Fellowship 2017 to work at the University of Waterloo, Canada.
12	Visiting Associate Professorship, University of Waterloo Canada 2017
13	Best paper award in IEEE IEMCON 2017 (3-5 October, 2017), University of British Colombia, Canada, 2017
14	Best paper award (Device modelling) in IEEE IMPACT 2017, AMU Aligarh 2017
15	Best paper award (Signal Processing) in IEEE IMPACT 2017, AMU Aligarh 2017
16	Best paper presentation award in IEEE-ICEEE-2018 Istanbul Turkey 2018.
17	Visiting Professorship, University of Waterloo Canada 2018
18	Fellow IETE 2019
19	Best paper award in IEEE ic-ETITE'20, VIT Vellore, India February 2020
20	DR. Sarvapalli Radhakrishnan (2nd President of India) Teacher/Researcher Excellence Award 2022
21	Visiting Professorship offered by Islamic University of Madinah-2022

Research interests

S. No.	Electronics/Electrical and Computer Engineering	
1	VLSI Design at Algorithmic and architecture level	Digital VLSI Design
2	Microprocessor /Microcontroller design and application	High Power Device designing
3	Computer architecture and Processor Designing	Nanoelectronics and Devices
4	Artificial Intelligence/ANN/Robotics/Drone technology	Power Electronics Devices
5	High level designing/ VHDL/Verilog//FPGA implementation	Emerging Devices
6	Low Power Chip Designing	
7	Fuzzy logic processor Designing.	CNT analog and digital circuits
8	Neromorphic Computing and chip designing	Memrister based designing
9	IOT, Design and development	Energy Harvesting IR and Solar
10	Analog Circuit Designing	GaN devices
11	Microelectronics	SOI based devices
12	Approximate circuit designing	Robotic Vision

Subjects taught at B.Tech/M.Tech/PhD levels (COMPUTER /Electronics/Electrical Engineering)

S. No.	Name	Computer/Electronics/Electrical	Level
1	**Computer architecture**	**ALL**	**BT**
2	**Microprocessors and Microcontrollers**	**All**	**BT**
3	**Digital Logic Designing**	**All**	**BT**
4	**Fuzzy logic**	**All**	**BT/MT**
4	**Embedded System**	**E/C**	**MT**
5	**VHDL programming**	**E/C**	**BT/MT/PhD**
6	**Digital Circuit Designing**	**All**	**BT**
7	**Analog Circuits I and II**	**All**	**BT**
8	**Basic Electronics**	**All**	**BT**
9	**Basic Communication Engineering**	**All**	**BT**
10	**Signals and systems**	**ALL**	**BT**
11	**Digital VLSI design**	**ALL**	**BT**
12	**VLSI fabrication**	**Electronics**	**BT**
13	**Low Power VLSI Designing**	**E/C**	**BT/MT/PhD**
14	**Control System Engineering**	**Electronics/Electrical**	**BT**
15	**EMFT**	**Electronics/Electrical**	**BT**
16	**Microwave Engineering**	**Electronics/Electrical**	**BT**
17	**Emerging electronics Devices**	**Electronics/Electrical**	**MT/PhD**
18	**Semiconductor devices and modelling**	**Electronics/Electrical**	**MT/PhD**
19	**Electronics Instrumentation**	**Electronics/Electrical**	**BT**
20	**Computer Networking**	**Electronics/Computer Engg**	**BT**

Research activity (PhD thesis guided :10, submitting soon/: 02; Undergoing:7)

Registration Date	PhD Scholars name and thesis title	Status
1: 2010	Asim M. Murshid (Iraq) : Low Power VLSI Design of Fuzzy Processors	**(Completed:2013)**
2: 2011	Nizamuddin : Design and simulation of CNTFET based analog circuits	**(Completed :2015)**
3: 2012	Faisal Bashir: Modelling and Simulation of SOI technology based Novel Nanoelectronics devices	**(Completed:2016)**
4: 2013	Sunil Kumar: Design and simulation of novel SOI based emerging devices for Nanoelectronics applications	**(Completed:2018)**
5: 2014	Sumit Verma: Design and simulation of high performance GaN based devices	(**Completed :2019**)
6: 2015	M. RizwanShiek; Design and simulation of Green Nanoelectronics	**Completed : 2021**
7: 2015	Ms Ashita Kumar: Design and Modelling of Energy Efficient Nanoelectronics Devices at Device and Circuit Levels	**Completed : 2021**
8: 2015	Mr.Ehtisham: Design and simulation of high performance emerging Nanoelectronics devices	**Completed : 2021**
9: 2015	Mr Haris: Design and simulation of III-V compound semiconductor based semiconductor devices	**Completed : 2021**
10: 2015	Mrs Seema Jogad; Design and simulation of CNT based digitally programmable circuits	**Completed 2022**
11: 2016	Hafsa Nigar: Design and simulation of SJ power devices	**(Submitting December 2022)**
12: 2017	Anam Kham: Design and simulation of energy efficient Tunnel FET **devices.**	**(Submitting December 2022)**
13: 2017	Suvarnima Mujamdar : Design and simulation of CNT based analog signal processing circuits	In process
14: 2019	Ajaz Ahmad Lodhi: Design and simulation of high performance Power semiconductor devices.	In process
15:2021	Mohd Saqib Akhoon: Design and development of DNN accelerators for Artificial Intelligence Applications (Universiti Sains Malaysia, USM)	In process **(Field supervisor)**
16: 2021	Neha Mubarak: Design and simulation of energy efficient Tunnel FET	In process
17:2021	Taranum Parveen :GNRFET based analog signal processing: Design and analysis	In process
18:2021	Azka Khanum: Energy efficient tunnel Field Effect transistors	
19: 2022	M. Faizan Khan: Design and simulation of nanoelectronics devices for spiking neural networks	New

Research activity (M.Tech. thesis guided:28, Guiding :5), B.Tech. projects: >50

Dates	M.Tech. Scholars name and thesis title	University
1: 2012	Ms.HafsaNigar: Simulation studies of overlap and underlap Silicon on nothing MOSFET	JMI New Delhi
2: 2013	Mr.MohdShafique: Design of CNT based high performance analog circuits.	JMI
3: 2013	Mr.Faizan A Khan : Design and simulation Tunnel FET devices	JMI
4: 2014	Mr.Affan Abbasi: VLSI design and FPGA implementation of Wavelet Transforms	KSU Saudi Arabia
5: 2014	Ms.Iram Malik: Design and simulation of nanoscaled TFET for nano-circuit realization.	JMI
6: 2014	Mr.Shariq Ali Asghar : Design and simulation of memrister based digital circuitry	JMI
7: 2015	Mr Zaid Shah: Design of GaN based devices	JMI
8: 2015	Ms Atifa Begum: Design of energy efficient TFET devices	JMI
9: 2017	M. Asif Bhat: Design and simulation of energy efficient TFET designing	JMI
10:2018	Amina Haroon: Design and simulation of high performance power devices	JMI

11:2018	Sadaf: Design and simulation of CNT based current conveyers	Alfalah Uni.
12:2919	Mehak Mir: Design and simulation of energy efficient Tunnel transistors	JMI
13:2019	Misbah Noor: Design and simulation of III-V group based devices	JMI
14:2919	Saima Hamid: CNT based high frequency rectification for energy harvesting.	JMI
15:2019	Zarak Bhat: Approximate Circuit Designing	JMI
15:2019	Mohd Saqib: Energy efficient nanoscaled SOI devices: design and simulation	Alfalah Uni.
17:2019	Majid Ahmad Bhat: CNT based analog Circuit Designing	Alfalah Uni.
18:2019	Syed Asrarul Haq: Architectural level designing of modified EYERISSS based on Rostationary algorithm: Design and FPGA implementation	JMI
19:2019	Aqsha Amin: VLSI architecture level designing of Neuromorphic algorithms and FPGA implementation	JMI
20:2020	Sabia Gul: Design and simulation of energy efficient TFET devices.	JMI
21:2021	Ankita: Design and simulation of CNT based fractional circuits	BITS Pilani
22:2021	Udit: Design and simulation of FinFET based fractional order circuits	BITS Pilani
23:2021	Basit Aalam: Design and simulation of high performance Neuromorphic computing circuits	JMI
24:2021	Mohammad Azam: Design and simulation of FinFET based Fractional order circuits	JMI
25:2021	Syed Ashad Ali: Design and simulation of Approximate Circuits	JMI
25:2021	Samreena Shahbat: Design and development of Neuromorphic computing circuitry	JMI
27:2021	Mehruk Shah: AI based object trafficking systems	JMI
28: 2021	Rakesh : Design, VHDL modelling and FPGA implementation of FFT and DFT	JMI
29:2022	Afreen Taygi: TFET based sensors, design and simulation	JMI
30:2022	Altaf Hussian: Design and simulation of multitechnology sensing devices	JMI
31:2022	Salim Wani: Design and simulation based fractional circuits	JMI
32:2022	Tahmina Andrabi: Solar cell designing and simulation.	JMI
33: 2033	Zeenath Firdos: Epileptic seizure prediction in brain tumour patients using artificial intelligence	JMI

Academic and administrative responsibilities.

1	Teaching and research at UG/PG/PhD level.
2	Coordinator Bachelor of Engineering, Electronics and Communication Engineering JMI ND
3	Coordinator Training and Placement, Electronics and Communication Engineering JMI ND
4	Student Advisor / Incharge Tour
5	Departmental Coordinator (2013-2016)
6	Assistant Superintendent of Examination
7	Identification officer in B.Tech/B.E. and NET Entrance examination
8	Expert faculty of INSPIRE, DST programme.
9	Expert UPSC New Delhi
10	PhD coordinator-2014-till date
11	CBCS departmental coordinator
12	Member, International Collaboration Committee, JMI New Delhi
13	Member Board of studies, AMU Polytechnic, AMU Aligarh-2018-2021
14	VC nominee for Departmental Research Committee (DRC) of the Department of Chemistry. Jamia Millia Islamia New Delhi-25
15	Convenor DRC, Department of Electronics and Communication Engineering, JMI New Delhi-110025
16	Member Patent Committee
17	Member BORS, IUST Kashmir.

National and international Collaboration

S. No	**Partner institute**
1	University of Waterloo Canada
2	Indian Institute of Technology Kanpur
3	Indian Institute of Technology Bombay under INUP program.

4	Aligarh Muslim University
5	King Saud University, Saudi Arabia
6	Jeddah University Saudi Arabia.
7	Jouf University Saudi Arabia.
8	NIT Srinagar
9	University of Kashmir
10	Ain Shams University in Cairo, Egypt
11	Taif University
12	University of Mascara, Algeria.

Countries visited for academic and research purposes//Lectures/Conference presentations

S. No/Year	Country	Purpose	Sponsor
1/2002	Manila	Participated in a Workshop on Advanced VLSI design and microprocessor lab.	ICTP Italy
2/2006	Pakistan	International Summer College on Physics and Contemporary needs, Islamabad Pakistan	ICTP Italy/Ministry of S and T Pakistan
3/2007	Italy	International Conference on Milankovitch Cycles, ICTP Italy 2007.	ICTP Italy
4/2008	Jeddah KSA	Presented a paper in ICON 2008 Jeddah KSA	KAU university KSA
5/2008	London UK	Presented a paper in WCE 2008 England	DST India/IIT K
5/2008	Malaysia	Presented a paper in IEEE ICSE 2008 Malaysia.	IIT Kanpur India
7/2009	Malaysia	Presented a paper in IEEE RSM 2009 Malaysia	IIT Kanpur India
8/2010	Japan	Presented a paper in Int. Collaborators Conference in Waseda University Japan	Waseda University Japan
9/2011	Riyadh KSA	Presented a paper in IEEE-SICEPC-2011	KACST KSA
10/2012	Riyadh KSA	Conducted a 2 days workshop on VLSI Designing	KSU Saudi Arabia
11/ 2015	Riyadh KSA	Delivered invited talk at the King Saud University	KSU Saudi Arabia
12/2016	San Francisco USA	Presented a paper in IEEE S3S conference	JMI ND/DST
13/2017	Canada	Visited the University of Waterloo as a visiting professor 18 September-8 October, 2017	SICI New Delhi
14/2017	**Bahrain**	Presented a paper in IEEE GCC Bahrain	
15/2018	Istanbul Turkey	Presented a paper in IEEE-ICEEE-2018	Jouf University, KSA
16/2018	Saudi Arabia	Delivered talks at the Umul Qura university Mecca and Taiba University Jeddah	
17/2018	Canada	University of Waterloo as a Visiting Professor (14Oct-25 Nov-2018), Presented a paper in University of British Colombia, Vancouver, Canada	University of Waterloo, Canada
18/2019	Madina KSA	Delivered a talk in the Taiba University, Madina	Jouf University-KSA
19/2019	Madina KSA	Delivered a talk in Islamic University of Madina	Jouf University KSA
20/2019	Egypt	Presented a Paper in ICM-2019 in Cairo Egypt	Jouf University KSA

Research projects (Completed/under process/submitted)

Role	Title	Sponsor	Cost
PI	Modernization of VLSI and Nanoelectronics Lab, JMI New Delhi (2013-2014) **(completed)**	AICTE, Govt of India	7 lacs INR
PI	Design and fabrication of SELBOX MOSFET **(completed) (2013-2014)**	INUP IIT Bombay/DST (Fully supported)	~5 lacs total expenditure
Consultant	An Advanced Application Specific IC Research Center, **(09-ELE-854-02)**	NPST/King Saud University. 2012-2014	2 Million SAR
Co-PI	Design and development of SCE efficient SOI based Nanoelectronics devices **(completed) (11-NAN2118-02) (2013-16)**	NPST/King Saud University. 2012-2014	2 Million SAR
Co-PI	Design and development of energy efficient and highly scalable SOI based tunnel-FET	NPST/King Saud University. 2014	2 Million SAR

	devices for nanoelectronics applications **(14-NAN- 2612-02)**	(Accepted---NOT started yet)	
PI	Modernization of Semiconductor Devices and Nanoelectronics Lab, JMI New Delhi (December 2016)	Submitted to AICTE, Govt. of India	20 lacs INR

Invited Lectures and Chairmanships at national or international/conference/ seminar etc

S. No	Title of Lecture/Invited talk Academic Session	Title of Conference / Seminar	Organizer
1	**Session Chair** WCE-2008	World Congress on Engineering	International Association of Engineers London
2	SCE suppression using PGP Tech.	International Collaborators Conference ICC 2010,	Waseda University Japan
3	PGP tech. for Nanoelectronics	Departmental Seminar	Electrical Engg, KAU Jeddah, KSA
4	Nanoelectronics	Workshop on Nano science Nov. 2011	Kashmir University
5	Nanoelectronics	Short term course on VLSI System Design 29th April, 2012 , VLSI group of Electrical Engineering Department, King Saud University, KSA	King Saud University, KSA
6	FPGAs	Short term course on VLSI System Design	-do-
7	High level designing"	Short term course on VLSI System Design	-do-
8	"Low power designing",	Short term course on VLSI System Design	-do-
9	Low power designing",	Short term course on VLSI System Design	-do-
10	"Nanoelectronics and VLSI",	INSPIRE at NIT Srinagar, 25/5/2012	DST and NIT Srinagar
13	Vacuum tube to Nanoelectronics paradigm shift	INSPIRE at NIT Srinagar	DST and NIT Srinagar
14	Multi functional Nanoelectronics Devices	Maharaja Agersen College of Technology, Delhi, 4-April-2019	
15	Design and development of Multifunctional nanoelectronics devices	International Conference on nanotechnology for better living-2019-NIT/SKUST Kashmir-7-4-2019	SKUST Kashmir
16	Multifunctional Nanoelectronics Devices: A novel way to enhance Moore's law	One week workshop by Computer Engineering Department, Islamic University Kashmir/2019	IUST Kashmir
17	Multifunctional Nanoelectronics Devices: A novel way to enhance Moore's law	Invited talk in a one week course of Emerging nanoelectronics devices/2019	NIT Srinagar Kashmir.
18	Multifunctional Nanoelectronics	Invited talk in an FDP at MANNU university Hydrabad/2018	MANNU Hydrabad

	Devices for IOT applications		
19	Nanoelectronics Devices and applications in Agriculture	Invited talk at SKUST Kashmir/2020	ONLINE
20	Multifunctional Nanoelectronics devices: A Novel Way to Enhance Moore's Law Life	Invited talk in NIT Srinagar Kashmir /2020	NIT Srinagar Kashmir.
21	Multifunctional Nanoelectronics devices: A Novel Way to Enhance Moore's Law Life	Invited talk at Hyderabad/27/9/2021	IEEE Hyderabad section
22	High performance devices for the efficient realization of IOT with applications in Agriculture	Expert Lecture in a Refresher course on computer science and information technology	Maulana Azad National Urdu University (MANUU), Hyderabad-India

International Journal Editorial Board Member

1	**Nanoelectronics and Optoelectronics Journal** : **American Scientific Publication** (**INTERNATIONAL EDITORIAL BOARD MEMBER**)
2	**Chip Design and Manufacturing Journal** : **Academic Publishing Pvt. Ltd Singapore** (**INTERNATIONAL EDITORIAL BOARD MEMBER**)
3	**Artificial Intelligence and Applications (AIA) Journal** : **Bon View Publications Singapore** (**INTERNATIONAL EDITORIAL BOARD MEMBER**)
4	**Frontiers in Electronics** : **Frontiers** (**ASSOCIATE EDITOR**)

Reviewer of the International Journals

S. No	Name of the journal
1	IEEE Transactions on Electron Devices
2	IEEE Electron Device Letters
3	IEEE Transactions on Nanotechnology
4	IEEE Journal of Electron Devices Society
5	IEEE Access
6	IET Electronics Letters
7	IET Circuits, Devices and Systems,
8	IOP Semiconductor Science and Technology
9	IOP Nanotechnology
10	Superlattice and Microstructures :Elsevier
11	Solid State Electronics: Elsevier
12	Journal of Computational Electronics: Springer
13	Silicon: Springer
14	International Journal of Numerical Modelling: Electronic Networks, Devices and Fields : Wiley
15	Scientific Reports : Nature
16	International Journal of Electronics: Taylor and Francis
17	Nanoelectronics and Optoelectronics
18	Microprocessor

19	Frequenz Journal

PhD theses evaluated/conducted final defence as External Examiner for different universities

S. No	PhD Scholar (Guide)	PhD thesis title	Department/Univer-sity/Year
1	Ms Usma (Prof. G. M. Bhat)	Performance evaluation and channel characterization of MIMO orthogonal FDM communication	Electronics and Instrumentation, University of Kashmir-India-2018
2	Yogendra Kumar (Prof. M. Hasan)	Design of Spintronic devices based Electronics Circuits	Electronics Engineering, AMU Aligarh-India-2018
3	Syed Ahmad (Prof. M. Hasan and Prof. Naushad Aalam)	Robust and low power memory circuit design using CMOS and beyond CMOS devices	Electronics Engineering, AMU Aligarh-India-2019
4	Ajay Kumar (Prof. S. Alam)	Multiband Antenna's for wireless applications	Electronics Engineering, AMU Aligarh-India-2019
5	Adil Tahir Shora (Dr. Farooq A Khanday)	Comprehensive analytical modelling and characterization of multigate nanoscaled devices	Electronics and Instrumentation, University of Kashmir-India-2020
6	Mohd Adil Raushan (Prof. Javed Sidiqqui)	Semiconductor device analysis of junctionless transistors	Electronics Engineering, AMU Aligarh-India-2021
7	Mohd Asif Dar (DR. Feroze Ahmad)	Optical millimetre wave generation using Mach-Zehnder Modulators	Electronics Engineering, IUST Kashmir
8	Sumina Sadiq (Dr. Shaikh Javed)	Design and development of energy efficient signal processing techniques for the future broadband wireless networks	Electronics and Instrumentation, University of Kashmir-India-2022

List of Publications (Total 153)

https://scholar.google.com/citations?user=XPD2_KkAAAAJ&hl=en

PATENTS GRANTED/FILED (10)

1. **Loan, Sajad A,** Qureshi, S. and Iyer, S.S.K.; An improved lateral bipolar junction transistor (BJT) on selective buried oxide (SELBOX) and a method for manufacturing the same", **Granted Indian Patent No. 300909, Sep. 2018**

2. **Loan, Sajad A.** and Kumar S.; A Novel Metal Source/Drain Schottky Device based Digital Circuit Designing, Indian Patent application no. (**2743/DEL/2015), Publication date:** 04/11/2016, Reply to FER : **08/06/2021 (About to be finally granted)**

3. **Loan, Sajad A.** and Kumar S; Patterned Gate electrode for implementing any Boolean equation and a method for implementing the same, Indian Patent application no. (**201711041136). Publication date: 24/05/2019, Reply to FER: 24-03-2022 (About to be finally granted)**

4. **Loan, Sajad A.** and Verma, S.; Polarization Engineered Enhancement Mode Iii-V Group Based Devices, Inventors, India.Patent application no. 201611018596; **Publication date: 09/02/2018, Reply to FER: 17/12/2021(About to be finally granted)**

5. **Loan, Sajad A.** and Ehteshamuddin, M.; Planner Junctionless transistor with buried metal layer. Inventors , , Indian Patent application no. (201811019576) . Publication date: 29/11/2019, **Reply to FER: 26/05/2021(About to be finally granted)**

6. **Loan, Sajad A. and** Nigar H.,; Selective buried double gate power MOSFET: A method of manufacturing the same, Inventors, Patent application No. 201911008499, Publication date: 11/09/2020, **Reply to FER: 05/11/2021 (About to be finally granted)**

7. **Loan, Sajad A.** and Shaikh, M. Rizwanuddin, Drain-Engineered TFET with Fully Suppressed Ambipolarity, A method of manufacturing the same, Patent application No. 201911008491, Publication date: 11/09/2020, **Reply to FER: 05/10/2021(About to be finally granted)**

8. **Loan, Sajad A.** and Verma, S; Polarization doped enhancement mode P-type GaN (PD-GaN) MOSFET, a method of manufacturing the same. Patent application 202111050241, **Filed on 02/11/2021**

9. **Loan, Sajad A,** and Nigar; H., A Uni-gate Vertical Power MOSFET With Record High Balliga's Figure-of-Merit, a method of manufacturing the same. Filing in a couple of days.

10. **Sajad A Loan**, Ajaz A. Lodhi, and A. Q. Ansari, Triple gate Power MOSFET, Filing in a couple of days.

BOOK CHAPTERS (5):

1. **Loan, Sajad A,**, Qureshi S.and.Iyer, S.S.K (2009), Investigation of a Multizone Drift Doping Based Lateral Bipolar Transistor on Buried Oxide Thick Step, Springer's Advances in Electrical Engineering and Computational Science, vol. 39, pp.23-32, ISBN: 978-90-481-2311-7
2. **Loan, Sajad A.,** Shabir, H., Bashir, F., , Nizammuddin, M. (2015), "Simulation Study of a Novel High Performance Oxide Engineered Schottky Collector Bipolar Transistor" Springer's Transactions on Engineering Technologies, vol. 1, pp. 253-262.
3. **Loan, Sajad A,,** Shabir, H., Bashir, F., , Nizammuddin, M. (2015), "Carbon nanotube based operational transconductance amplifiers, a simulation study" Springer's Transactions on Engineering Technologies, vol. 1, pp. 231-242.
4. **Loan, Sajad A,**, Shabir, H., Bashir, F., Nizammuddin, M, Abbasi, S. A. and Alamoud, A.R.M, (2015) , Charge plasma based bipolar junction transistor on silicon on insulator, Springer's Transactions on Engineering Technologies, vol. 1, pp. 219-229.
5. **Loan, Sajad A.** Carbon based nanoelectronics: a way forward: Technology and Youth, Institute of objective studies (IOS), New Delhi. In press, 2022.

SCI LISTED/ISI LISTED (WOS) JOURNAL PUBLICATIONS (68)

(a) IEEE Transactions, Journals and Letters (10)

1. **Loan, Sajad A,**, Qureshi, S and Iyer, S.S.K., (2010) A New Partial Ground Plane Based MOSFET on Selective Buried oxide, A 2D simulation study" **IEEE Transactions on Electron Devices**, Vol. 57, No. 3, pp.671-680; . **Q1**
2. Ashita, **Loan, Sajad A.,** Rafat, M.(2018) "A High Performance Inverted-C Tunnel Junction FET with source channel overlap pockets" **IEEE Transactions on Electron Devices**, vol. 65, no. 2, pp. 763 – 768,. **Q1**
3. Bashir, F., **Loan, Sajad A.,** Alharbi A.G.(2018) "Electrostatically doped DSL Schottky Barrier MOSFET on SOI for Low power Applications, **IEEE Journal of Electron Device Society**, vol. 6, no. 1, pp. 19-25**, Q1**
4. Bashir, F., **Loan, Sajad A.,** Alamoud, A.R.M**. (2015)** A High Performance Source Engineered Charge Plasma based Schottky MOSFET on SOI, **IEEE Transactions on Electron Devices, vol. 9. Q1**
5. Ehteshamuddin. M., **Loan, Sajad A,**, and Rafat M. (2018) "Planar Junctionless Silicon on Insulator Transistor with Buried Metal Layer" **IEEE Electron Device Letters**, Volume: 39, Issue: 6. **Q1**
6. Ehteshamuddin. M., **Loan, Sajad A,**, Alharbi, A.G.,(2018); Electrostatically-Doped Hetero-barrier Tunnel FET: Design And Investigation, **IEEE Access**, vol. 6, pp. 65376–383, Q1.
7. Ashita, **Loan, Sajad A.,** Rafat**,** M. (2018) Insights into the impact of pocket and source elevation in Vertical Gate Elevated Source Tunnel FET structure " **IEEE Transactions on Electron Devices**, vol. 66, no. 1, pp. 752-758**, Q1**
8. Syed, A. Hafiz, Iltesha, Ehteshamuddin, M., and **Loan, Sajad A., (2019)** Dielectrically-Modulated Source-Engineered Charge-Plasma Based Schottky-FET as a label-free Biosensor, **IEEE Transactions on Electron Devices**, pp. 1905-1910, volume: 66 , no. 4, **Q1**
9. Shaikh, M. Rizwan Uddin, and **Loan, Sajad A,** (2019) Drain-Engineered TFET with Fully Suppressed Ambipolarity for High Frequency Application, **IEEE Transactions on Electron Devices,** pp.1628-34, volume: 66 , Issue: 4, **Q1**
10. Ehteshamuddin. M., **Loan, Sajad A.,** Alamoud, A. R. M.,(2019) Abdulrahman**,** Investigating a Dual MOS-CAP Variant of Line-TFET With Improved Vertical Tunnelling incorporating FIQC Effect, **IEEE Transactions on Electron Devices,** vol. 66, no. 11, pp. 4638 - 4645; **Q1**

(a) IEE/IET publications (4)

11. Verma, S., **Loan, Sajad A.,** and Alamoud, A. R. M. (2018); "Hybrid AlGaN/GaN High Electron Mobility Transistor: Design and Simulation", IET Circuits, Devices and Systems, vol. 12, no. 1, pp.33–39, **Q3**

12. **Loan, Sajad A.,** Kumar Sunil, Alamoud, A. R. M. (2017); , High performance Engineered Gate Transistors based Compact Digital Circuits, IET Electronics Letters, vol. 53, no. 3, p. 138 – 140. **Q2**
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