Curriculum Vitae

Dr. Shams Ul Haq
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I am a dedicated and accomplished low-power nanoscale circuit design researcher, with expertise in VLSI, multi-valued logic, and SRAM design. I have defended my PhD on "Design and Analysis of Low Power and Reliable Nanoscale Circuits" and contributed significantly to the field through 14 SCI-listed journal publications, 3 Scopus-listed papers, multiple patents, and conference presentations. My ongoing research focuses on SRAM stability, radiation-hardened SRAM cells, and low-power ternary arithmetic circuits.
In addition to my research contributions, I have teaching experience as an Assistant Professor, delivering courses in analog and digital electronics, circuit design, control systems, and VLSI design. I have also conducted hands-on lab sessions in Verilog, signal processing, and computer architecture, helping students gain practical skills in hardware design and simulation tools. With teaching experience as an Assistant Professor and proficiency in industry-standard tools like HSPICE, Cadence, and Silvaco, I am committed to advancing research and education in electronics and VLSI design.

Education

- **PhD (Awarded on 29th October 2024):** Successfully defended my PhD thesis from the School of Electronics & Communication Engineering, SMVD University, Katra, Jammu & Kashmir, India with
- **Thesis title**: "Design and Analysis of Low Power and Reliable Nanoscale Circuits"
- **Master of Technology (M. Tech) in VLSI Design** (2015-2017) from the School of Electronics & Communication Engineering, SMVD University, Katra, Jammu & Kashmir, India
- **Bachelor of Technology (B. Tech)** (2011-2015)inElectronics and Communication Engineering from Kashmir University, Srinagar, Jammu & Kashmir, India
- Intermediate (2006-2008): in Mathematics, Physics, and Biology as major subjects from Presentation Convent, Srinagar, Jammu & Kashmir, India.
- 10th (2005-2006): Shah-I-Hamdan Memorial Institute, Shopian, Jammu & Kashmir, India

Professional Experience

- **Assistant Professor (Contractual) (May 2017 – April 2018)**: Department of Electronics and Communication Engineering: **Kashmir University**, Srinagar, Jammu & Kashmir, India.
- **Assistant professor (Contractual) (Aug 2024** till date**):** Department of Electronics and Communication Engineering: **Jamia Millia Islamia**, Jamia Nagar, New Delhi-110025

Courses Taught

- **Analog Electronics**
- **Circuits Analysis**
- **Digital Electronics**
- **Electronic Devices and Circuits**
- **Control systems**
- **CMOS design**
- **Computer Architecture**

Labs Conducted

- **Digital Electronics**
- **Analog Electronics**
- **Digital Signal Processing**
- **Computer Networks**
- **Verilog**
- **Computer Architecture**

Research Work

Ph.D. Work

My doctoral research titled "***Design and Analysis of Low Power and Reliable Nanoscale Circuits***" delves into the intricate design and analysis of low-power nanoscale digital logic circuits including both binary and Multivalued logic design, an emerging frontier in electronics and communication engineering. By exploring novel approaches, I have contributed to advancing the understanding of the potential applications and benefits of low-power nanoscale circuits. I filed two patents and published 14 SCI Listed, 3 Scopus papers, and 3 Conference papers. I have five papers under review.

Technical Proficiency

- **SPICE simulation**
- **Silvaco simulation**
- **Cadence tools/Mentor Graphics**
- **Layout design**
- **Post layout simulation**
- **Monte Carlo simulations**
- **Sub circuit design**

Awards Received

- **Qualified NTA-NET**
- **Qualified JKSET**
- **Received Best Paper Award in 6th International Conference on Emerging Technologies: Micro to Nano (*ETMN 2024*).**

Patents Filed

- Buffer-based single-ended ternary SRAM cell [**App. No. 202411057580**]
- Energy efficient 3:1 ternary Multiplexer [**App. No. 202411057579**]

Publications (Journals)

1. Energy-Efficient and high-Speed dynamic logic based 1-trit Multiplier in CNTFET technology (*International journal of Electronics and Communication*, vol:175, year 2024, page:155088, doi: 10.1016/J.AEUE.2023.155088.) Index: **SCIE**

2. Tri-state GNRFET-based fast and energy-efficient ternary multiplier (*International journal of Electronics and Communication*, Volume 177, year 2024, page 155239) Index: **SCIE**
3. Low power and robust ternary SRAM cell with improved noise margins in CNTFET technology (*Physica Scripta*) (https://doi.org/10.1088/1402-4896/ad451c) Index: **SCIE**.
4. Energy-efficient design of quaternary logic gates and arithmetic circuits using hybrid CNTFET-RRAM technology (DOI:10.1088/1402-4896/ad6194**)** Index: **SCIE**
5. Design and Analysis of a low-power and high-speed CNTFET based 8T SRAM cell (*Physica Scripta*, Vol: 99, Year: 2024, Page: 085237) Index: **SCIE**
6. Modified ON-OFF Logic Technique for Low Leakage CMOS Circuits (*Journal of Nanoelectronics and Optoelectronics*, American Scientific Publisher, Volume 13, Number 1, Page 55-67) Index: **SCIE**.
7. Review of Nanoscale FinFET devices for the Applications in Nano-regime (*Current Nanoscience journal* Volume 19, year 2023 page 1-12) Index: **SCIE.**
8. FinFET based Energy efficient approximate 4:2 compressor design (*Journal of circuits systems and computers*) (https://doi.org/10.1142/s0218126624502530) Index: **SCIE**
9. Improved Stability for Robust and Low Power SRAM Cell using FinFET Technology (*Journal of Circuits Systems and Comp*): https://doi.org/10.1142/S0218126624501068 Index: **SCIE**
10. Reliable and ultra-low power approach for designing of logic circuits (*Analog Integrated Circuits and Signal Processing*, year 2023) Index: **SCI**
11. An efficient design methodology for a tri-state multiplier circuit in carbon nanotube technology (*Physica Scripta*): Vol:100, year 2025, page: 015008, https://doi.org/10.1088/1402-4896/ad9646: Index: **SCI**
12. Robust logic design using SOI shorted-gate FinFETs (*Indian Journal of Pure and applied physics*, vol 61, year 2023, page 57-66,). Index: **SCIE**.
13. Ternary Encoder and Decoder Designs in RRAM and CNTFET Technologies (*e-Prime - Advances in Electrical Engineering, Electronics and Energy*, Year 2024, vol 7, https://doi.org/10.1016/j.prime.2023.100397) Index: **SCIE.**
14. Energy-efficient and Process Variation aware Buffer-based Ternary SRAM Cell (**Accepted**): (*Circuits systems and signal processing*) **(A)** Index: **SCIE**
15. An Approach for Low Power Circuit Design Using Low Threshold Transistors (*Journal of active and passive devices*, OLD City Publishing. Page 173-174) Index: **ESCI.**

16. Energy-efficient design of logic circuit using a leakage control configuration in FinFET technology (*Journal of Institution of Engineers*) (https://doi.org/10.1007/s40031-024-01026-x) Index: **Scopus**

Publications Under Consideration

17. Energy efficient and fast ternary full adder with applications to image blending (**Under Revision:(** *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*) Index: **SCIE**
18. Low-Power 7T SRAM cell with write Bitline-Free structure: **Under Revision**: (*IEEE Transactions on VLSI*): **SCIE**
19. A novel low-power and robust 9T SRAM cell with a built-in read assist mechanism for portable electronic devices: **Under Revision** (*International Journal of Electronics and Communication*): **SCIE**
20. Design-Analysis of a novel radiation-resistant self-recoverable SRAM cell (**Submitted**: Computer and Electrical Engineering) Index: **SCIE**
21. Design and analysis of CNTFET-based 3:1 Multiplexer using unbalanced Ternary logic (**Submitted**: Silicon) Index: **SCIE**
22. Design and Analysis of Energy Efficient ternary logical and arithmetic Circuits using CNTFET technology (**Submitted**: *Journal of supercomputing*) Index: **SCIE**
23. Design of a low complexity power efficient approximate ternary full adder in CNTFET technology (**In preparation**)

Publications (Conferences)

- Attended and presented a research paper titled Design-Analysis of CNTFET-based Energy Efficient Ternary Logic gate in 6^{th} *International Conference on Emerging Technologies: Micro to Nano ETMN 2024*
- Attended and presented a research paper titled 'Challenges in Low power VLSI design (IEEE explore)' in *5th International conference on Electronics, communication and Aerospace Technology* (ICECA-2021): **Scopus Indexed**

- Attended and presented a research paper titled CNTFET-based Multiplexer Unit using INDEP Method in *International Conference on Sustainable Computing and Smart Systems* (ICSCSS-2023): **Scopus Indexed.**
- Presented a research paper titled 'A Novel Energy Efficient CNTFET-RRAM based Ternary Logic Design' *3rd international conference in advancement in electronics and communication engineering (*AECE-2023): **Scopus Indexed.**
- Attended the *First International Conference on Modern materials for engineering and Research* (ICMMER 2022).
- Attended *3rd International Conference on Recent Trends and Advancements in Engineering and Technology* **(ICRTAET 2016).**

Workshops/ FDPs/Trainings

- Attended one-month online workshop on "**BSNL Certified Advance Vocational Telecom Training**" organized by **BRBAIT, Jabalpur**.
- Attended State Level one-week Residential Program on ("**Skill development in Electronics (Hardware, Software and Devices**") organized by school of E&C Engineering SMVDU Katra
- Attended three days' workshop on "**Sixth Sense Technology Workshop"** conducted by the Technophilia systems in association with Robotics and Computer Applications Institute of USA held at university of Kashmir.
- Attended one day workshop "**Promoting Innovations in Individuals Start-ups Micro Small and Medium Enterprises and Technopreneurship Promoting Program Sensitization**" conducted by university of Kashmir
- Attended **"T2B Robotics Workshop based on LEGO® MINDSTORMS® & NEXT9797 NEXT-G programming"** conducted by university of Kashmir

Research Profile IDs

Google Scholar: Shams Ul Haq-Google Scholar

Research Gate: Shams Ul Haq-ResearchGate

References

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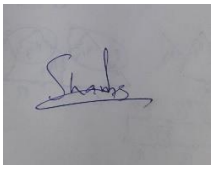
Declaration: I hereby declare that the particulars furnished herein by me are true to the best of my knowledge and belief**.**



Place: New Delhi **(Shams Ul Haq)**

Date: