# Assignment - 10

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In this assignment we extend our pipelined MIPS Simulator from the Assignment 9 to account for the fact that a the data memory follows a hierarchy to improve efficiency. Since, a memory unit closer to the processor has to small to increase it's performance there is a chance of the data we are accessing not being in the nearest level in that hierarchy. This situation is termed as a MISS and hence the pipeline needs to stalled for the processor to access the required data from the farther levels in the hierarchy. This increases the total clock cycle count.
There are two additional inputs in this assignment, x and N. x is the probability of a HIT and N is the number of clock cycles needed to access the memory in case of a MISS. We have implemented a function that returns 1 when there is a hit and 0 when there is a miss. Whenever there is a MISS we stall the later instructions for N-1 cycles.
We have indicated a HIT or a MISS after every load word instruction.
We have printed the active instruction at every stage of the pipeline by specifically stating the name of the stage and the exact instruction in that particular stage. In the end we have printed the register file, occupied memory elements, total number of clock cycles passed and the Instruction Per Cycle(IPC) as done in previous assignments.
Assumption(s) : $0.0<x<1.0$ (inclusive)

We have provided six test cases along with the submission and have explained test case 1 below,

```
lw $0 1024
lw $1 1025
lw $2 1026
sub $7 $0 $1
add $8 $1 $2
lw $3 1027
add $9 $2 $3
sw $7 1031
sw $9 1032
exit
```

We have tested the above test cases for 3 different values of x (keeping N = 3),
For x = 0.35, Total Clock Cycle Count = 21 and IPC = 0.428571
For x = 0.65, Total Clock Cycle Count = 19 and IPC = 0.473684
For x = 0.95, Total Clock Cycle Count = 13 and IPC = 0.692308

From the above output, we can see that as the probability of a HIT increases the number of clock cycles decreases which is completely coherent with our logic as there would be no stall is we have all hits.

We are also attaching the screenshot of outputs of all the test cases in the submission folder for reference.