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DETAILED LECTURE NOTES

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Unit 2:- Programming the Basic Computer

1. Introduction
2. M/C language
3. Assembly language
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5. Program loops
6. Programming Arithmetic & logic Operations
7. Subroutines
8. I-O Programming
9. Micro Programmed Control: Control Memory
Address sequencing
Micro program Example
Design of control Unit

Computer → hardware & physical Components
Computer → software & Program

- Program written by user independent of hardware

Machine Language :-

- Program is a list of instructions or statement for directing the comp. to perform a required data-processing task.
 - Programs are translated into binary representation.
- (1) Binary code:-
(2) Octal or hexadecimal code
(3) Symbolic code (letter, numerals, special char)
(4) High-level programming language
- M/C Language program is a binary program.
- Book
15. Octal 25 instruction
17. memory
18. register

Assembly Language :-

- A programming language is defined by a set of rules.
- Basic unit of an assembly lang. program is a line of code.

Rules of Language :-

AL arranged in 3 columns called fields

1. Label field : empty or symbolic address
2. Instruction field : M/C instruction or pseudoinstruction
3. Comment field : empty or include comment.



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Instruction field in AL

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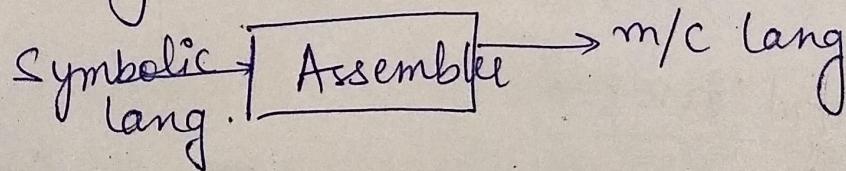
ADD OPR
ADD PTR 1

- ① Memory-reference instr. (MRI)
- ② Reg - Reference or I/P - O/P Instruction (non-MRI)
- ③ pseudo instruction with or without an operand.

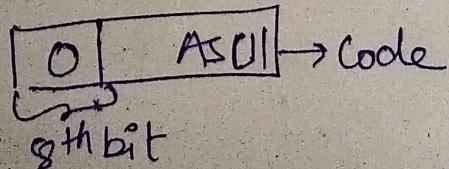
- first program is written in assembly language and converted into hexadecimal code

The Assembler: →

An assembler is a program that accepts a symbolic language program and produces its binary m/c lang equivalent.



- user type symbolic program on a System, each char is represented by 8-bit



- CR is used to produce the return key

e.g. → PL3, LD A SUB I → if I missing di.
if I missing di. → in-direct add.

- Line of code stored in consecutive memory location

1 PL
2 3,
3 LD
4 A Space
5 S U
6 B Space
7 I CR

This code stored at 7
location

if comment is // there
neglect the comment

- Assembler have two-pass

- o In first pass:-

- Read/Scan symbolic program twice.

- In 1st scan - convert symbols into binary value.

- 2nd scan convert into binary translation.

- Track memory with the help of LC (location counter)
- ORG pseudo-instruction initialize the location counter / if ORG missing LC=0

- Second Pass :-

- M/C instructions are translated during the second pass by means of table-lookup procedures.
- Assembler uses four table for this
 - (1) Pseudo-instruction table → used for subrou
 - (2) MRI table - Memory Ref. Inst. → HEX
 - (3) Non-MRI table - Reg. Ref. & I/O instru
 - (4) Address symbol table

Program Loops :-

- A program loop is a sequence of instructions that are executed many times, each time with a different set of data.

eg:-

```
int i, sum = 0, a[100];
for (i=1; i<=100; i++)
{
    sum = sum + a[i];
}
```

So, this program is converted into symbolic program and assembler work on it.

Programming Arithmetic & Logic Operations :-

- System have hundreds of instructions to perform operations, but few systems have basic operations to perform.
- Operations that are implemented in a computer with one m/c instruction are said to be implemented by hardware.

- Operations implemented by a set of instruction that constitute a program are said to be implemented by S/W.
- H/W implementation more costly (due to additional circuits)
- S/W implementation result in long programs both in no. of instructions and in execution time.

X holds multiplicand
 Y holds multiplier
 P forms product

$$\begin{array}{r}
 0000\ 1111 \\
 0000\ 1011 \\
 \hline
 0000\ 1111 \\
 0001\ 1110 \\
 0000\ 0000 \\
 0111\ 1000 \\
 \hline
 1010\ 0101
 \end{array}$$

Double-precision Addition:-

- When 2 16-bit unsigned no. are multiplied the result is 32-bit product that must be stored in 2 memory words.
- A no. stored in two memory words is said to have double precision.
- When a partial product is computed, it is necessary that a double-precision no. be added to the shifted multiplicand, which is also a double precision no.



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- 2 16-bit no's are stored as follows

1st no in AL & AH
low high

2nd no in BL & BH
low high

- 2 low (AL+BL) order portions are added and carry transferred into L.
- AC is cleared and bit in L is circulated into LSB of AC
- Two high order portions are added and carry also and stored in CL and CH

Logic Operations :-

- 3 M/C instructions to perform logic operations

AND

CMA — complement of A

CLA — carry look ahead Adder

CLA — logic

OR is not in M/C instruction

No perform OR do this

LDA A

CMA

STA TMP

LDA B

CMA

AND TMP

— Load first operand A

— complement of A

— store in Temp location

Load B

complement of B

AND with A to get A \wedge B

Shift Operations:-

- Circular shift op. are basic m/c instructions
- Two more shift are there → logic CLE, CIR
→ Arithmetic CLE
+ CIL

Subroutines :-

- Set of common instructions that can be used in a program many times is called a subroutine.
- It is used in main program. A branch is executed to the beginning of subroutine. After the subroutine, branch is back to main program.
- It's consist of self contained sequence of instructions that carries out a given task.
- Branch can be made to the subroutine from any part of the main program.
- In Computer, BSA (branch & save return add) is the link b/w the main program & a subroutine.
- The procedure for branching to a subroutine and returning to the main program is referred to as a subroutine linkages.
- BUN instruction is used for branch unconditionally.



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Input - Output Programming

- The symbols in which program is defined as string of characters and each char is assigned an 8-bit code, so that it can be stored in computer memory.
- Binary-coded character enters the computer when an INP instruction is executed.
- Binary-coded character is transferred to the O/P device when OUT instruction is executed.
- SKI instruction check input flag to see char. is available for transfer.
if flag = 1, next instruction skipped
else flag = 0, next instruction executed in sequence

eg: Input char:-

CIF

SKI

— check input flag

BNN

CIF

— flag = 0 branch to check

INP

— flag = 1, input char again

OUT

— print char

STA CHR

— store char

CHR

HLT

— / store char here

Output char:-

LDA CHR — Load char in A-C
COF SKO — I check o/p flag
BUN COF — I flag = 0, branch to check
OUT — if flag = 1, O/P char again
HLT
CHR HEX 0057 I Character is "W"



Assignment Questions:-

- ① Describe the Input - Output Programming with examples.
- ② Explain Subroutines.
- ③ Explain Assemblers.
- ④ Explain direct & indirect ^{register} addressing mode with suitable examples.
- ⑤ Explain arithmetic micro-operations in register transfer language.
- ⑥ Write the difference b/w Hardwired CV and Micro programmed CV.



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eg: of Assembly program

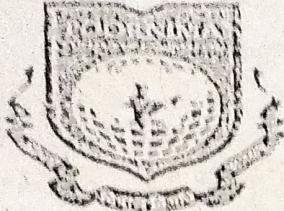
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Subtract Two numbers

ORG	100	Origin of prog. 100
LDA	SUB	Load Subtrahend to AC
CMA		Complement AC
INC		Increment AC
ADD	MIN	Add minuend to AC
STA	DIF	Store diff
HLT		Halt computer
MIN,	DEC 83	Minuend
SUB	DEC -23	Subtrahend
DIF	Hex 0	Diff stored
	END	End of symbolic program

Program Loop Example:- (Add 100 no.s)

1.	ORG	100	/ origin 100
2.	LDA	ADS	/ load 1 st operands
3.	STA	PTR	/ store in Pointer
4.	LDA	NBR	/ load minus 100
5.	STA	CTR	/ clear AC Store in counter
6.	CLA		/ clear AC operand
7.	LOP	ADD PTR L	/ Add L to AC
8.	ISZ	PTR	/ increment pointer
9.	ISZ	CTR	/ increment counter
10.	BUN	LOP	/ Repeat loop again
11.	STA	SUM	/ store sum
12.	HLT		/ Halt
13.	ADS,	HEX <u>150</u>	/ first add of operands
14.	PTR,	HEX 0	/ loc for pointer
15.	NBR,	DEC -100	/ counter value
16.	CTR,	HEX 0	/ counter after value
17.	SUM,	HEX 0	/ sum is stored
18.		ORG 150	/ origin of operand
19.		DEC 75	/ first operand
:			
118		DEC 23	/ last operand
119		END	/ end of symbolic program



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(2)

Arithmetic & Logic Op:-

Multiply Two Positive
No.

ORG, 100

LOP,	CLE	Clear E
	LDA Y	Load multiplier ^{in AC}
	CIR	Transfer multiplier bit to E
	STA Y	stored shifted multiplicand
	SZE	Check if bit is zero
bit is one go to ONE bit is zero go to ZRO	BUN ONE	Bit is zero: go to ZRO
	BUN ZRO	Load multiplicand
ONE,	LDA X	
	ADD P	— Add to partial product
	STA P	— store partial product
	CLE	— clear E
ZRO,	LDA X	— Load multiplicand
	CIL	— Shift left
	STA X	— store shifted multiplicand
	ISZ CTR	— Increment counter
	BUN LOP	— Counter not zero, Repeat loop
	HLT	— Counter is zero; halt
CTR,	DEC -8	— This loc — counter
X,	HEX 000F	— Multiplicand stored here
Y,	HEX 000B	← Multiplier stored here
P,	HEX 0	— product formed here
	END	

Use of Subroutines ! -

ORG 100

100 LDA X — Load X

101 BSA SH4 — Branch to subroutine

102 STA X — Store shifted no.^{time}

103 LDA Y — Load Y

104 BSA SH4 — Branch to subtraction

105 STA Y — Store shifted no.

106 HLT

107 X HEX 1234

108 Y HEX 4321

109 SH4 , HEX 0 | Subroutine to shift left
 | Store return add here 4 times

10A CIL | Circulate left once

10B CIL

10C CIL

10D CIL | Circulate left fourth time

10E AND MSK | Set AC(13-16) to zero

10F BUN SH4 I — Return to main program

110 MSK, HEX FFF0 | Mask operand

END



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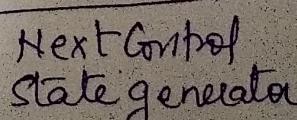
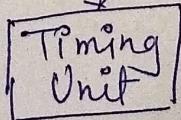
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Microprogrammed Control

Function of CU in DC is to initiate
Control Memory → Seq. of micro-op.

- To execute an instruction, CU generate the required control signal in the proper sequence.
- There are 2 approaches for generating control signals
 - ① Hardwired Control Unit:- When signals are generated by h/w using conventional logic
 - It is a structure of making control signals using finite state Machine (FSM) that changes from one state to another in every clock cycle depending on the contents of IR, condition codes & external inputs.
 - The final circuit is generated by physically linking the components including gates, flip-flops and drivers are known as Hardwired controllers.
 - It is faster than Micro-programmed

Regular signal
from quartz generator



Flags & Variables

control
opcode Add field

instruction
decoder

Control Signal
Generation matrix

Control
Signals
for
other
Computers

External
Signals

- RISC Architecture is based on the Hard control units.

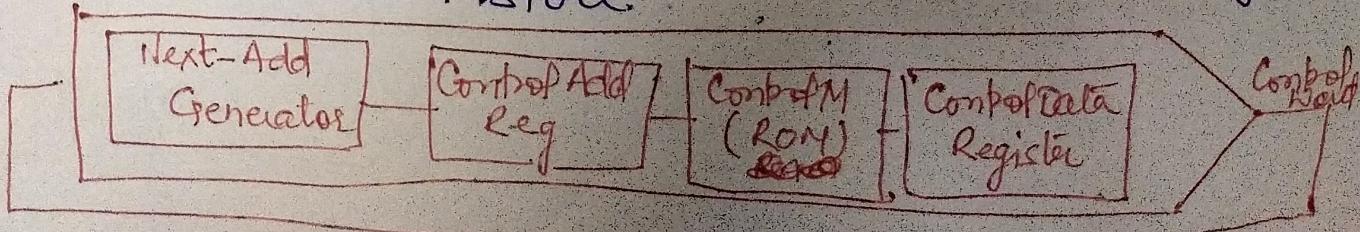
② Micro programmed Control Unit: →

- A control unit whose binary control values are saved as word in memory is called a microprogrammed control unit.
- Control signals are generated by a program that is similar to m/c lang programs.
- The micro-pro Memory add of the control unit denotes the add off micro-instruction.
- The microinstruction has a control word.

Important Term in micro-programmed CU

- ① Control Word - Word individual bit represent various control signals
(CW)
- ② Micro routine - Seq. of CW to control Seq of a m/c instruction constitutes MR.
(MR)
- ③ Micro Instruction: - Individual CW in MR is MI
- ④ Micro-program Sequence of MI is called MP,
(MP) stored in ROM or RAM
- ⑤ Control Store/M

MR for all instructions in Inst Set of a comp are stored in a special memory called Control store.





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Hardwired Control Unit

- Not applicable to change the structure and instruction set once it is developed.
- Design complex
- Architecture and Inst. are not specified
- Quick
- Processor to create signals executed in right seq.
- Operate through flip-flop drums, seq. circuit.

Microprogrammed Unit

- Applicable to make changes in microprogram saved in control memory.
- Design simplified.
- Arch. & Inst. are specified.
- Moderate
- Microseq from which Inst. are decoded and executed.
- Control through ALU, registers, buses, IR.

Address Sequencing

- MicroInst. are stored in control memory in groups, each group specifying a routine.
- So it follows following steps:
 - ① Initial add $\xrightarrow{\text{loaded}}$ Control Add Reg (CAR) when power on.
 - ② It is add. of first micro-inst. that activates the instruction fetch routine.
 - ③ CAR increment through micro inst.
 - ④ CM goes through routine and find the add of operand.
 - ⑤ Now add is available in Memory Add Reg.
 - ⑥ Generate micro-operations and execute inst fetched from M.
 - ⑦ Mapped b/w inst code & control memory.

So we can say that basically these 7 steps take place.

- ① Increment of the Control Add Reg.
- ② Unconditional branch or conditional branch, depending on status bit conditions.
- ③ A mapping process from bits of Inst to an add for CM.
- ④ A facility for subroutine call and return.

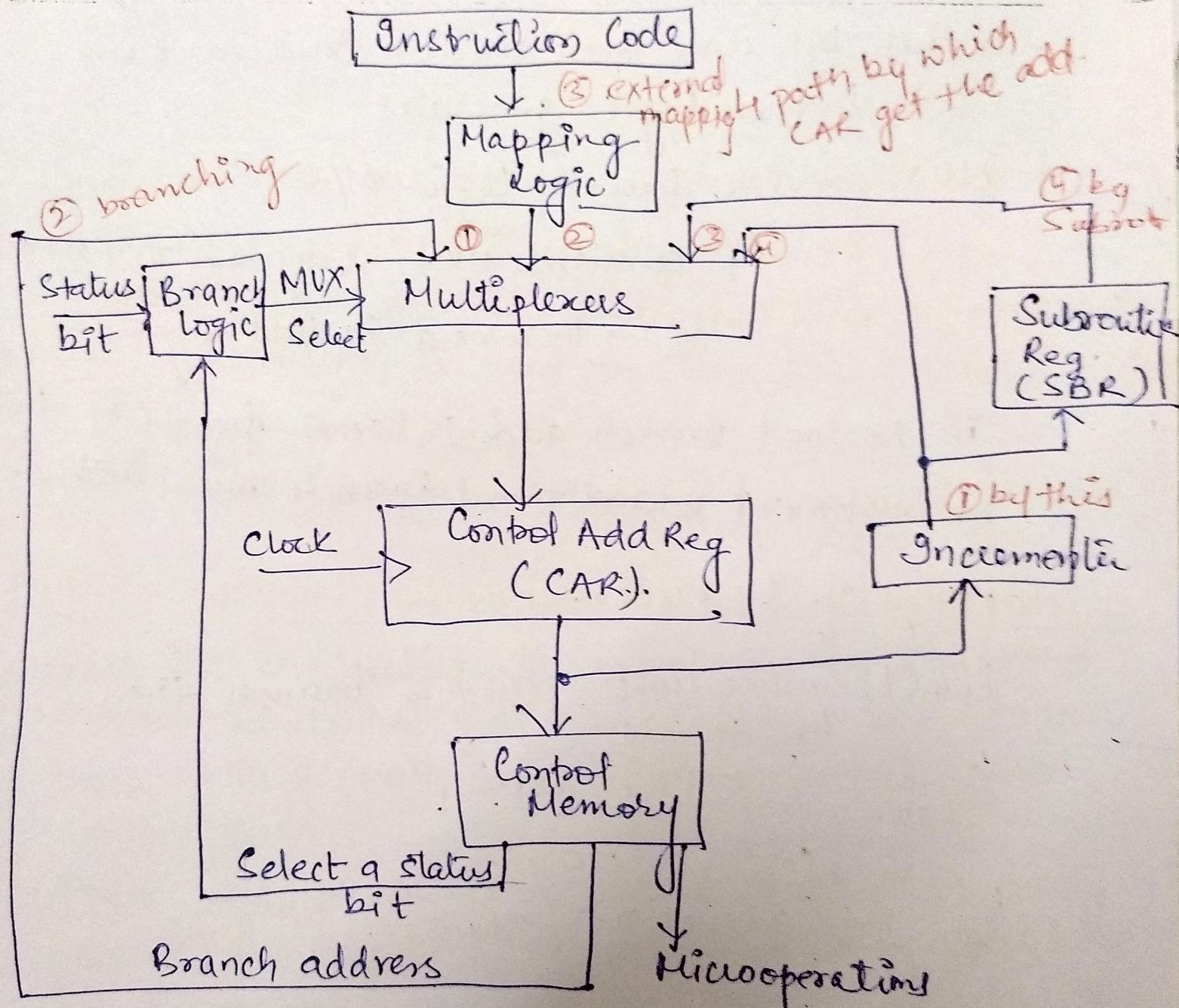


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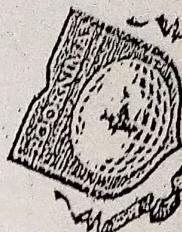
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- In this diagram micro instructions is used to contain a set of bits in CM.
- with the help of Micro instr. we able to start micro-operations in comp. Reg.

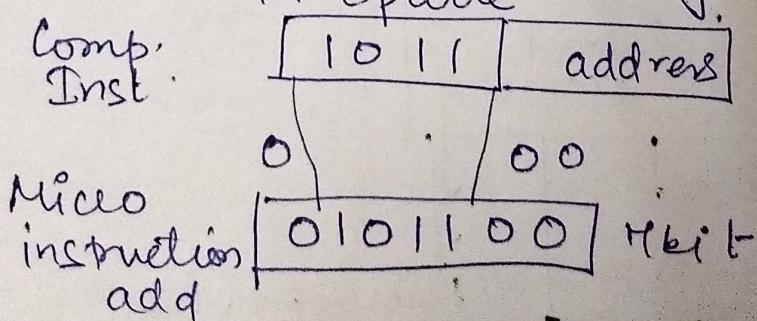
① Conditional Branching:-



- In diagram branch logic used to provide decision making capabilities in CU.
- Special bits (status condition) provide parametric info such as mode bit, sign bit, carry-out, input & output status.
- If these bits come with microinstruction then branch logic generates.
- MUX provide branch logic H/W
 - if condition met \rightarrow branch to initial add
 - else \rightarrow increment in Add. Reg.
- if we load branch add in CAR from CM then we implement unconditional branch micro instn.

② Mapping of Instructions:-

If in CM micro-inst specify a branch then



With the help of mapping 4-bit Opcode convert into 7-bit micro instruction add for CM.

- opcode - Mapped with memory using ROM or PLD (Programmable logic device) and

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With the help of CAR come to CM.

Subroutine: →

- Subroutines are programs that are used to accomplish a task by other routines.
- Subroutine use the common section of microcode.
- Register file is used to store the address for subroutines.
- Register files are structured by stack.

Microprogram Example: →

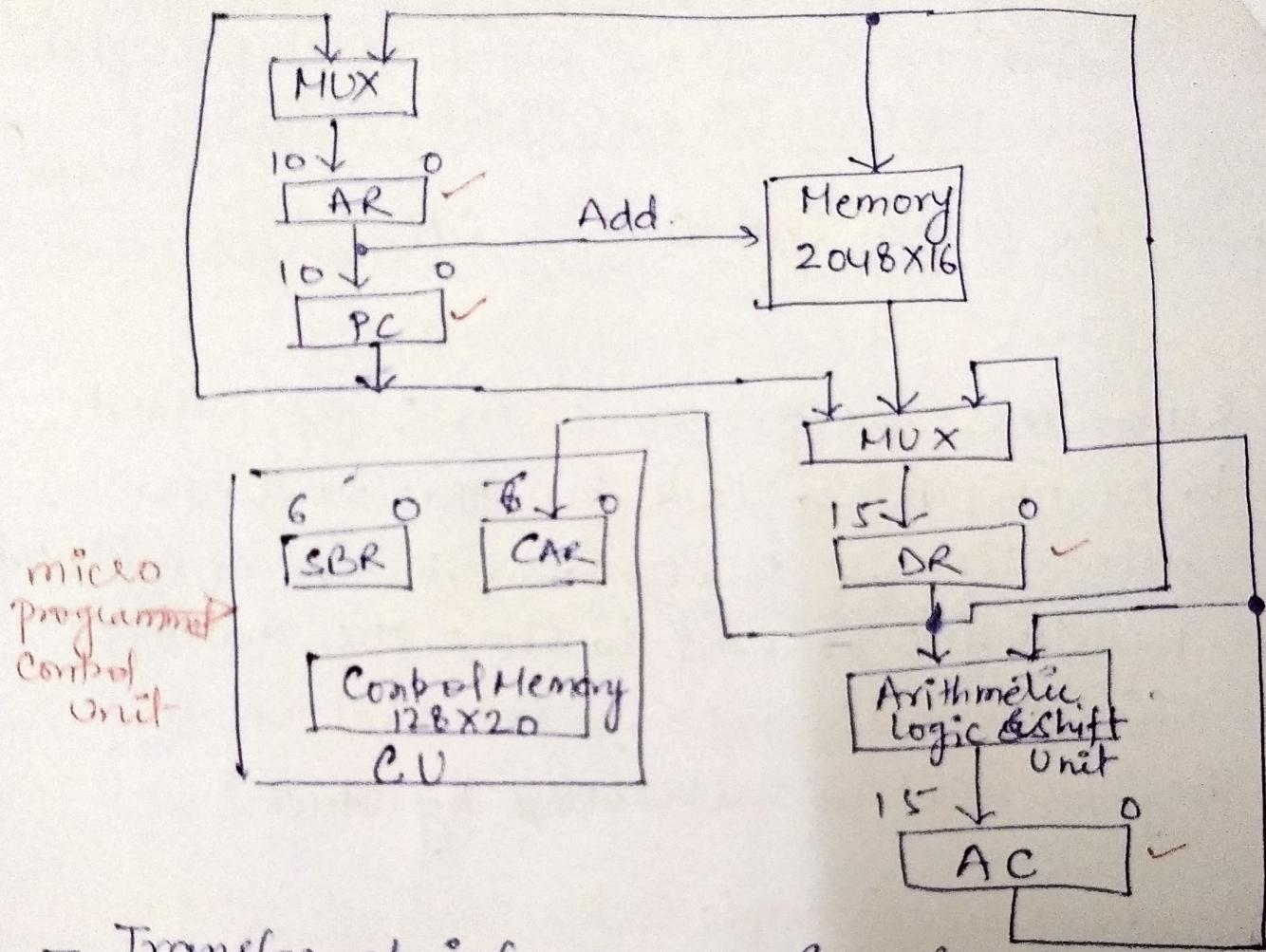
- Once the configuration of a computer and its micro programmed control unit is established, the designer task is to generate the microcode for the control memory.
- This code generation is called micro programming and is a process similar to conventional m/c lang programming.

It consists of 2 memory units

- Main Memory
- Storing instruction & data

- ↓ Control memory
- Storing micro programs

- 1 Reg with Processor unit & 2 with CU
- Processor Register are PC, MAR, MDR & AC
- CU has CAR & SBR (Subroutine register)

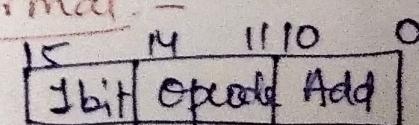


- Transfer of info among Reg. in the Processor through MUX.

DR from AC, PC, Memory.
 AR from PC or DR
 PC from AR only

Instruction format:-

- 3 fields,



Indirect bit-
Addressing

e.g.: ADD 0000 [op code] AC \leftarrow AC + M[6A]



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BRANCH :: branch of effective add if

the operand in AC is negative.

BRANCH 0001

If $(AC \geq 0)$ then / effective Add.

STORE 0010

$M[EA] \leftarrow AC$

EXCHANGE 0011

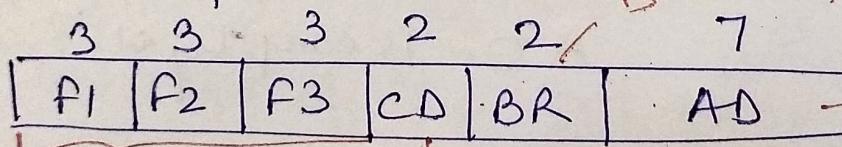
$AC \leftarrow M[EA]$, $M[EA] \leftarrow AC$

Microope

MicroInstruction format →

- Micro instruction format for the CM.

- 20 bits of the MI are divided into four functional part



Branch field if $BR = 00$
 $BR = 01 \rightarrow$ Jump
 $BR = 10 \rightarrow$ sub
 $BR = 11 \rightarrow$ sout ne

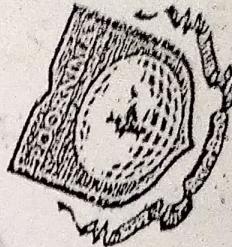
Micro-operation field → condition for branching ($00 \rightarrow$ True)

3 field (f_1, f_2, f_3)
 → 7 diff micro operation

$DR \leftarrow M[AR]$
 & $PC \leftarrow PC + 1$

with $f_2 = 100$
 with $f_3 = 101$

Symbolic Micro-Instruction:-



- A microprogram is to define symbols for each field of the microinstruction and to give user the capability for defining their own symbolic addresses.

1. Label field - empty or specify symbolic add.
Label terminated with ()

2. Micro-operation field consist of 1, 2 or 3 symbols
separated by comma
No more than one symbol in a field.

3. CD - letter U, I, S2

4. BR - four symbols.

5. AD field

- ① symbolic add
 - ② symbol NEXT → next add in sequence
 - ③ if BR have RET
MAP
- AD - is empty or 7zeros.

ORG: - define as first add of micro program routine

Fetch Routine:-

- CM has 128 words
- each word contain 20 bits
- When microprogram the CM, it is necessary to determine bit value of all 128 words.

$AR \leftarrow PC$

$DR \leftarrow M[AR], PC \leftarrow PC + 1$

$AR \leftarrow DR(0-10), CAR(2-5) \leftarrow DR(11-14),$
 $CAR(0,1,6) \leftarrow 0$

- The fetch routine needs 3 micro-instructions which are placed in CM at add 64, 65 & 66.

Symbolic Micro-program:

- The executed of the 3rd micro-instruction in the fetch routine result in a branch to add OXXXOO, where XXXX are 4-bit operation code.
- Each routine we must provide microinstructions for evaluating the effective add and for executing the instruction. Indirect add mode is associate with all memory-reference inst.