PRAKHAR SHARMA

National University of Singapore (NUS)
Email: prakhar.gtm@gmail.com, elepshr@nus.edu.sg
Ph: +65-9370-9378
Website: sharmaprakhar.github.io

EDUCATION

2013	B.E.(Hons) Electronics and Instrumentation, MSc.(Hons) Economics, B.I.T.S. Pilani, India	Major GPA: 8.8/10 (senior & junior year)
2007	Senior Secondary Education (Class XII) | AISSCE, DDPS, Ghaziabad, India	82%

RESEARH EXPERIENCE

Research Engineer, **National University of Singapore** **Jan '16 - present**

Advisor: Prof. Massimo Alioto

- **DSO (Defense Science organization - Singapore) funded scholar and University Research Staff**
- **Reconfigurable hardware for Computer Vision**
  - Designed custom hardware architecture for super-pixel segmentation by region growing
  - Designed a hand stitched framework for plug and play DRAM communication on Xilinx Zynq-7000 FPGAs
  - Designed hardware architecture for 2D gaussian convolution filter for custom pixel throughput
  - Designed novel memory-centric implementation of union-find graph algorithm on FPGA
  - Designed real time feature extraction engine (color, anisotropic gaussian) on FPGA (VGA @ 30 FPS)
  - Executed custom IP generation and integration on Xilinx Zynq-7000 FPGAs (HW-SW co-design)
  - Coded feature extraction (color, anisotropic Gaussian, Gabor filter, LBP) using OpenCV and C++
- **Machine Learning and Deep Learning**
  - Coded real-time image segmentation using bayesian graphical models for autonomous vehicles
  - Trained deep convolutional neural networks [Imagenet, CIFAR-10, MNIST] using Caffe and Torch
  - Implemented flow of bayesian inference on MATLAB and SAMIAM
  - Prepared a plan of action for FPGA accelerators for Deep Learning – project set to begin in December
- **Contribution to University coursework as research staff**
  - Worked on plug-and-play DRAM communication models released as open source material
  - Delivered two lab sessions to EE-4218 students on "DDR communication on Xilinx Zynq-7000 SoCs"
  - Guided a Masters student in a research project on "low power architectures for colour image normalization"

WORK EXPERIENCE

SoC Design Engineer, AMD, Bangalore **Aug '13 – Dec'15**

Manager: Prashanth Vallur

- **Carried out all aspects of design, verification and testing of Clocking Architectures for GPUs**
  - Designed clock distribution architectures for dGPUs – floorplan based clock routing and tree synthesis(14nm)
  - Designed clock buffers with optimized wire model drive strength and minimum power delay product
  - Designed the first clock distribution elements for finfet technology at AMD and released as standard cell library
  - Automated layout place and route for clock spines using Perl, Tcl, Python and Cadence-skill
  - Maintained CAD toolchain regression for DK tech-file and tool version consistency
  - Implemented latin hypercube sampling and importance sampling for SRAM yield analysis Monte-Carlo runs
  - Carried out first order & second order variable parameter sensitivity analysis in planar and finfet device models

TOOL PROFICIENCY AND RELEVANT COURSES

Tools	Xilinx[Vivado, SDK, XMD], Caffe, Torch, Cadence Virtuoso, HSPICE
Software	Python, C++, MATLAB, (system)Verilog, unix, Perl, tcl, Skill, Embedded C, Bash
MOOC Courses	machine learning, object oriented programming, data structures and Algorithms
Audited at NUS	advanced computer architecture, pattern recognition, probabilistic graphical models

PUBLICATIONS

IEEE Conference Publications:

- **P. Sharma** and I Garg, "method for sizing complex CNFET bitcell for balanced read write operation", *6th International Conference on computing communication and networking technologies*, 2015
- I.Garg and **P. Sharma**. "Estimation of SNM in latches and subsequent formation of a 10T CNFET bitcell", *11th workshop on intelligent solutions in embedded systems (WISES)*, 2013

TALKS AND ORAL PRESENTATIONS

- "Bridging the industry academia gap – a research's perspective on innovation in industry", *ECE department, NUS*
- "Getting the message across", *EE4218 graduate lab session, ECE department, NUS*
- "Method for sizing complex CNFET bitcell for balanced read write operation", *paper presentation, 6th International Conference on computing communication and networking technologies*, 2015
- "Estimation of SNM in latches and subsequent formation of a 10T CNFET bitcell", *paper presentation, 11th workshop on intelligent solutions in embedded systems (WISES)*, 2013

RELEVANT PROJECT DETAILS

1. **Senior year undergraduate thesis on SNM estimation in latches and formation of a CNFET bitcell (Under Dr. Anu Gupta. H.O.D. Electronics Dept, BITS Pilani)**
   - Aimed at increasing Static Noise Margin (SNM) of the bitcell.
   - Designed novel bitcell using the 4 MOS design of Schmitt Trigger Inverter
   - Employed CNFET technology using Stanford provided open source models.
   - Varied parameters such as chirality vectors and number of tubes to improve SNM
   - Explored the trade-off between read and write via both the Butterfly and the N-Curve.

2. **Design of High altitude balloon communication**
   - Designed packet data communication framework for a near space balloon using APRS protocol
   - Designed frame generator for communication protocol based on AX.25
   - Built a HAM radio ground station at BITS Pilani and conducted transmission runs with home brewed equipment
   - Programmed an array of Microcontrollers, and systems like Arduino, Stellaris Launchpad
   - Gathered telemetry data through an array of sensors – pressure, temperature, humidity, force and accelerometer

3. **Importance Sampling for SRAM yield analysis Monte-Carlo**
   - Studied independently, focusing on rare event detection for 6-sigma corner analysis
   - Generated psuedo-random samples using Latin hypercube sampling for circuit simulation
   - Studied importance sampling with single variable parameter in Monte-Carlo runs
   - Studied second order hyperparameter sensitivities in device models using ANOVA (analysis of variance)

4. **Method for Sizing Complex CNFET Bitcells for Balanced Read Write Operation**
   - A new experimental method to size CNFET circuits, especially SRAM bitcells
   - The trade-off philosophy between read and write operations in sizing is established.
   - Data is presented to verify the balancing criteria and balancing point.
   - The algorithm achieves balance in the SRAM bitcell between the read and write trade-offs whilst maintaining good individual read and write metrics.

5. **Design of Propeller Display with Atmega8**
   - A Persistence of Vision Based Propeller display was designed using an Atmega8 coded using USBASP
   - A string was displayed on a rotating array of LEDs mounted on a motor.
   - Watchdog timer concepts were employed to calculate RPM of motor, and IR sensors to sense the homing point
   - Got hands-on experience with the TI Stellaris LM4F120 LaunchPad Evaluation Board

REFEREES

Massimo Alioto
Research Advisor
Senior IEEE Fellow
Associate Professor, ECE Dept.
National University of Singapore

Nitin Chaturvedi
Undergrad Thesis Advisor
Assistant Professor, ECE Dept.
BITS Pilani, India

Prashanth Vallur
Senior Manager
Member of technical staff
AMD, India