

PRAKHAR SHARMA

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EDUCATION

University of Massachusetts

Masters in Computer Science

Courses: Deep Learning, Reinforcement Learning, Machine Learning

Amherst, MA

Expected: May 2019

Birla Institute of Technology and science

B.E. Electronics and Instrumentation

Pilani, India

Grad: May 2013

EXPERIENCE

National University of Singapore

Research Associate

Singapore

Jan 2016 — August 2017

- Designed contextual bandit RL algorithms for efficient IoT service discovery
- Coded feature extraction from raw images using C++ and openCV
- Studied adversarial bandits for document ranking (MAB and Exp3)
- Trained deep convolutional neural networks [Imagenet, CIFAR-10, MNIST] using Caffe and Torch
- Designed resource efficient heterogeneous platform accelerators for deep learning architectures
- Designed a plug and play DRAM framework on Xilinx Zynq-7000 FPGAs
- Designed a novel memory-centric implementation of Union-Find graph algorithm
- Conducted lab sessions for the course "Real time computing"

AMD

Design Engineer

Bangalore, India

August 2013 — December 2015

- Automated layout place and route for clock spines using Perl, Tcl, Python and Cadence-skill
- Implemented importance sampling for SRAM yield analysis Monte-Carlo runs
- Designed floorplan based clock architectures for dGPUs (14nm finfet technode)
- Maintained CAD toolchain regression for DK tech-file and tool version consistency

COMPUTER PROFICIENCY

Language:	Python, C++, Perl, Shell, Embedded C, MATLAB, Latex
Scientific computing:	pyTorch, Caffe, Numpy
Hardware:	Vivado, ZC-706, Verilog, Arduino, TI-stellaris

PUBLICATIONS AND TALKS

P. Sharma and I Garg, "method for sizing complex CNFET bitcell for balanced read write operation", 6th International Conference on computing communication and networking technologies, 2015

I.Garg and **P. Sharma**. "Estimation of SNM in latches and subsequent formation of a 10T CNFET bitcell", 11th workshop on intelligent solutions in embedded systems (WISES), 2013

PROJECTS

Scene segmentation for autonomous vehicles (C++, OpenCV, Xilinx ZC706)

The aim of this project was to achieve real time speed-up in autonomous driving scenarios to overcome the slow superpixel segmentation approach. Hardware design for Bayesian algorithms using Xilinx heterogeneous FPGA systems and design of efficient convolution accelerators for deep learning were achieved.

MCDP - Reinforcement learning and TOPSIS (Python, Numpy, Git)

Traditional multi-criteria decision making techniques are often slow and inaccurate in large sized problems. An IoT paradigm with $> 10^5$ sensors was considered and RL algorithms for service discovery were designed and compared against existing proven techniques. The study was extended to diverse online document ranking

High altitude balloon communication (Arduino, Embedded C, Sensors)

While leading a team that built a HAM radio ground station at BITS Pilani, I programmed Microcontrollers, and systems like Arduino and TI Stellaris Launchpad. We gathered telemetry data through an array of sensors - pressure, temperature, humidity, force and accelerometer