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Experiment - 1

Objective :- To investigate AND, OR, NOT, Exclusive OR (EX-OR), Exclusive NOR (EX-NOR), NAND and NOR Gate operation.

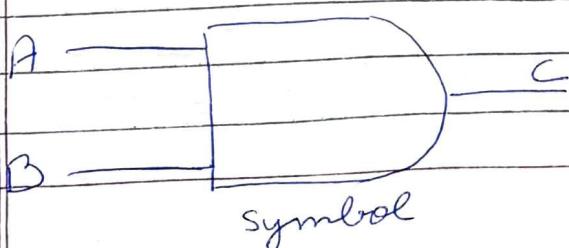
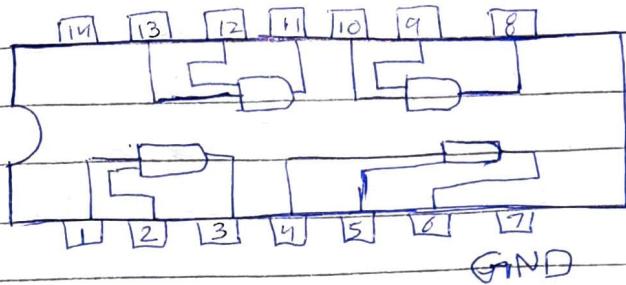
APPARATUS REQUIRED :- Integrated chips (IC), connecting wires, Digital Trainer Kit

Theory :-

2 Input AND Gate : And gate is physical realization of the logical multiplication output of AND gate will be only when all the inputs are 1. If the inputs are A & B then AND gate output is given as :-

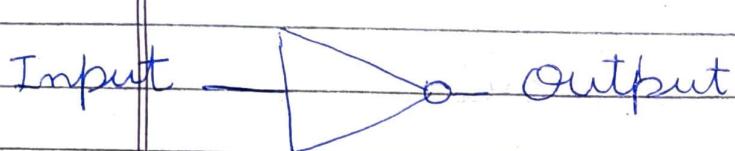
$$Y = A \cdot B$$

$$\text{AND} = \text{NAND} + \text{NOT} \quad \text{or} \quad \text{NAND} = \text{AND} + \text{NOT}$$

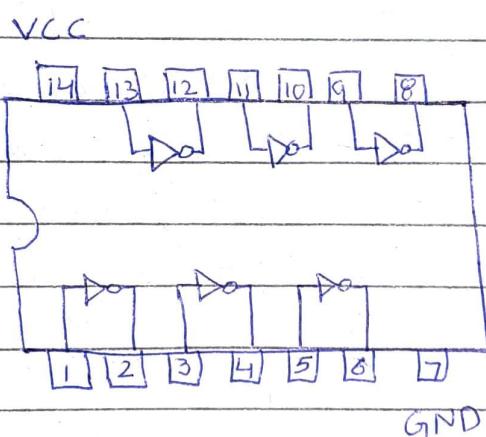


2 Input AND Gate		
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

2 Input Not Gate :- It is called not gate IC and is also called MVX inverter as there are 6 not gates in it. If we give input '0' then we get '1' as output and vice versa.



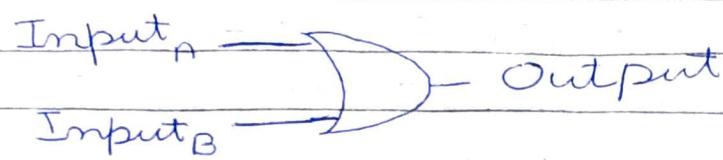
Not gate truth table



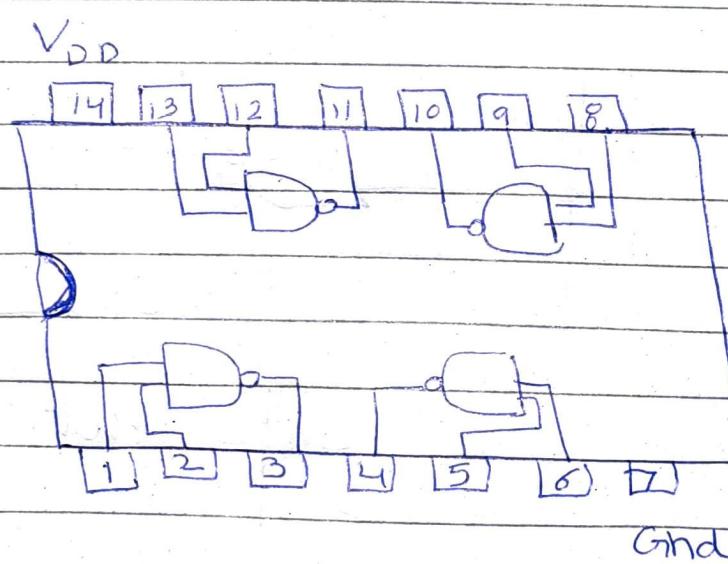
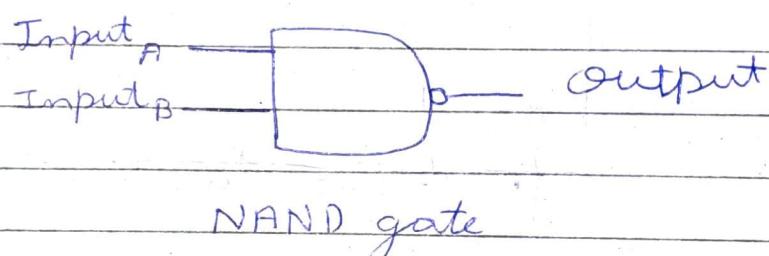
2 Input OR gate :- OR gate is physical realization of logical Addition. Output of OR gate will be 1 if any of the input signal is 1. If the input are A & B of a OR gate then output is given as:

$$Y = A + B$$

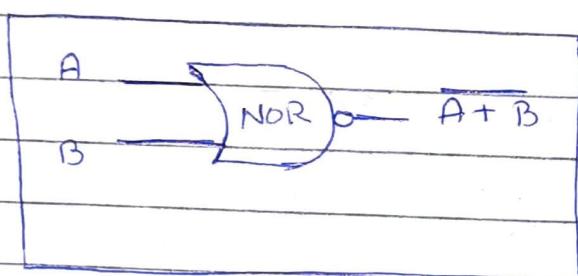
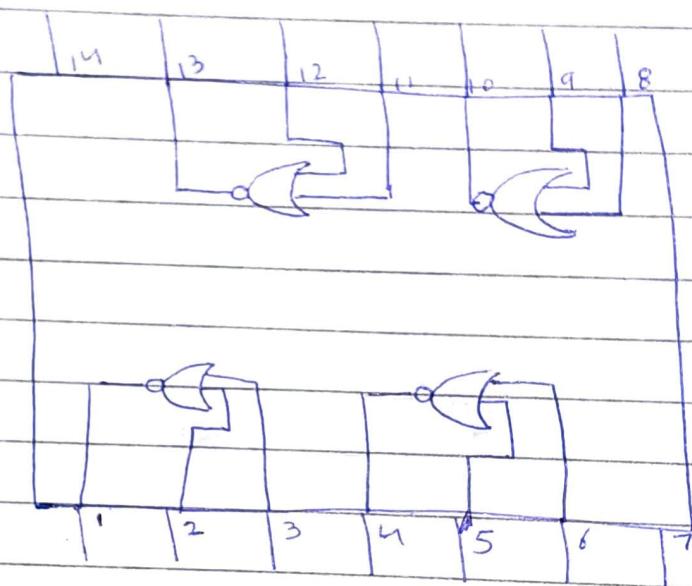
$$OR = NOR + NOT \quad OR \quad NOR = OR + NOT$$



2 Input NAND Gate : In this IC there are four nand gates Pin no 7 is grounded and 14 is connected to power supply. Input pins are (1, 2), (4, 5), (9, 10), (12, 13) and output of these nand gates is taken across pin 3, 6, 8 and 11 respectively.

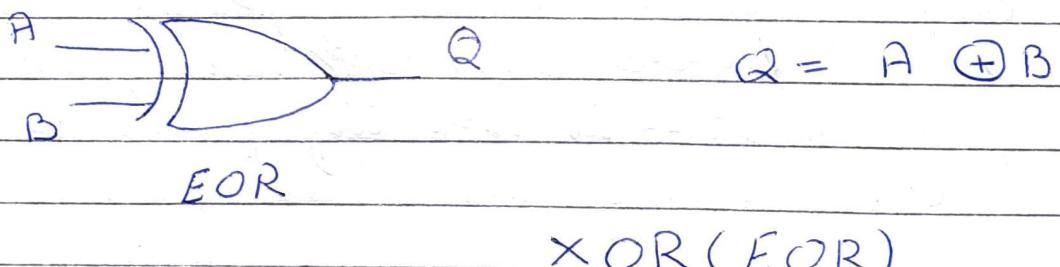
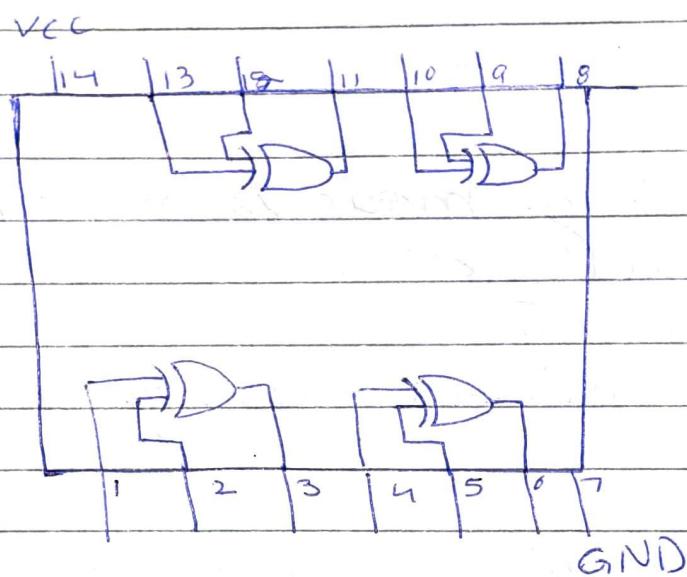


2 Input NOR Gate:- It is also called quad-2 input nor gate IC. In this IC nor gate input is given from (2,3), (5,6), (8,9) and output pins are 1, 4, 10 and 14 respectively.



A	B	Out
0	0	1
0	1	0
1	0	0
1	1	1

2 Input EX-OR Gate: In this IC there are four nand gates. Pin no 7 is ground-dead and 14 is connected to power supply. Input pins are (1,2), (4,5), (9,10) and output of these nand gates is taken across pin 3,6,8 and 12 respectively.



$\text{XOR}(\text{EOR})$

A	B	Q
0	0	0
1	0	1
0	1	1
1	1	0

2 Input Ex-NOR Gate :-

It is also called quad-2 input nor gate IC. In this IC nor gate input is given from (2,3), (5,6), (8,9), (11,12) and output pins are 1,4,10 and 14 respectively.

Procedure :-

- 1) IC testing mode is mode 1 of system, selected at power ON and hardware result. This mode can also be selected from other modes by pressing "IC Test key".
- 2) On selection of this mode by default self diagnostic RAM test ~~or~~ message is displayed followed by prompt "IC no...? If at power on self-diagnostic test fails. System is waiting for number of IC to be tested.
- 3) At this stage TEST SOCKET is potential free. User IC should be tested in test socket properly.
- 4) While inserting IC under test in the socket, care should be taken to align bottom edge of IC under test with bottom edge of the test socket.

Precaution :-

- 1) IC should be inserted carefully
- 2) Handle the IC carefully.

Result :-

Various IC's have been tested successfully using IC tester.

~~Discussion~~

Experiment - 2

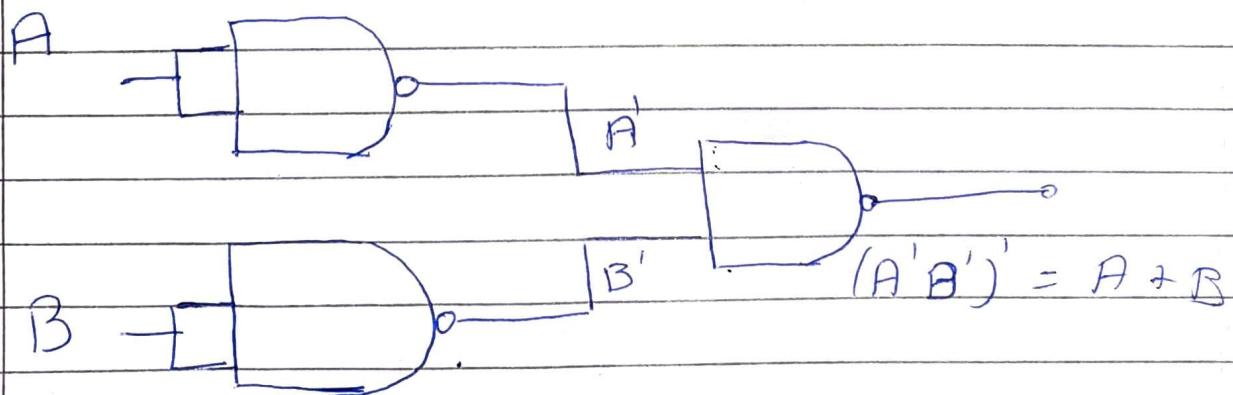
Objective:- To verify the truth tables of AND, OR, NOT, EX-OR, EX-NOR realized using NAND and NOR gates

APPARATUS REQUIRED:- Integrated chips (I.C), connection wires, digital trainer kit.

Theory:-

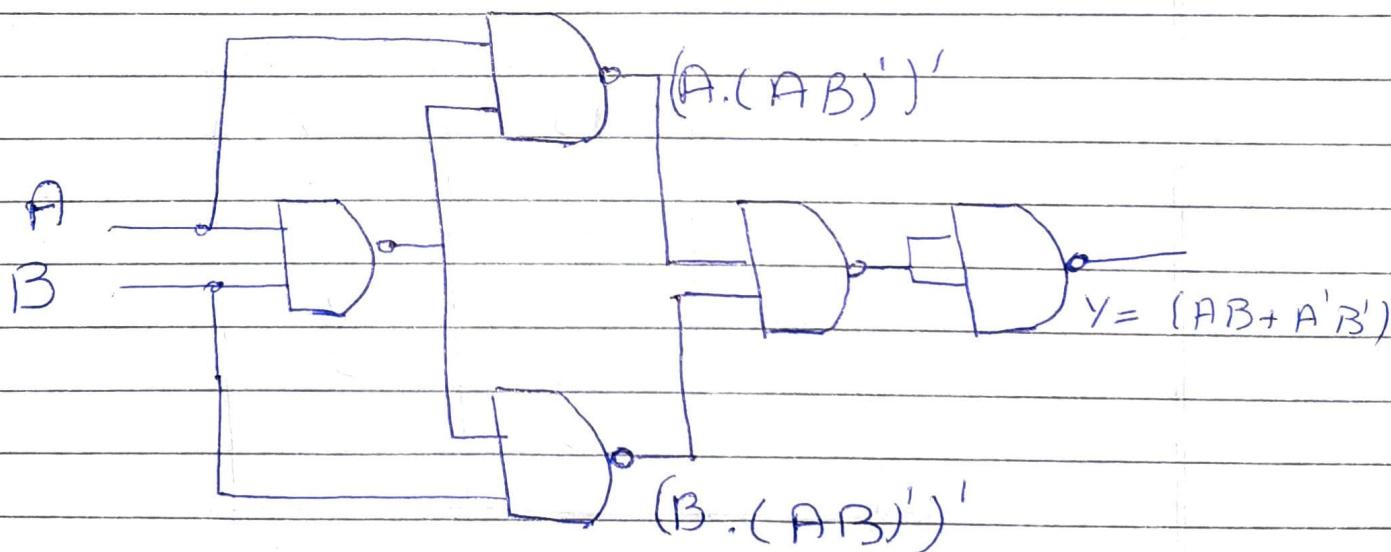
Implementing OR Gate using NAND Gate :-

An OR Gate can be realized by a NAND Gate with all its inputs complemented by a NAND Gate inverter



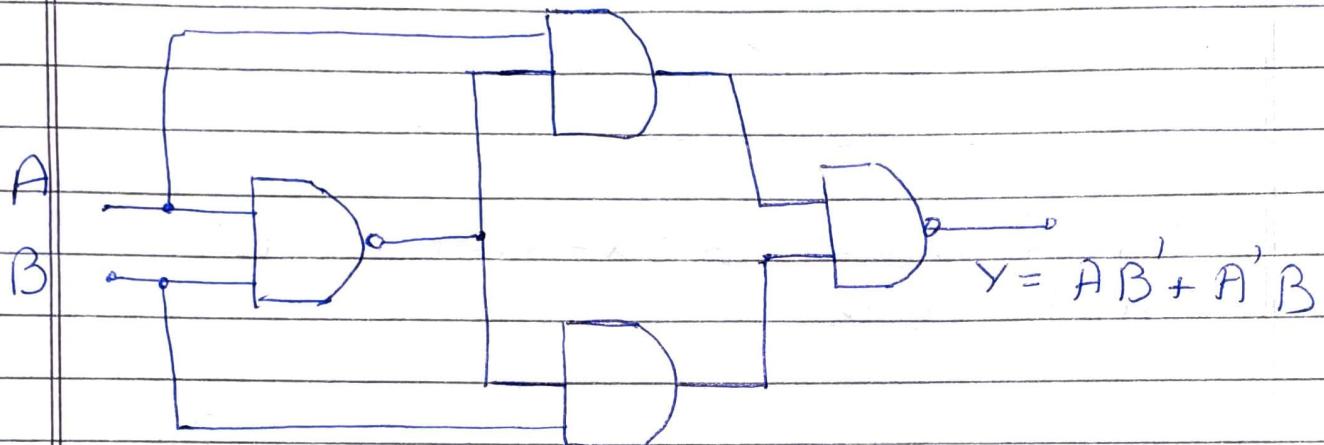
A	B	Y
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	5V

Implementing Ex-NOR Gate using
NAND Gate



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Implementing Ex-OR Gate using
NAND Gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Procedure:-

- 1) Plug the chips you will be using into the bread-board with pin 1 at the upper left corner (Pin 1 is identified by a dot or notch next to it on the chip package).
- 2) Connect +5V and Gnd pins of each chip to the power and ground bus strips on the bread-board.
- 3) Make the connections as per the pin diagram.
- 4) Switch on VCC and apply various combination of input according to the Truth table.
- 5) Note down the output reading for different combinations of inputs where 5V indicates logic 1 and 0V indicates logic 0.
- 6) Repeat step 1 to 4 for NOT, AND, OR, EX-OR & EX-NOR.

Precautions :-

- 1) All the connections should be made properly.
- 2) IC should not be reversed.

Result :- The basic logic gates were successfully constructed using NAND and NOR gates this verifies that they are Universal gates.

Experiment - 3

Objective - To realize an SOP and POS expression.

Apparatus Required:- Integrated Chips (IC), connecting wires, Digital Trainer Kit

Theory :-

- SOP: It is often the case that the canonical min-term form can be simplified to an equivalent SOP form. This simplified form would still consist of a sum of product terms.

$$Y = A + B$$

$$Y = A(B + B') + B(A + A')$$

$$Y = AB + AB' + BA + BA'$$

$$Y = AB + A\bar{B} + \bar{A}B$$

- POS: A standard POS form is product of sum, and one which is no. of sum terms, each one of which contains all the variable by the functions either in complemented and non-complemented form are multiplied together.

$$Y = A \cdot B$$

$$Y = (A + B, B') B (A \cdot A')$$

$$Y = (A + B)(A + B')(A + B)(A' + B)$$

$$Y = (A + B)(A + B')(A' + B)$$

Procedure :-

- 1) Insert the IC on bread-board.
- 2) Make pin no 7 grounded and connect pin no 14 to power supply.
- 3) Now provide inputs as specified in circuit diagram.
- 4) Take output across respective pins.
- 5) Any operation such as and, or, half adder etc. can be performed using these IC's

Precautions :-

- 1) Insert IC on bread-board tightly.
- 2) Don't forget to ground pin no 7.
- 3) Hold the IC properly.

Result:- Study SOP and POS expression had been done using IC 7400, 7402, 7408, 7432 S

Experiment - 4

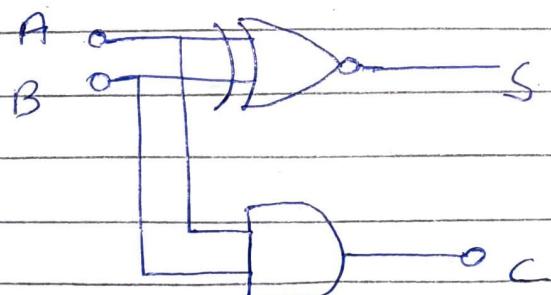
Objective :- To study & realize half and full adder.

- (i) Using Basic Gates
- (ii) Using only NAND Gates

Apparatus Required:- Integrated chips (IC)
 connecting wires,
 power supply,
 digital trainer
 kit, multi meter.

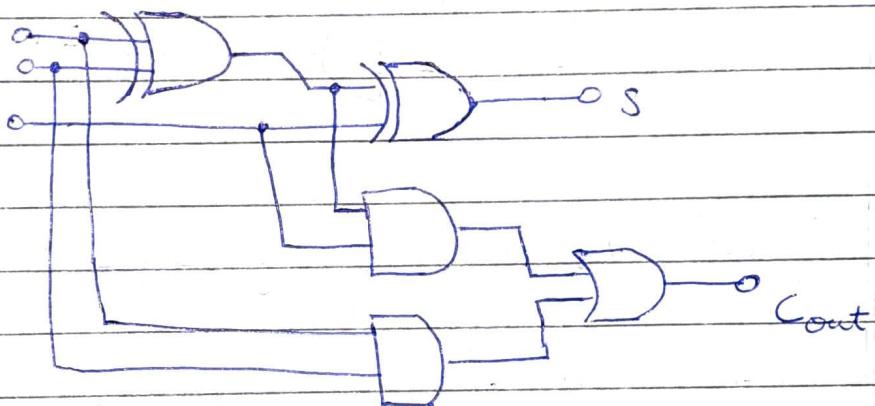
Theory :-

Half-Adder \rightarrow The simplest combinational circuit which performs the arithmetic addition of two binary digit is called half-adder. A half adder add two one-bit binary numbers A and B. It has two outputs S and C the final sum is $S + C$.



From the truth table, the logic expression for the sum output can be written as a Sum of Product expression by summing up the input combinations for which the sum is equal to 1.

Full-Adder:-

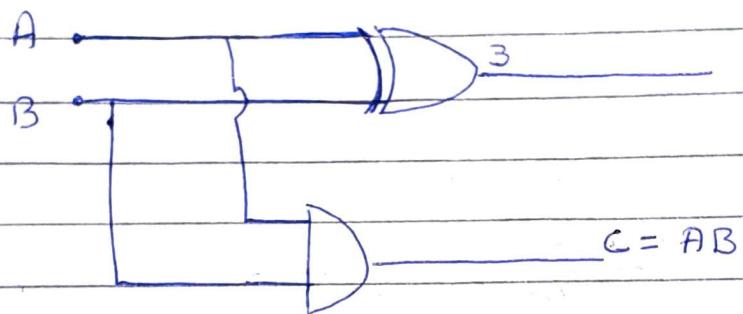


A full-Adder is a combinational circuit that performs the arithmetic sum of three input bits and produces a sum output and a carry.

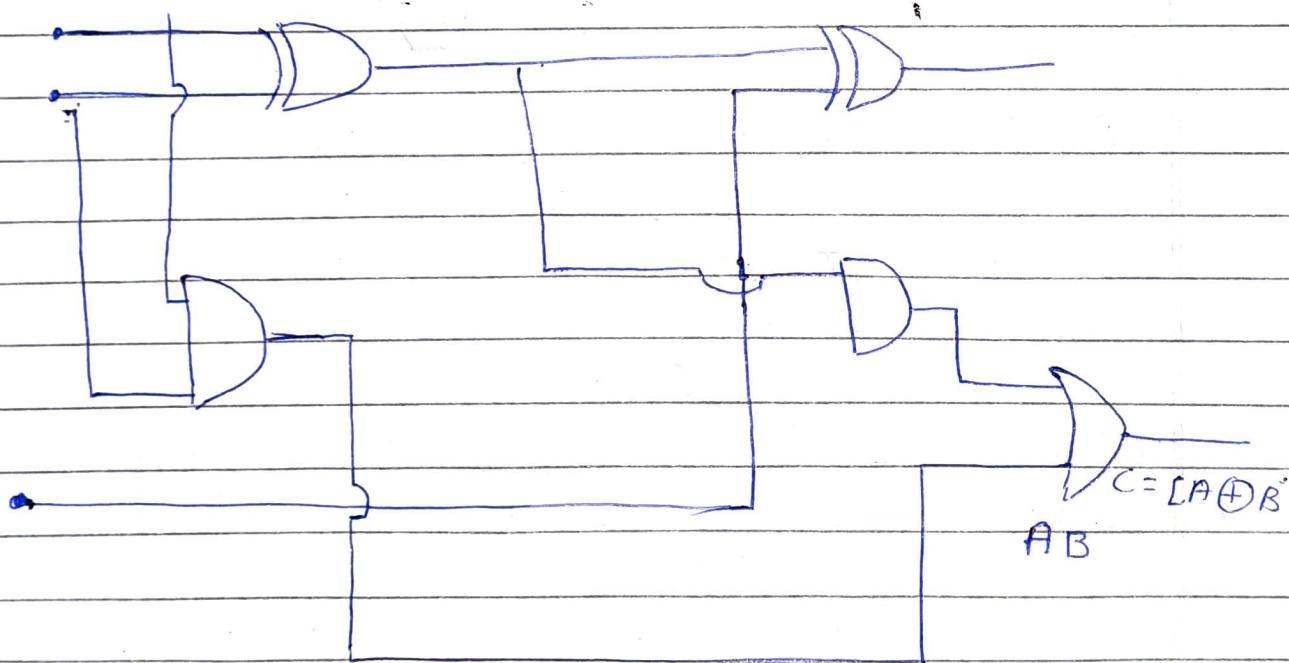
From the truth table, the logic expression for S can be written by summing up the input combination for which the sum output is 1 as:

Circuit Diagram:-

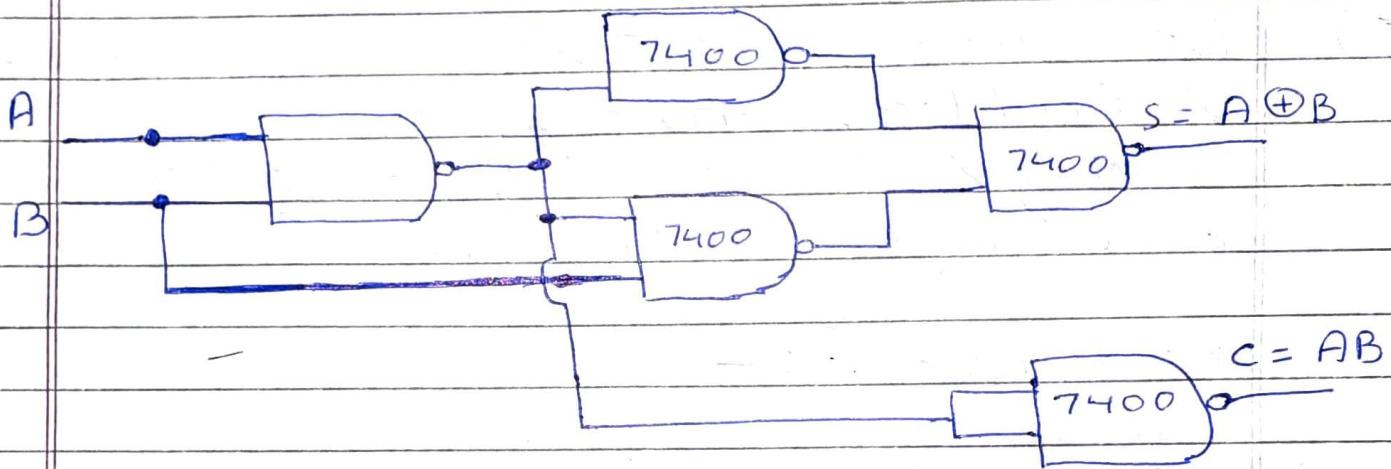
Half Adder using basic gates:-



Full Adder using basic gates:-



Half Adder using NAND gates only:-



Input		Output	
A	B	S(sum)	C(carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Procedure :-

- 1) Verify the gates
- 2) Make the connections as per the circuit diagram.
- 3) Make pin no 7 grounded and connect pin no 14 to power supply.

- 4) Switch on VCC and apply various combinations of input according to the truth table.
- 5) Note down the output reading for half/full adder sum/difference and the carry/borrow bit for 8 different combination of inputs.

Precautions:-

- 1) Insert IC on bread-board tightly
- 2) Don't forget to ground pin no. 7
- 3) Hold the IC properly.

Result:-

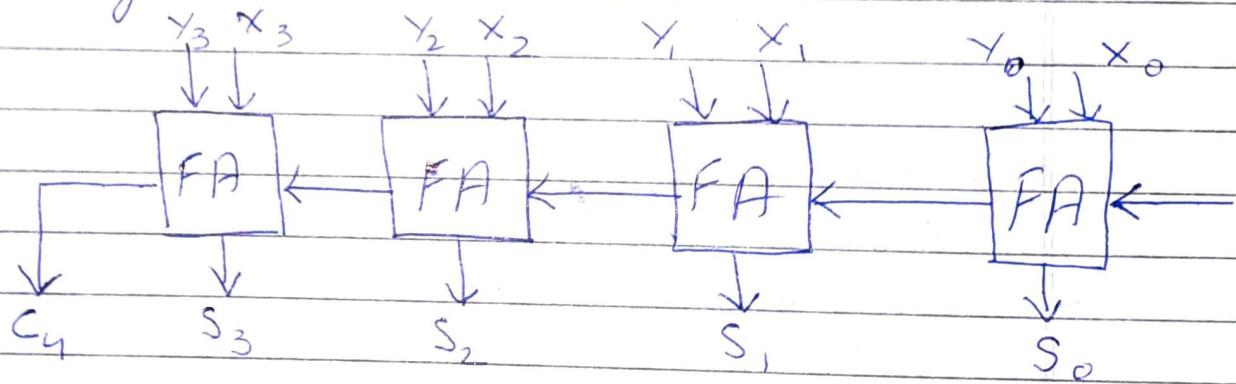
Study and realization of half adder & full Adder circuits have been done using IC's 7400, 7408, 7432 etc.

Experiment - 6

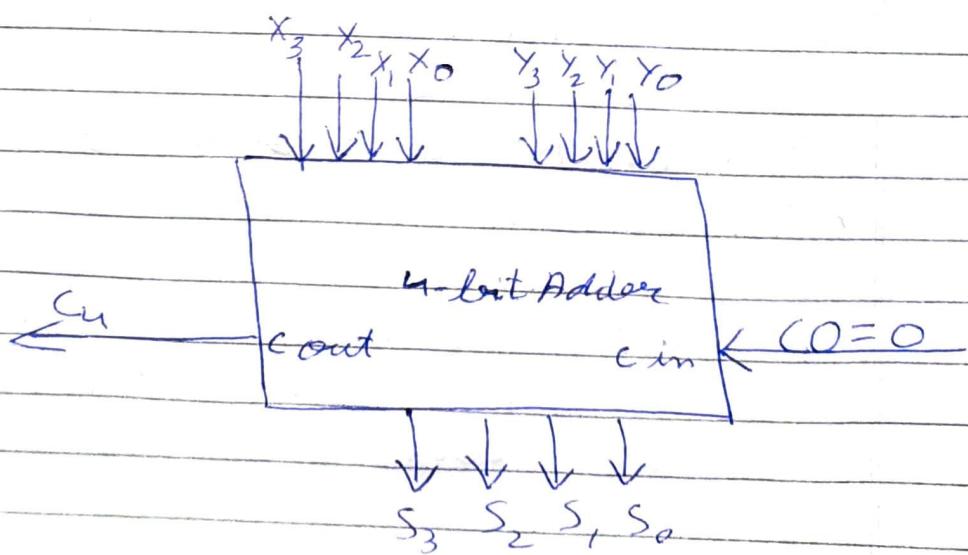
Objective :- To realize a 4-bit ripple adder/subtractor using basic half adder/subtractor & basic Full Adder/Subtractor.

Apparatus Required :- Integrated Chips (IC), connecting wires, power supply, Digital trainer kit, multi meter.

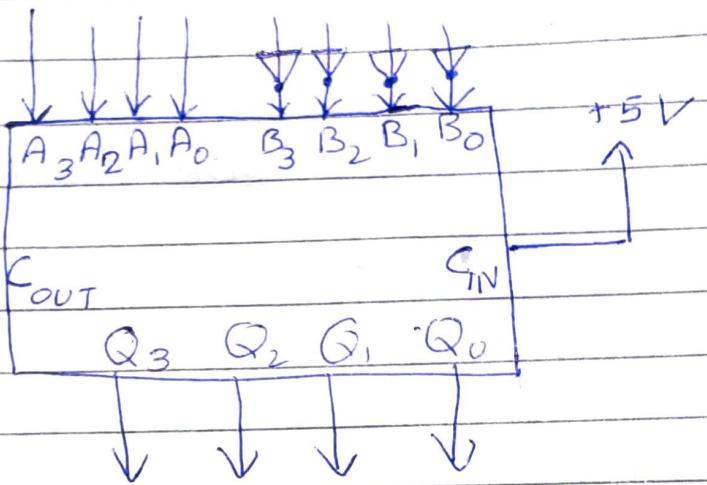
Theory :-



Adder



Subtractor



Procedure:-

- 1) Verify the gates.
- 2) Make the connections as per the circuit diagram.
- 3) Make pin no 12 grounded and connect pin no 5 to power supply.
- 4) Switch on V_{cc} and apply various combinations of input according to the truth table.

5) Note down the output reading for adder and subtractor and the sum and carry bit for different combination of inputs.

Precautions:-

- 1) Insert IC on bread-board tightly
- 2) Don't forget to ground pin no. 12
- 3) Hold the IC properly.

Result:-

Study and realization of a 4-bit ripple-carry adder / Subtractor using basic Half adder / Subtractor & basic Full Adder/ Subtractor.

Experiment - 7

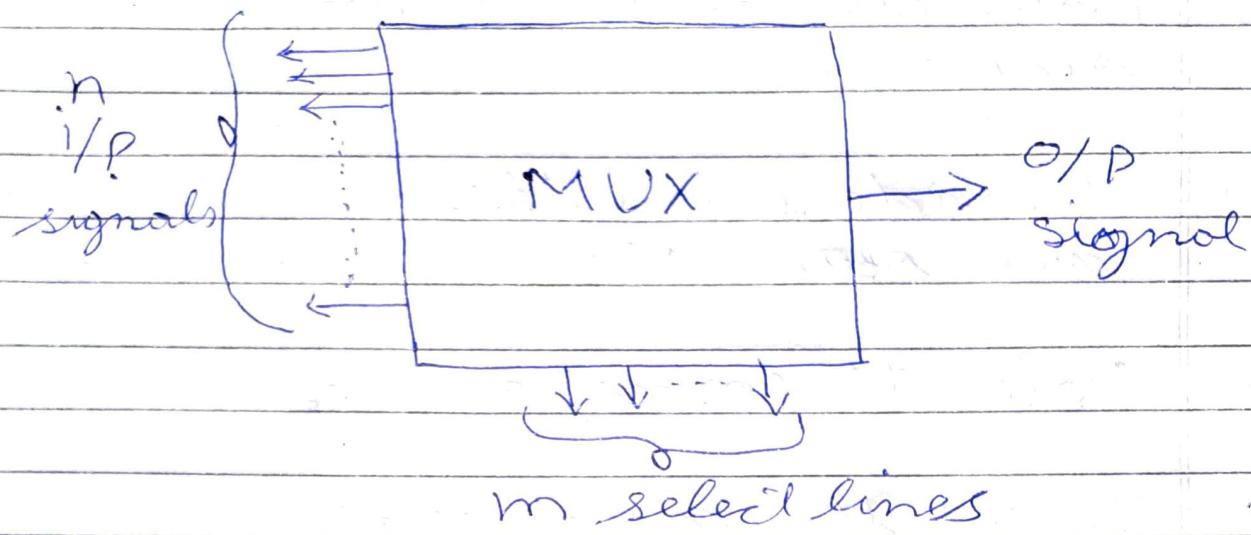
Objective:— To verify the truth table of 4-to-1 multiplexer and 1-to-4 demultiplexer. Realize the multiplexer using basic gates only. Also to construct and 8-to-1 multiplexer and 1-to-8 demultiplexer using block of 4-to-1 multiplexer and 1-to-4 demultiplexer.

Apparatus Required:— Integrated chips (IC), connecting wires, Digital trainer kit

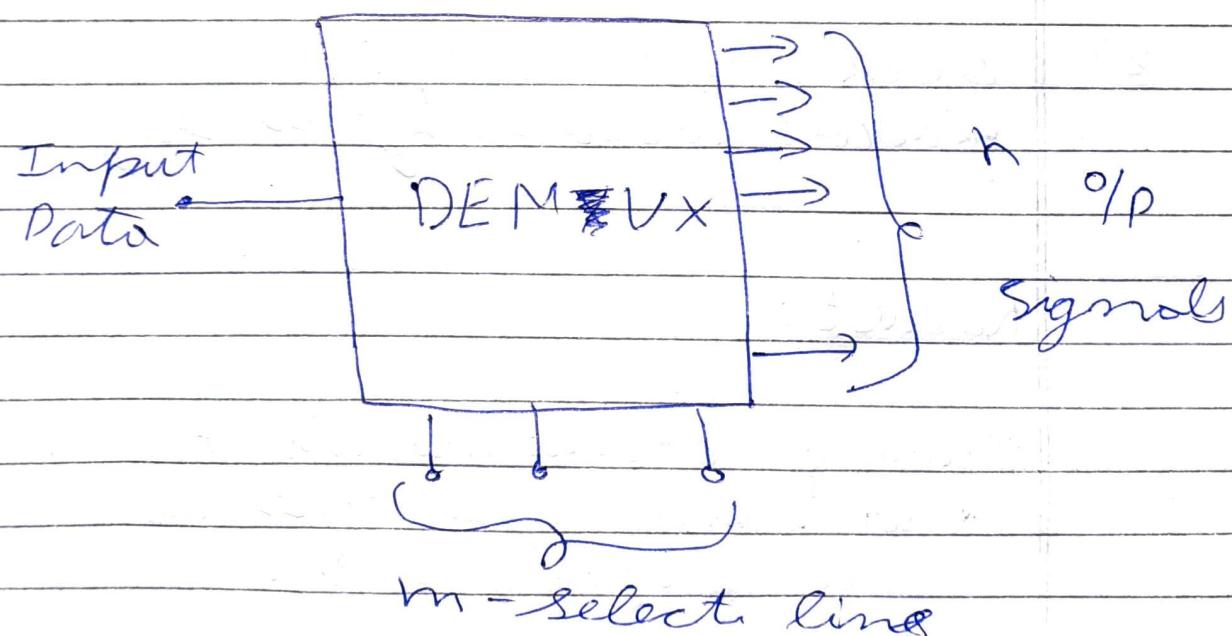
Theory:-

Multiplexers:— It is a digital circuit which has many inputs and single output. The function of multiplexer is to select one of the input lines and connect it to the output. It is also known as data selector.

Multiplexer - (Block diagram)



Block diagram of demultiplexer



Procedure:-

- 1) Make connections, as per the circuit diagram.
- 2) Provide input through input lines and obtain the multiplexed output.
- 3) Note the corresponding output.
- 4) Repeat the same process for demultiplexer.

Precautions:-

- 1) All connections must be tight.
- 2) Check power supply circuit and other factors according to requirement.

Result :-

Study of 8-channel digital multiplexer and demultiplexer has been done successfully.